



1Mx32 SRAM MODULE

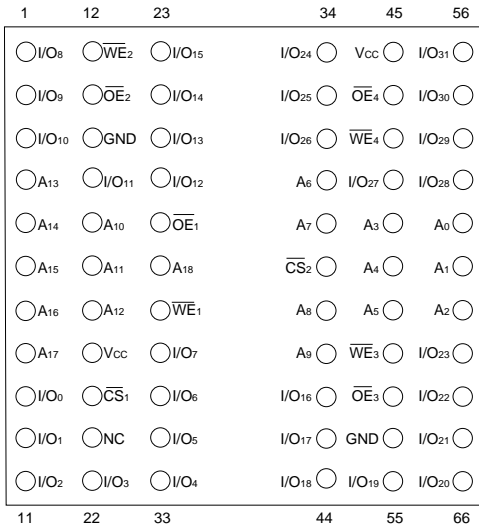
FEATURES

- Access Times of 17, 20, 25ns
- Packaging
 - 84 lead, 28mm CQFP, (Package 511)
 - 66 pin PGA Type, 1.385" sq., Hermetic Ceramic HIP (Package 402)*
- Organized as two banks of 512Kx32, User Configurable as 2Mx16 or 4Mx8
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WS1M32-XH2X* - 13 grams (typical)
 - WS1M32-XG3X - 20 grams (typical)

* Package to be developed.

PIN CONFIGURATION FOR WS1M32-XH2X*

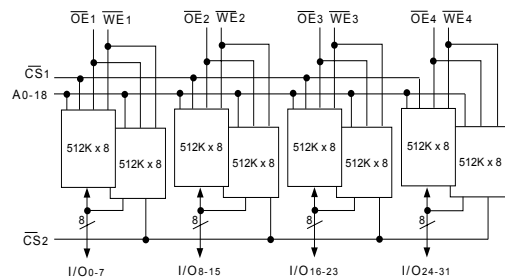
TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
\overline{WE} 1-4	Write Enables
\overline{CS} 1-2	Chip Selects
\overline{OE} 1-4	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

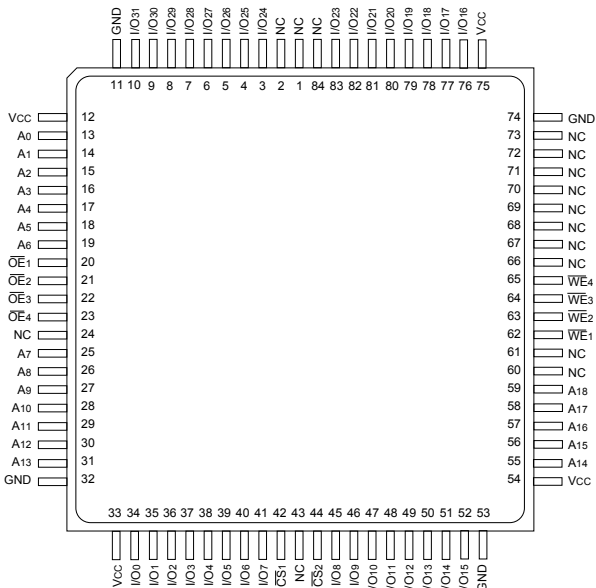


NOTE: \overline{CS} 1 & \overline{CS} 2 are used as bank select



PIN CONFIGURATION FOR WS1M32-XG3X

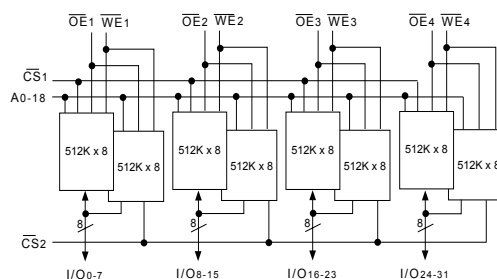
TOP VIEW



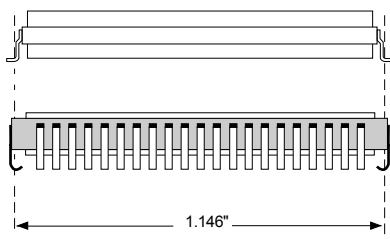
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NOTE: \overline{CS} 1 & \overline{CS} 2 are used as bank select



The WEDC 84 lead G3 CQFP fills the same fit and function as the JEDEC 84 lead CQFJ or 84 PLCC. But the G3 has the TCE and lead inspection advantage of the CQFP form.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} + 0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
\overline{OE} ₁₋₄ capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	30	pF
\overline{WE} ₁₋₄ capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	30	pF
\overline{CS} ₁₋₂ capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	30	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	30	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	75	pF

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp (Mil)	T _A	-55	+125	°C
Operating Temp (Ind.)	T _A	-40	+85	°C

This parameter is guaranteed by design but not tested.

TRUTH TABLE

\overline{CS} ₁	\overline{CS} ₂	\overline{OE}	\overline{WE}	Mode	Data I/O	Power
H	H	X	X	Standby	High Z	Standby
L	H	L	H	Read	Data Out	Active
L	H	H	H	Out Disable	High Z	Active
L	H	X	L	Write	Data In	Active
H	L	L	H	Read	Data Out	Active
H	L	H	H	Out Disable	High Z	Active
H	L	X	L	Write	Data In	Active
L	L	X	X	Invalid State	Invalid State	Invalid State

DC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Units	
			Min	Max
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10 μA
Output Leakage Current	I _{LO}	\overline{CS} = V _{IH} , \overline{OE} = V _{IH} , V _{OUT} = GND to V _{CC}		10 μA
Operating Supply Current x 32 Mode	I _{CC x 32}	\overline{CS} = V _{IL} , \overline{OE} = V _{IH} , f = 5MHz, V _{CC} = 5.5		720 mA
Standby Current	I _{SB}	\overline{CS} = V _{IH} , \overline{OE} = V _{IH} , f = 5MHz, V _{CC} = 5.5		120 mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA, V _{CC} = 4.5		0.4 V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA, V _{CC} = 4.5	2.4	V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V



AC CHARACTERISTICS
(V_{CC}=5.0V, GND=0V, T_A=-55°C to +125°C)

Parameter	Symbol	-17		-20		-25		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	17		20		25		ns
Address Access Time	t _{AA}		17		20		25	ns
Output Hold from Address Change	t _{OH}	0		0		0		ns
Chip Select Access Time	t _{ACS}		17		20		25	ns
Output Enable to Output Valid	t _{OE}		10		10		12	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	2		2		2		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		12		12		12	ns
Output Disable to Output in High Z	t _{OHZ} ¹		12		12		12	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS
(V_{CC}=5.0V, GND=0V, T_A=-55°C to +125°C)

Parameter	Symbol	-17		-20		-25		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	17		20		25		ns
Chip Select to End of Write	t _{CW}	15		15		17		ns
Address Valid to End of Write	t _{AW}	15		15		17		ns
Data Valid to End of Write	t _{DW}	11		12		13		ns
Write Pulse Width	t _{WP}	15		15		17		ns
Address Setup Time	t _{AS}	2		2		2		ns
Address Hold Time	t _{AH}	0		0		0		ns
Output Active from End of Write	t _{OW} ¹	2		3		4		ns
Write Enable to Output in High Z	t _{WHZ} ¹		9		11		13	ns
Data Hold Time	t _{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

The diagram shows a bridge circuit used for AC testing. A central component is the Device Under Test (D.U.T.). To its left, a capacitor with effective capacitance C_{eff} = 50 pf is connected to ground. To its right, a voltage source V_Z ≈ 1.5V (Bipolar Supply) is connected. Two current sources are connected to the top and bottom nodes of the bridge, with currents labeled I_{OL} and I_{OH} respectively.

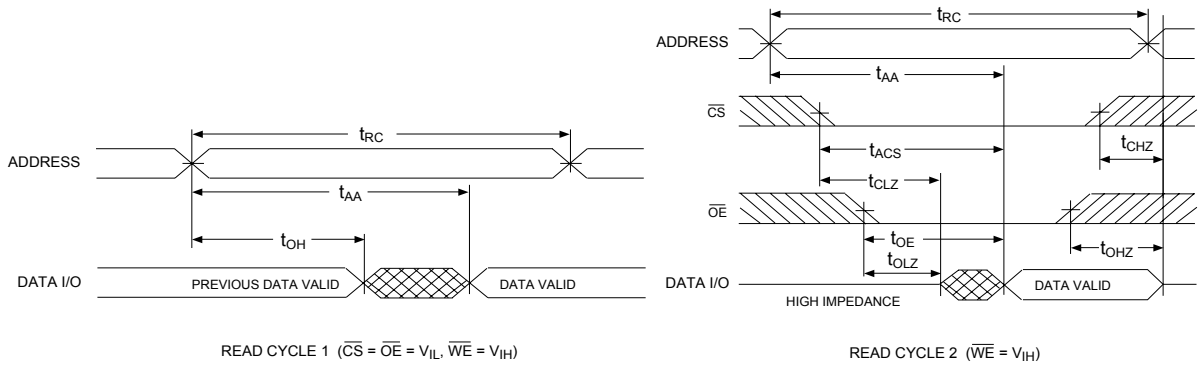
AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

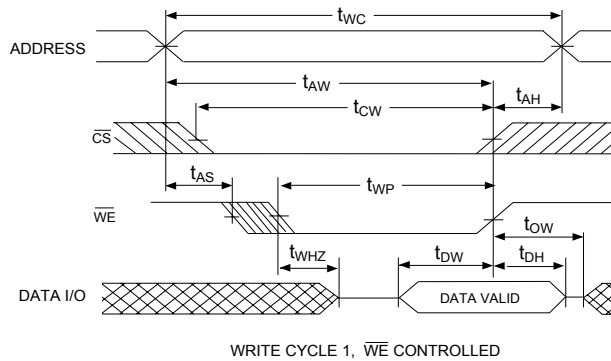
NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



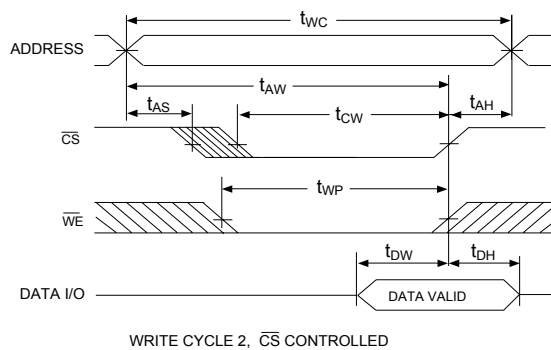
TIMING WAVEFORM - READ CYCLE



WRITE CYCLE - \overline{WE} CONTROLLED

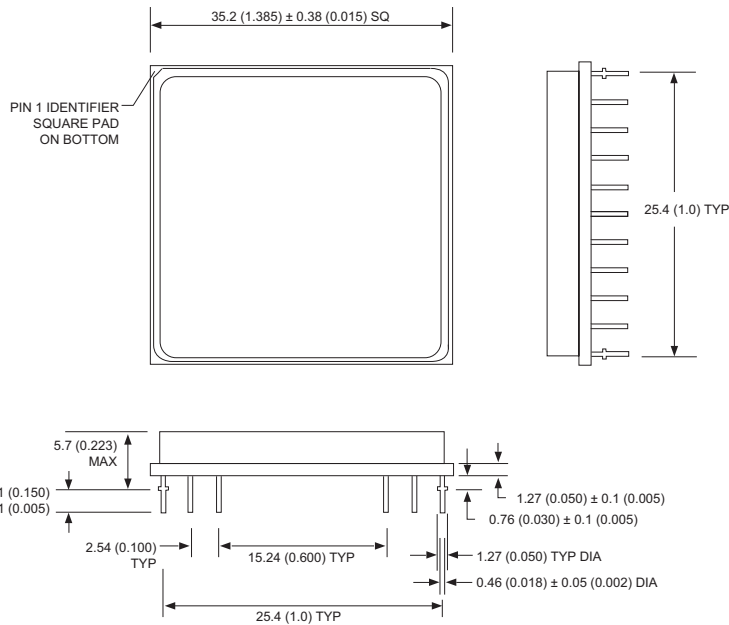


WRITE CYCLE - \overline{CS} CONTROLLED





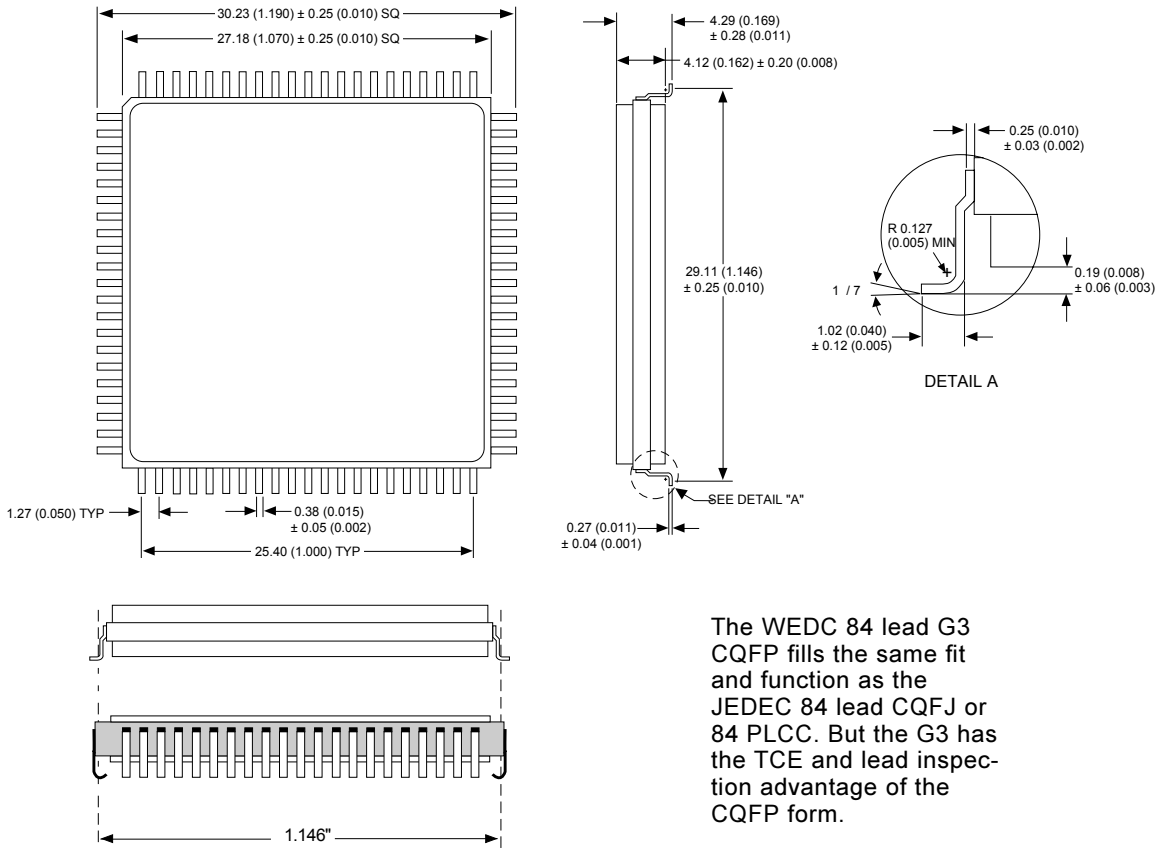
PACKAGE 402: 66 PIN, PGATYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 511: 84 LEAD, CERAMIC QUAD FLAT PACK (G3)



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ORDERING INFORMATION

W S 1M32 - XX X X X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE TYPE:

- H2 = Ceramic Hex-In-line Package, HIP (Package 402)*
- G3 = 28 mm Ceramic Quad Flatpack, CQFP (Package 511)

ACCESS TIME (ns)

ORGANIZATION, two banks of 512Kx32

User configurable as 2Mx16 or 4Mx8

SRAM

WHITE ELECTRONIC DESIGNS CORP.

* Package to be developed.