

5 Volt, Byte Alterable E²PROM

FEATURES

- Access Time: 90ns
- Simple Byte and Page Write
 - Single 5V Supply
 - No External High Voltages or V_{PP} Control Circuits
 - Self-Timed
 - No Erase Before Write
 - No Complex Programming Algorithms
 - No Overerase Problem
- Low Power CMOS:
 - Active: 50mA
 - Standby: 500µA
- Software Data Protection
 - Protects Data Against System Level Inadvertant Writes
- High Speed Page Write Capability
- Highly Reliable Direct Write™ Cell
 - Endurance: 100,000 Write Cycles
 - Data Retention: 100 Years
- Early End of Write Detection
 - DATA Polling
 - Toggle Bit Polling

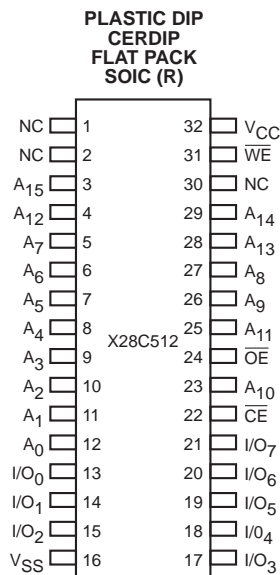
- Two PLCC and LCC Pinouts
 - X28C512
 - X28C010 E²PROM Pin Compatible
 - X28C513
 - Compatible with Lower Density E²PROMs

DESCRIPTION

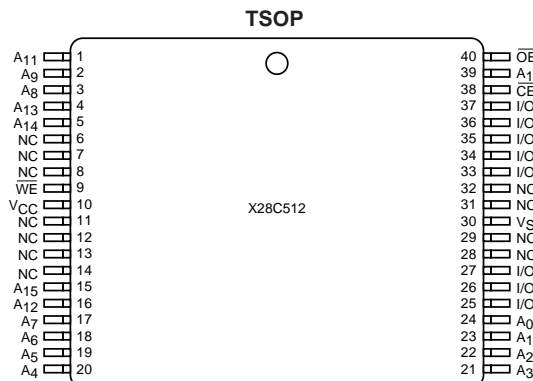
The X28C512/513 is an 64K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C512/513 is a 5V only device. The X28C512/513 features the JEDEC approved pinout for bytewise memories, compatible with industry standard EPROMS.

The X28C512/513 supports a 128-byte page write operation, effectively providing a 39µs/byte write cycle and enabling the entire memory to be written in less than 2.5 seconds. The X28C512/513 also features DATA Polling and Toggle Bit Polling, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28C512/513 supports the Software Data Protection option.

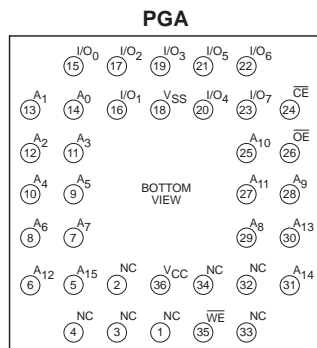
PIN CONFIGURATIONS



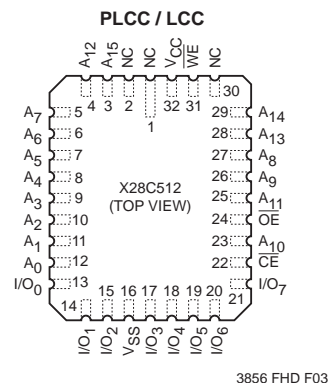
3856 FHD F01



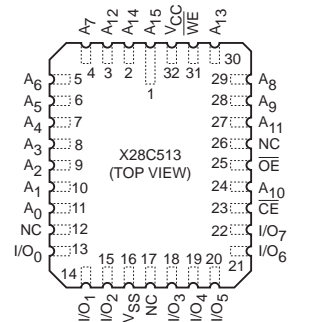
3856 ILL F22



3856 FHD F02



3856 FHD F03



3856 FHD F04

X28C512/X28C513

PIN DESCRIPTIONS

Addresses (A_0 – A_{15})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable (\overline{CE})

The Chip Enable input must be LOW to enable all read/write operations. When \overline{CE} is HIGH, power consumption is reduced.

Output Enable (\overline{OE})

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0 – I/O_7)

Data is written to or read from the X28C512/513 through the I/O pins.

Write Enable (\overline{WE})

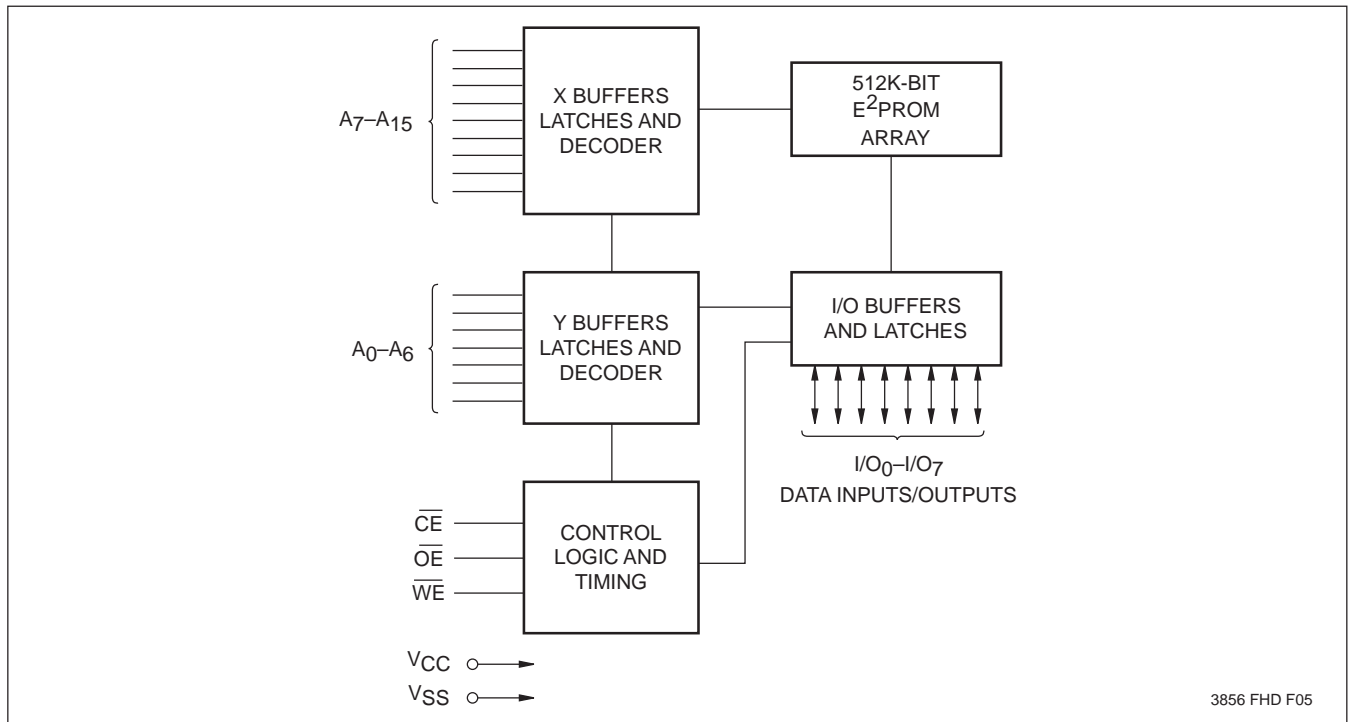
The Write Enable input controls the writing of data to the X28C512/513.

PIN NAMES

Symbol	Description
A_0 – A_{15}	Address Inputs
I/O_0 – I/O_7	Data Input/Output
\overline{WE}	Write Enable
\overline{CE}	Chip Enable
\overline{OE}	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

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FUNCTIONAL DIAGRAM



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DEVICE OPERATION

Read

Read operations are initiated by both \overline{OE} and \overline{CE} LOW. The read operation is terminated by either \overline{CE} or \overline{OE} returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either \overline{OE} or \overline{CE} is HIGH.

Write

Write operations are initiated when both \overline{CE} and \overline{WE} are LOW and \overline{OE} is HIGH. The X28C512/513 supports both a \overline{CE} and \overline{WE} controlled write cycle. That is, the address is latched by the falling edge of either \overline{CE} or \overline{WE} , whichever occurs last. Similarly, the data is latched internally by the rising edge of either \overline{CE} or \overline{WE} , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation

The page write feature of the X28C512/513 allows the entire memory to be written in 2.5 seconds. Page write allows two to one hundred twenty-eight bytes of data to be consecutively written to the X28C512/513 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_7 through A_{15}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

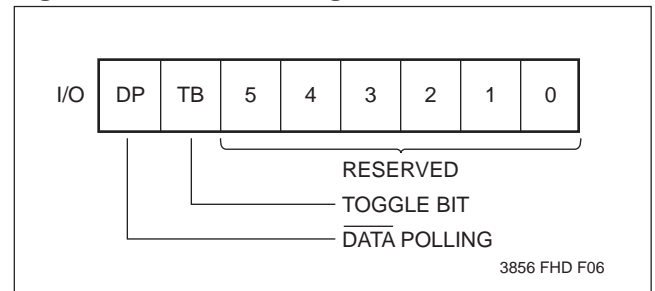
The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to one hundred twenty-seven bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the \overline{WE} HIGH to LOW transition, must begin within 100 μ s of the falling edge of the preceding \overline{WE} . If a subsequent \overline{WE} HIGH to LOW transition is not detected within 100 μ s, the internal automatic programming cycle will commence. There is no page write window limitation.

Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 μ s.

Write Operation Status Bits

The X28C512/513 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



\overline{DATA} Polling (I/O₇)

The X28C512/513 features \overline{DATA} Polling as a method to indicate to the host system that the byte write or page write cycle has completed. \overline{DATA} Polling allows a simple bit test operation to determine the status of the X28C512/513, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O₇ (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O₇ will reflect true data.

Toggle Bit (I/O₆)

The X28C512/513 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle, I/O₆ will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

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DATA Polling I/O₇

Figure 2a. DATA Polling Bus Sequence

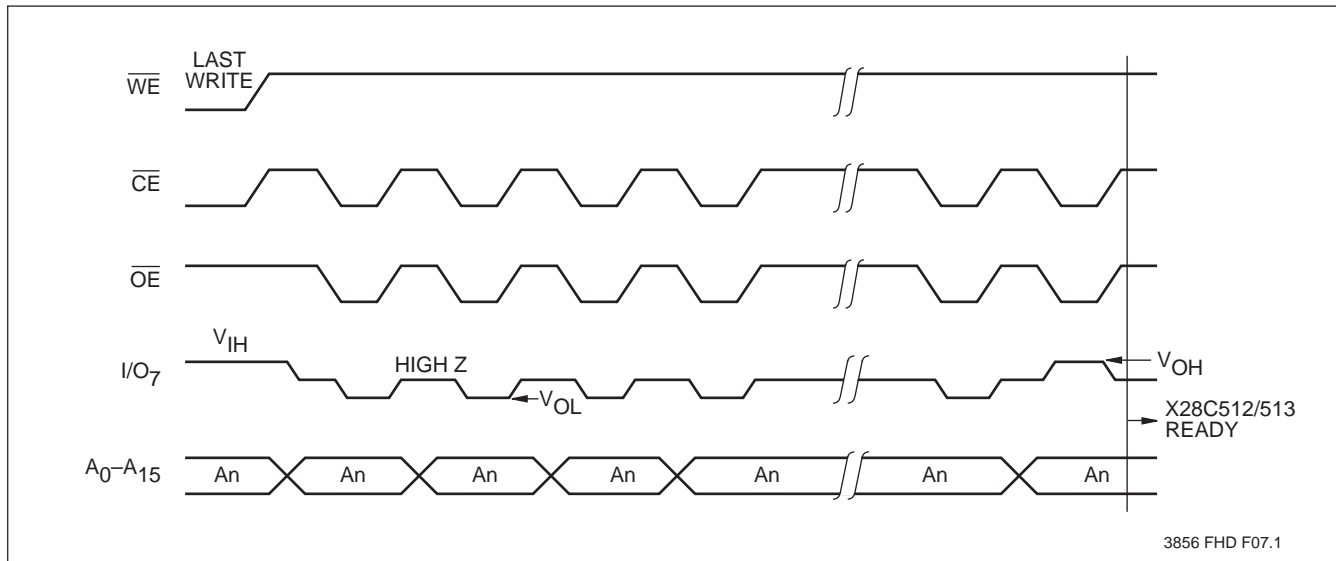
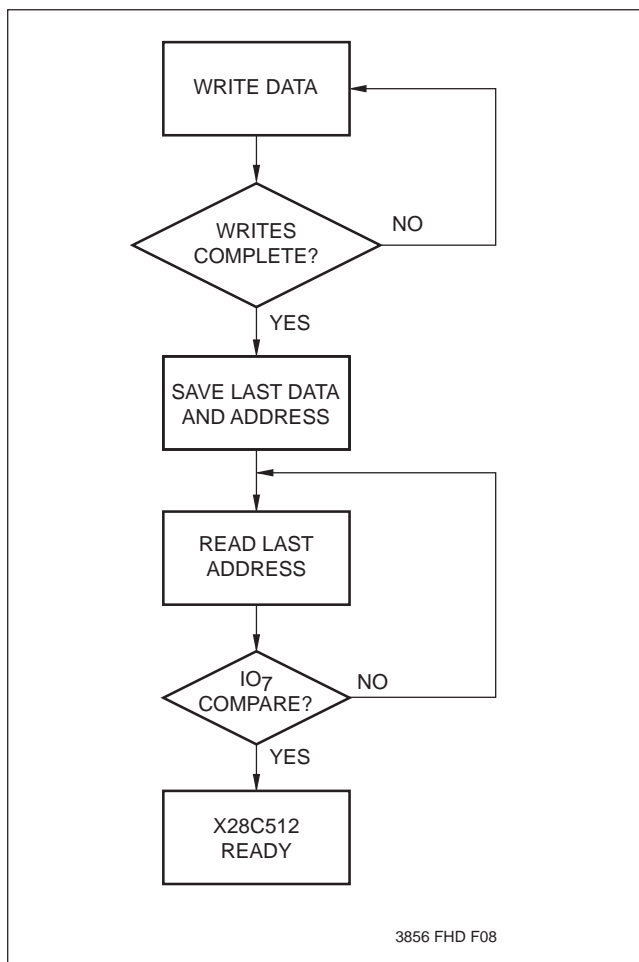


Figure 2b. DATA Polling Software Flow



DATA Polling can effectively halve the time for writing to the X28C512/513. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

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The Toggle Bit I/O₆

Figure 3a. Toggle Bit Bus Sequence

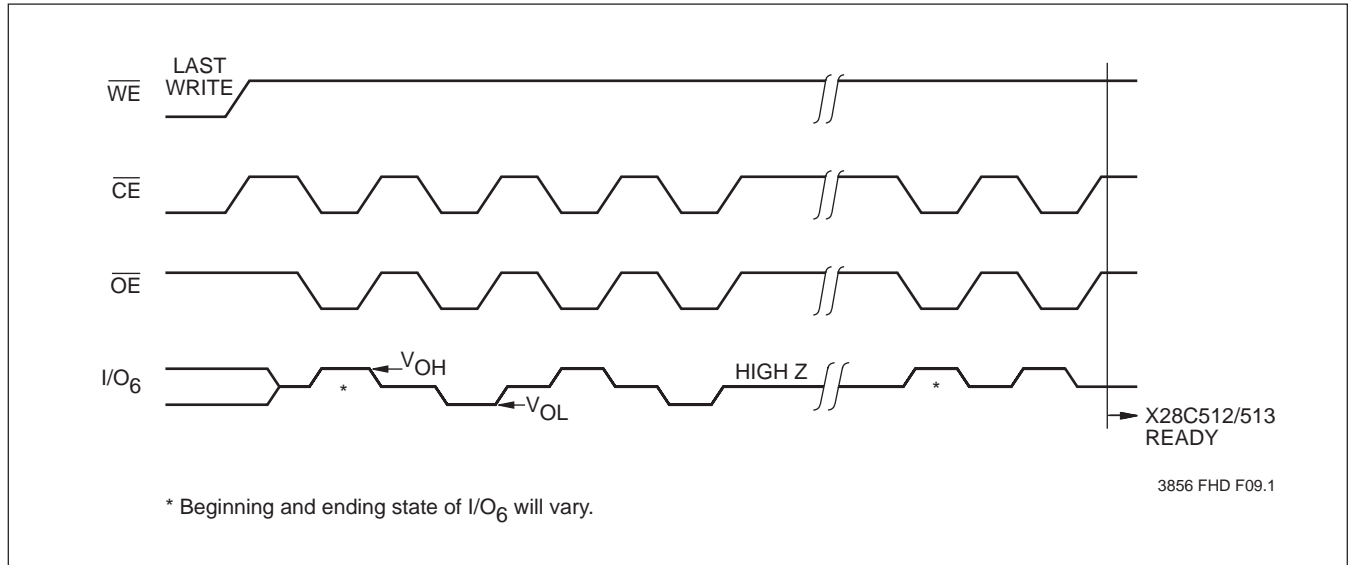
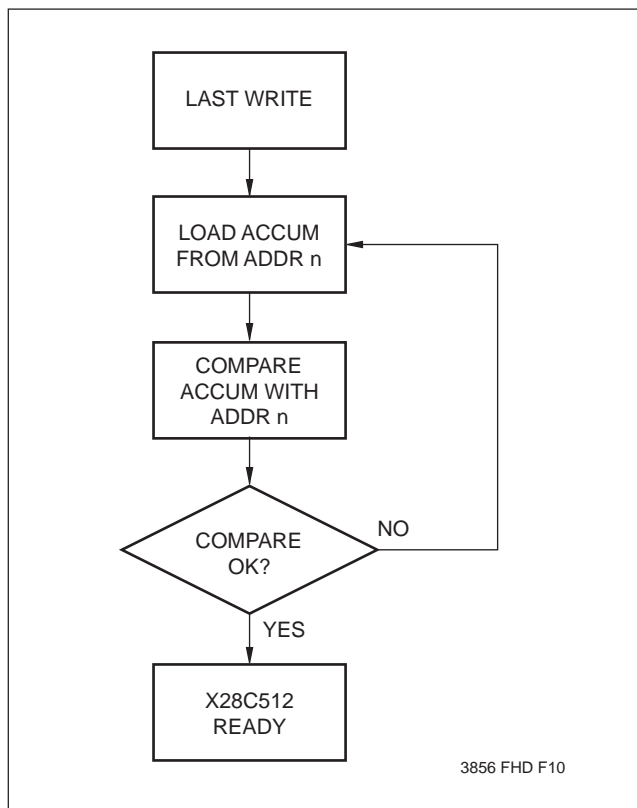


Figure 3b. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{\text{DATA}}$ Polling. This can be especially helpful in an array comprised of multiple X28C512/513 memories that is frequently updated. Toggle Bit Polling can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for polling the Toggle Bit.

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HARDWARE DATA PROTECTION

The X28C512/513 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A \overline{WE} pulse typically less than 10ns will not initiate a write cycle.
- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is $\leq 3.6V$.
- Write Inhibit—Holding either \overline{OE} LOW, \overline{WE} HIGH, or \overline{CE} HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity. Write cycle timing specifications must be observed concurrently.

SOFTWARE DATA PROTECTION

The X28C512/513 offers a software controlled data protection feature. The X28C512/513 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C512/513 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C512/513 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device. Note: The data in the three-byte enable sequence is not written to the memory array.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to one hundred twenty-eight bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

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Software Data Protection

Figure 4a. Timing Sequence—Software Data Protect Enable Sequence followed by Byte or Page Write

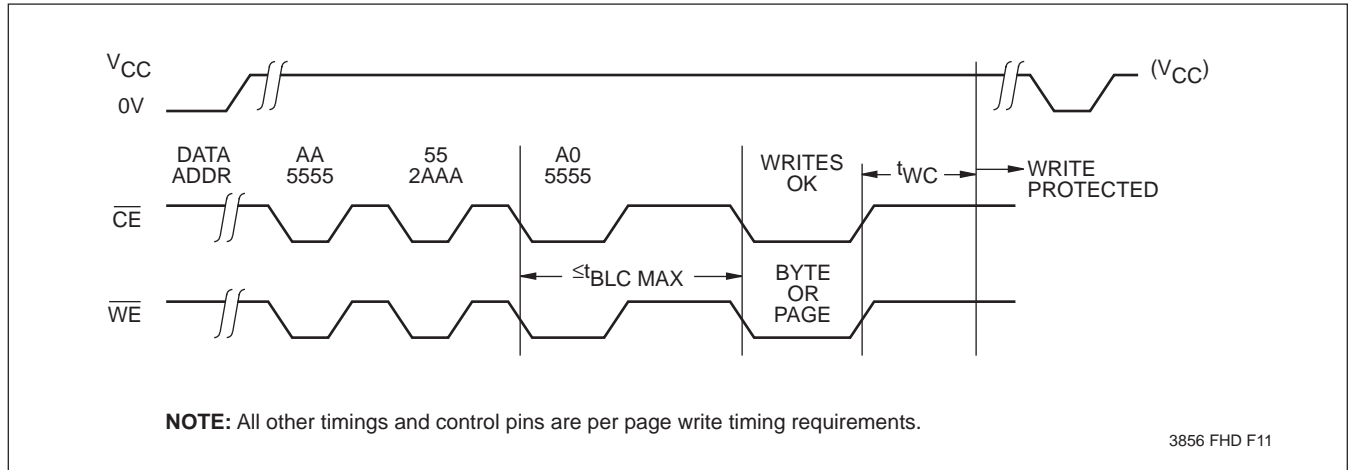
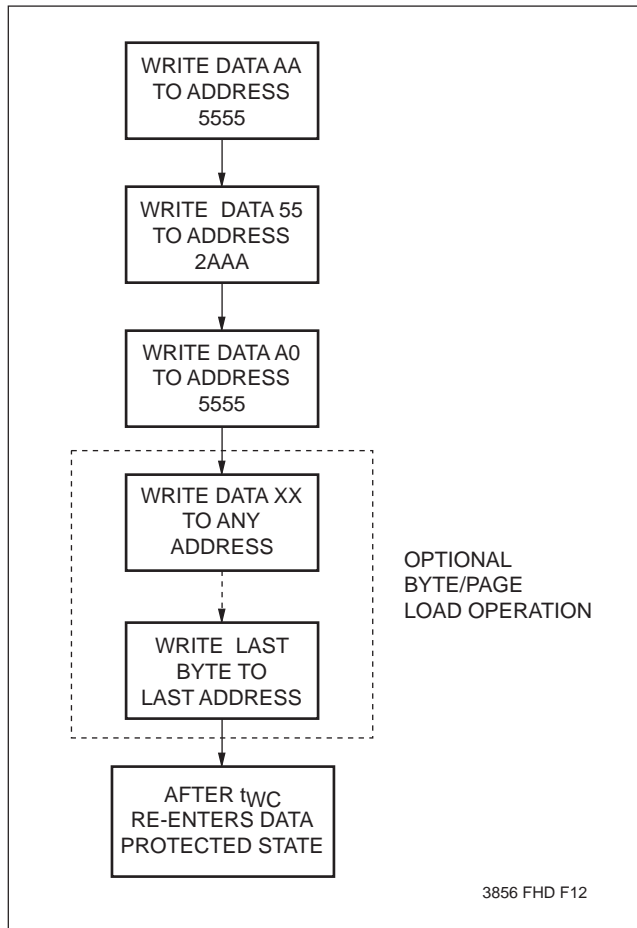


Figure 4b. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28C512/513 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C512/513 will be write protected during power-down and after any subsequent power-up. The state of A₁₅ while executing the algorithm is don't care.

Note: Once initiated, the sequence of write operations should not be interrupted.

X28C512/X28C513

Resetting Software Data Protection

Figure 5a. Reset Software Data Protection Timing Sequence

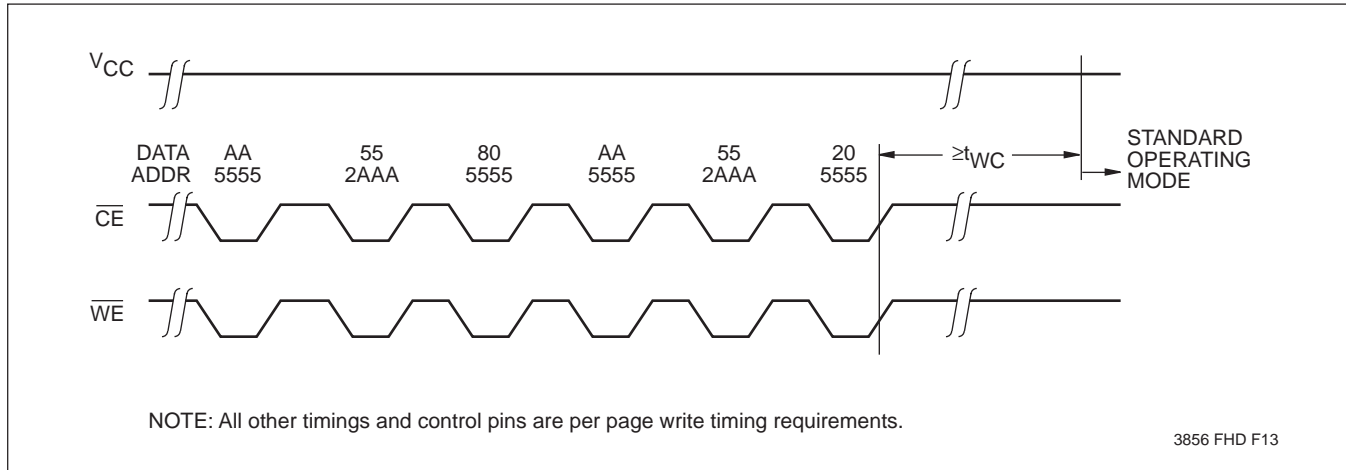
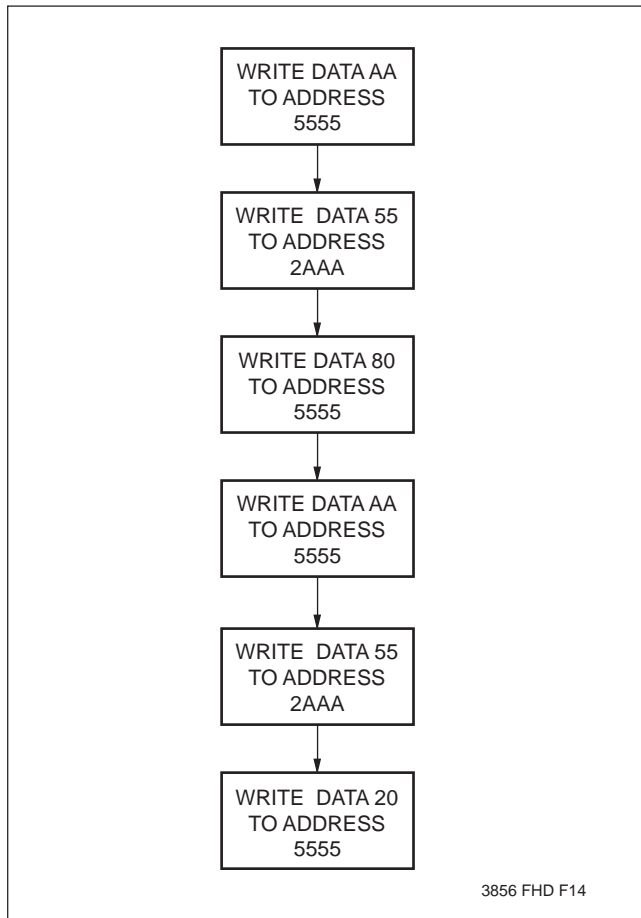


Figure 5b. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC} , the X28C512/513 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

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SYSTEM CONSIDERATIONS

Because the X28C512/513 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

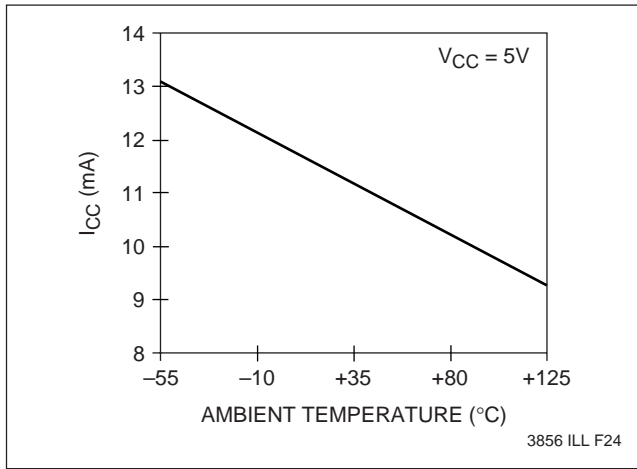
To gain the most benefit it is recommended that \overline{CE} be decoded from the address bus and be used as the primary device selection input. Both \overline{OE} and \overline{WE} would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C512/513 has two power modes, standby and active, proper decoupling of the memory

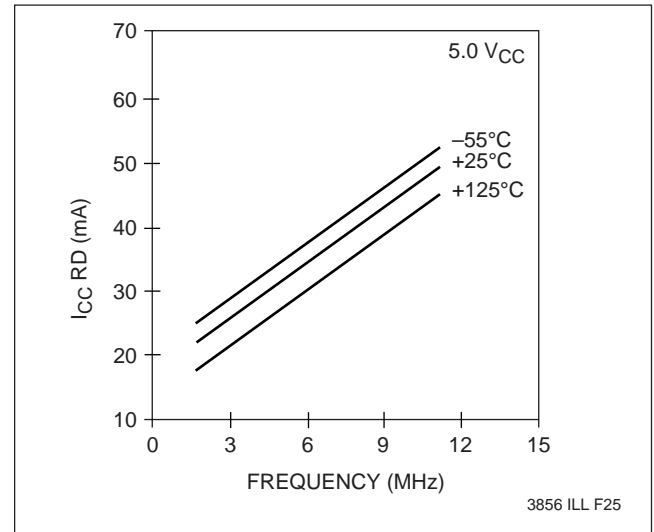
array is of prime concern. Enabling \overline{CE} will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μ F high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μ F electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

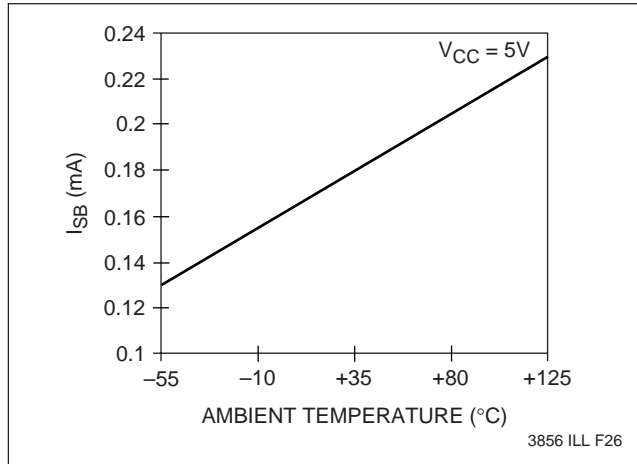
Active Supply Current vs. Ambient Temperature



I_{CC} (RD) by Temperature over Frequency



Standby Supply Current vs. Ambient Temperature



X28C512/X28C513

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias	
X28C512/513	-10°C to +85°C
X28C512I/513I	-65°C to +135°C
X28C512M/513M	-65°C to +135°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with	
Respect to V _{SS}	-1V to +7V
D.C. Output Current	5mA
Lead Temperature	
(Soldering, 10 seconds)	300°C

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMEND OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

3856 PGM T02

Supply Voltage	Limits
X28C512/513	5V ±10%

3856 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I _{CC}	V _{CC} Current (Active) (TTL Inputs)		50	mA	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$, All I/O's = Open, Address Inputs = .4V/2.4V Levels @ f = 5MHz
I _{SB1}	V _{CC} Current (Standby) (TTL Inputs)		3	mA	$\overline{CE} = V_{IH}, \overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V _{IH}
I _{SB2}	V _{CC} Current (Standby) (CMOS Inputs)		500	μA	$\overline{CE} = V_{CC} - 0.3V, \overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V _{IH}
I _{LI}	Input Leakage Current		10	μA	V _{IN} = V _{SS} to V _{CC}
I _{LO}	Output Leakage Current		10	μA	V _{OUT} = V _{SS} to V _{CC} , $\overline{CE} = V_{IH}$
V _{IL} (1)	Input LOW Voltage	-1	0.8	V	
V _{IH} (1)	Input HIGH Voltage	2	V _{CC} + 1	V	
V _{OL}	Output LOW Voltage		0.4	V	I _{OL} = 2.1mA
V _{OH}	Output HIGH Voltage	2.4		V	I _{OH} = -400μA

3856 PGM T04.2

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

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POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(2)}$	Power-up to Read Operation	100	μs
$t_{PUW}^{(2)}$	Power-up to Write Operation	5	ms

3856 PGM T05

CAPACITANCE $T_A = +25^\circ\text{C}$, $f = 1\text{MHz}$, $V_{CC} = 5\text{V}$

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}^{(2)}$	Input/Output Capacitance	10	pF	$V_{I/O} = 0\text{V}$
$C_{IN}^{(2)}$	Input Capacitance	10	pF	$V_{IN} = 0\text{V}$

3856 PGM T06.1

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance	10,000		Cycles Per Byte
Endurance	100,000		Cycles Per Page
Data Retention	100		Years

3856 PGM T07.1

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

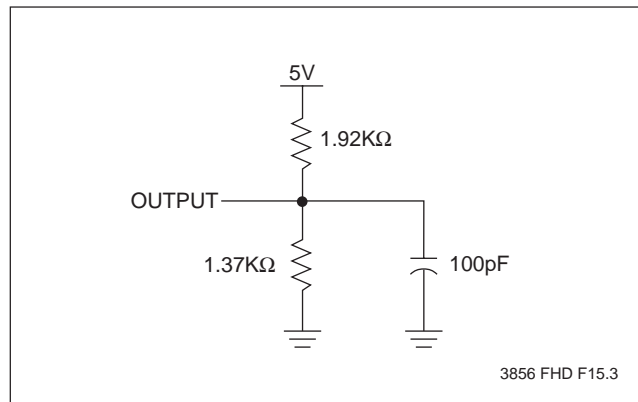
3856 PGM T07.1

MODE SELECTION

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3856 PGM T08

EQUIVALENT A.C. LOAD CIRCUIT



Note: (2) This parameter is periodically sampled and not 100% tested.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

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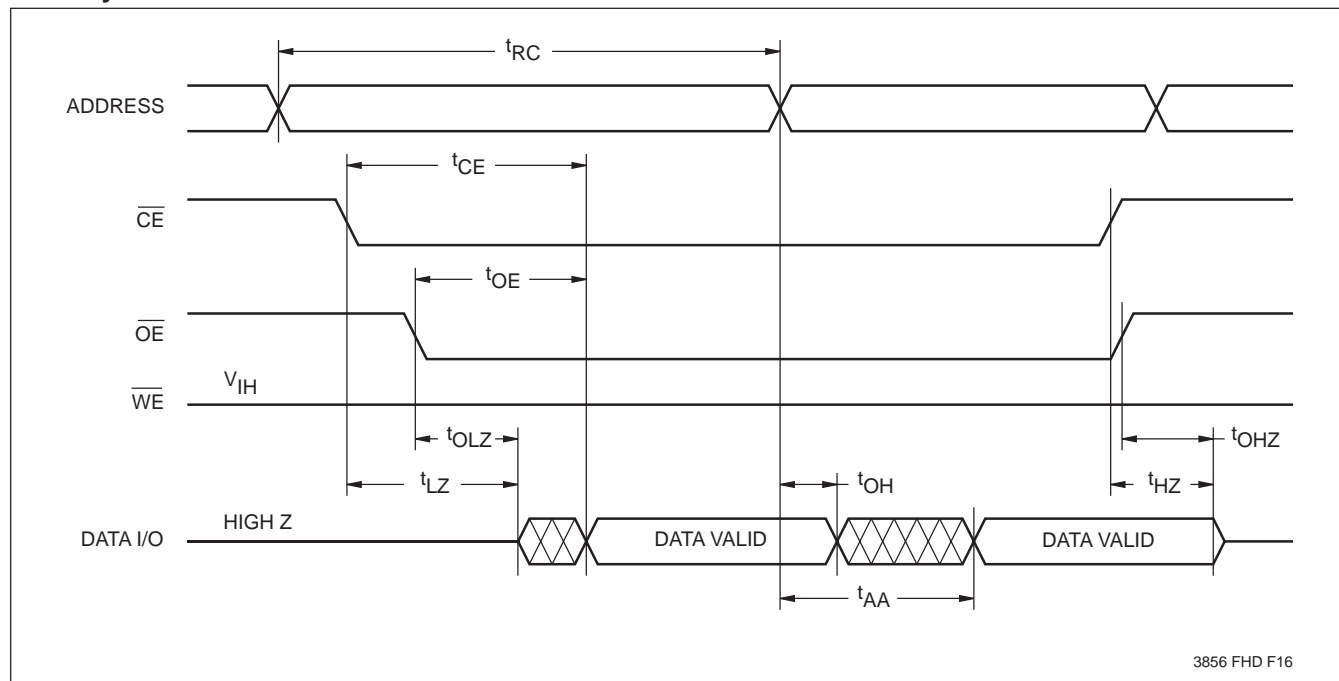
A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	X28C512-90 X28C513-90		X28C512-12 X28C513-12		X28C512-15 X28C513-15		X28C512-20 X28C513-20		X28C512-25 X28C513-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	90		120		150		200		250		ns
t_{CE}	Chip Enable Access Time		90		120		150		200		250	ns
t_{AA}	Address Access Time		90		120		150		200		250	ns
t_{OE}	Output Enable Access Time		40		50		50		50		50	ns
$t_{LZ}^{(3)}$	\overline{CE} LOW to Active Output	0		0		0		0		0		ns
$t_{OLZ}^{(3)}$	\overline{OE} LOW to Active Output	0		0		0		0		0		ns
$t_{HZ}^{(3)}$	\overline{CE} HIGH to High Z Output		40		50		50		50		50	ns
$t_{OHZ}^{(3)}$	\overline{OE} HIGH to High Z Output		40		50		50		50		50	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		0		ns

3856 PGM T09.4

Read Cycle



3856 FHD F16

Notes: (3) t_{LZ} min., t_{HZ} , t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with $C_L = 5\text{pF}$ from the point when \overline{CE} or \overline{OE} return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

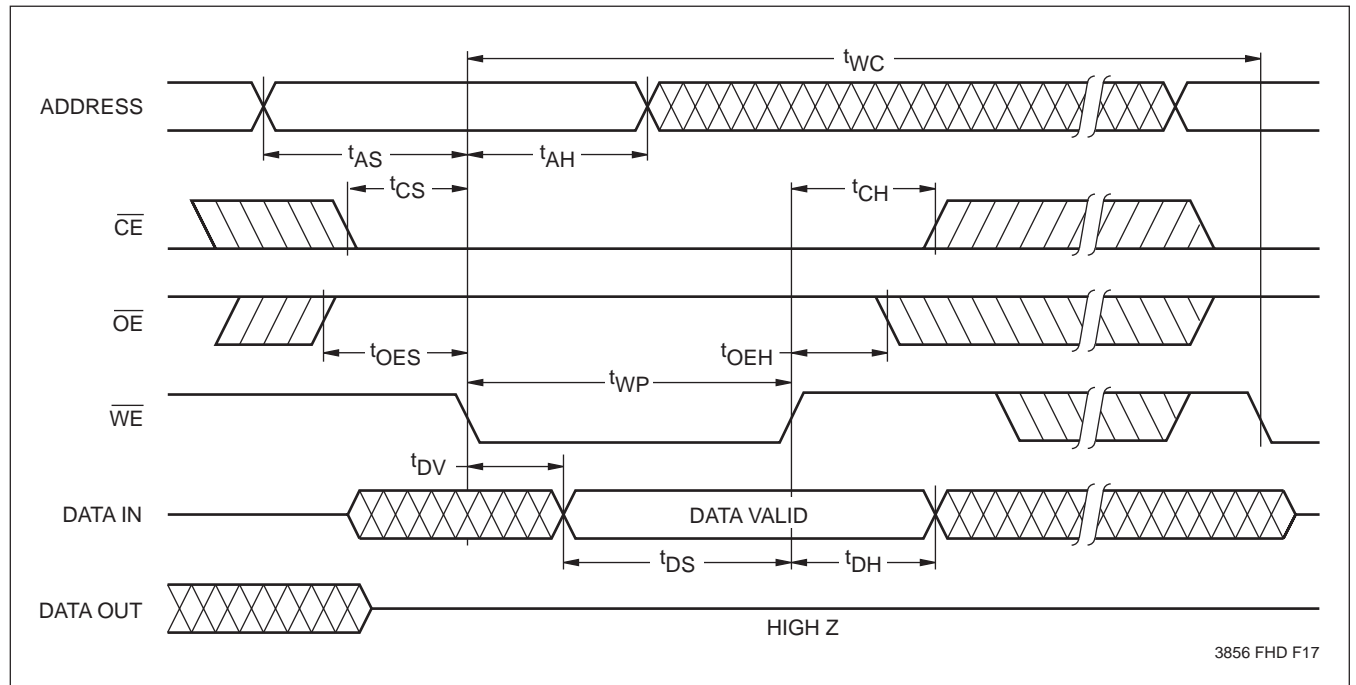
X28C512/X28C513

WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Max.	Units
$t_{WC}^{(4)}$	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	\overline{CE} Pulse Width	100		ns
t_{OES}	\overline{OE} HIGH Setup Time	10		ns
t_{OEH}	\overline{OE} HIGH Hold Time	10		ns
t_{WP}	\overline{WE} Pulse Width	100		ns
t_{WPH}	\overline{WE} HIGH Recovery	100		ns
t_{DV}	Data Valid		1	μ s
t_{DS}	Data Setup	50		ns
t_{DH}	Data Hold	0		ns
t_{DW}	Delay to Next Write	10		μ s
t_{BLC}	Byte Load Cycle	0.2	100	μ s

3856 PGM T10.2

\overline{WE} Controlled Write Cycle

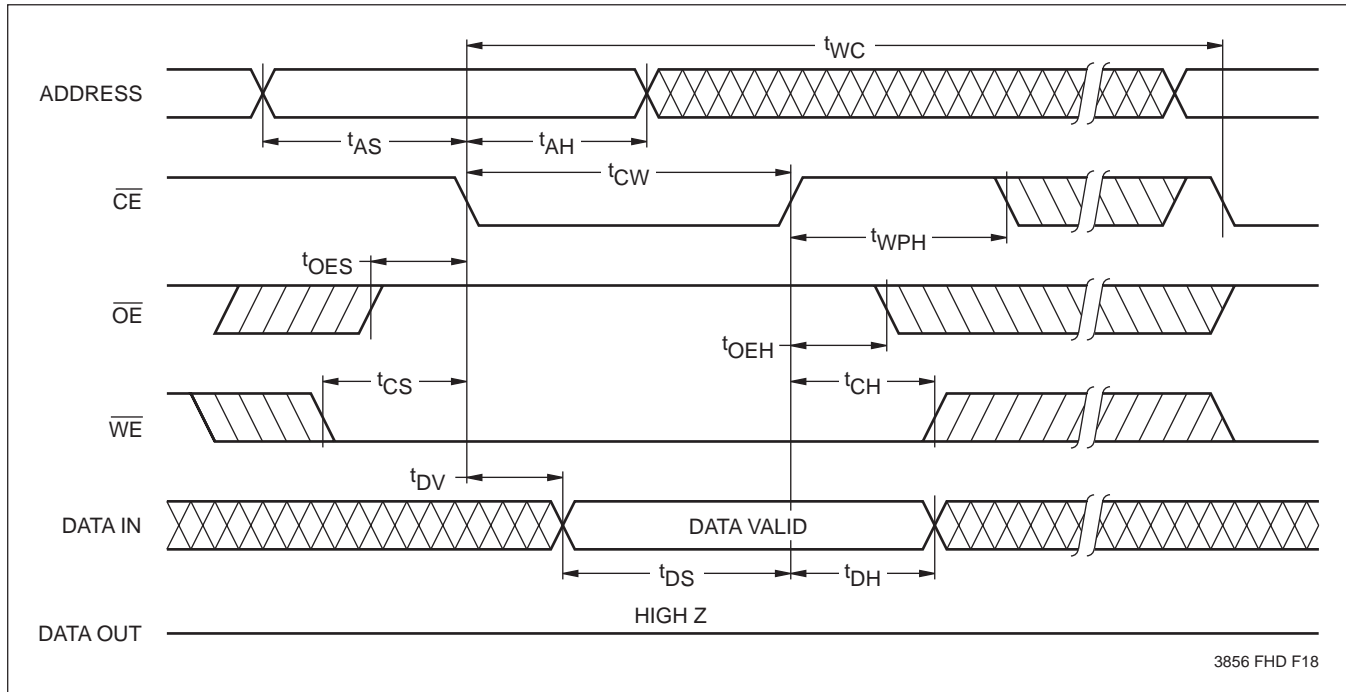


3856 FHD F17

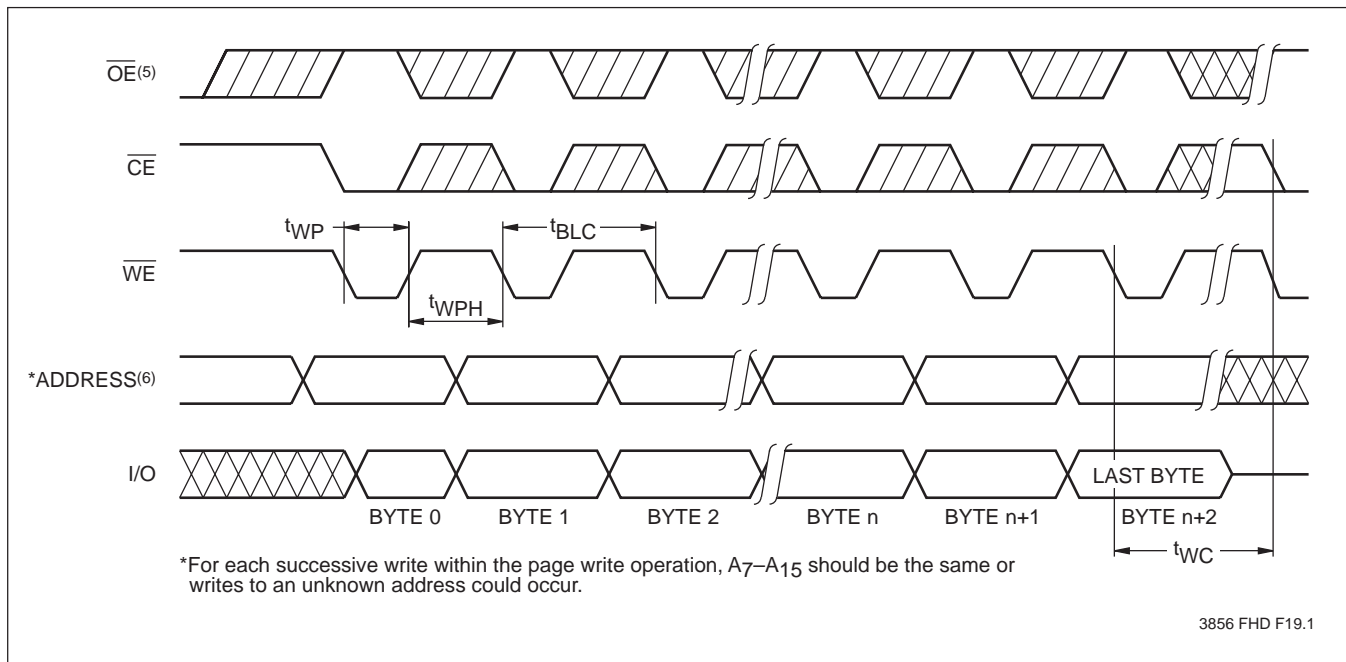
Notes: (4) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete the internal write operation.

X28C512/X28C513

\overline{CE} Controlled Write Cycle



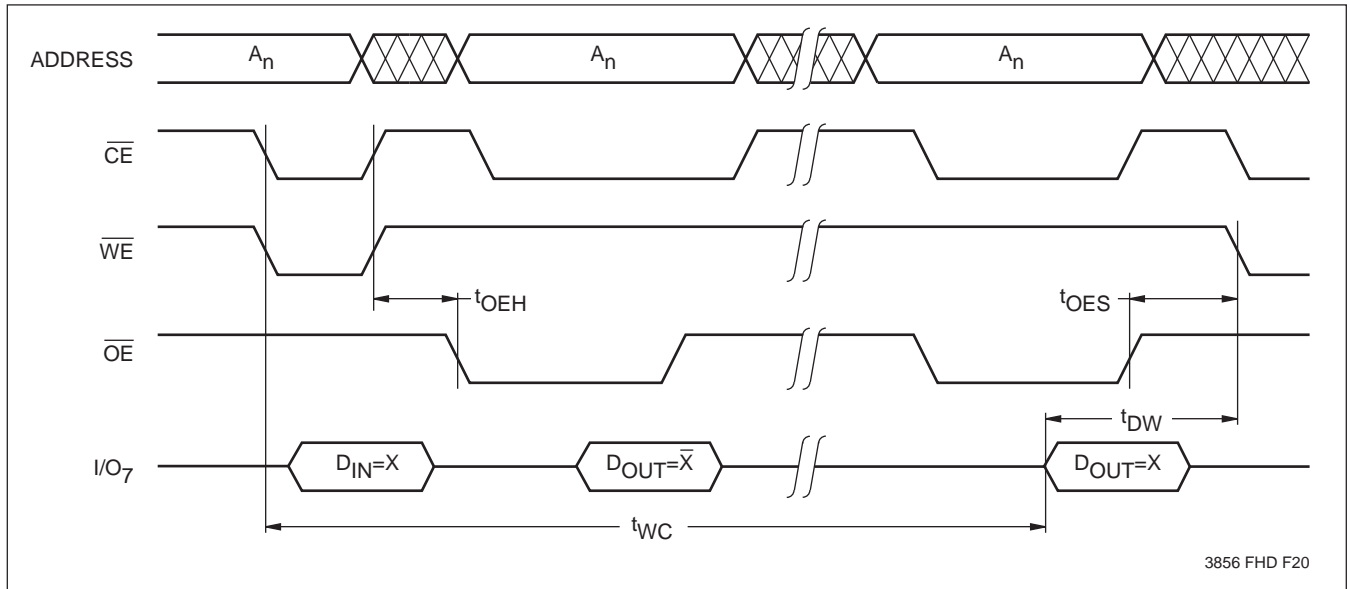
Page Write Cycle



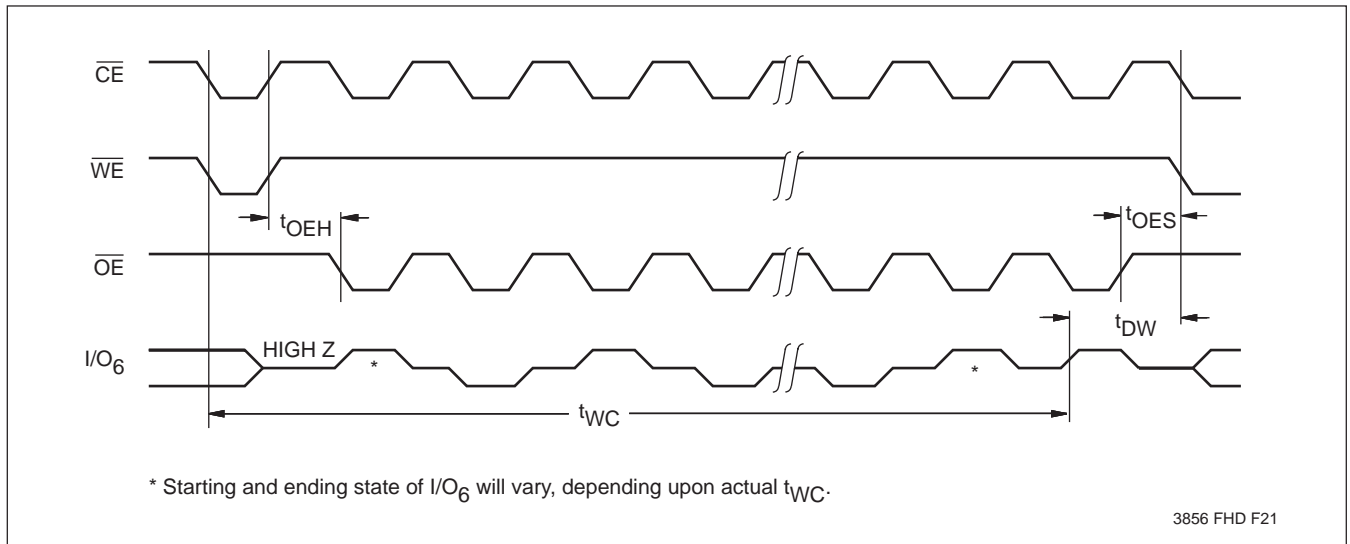
- Notes:**
- (5) Between successive byte writes within a page write operation, \overline{OE} can be strobed LOW: e.g. this can be done with \overline{CE} and \overline{WE} HIGH to fetch data from another memory device within the system for the next write; or with \overline{WE} HIGH and \overline{CE} LOW effectively performing a polling operation.
 - (6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the \overline{CE} or \overline{WE} controlled write cycle timing.

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DATA Polling Timing Diagram(7)



Toggle Bit Timing Diagram



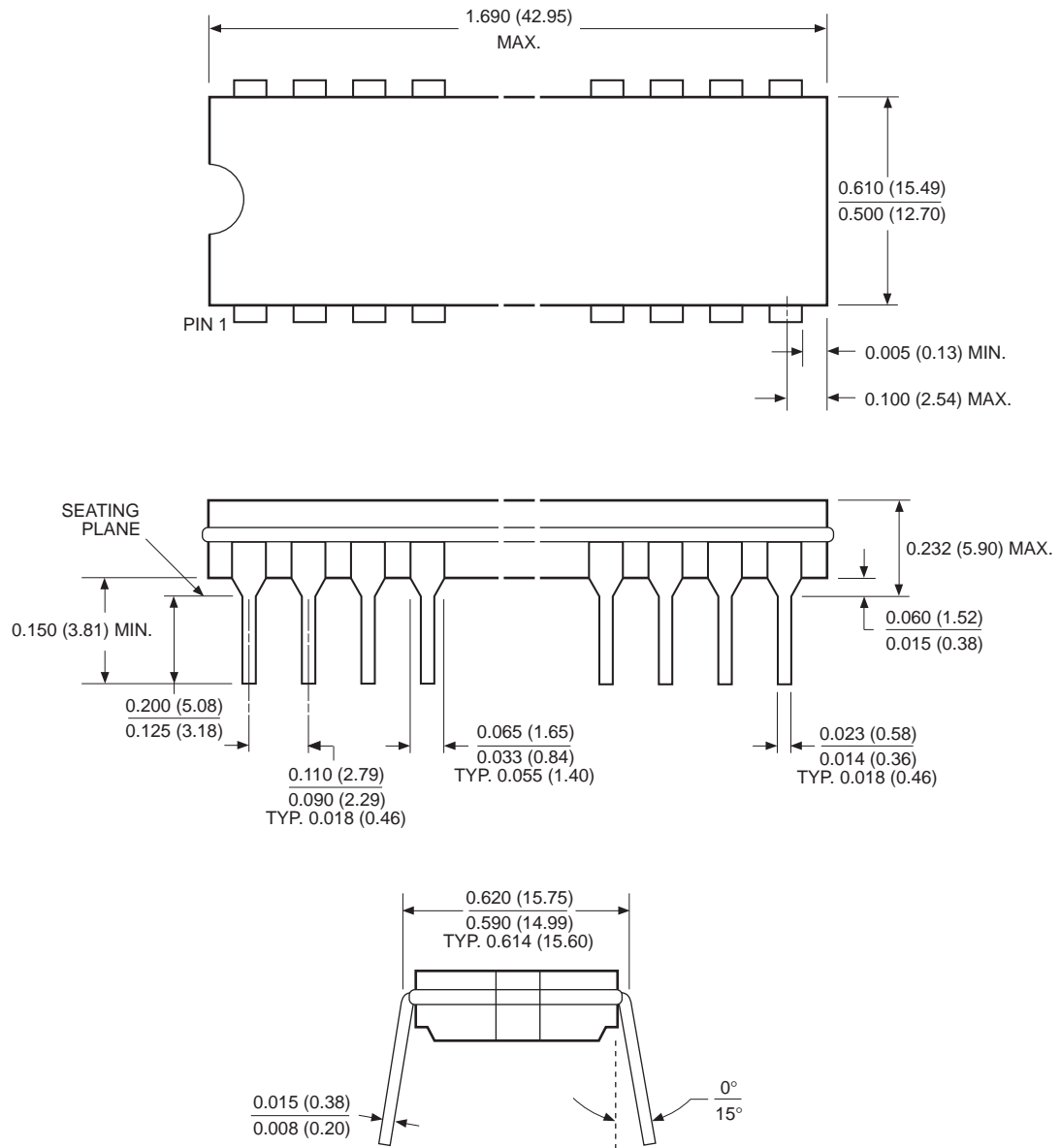
Note: (7) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

NOTES

X28C512/X28C513

PACKAGING INFORMATION

32-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



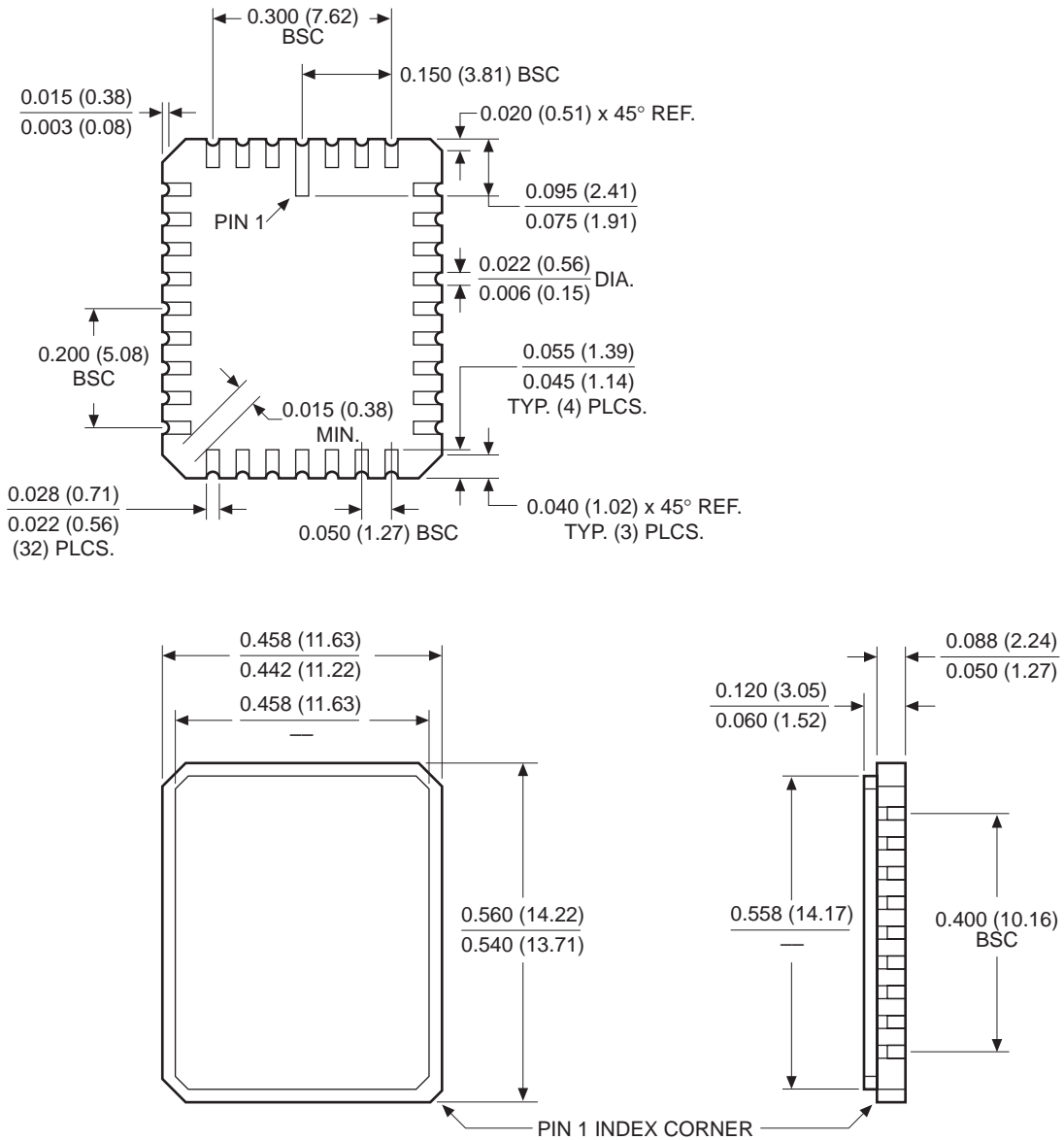
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F09

X28C512/X28C513

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E



NOTE:

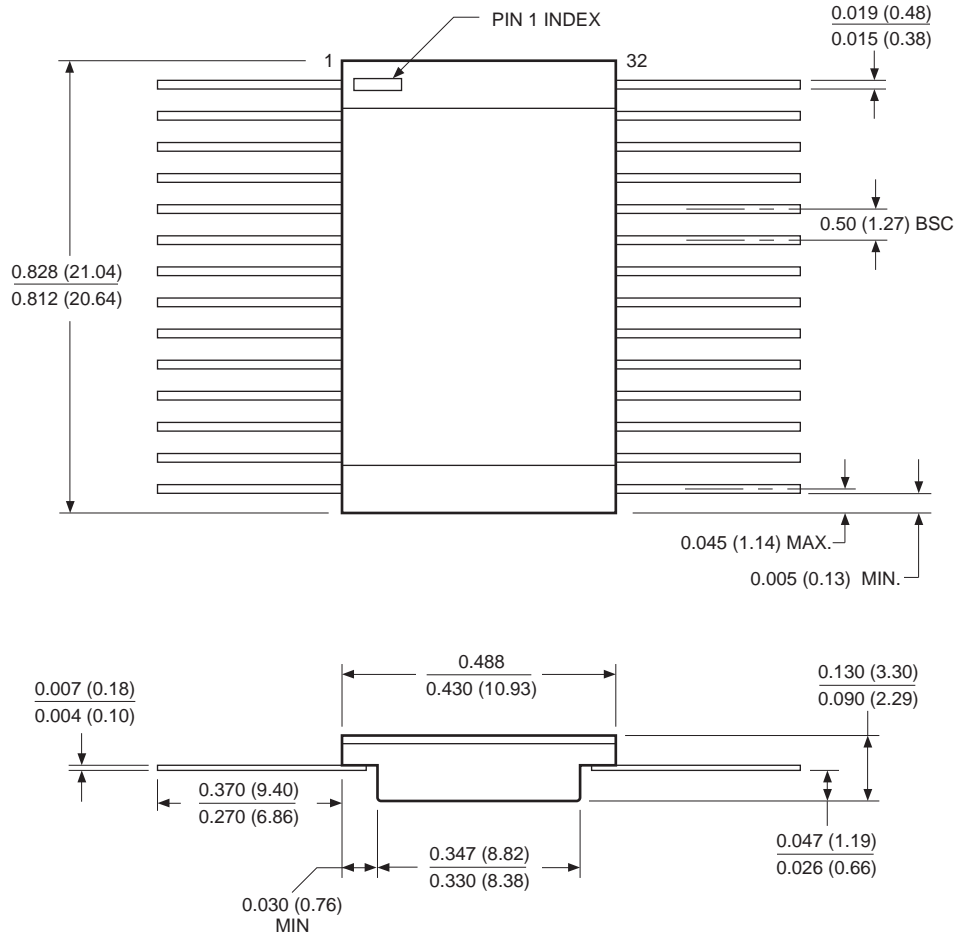
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: $\pm 1\%$ NLT ± 0.005 (0.127)

3926 FHD F14

X28C512/X28C513

PACKAGING INFORMATION

32-LEAD CERAMIC FLAT PACK TYPE F



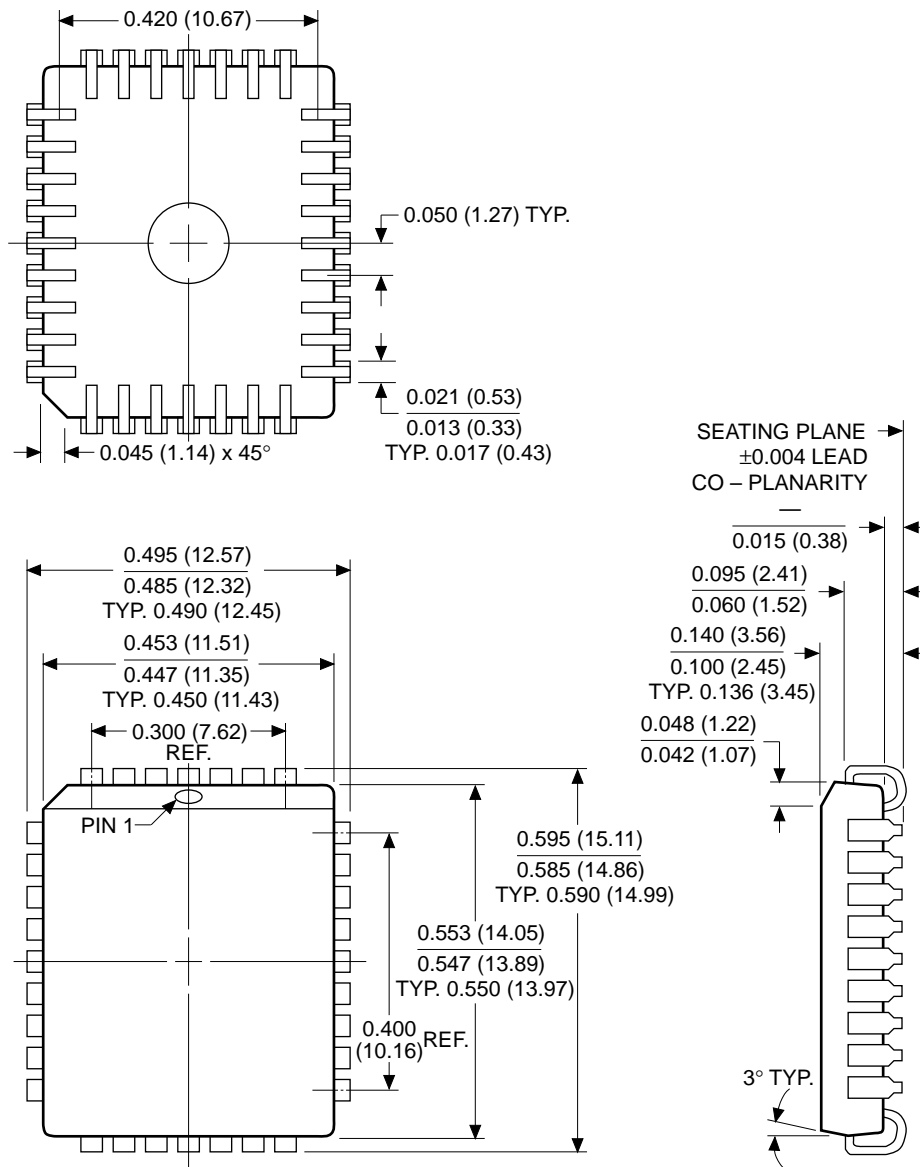
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F20

X28C512/X28C513

PACKAGING INFORMATION

32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J



NOTES:

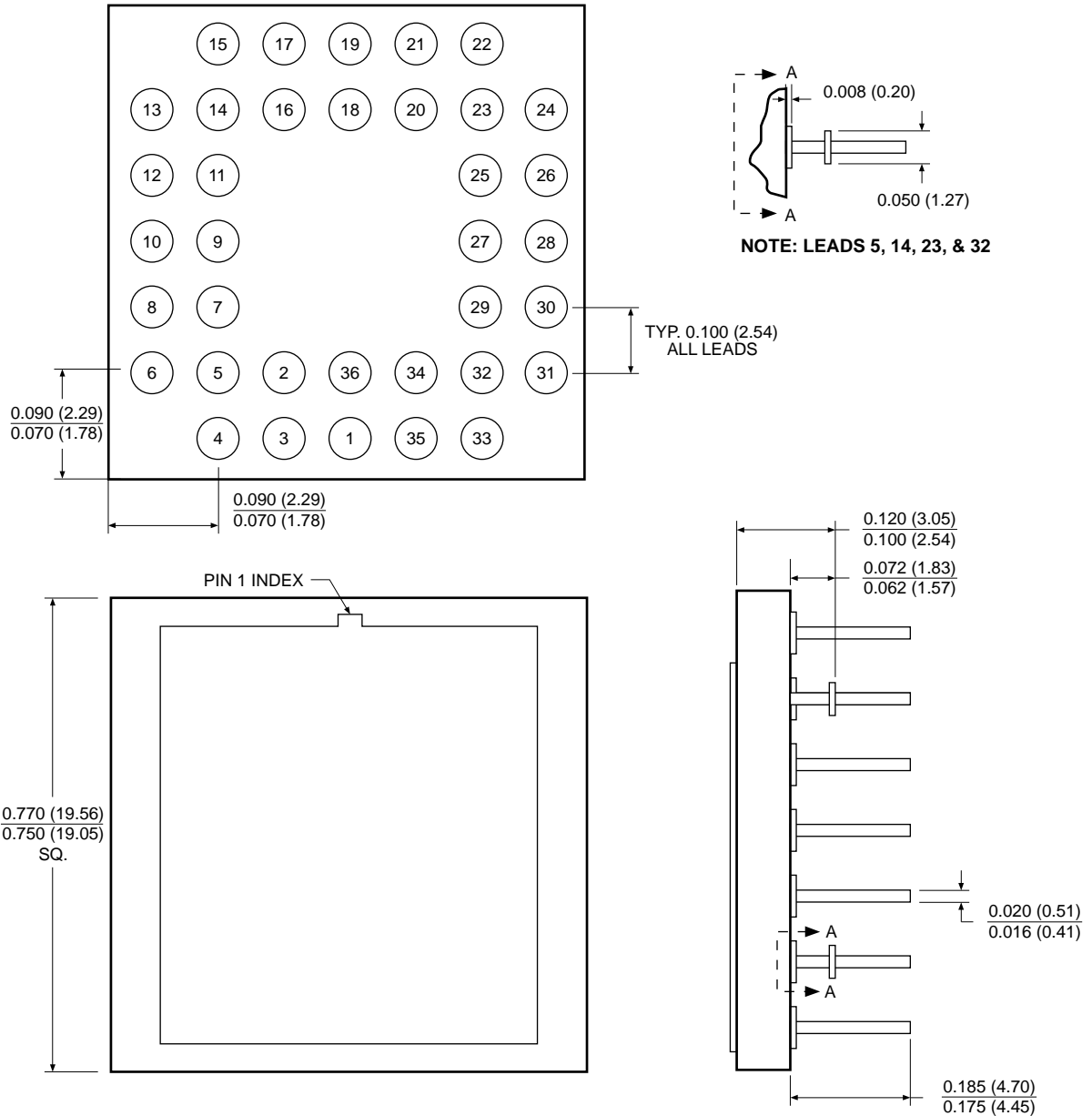
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

3926 FHD F13

X28C512/X28C513

PACKAGING INFORMATION

36-LEAD CERAMIC PIN GRID ARRAY PACKAGE TYPE K

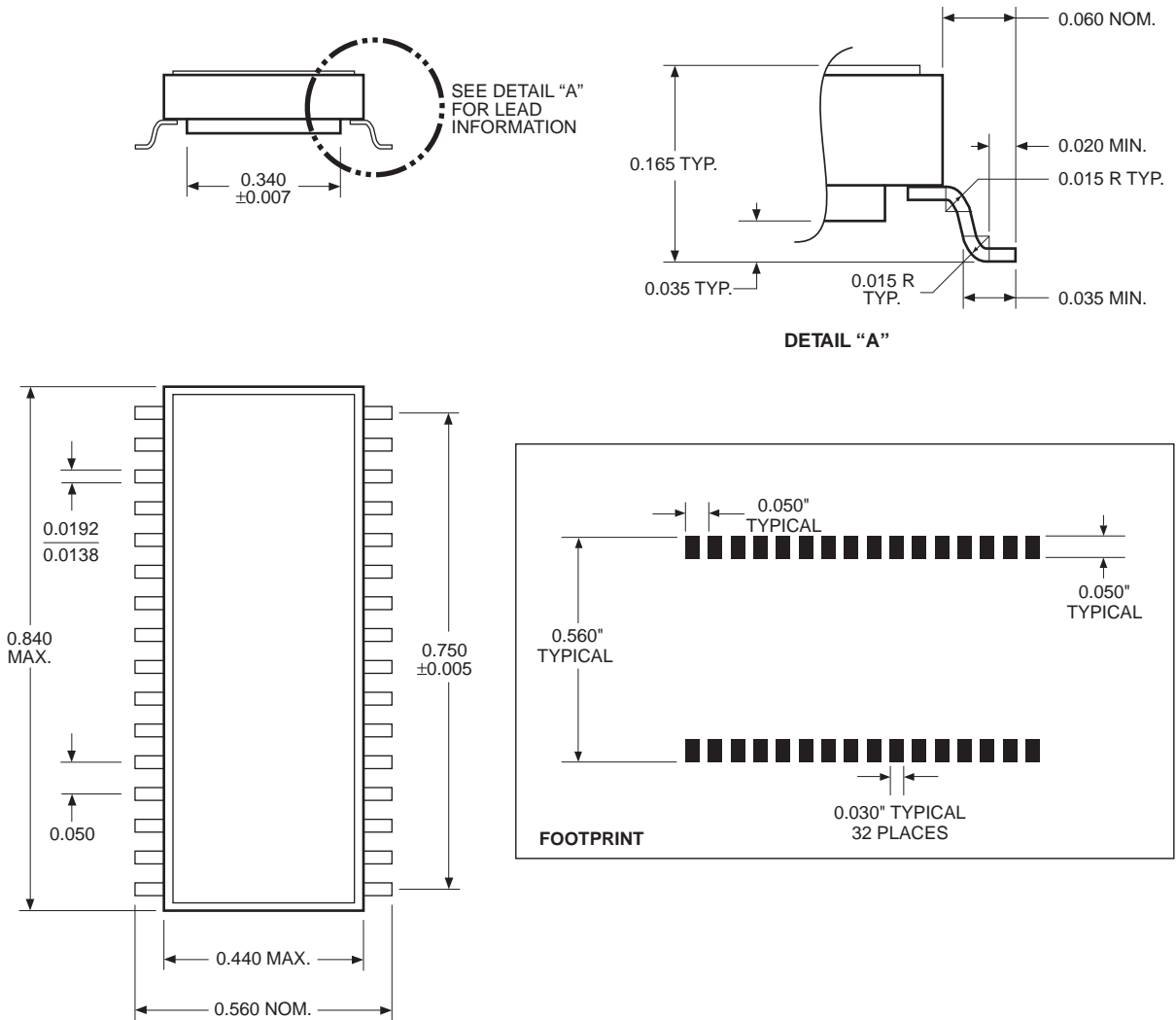


3926 FHD F21

X28C512/X28C513

PACKAGING INFORMATION

32-LEAD CERAMIC SMALL OUTLINE GULL WING PACKAGE TYPE R



NOTES:

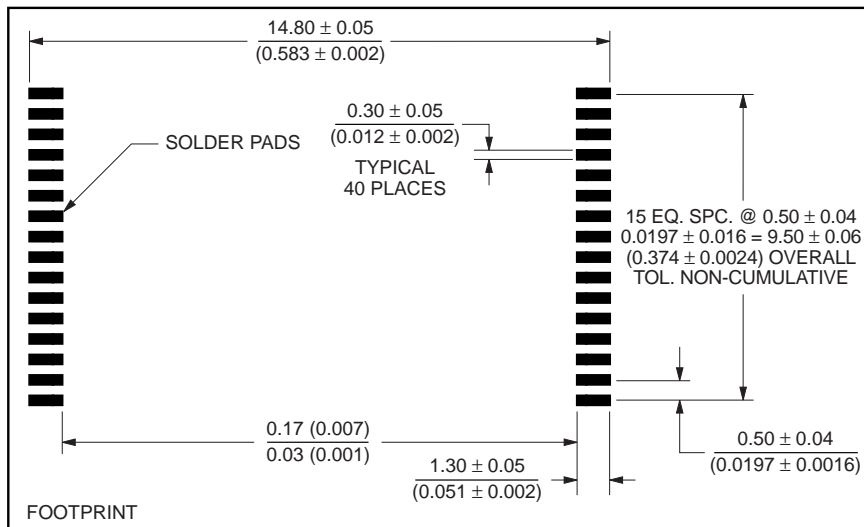
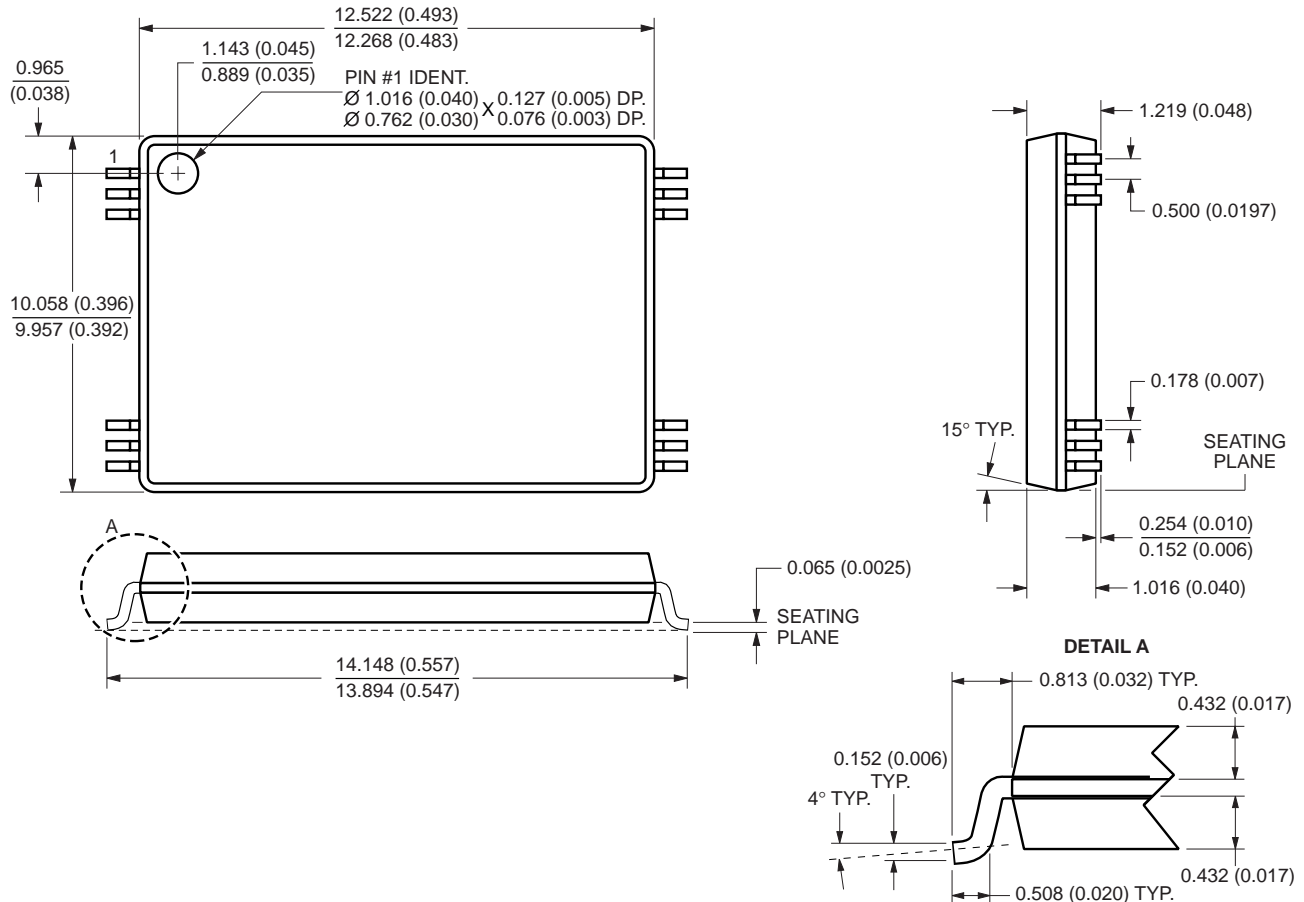
1. ALL DIMENSIONS IN INCHES
2. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.004 INCHES

3926 FHD F27

X28C512/X28C513

PACKAGING INFORMATION

40-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) TYPE T

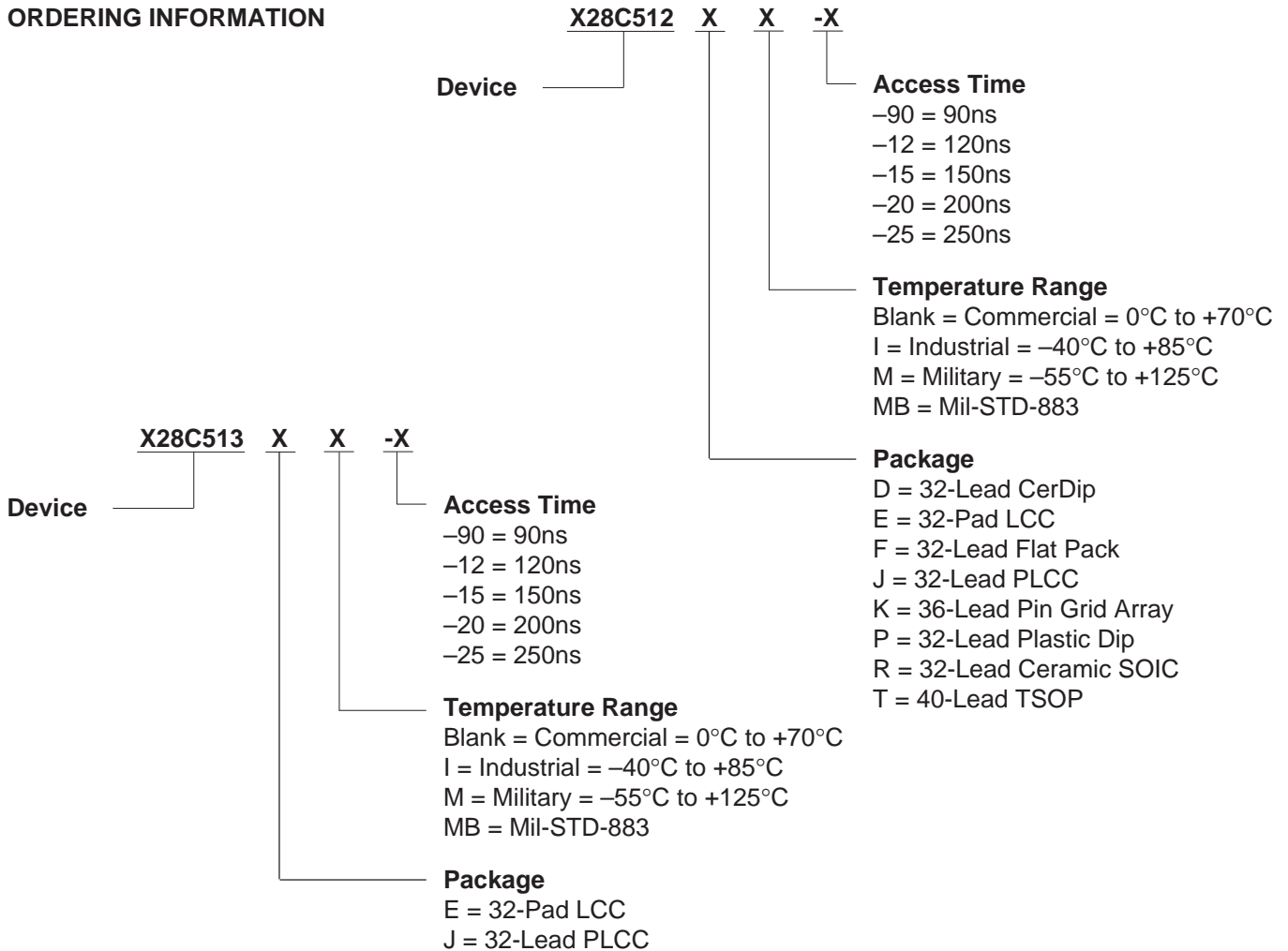


NOTE:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES IN PARENTHESES).

3926 ILL F39.2

X28C512/X28C513

ORDERING INFORMATION



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US. PATENTS

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.