4K X84041 MPS™ E²PROM

Micro Port Saver E²PROM

FEATURES

- **Direct Interface to Micros**
  - **—Eliminates I/O port requirements**
  - **—No interface glue logic required**
  - **—Eliminates need for parallel to serial converters**
- **3.3Mbps data transfer rate**
- **Low Power CMOS**
  - **—2.7V to 5.5V Operation**
  - **—Standby Current Less than 50μA**
  - **—Active Current Less than 1mA**
- **45ns Read Access Time**
- **8-Byte Page Write Mode**
- **Typical Nonvolatile Write Cycle Time: 5ms**
- **High Reliability**
  - **—100,000 Endurance Cycles**
  - **—Guaranteed Data Retention: 100 Years**
- **8-Lead PDIP, 8-Lead SOIC, and 14-Lead TSSOP Packages**

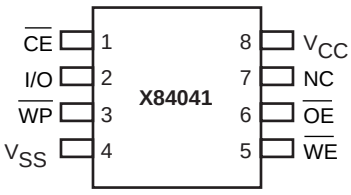
DESCRIPTION

The X84041 Micro Port Saver is a 4096-bit CMOS E²PROM designed for a direct interface to port limited microcontroller or I/O limited microprocessor designs. The X84041 provides all of the benefits of serial memories, such as low cost, low power, low voltage operation, and small package size, while featuring higher data transfer rates and reduced interface code requirements—without the need for a dedicated serial bus. The X84041 is organized as a 512 x 8, but is also suitable in 16-bit or 32-bit environments, due to the bit serial nature of the interface.

The X84041 directly connects to the processor bus and communicates over a single data line using a sequence of standard bus read and write operations. This eliminates the need for dedicated port pins, parallel to serial converters, complicated ASIC implementations, or other glue logic, lowering system cost.

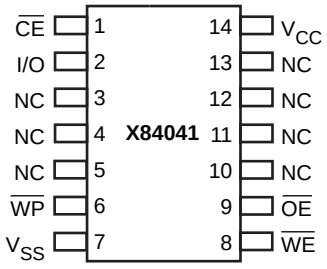
PIN CONFIGURATION

DIP/SOIC



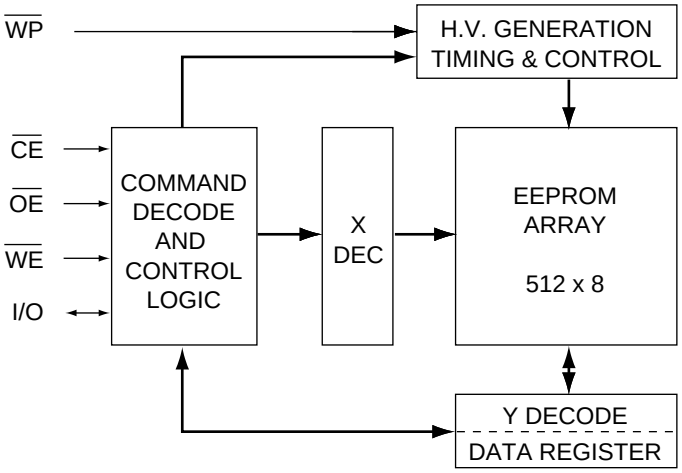
2704 ILL F01.2

TSSOP



2704 ILL F02a.1

BLOCK DIAGRAM



2704 ILL F02

PIN NAMES

I/O	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{WP}$	Write Protect Input
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	No Connect

2704 PGM T01

A Write Protect ($\overline{WP}$) pin provides hardware protection against inadvertent writes to the memory.

Xicor E^{2}PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

PIN DESCRIPTIONS

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, the chip is deselected, the I/O pin is in the high impedance state, and unless a nonvolatile write operation is underway, the X84041 is in the standby power mode.

Output Enable ($\overline{OE}$)

The Output Enable input must be LOW to enable the output buffer and to read data from the X84041 on the I/O line.

Write Enable ($\overline{WE}$)

The Write Enable input must be LOW to write either data or command sequences to the X84041.

Data In/Data Out (I/O)

Data and command sequences are serially written to or serially read from the X84041 through the I/O pin.

Write Protect ($\overline{WP}$)

When the Write Protect input is LOW, nonvolatile writes to the X84041 are disabled. When $\overline{WP}$ is HIGH, all functions, including nonvolatile writes, operate normally. If a nonvolatile write cycle is in progress, $\overline{WP}$ going LOW will have no effect on the cycle already underway, but will inhibit any additional nonvolatile write cycles.

DEVICE OPERATION

The X84041 is a serial 512 x 8 bit E^{2}PROM designed to interface directly with most microprocessor buses. Standard $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ signals control the read and write operations, and a single I/O line is used to send and receive data and commands serially.

Data Timing

Data input on the I/O line is latched on the rising edge of either $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Data output on the I/O line is active whenever both $\overline{OE}$ and $\overline{CE}$ are LOW. Care should be taken to ensure that $\overline{WE}$ and $\overline{OE}$ are never both LOW while $\overline{CE}$ is LOW.

Read Sequence

A read sequence consists of sending a 16-bit address followed by the reading of data serially. The address is written by issuing 16 separate write cycles ($\overline{WE}$ and $\overline{CE}$ LOW, $\overline{OE}$ HIGH) to the part without a read cycle between the write cycles. The address is sent serially, most significant bit first, over the I/O line. Note that this sequence is fully static, with no special timing restrictions, and the processor is free to perform other tasks on the bus whenever the X84041 $\overline{CE}$ pin is HIGH. Once the 16 address bits are sent, a byte of data can be read on the I/O line by issuing 8 separate read cycles ($\overline{OE}$ and $\overline{CE}$ LOW, $\overline{WE}$ HIGH). At this point, issuing a reset sequence will terminate the read sequence, otherwise the X84041 will await further reads in the sequential read mode.

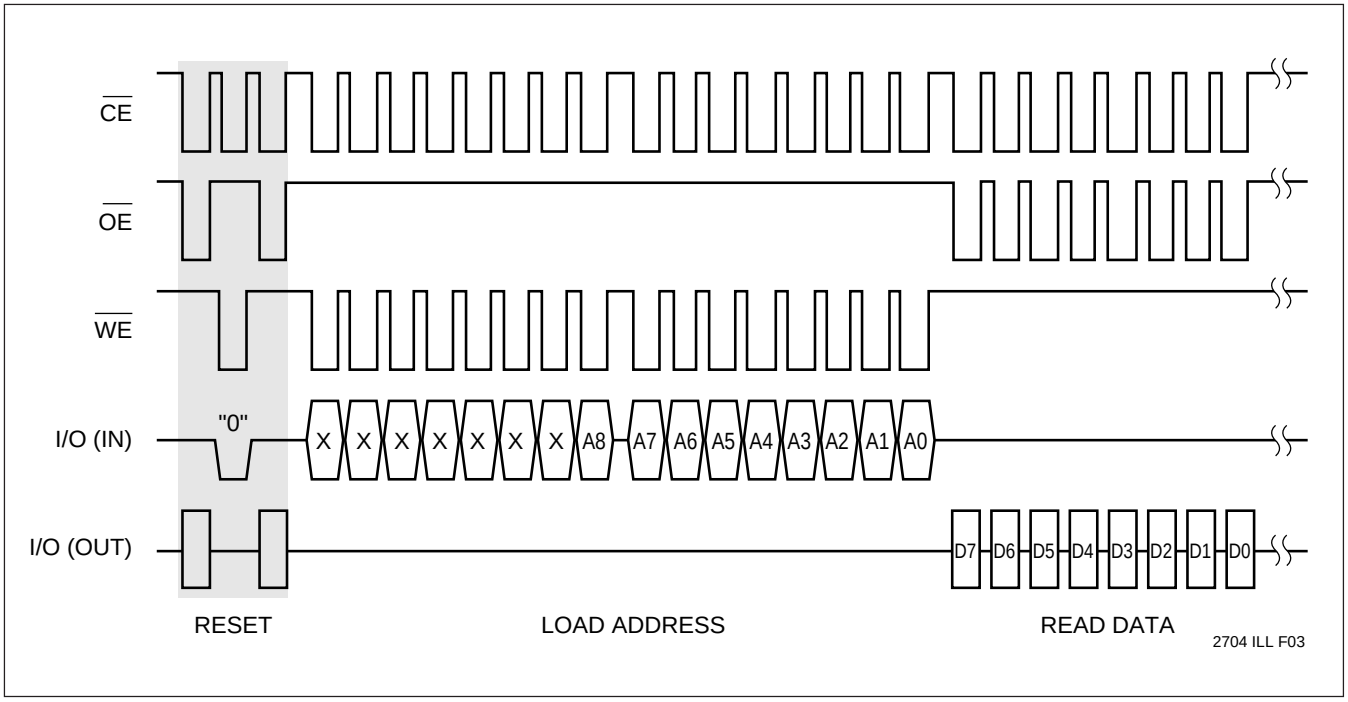
Sequential Read

The byte address is automatically incremented to the next higher address after each byte of data is read. The data stored in the memory at the next address can be read sequentially by continuing to issue read cycles. When the highest address is reached ($1FF), the address counter rolls over to address $000 and reading may be continued indefinitely.

Reset Sequence

The reset sequence resets the X84041 and sets an internal write enable latch. A reset sequence can be sent at any time by performing a read/write “0”/read sequence (see Figs. 1 and 2). This sequence breaks the multiple read or write cycle sequences that are normally used when reading from or writing to the part. This sequence can be used at any time to interrupt or end a sequential read or page load. As soon as the write “0” cycle is complete, the part is reset (unless a nonvolatile write cycle is in progress). The second read cycle in this sequence, and any further read cycles, will read a HIGH on the I/O pin until a valid read sequence is issued. The reset sequence must be issued at the beginning of both read and write sequences to be sure the X84041 initiates these operations properly.

Figure 1. Read Sequence



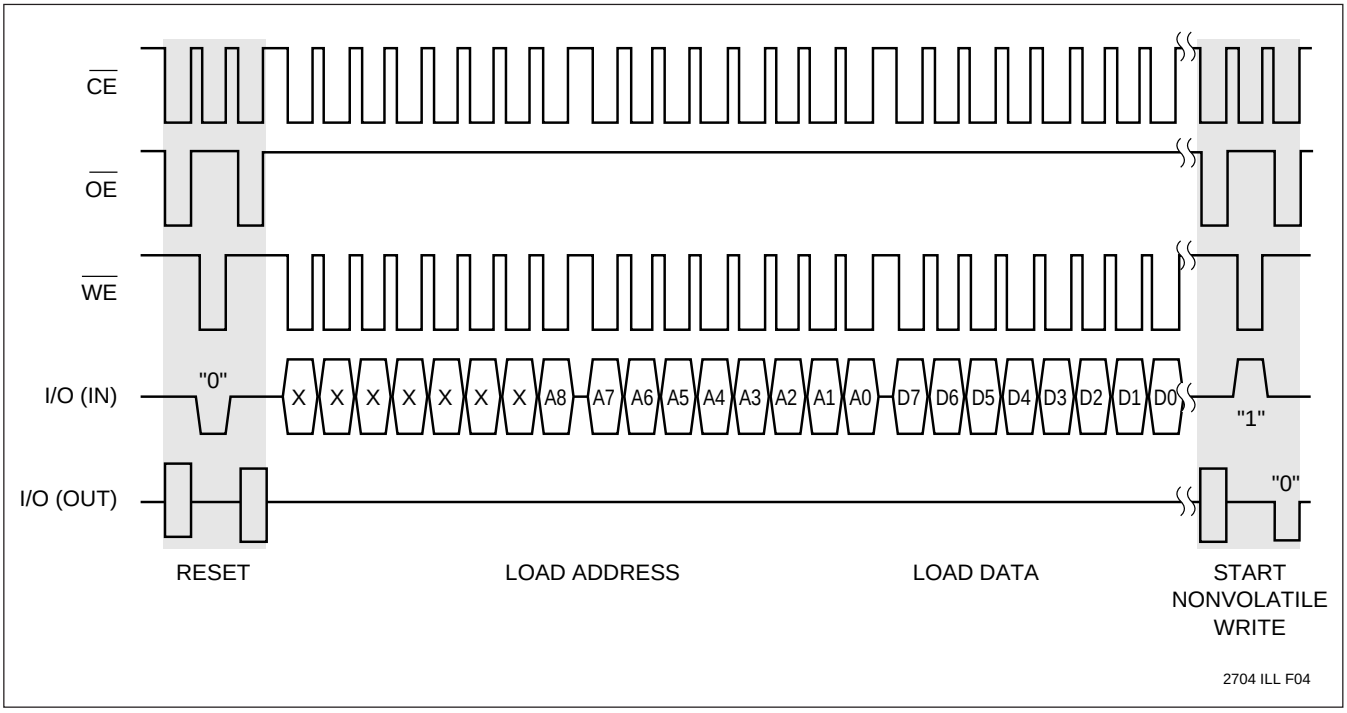
Write Sequence

A nonvolatile write sequence consists of sending a reset sequence, a 16-bit address (the first 7 of which are don't cares), up to 8 bytes of data, and then a special "start nonvolatile write cycle" command sequence. The reset sequence is issued first (as described in the Reset Sequence section) to set the internal write enable latch. The address is written serially by issuing 16 separate write cycles ($\overline{WE}$ and $\overline{CE}$ LOW, $\overline{OE}$ HIGH) to the part without any read cycles between the writes. The address is sent serially, most significant bit first, on the I/O pin. Up to eight bytes of data are written by issuing either 8, 16, 24, 32, 40, 48, 56, or 64 separate write cycles. Again, no read cycles are allowed between writes. The nonvolatile write cycle is initiated by issuing a special read/write "1"/read sequence. The first read cycle ends the page load, then the write "1" followed by a read starts the nonvolatile write cycle. The X84041 recognizes 8-byte pages beginning at addresses XXXXXX000. When sending data to the part, attempts to exceed the upper address of the page will result in the address counter "wrapping-around" to the first address on the page, where data loading can continue. For this reason, sending more than 64 consecutive data bits will result in overwriting previous data. A nonvolatile write cycle will not start if a partial or incomplete write sequence is issued. The internal write enable latch is reset when the nonvolatile write cycle is completed to prevent inadvertent writes. Note that this sequence is fully static, with no special timing restrictions. The processor is free to perform other tasks on the bus whenever the chip enable pin ($\overline{CE}$) is HIGH.

Nonvolatile Write Status

The status of a nonvolatile write cycle can be determined at any time by simply reading the state of the I/O pin on the X84041. This pin is read when $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH. During a nonvolatile write cycle the I/O pin is LOW. When the nonvolatile write cycle is complete, the I/O pin goes HIGH. A reset sequence can also be issued during a nonvolatile write cycle with the same result: I/O is LOW as long as a nonvolatile write cycle is in progress, and I/O is HIGH when the nonvolatile write cycle is done.

Figure 2. Write Sequence



Write Protection

The following circuitry has been included to prevent inadvertent nonvolatile writes:

— The internal Write Enable latch is reset upon power-up.

— A reset sequence must be issued to set the internal write enable latch before starting a write sequence.

— A special “start nonvolatile write” command sequence is required to start a nonvolatile write cycle.

— The internal Write Enable latch is reset automatically at the end of a nonvolatile write cycle.

— The internal Write Enable latch is reset and remains reset as long as the $\overline{WP}$ pin is LOW, which blocks all nonvolatile write cycles.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don’t Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Terminal Voltage with
Respect to V_{SS} ..... –1V to +7V
DC Output Current 5mA
Lead Temperature (Soldering, 10 seconds)..... 300°C

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

2704 PGM T02.2

Supply Voltage	Limits
X84041	5V ±10%
X84041 – 3	3V ±10%
X84041 – 2.7†	2.7V to 5.5V

† Contact factory for availability.

2704 PGM T03.2

D.C. OPERATING CHARACTERISTICS (V_{CC} = 5V ±10%)

(Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, I/O = Open, $\overline{CE}$ clocking @ 2MHz
I_{CC2}	V_{CC} Supply Current (Write)		3	mA	I_{CC} During Nonvolatile Write Cycle All Inputs at CMOS Levels
I_{SB}	V_{CC} Standby Current		50	µA	$\overline{CE}$ = V_{CC}, Other Inputs = V_{CC} or V_{SS} V_{CC} = 5V ±10%
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL} (1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH} (1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA, V_{CC} = 5V ±10%
V_{OH}	Output HIGH Voltage	V_{CC} – 0.8		V	I_{OH} = –1mA, V_{CC} = 5V ±10%

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

2704 PGM T04.3

D.C. OPERATING CHARACTERISTICS (V_{CC} = 3V ±10%)

(Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		250	µA	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, I/O = Open, $\overline{CE}$ clocking @ 2MHz
I_{CC2}	V_{CC} Supply Current (Write)		1	mA	I_{CC} During Nonvolatile Write Cycle All Inputs at CMOS Levels
I_{SB1}	V_{CC} Standby Current		10	µA	$\overline{CE}$ = V_{CC}, Other Inputs = V_{CC} or V_{SS} V_{CC} = 3V ±10%
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 1mA, V_{CC} = 3V ±10%
V_{OH}	Output HIGH Voltage	V_{CC} – 0.4		V	I_{OH} = –400µA, V_{CC} = 3V ±10%

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

2704 PGM T05.2

CAPACITANCE

T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

Notes: (2) Periodically sampled, but not 100% tested.

2704 PGM T06.2

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(3)	Power-up to Read Operation	2	ms
t_{PUW}(3)	Power-up to Write Operation	5	ms

Notes: (3) Time delays required from the time the V_{CC} is stable until the specific operation can be initiated. Periodically sampled, but not 100% tested.

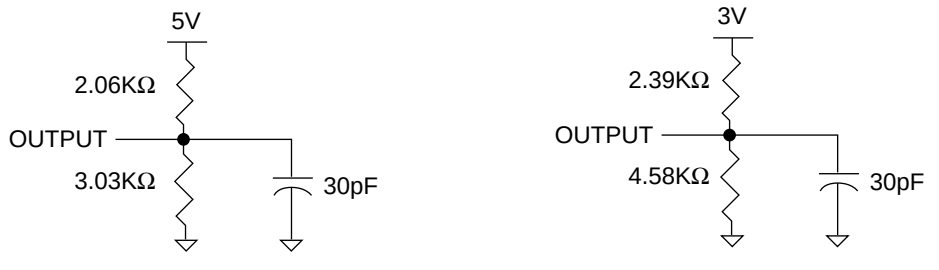
2704 PGM T07

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	5ns
Input and Output Timing Levels	V_{CC} x 0.5

2704 PGM T08.1

EQUIVALENT A.C. LOAD CIRCUITS



A.C. CHARACTERISTICS

(Over the recommended operating conditions, unless otherwise specified.)

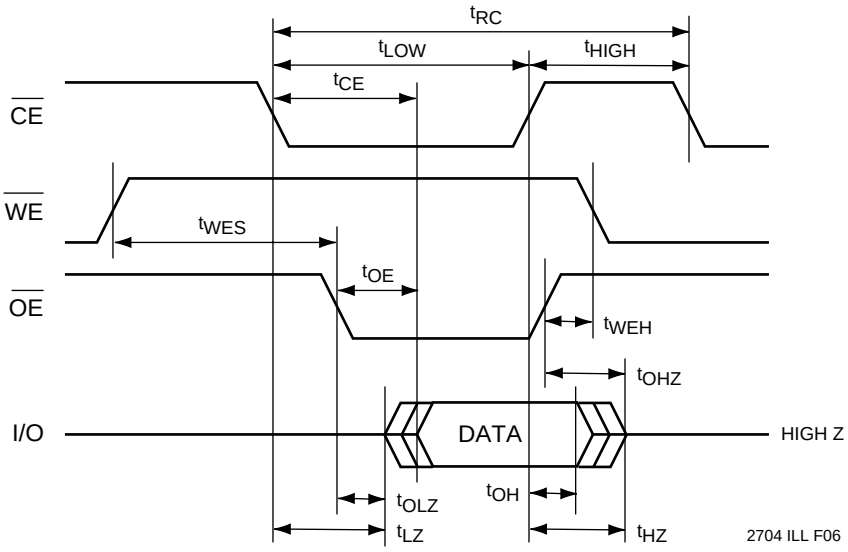
Read Cycle Limits – X84041

Symbol	Parameter	V_{CC} = 5V ±10%		V_{CC} = 3V ±10%		Units
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	300		300		ns
t_{CE}	$\overline{CE}$ Access Time		45		65	ns
t_{OE}	$\overline{OE}$ Access Time		45		65	ns
t_{LOW}	$\overline{CE}$ LOW Time	70		70		ns
t_{HIGH}	$\overline{CE}$ HIGH Time	70		70		ns
t_{LZ}(4)	$\overline{CE}$ LOW to Output In Low Z	0		0		ns
t_{HZ}(4)	$\overline{CE}$ HIGH to Output In High Z	0	30	0	35	ns
t_{OLZ}(4)	$\overline{OE}$ LOW to Output In Low Z	0		0		ns
t_{OHZ}(4)	$\overline{OE}$ HIGH to Output In High Z	0	30	0	35	ns
t_{OH}	Output Hold from $\overline{CE}$ or $\overline{OE}$ HIGH	0		0		ns
t_{WES}	$\overline{WE}$ HIGH Setup Time	25		25		ns
t_{WEH}	$\overline{WE}$ HIGH Hold Time	25		25		ns

Notes: (4) Periodically sampled, but not 100% tested. t_{HZ} and t_{OHZ} are measured from the point where $\overline{CE}$ or $\overline{OE}$ goes HIGH (whichever occurs first) to the time when I/O is no longer being driven into a 5pF load.

2704 PGM T09.3

Read Cycle



Write Cycle Limits – X84041

Symbol	Parameter	V_{CC} = 5V ±10%		V_{CC} = 3V ±10%		Units
		Min.	Max.	Min.	Max.	
t_{NVWC}(5)	Nonvolatile Write Cycle Time		10		10	ms
t_{WC}	Write Cycle Time	300		300		ns
t_{WP}	$\overline{WE}$ Pulse Width	30		30		ns
t_{WPH}	$\overline{WE}$ HIGH Recovery Time	200		200		ns
t_{CS}	Write Setup Time	0		0		ns
t_{CH}	Write Hold Time	0		0		ns
t_{CP}	$\overline{CE}$ Pulse Width	30		30		ns
t_{CPH}	$\overline{CE}$ HIGH Recovery Time	200		200		ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	50		50		ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	50		50		ns
t_{DS}(6)	Data Setup Time	30		30		ns
t_{DH}(6)	Data Hold Time	5		5		ns
t_{WPCS}(7)	$\overline{WP}$ HIGH Before $\overline{CE}$	500		500		ns
t_{WPCH}(7)	$\overline{WP}$ HIGH After $\overline{CE}$	500		500		ns
t_{WPWS}(7)	$\overline{WP}$ HIGH Before $\overline{WE}$	500		500		ns
t_{WPWH}(7)	$\overline{WP}$ HIGH After $\overline{WE}$	500		500		ns

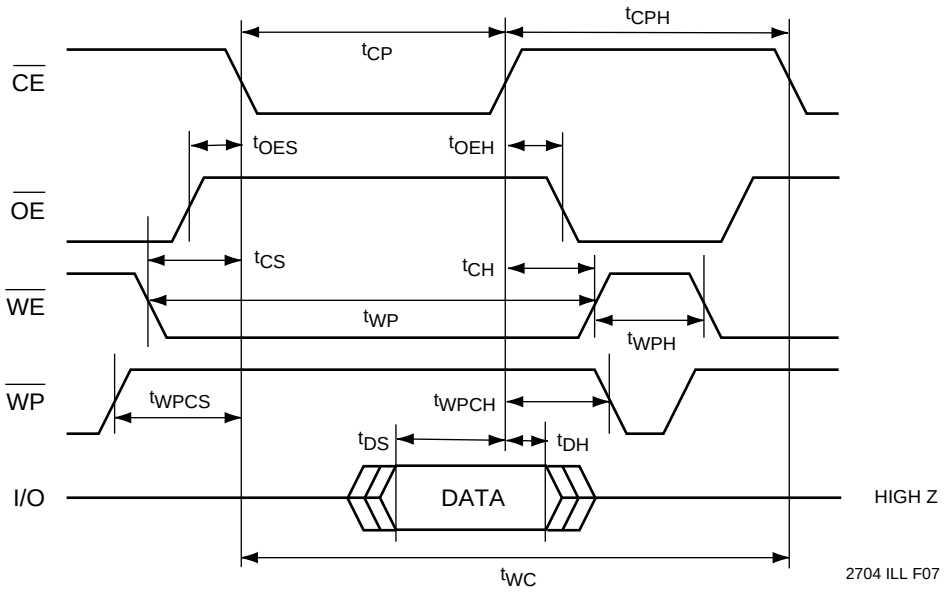
2704 PGM T10.3

Notes: (5) t_{NVWC} is the time from the falling edge of $\overline{OE}$ or $\overline{CE}$ (whichever occurs last) of the second read cycle in the "start nonvolatile write cycle" sequence until the self-timed, internal nonvolatile write cycle is completed.

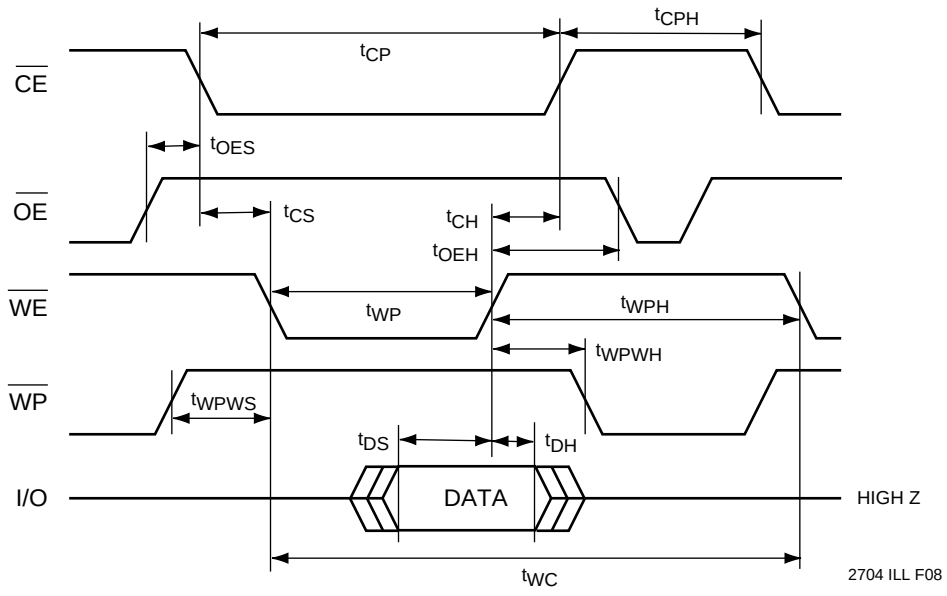
(6) Data is latched into the X84041 on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.

(7) Periodically sampled, but not 100% tested.

$\overline{CE}$ Controlled Write Cycle

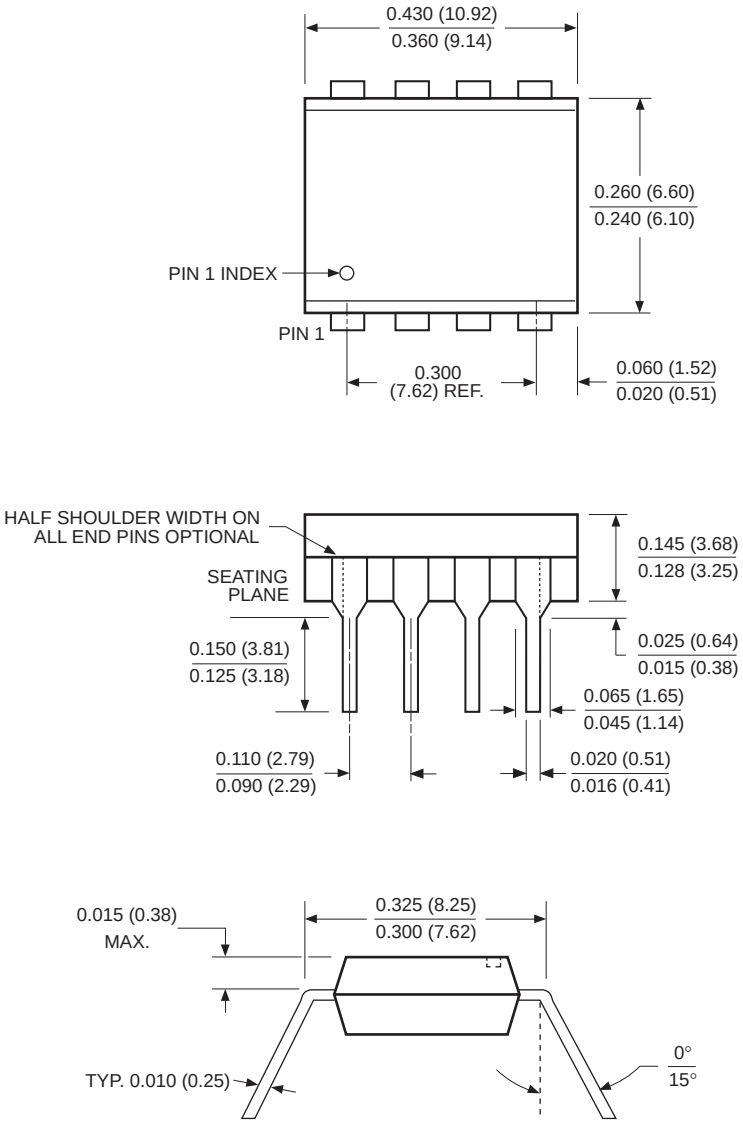


$\overline{WE}$ Controlled Write Cycle



PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



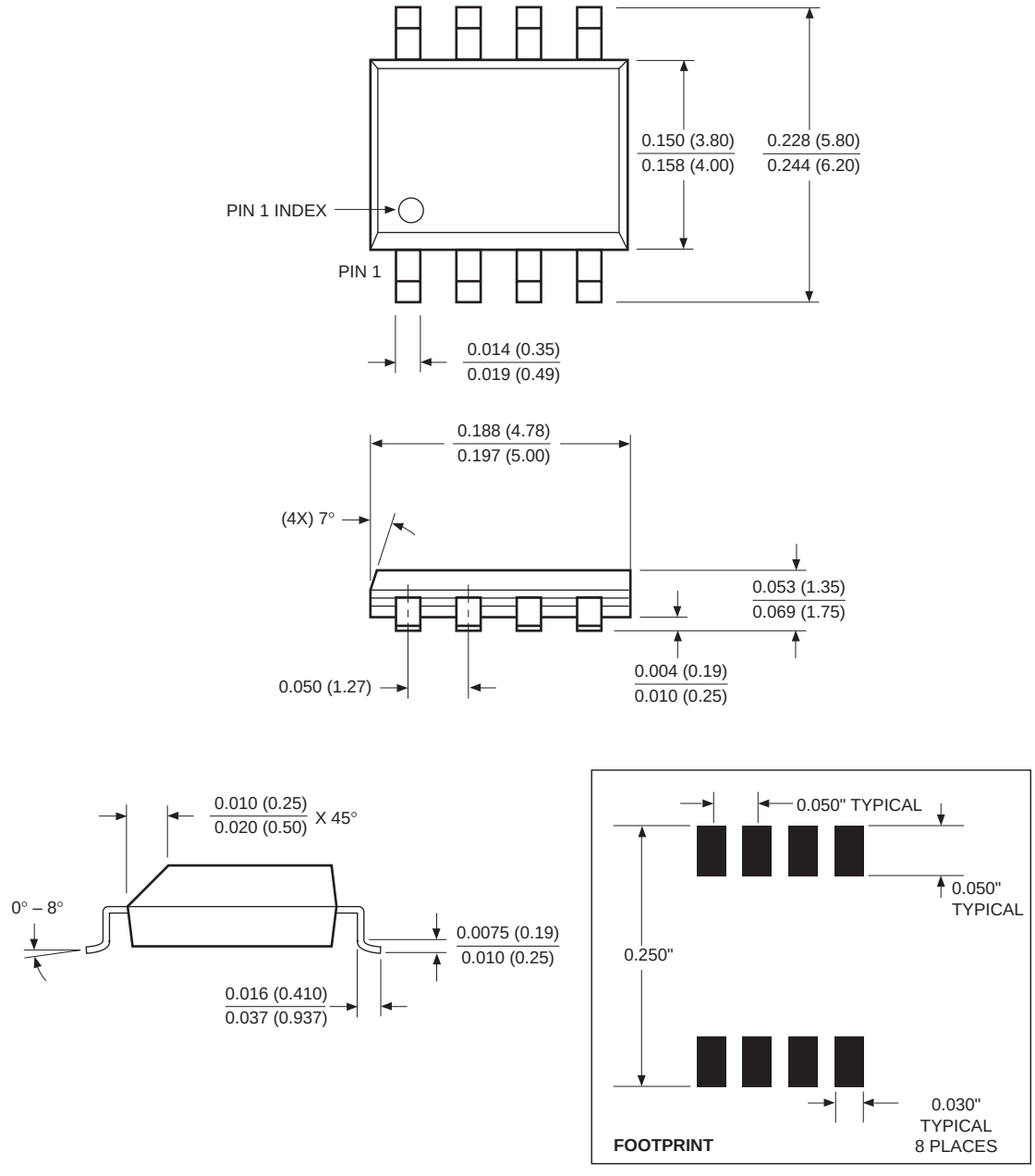
NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 FHD F01

PACKAGING INFORMATION

8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

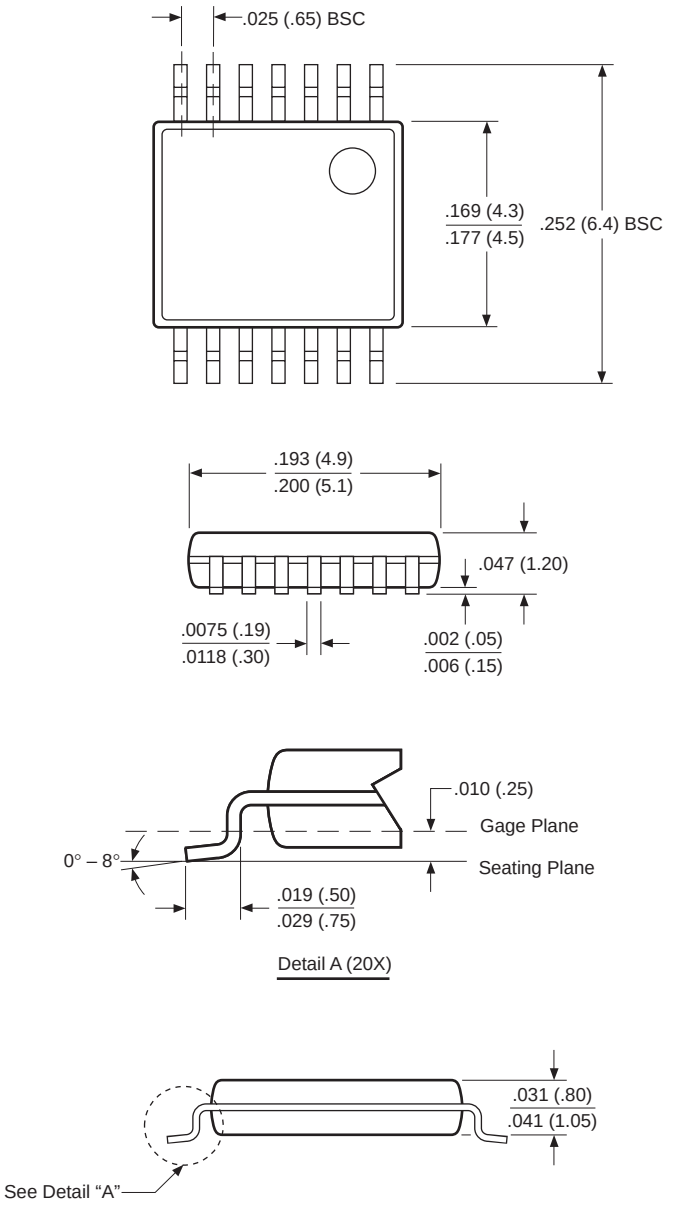


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F22.1

PACKAGING INFORMATION

14-LEAD PLASTIC, TSSOP PACKAGE TYPE V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F32

ORDERING INFORMATION