

**Terminal Voltage  $\pm 5V$ , 100 Taps, Log Taper**
**Description**

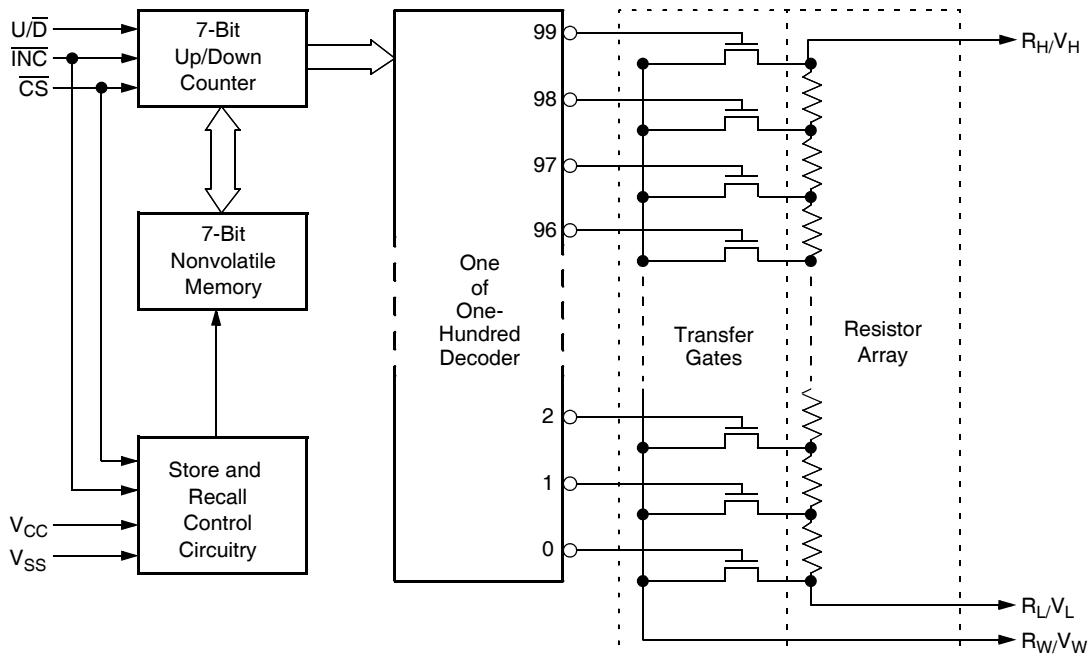
The Intersil X9C303 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a three-wire interface.

The resistor array is composed of 99 resistive elements. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the  $\overline{CS}$ ,  $\overline{U/D}$ , and  $\overline{INC}$  inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications ranging from control, to signal processing, to parameter adjustment. Digitally-controlled potentiometers provide three powerful application advantages; (1) the variability and reliability of a solid-state potentiometer, (2) the flexibility of computer-based digital controls, and (3) the use of nonvolatile memory for potentiometer settings retention.

**Features**

- Solid-state potentiometer
- Three-wire serial interface
- 100 wiper tap points
  - Wiper position stored in nonvolatile memory and recalled on power-up
- 99 resistive elements, log taper
  - Temperature compensated
  - End to end resistance,  $32k\Omega \pm 15\%$
  - Terminal voltages,  $\pm 5V$
- Low power CMOS
  - $V_{CC} = 5V$
  - Active current, 3mA max.
  - Standby current, 750 $\mu A$  max.
- High reliability
  - Endurance, 100,000 data changes per bit
  - Register data retention, 100 years
- Packages
  - 8 Ld TSSOP
  - 8 Ld SOIC
  - 8 Ld PDIP

**Block Diagram**


**Ordering Information**

PART NUMBER	PART MARKING	TEMPERATURE RANGE (°C)	PACKAGE	PKG. DWG. #
X9C303P	X9C303P	0 to +70	8 Ld PDIP	MDP0031
X9C303PI	X9C303P I	-40 to +85	8 Ld PDIP	MDP0031
X9C303PIZ (Note)	X9C303P ZI	-40 to +85	8 Ld PDIP (300 mil) (Pb-free)	MDP0031
X9C303PZ (Note)	X9C303P Z	0 to +70	8 Ld PDIP (300 mil) (Pb-free)	MDP0031
X9C303S8*	X9C303S	0 to +70	8 Ld SOIC (150 mil)	MDP0027
X9C303S8I*	X9C303S I	-40 to +85	8 Ld SOIC (150 mil)	MDP0027
X9C303S8IZ* (Note)	X9C303S ZI	-40 to +85	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X9C303S8Z* (Note)	X9C303S Z	0 to +70	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X9C303V8*	9C303	0 to +70	8 Ld TSSOP (4.4mm)	M8.173
X9C303V8I*	C303 I	-40 to +85	8 Ld TSSOP (4.4mm)	M8.173
X9C303V8IZ* (Note)	C303 IZ	-40 to +85	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X9C303V8Z* (Note)	9CC303 Z	0 to +70	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X9C303S8I-2.7	X9C303S G	-40 to +85	8 Ld SOIC (150 mil)	MDP0027
X9C303S8IZ-2.7 (Note)	X9C303S ZG	-40 to +85	8 Ld SOIC (150 mil) (Pb-free)	MDP0027

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

\*Add "T1" suffix for tape and reel.

**Pin Descriptions**

**$V_H$  and  $V_L$**

The high ( $V_H$ ) and low ( $V_L$ ) terminals of the device are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is  $-5V$  and the maximum is  $+5V$ . It should be noted that the terminology of  $V_L$  and  $V_H$  references the relative position of the terminal in relation to wiper movement direction selected by the  $U/\bar{D}$  input and not the voltage potential on the terminal.

**$V_W$**

$V_W$  is the wiper terminal, equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically  $40\Omega$ .

**Up/Down ( $U/\bar{D}$ )**

The  $U/\bar{D}$  input controls the direction of the wiper movement and whether the counter is incremented or decremented.

**Increment ( $\bar{INC}$ )**

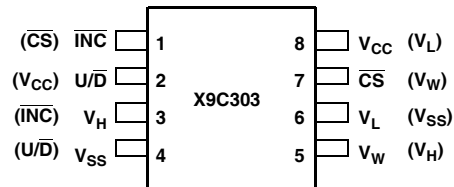
The  $\bar{INC}$  input is negative-edge triggered. Toggling  $\bar{INC}$  will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the  $U/\bar{D}$  input.

**Chip Select ( $\bar{CS}$ )**

The device is selected when the  $\bar{CS}$  input is LOW. The current counter value is stored in nonvolatile memory when  $\bar{CS}$  is returned HIGH while the  $\bar{INC}$  input is also HIGH. After the store operation is complete the device will be placed in the low power standby mode until the device is selected once again.

**Pinout**

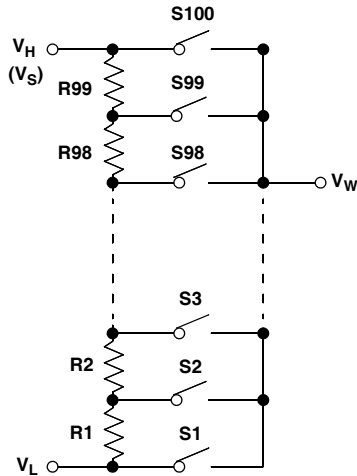
**X9C303**  
(8 LD SOIC, 8 LD TSSOP, 8 LD PDIP)  
TOP VIEW



**Pin Names**

SYMBOL	DESCRIPTION
$V_H$	High Terminal (Potentiometer)
$V_W$	Wiper Terminal (Potentiometer)
$V_L$	Low Terminal (Potentiometer)
$V_{SS}$	Ground
$V_{CC}$	Supply Voltage
$U/\bar{D}$	Up/Down Control Input
$\bar{INC}$	Increment Control Input
$\bar{CS}$	Chip Select Control Input
NC	No Connection

### Potentiometer Relationships



$$G_i = 20 \text{Log} \frac{R_1 + R_2 + \dots + R_i}{R_{\text{TOTAL}}} = \frac{V_W}{V_S} (V_L = 0V)$$

$$R_1 + R_2 + \dots + R_{99} = R_{\text{TOTAL}}$$

(Refer Test Circuit 1)

### Principles of Operation

There are three sections of the X9C303: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 99 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for  $t_{IW}$  (INC to  $V_W$  change). The  $R_{\text{TOTAL}}$  value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last counter position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is reset to the value last stored.

### Instructions and Programming

The  $\overline{\text{INC}}$ ,  $\overline{\text{U/D}}$  and  $\overline{\text{CS}}$  inputs control the movement of the wiper along the resistor array. With  $\overline{\text{CS}}$  set LOW the device is selected and enabled to respond to the  $\overline{\text{U/D}}$  and  $\overline{\text{INC}}$  inputs. HIGH to LOW transitions on  $\overline{\text{INC}}$  will increment or decrement (depending on the state of the  $\overline{\text{U/D}}$  input) a seven-bit counter. The output of this counter is decoded to select one of one-hundred wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever  $\overline{\text{CS}}$  transitions HIGH while the  $\overline{\text{INC}}$  input is also HIGH.

The system may select the X9C303, move the wiper, and deselect the device without having to store the latest wiper position in nonvolatile memory. The wiper movement is performed as described above; once the new position is reached, the system would keep  $\overline{\text{INC}}$  LOW while taking  $\overline{\text{CS}}$  HIGH. The new wiper position would be maintained until changed by the system or until a power-down/up cycle recalled the previously stored data.

This would allow the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference: system parameter changes due to temperature drift, etc...

The state of  $\overline{\text{U/D}}$  may be changed while  $\overline{\text{CS}}$  remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

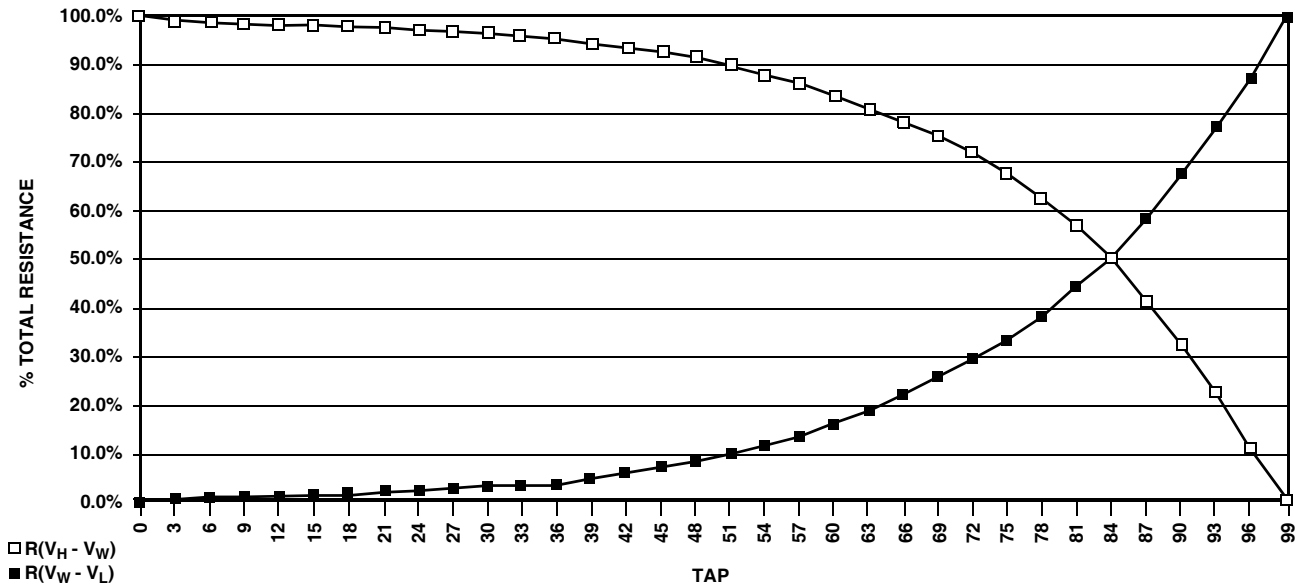
### Mode Selection

$\overline{\text{CS}}$	$\overline{\text{INC}}$	$\overline{\text{U/D}}$	MODE
L		H	Wiper Up
L		L	Wiper Down
	H	X	Store Wiper Position
H	X	X	Standby Current
	L	X	No Store, Return to Standby
	L	H	Wiper Up (not recommended)
	L	L	Wiper Down (not recommended)

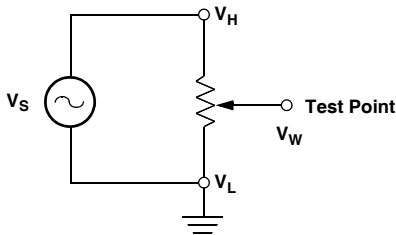
**Symbol Table**

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

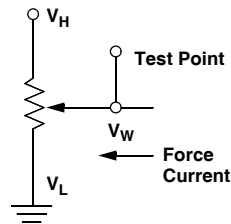
**Typical Electrical Taper**



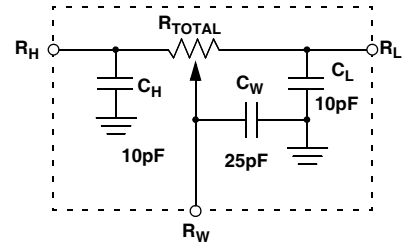
**Test Circuit #1**



**Test Circuit #2**



**Circuit #3 SPICE Macro Model**



**Absolute Maximum Ratings**

Temperature Under Bias . . . . . -65°C to +135°C  
 Storage Temperature . . . . . -65°C to +150°C  
 Voltage on  $\overline{CS}$ ,  $\overline{INC}$ ,  $\overline{U/D}$  and  $V_{CC}$  with Respect to  $V_{SS}$  . -1V to +7V  
 Voltage on  $V_H$  and  $V_L$  Referenced to  $V_{SS}$  . . . . . -8V to +8V  
 $\Delta V = |V_H - V_L|$  X9C303 . . . . . 10V  
 Lead Temperature (soldering, 10s) . . . . . +300°C  
 Wiper Current . . . . .  $\pm 1$ mA

**Recommended Operating Conditions**

Commercial Temperature Range . . . . . 0°C to +70°C  
 Industrial Temperature Range . . . . . -40°C to +85°C  
 Military Temperature Range . . . . . -55°C to +125°C  
 Supply Voltage Range . . . . . 5V  $\pm 10\%$   
 Power Rating at +25°C X9C303 . . . . . 10mW  
 Physical Characteristics  
 Marking Includes  
 Manufacturer's Trademark  
 Resistance Value or Code  
 Date Code

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**Analog Specifications** Over recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP (NOTE 1)	MAX	
R <sub>TOTAL</sub>	End-to-End Resistance			32		$\kappa\Omega$
	End-to-End Resistance Tolerance		-15		+15	%
V <sub>H</sub>	V <sub>H</sub> Terminal Voltage		-5		+5	V
V <sub>L</sub>	V <sub>L</sub> Terminal Voltage		-5		+5	V
R <sub>W</sub>	Wiper Resistance	Max Wiper Current $\pm 1$ mA		40	100	$\Omega$
	Tap position relative step size error	Error = $\log(V_w(n)) - \log(V_w(n-1))$ for tap n = 2 - 99, V <sub>H</sub> -V <sub>L</sub> = 10V	0.005		0.115	dB
	Resistor Noise	At 1kHz		23		nV(RMS)/ $\sqrt{\text{Hz}}$
	Charge Pump Noise	At 2.5MHz		20		mV(RMS)
	End-to-End Resistance Temperature Coefficient	T = -40°C to +85°C		$\pm 400$		ppm/°C
	Ratiometric Temperature Coefficient	Tap position 84		$\pm 20$		ppm/°C
C <sub>H</sub> /C <sub>L</sub> /C <sub>W</sub> (Note 3)	Potentiometer Capacitance	See Circuit 3		10/10/25		pF

**DC Electrical Specifications** Over recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP (NOTE 1)	MAX	
I <sub>CC</sub>	V <sub>CC</sub> Active Current	$\overline{CS} = V_{IL}$ , $\overline{U/D} = V_{IL}$ or $V_{IH}$ and $\overline{INC} = 0.4V$ to $2.4V$ @ Max t <sub>CYC</sub>		1	3	mA
I <sub>SB</sub>	Standby Supply Current	$\overline{CS} = V_{CC} - 0.3V$ , $\overline{U/D}$ and $\overline{INC} = V_{SS}$ or $V_{CC} - 0.3V$		200	750	$\mu A$
I <sub>LI</sub>	$\overline{CS}$ , $\overline{INC}$ , $\overline{U/D}$ Input Leakage Current	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>	-10		+10	$\mu A$
V <sub>IH</sub>	$\overline{CS}$ , $\overline{INC}$ , $\overline{U/D}$ Input HIGH Voltage		2			V
V <sub>IL</sub>	$\overline{CS}$ , $\overline{INC}$ , $\overline{U/D}$ Input LOW voltage				0.8	V
C <sub>IN</sub> (Note 3)	$\overline{CS}$ , $\overline{INC}$ , $\overline{U/D}$ Input Capacitance	V <sub>CC</sub> = 5V, V <sub>IN</sub> = V <sub>SS</sub> , T <sub>A</sub> = +25°C, f = 1MHz		10		pF

# X9C303

## DC Electrical Specifications Over recommended operating conditions unless otherwise specified. (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP (NOTE 1)	MAX	
<b>EEPROM SPECS</b>						
	EEPROM Endurance	Wiper storage operations over recommended operation conditions	100,000			Cycles
	EEPROM Retention	At +55°C		100		Years

## Standard Parts

PART NUMBER	MAXIMUM RESISTANCE	WIPER INCREMENTS	MINIMUM RESISTANCE
X9C303	32kΩ	Log Taper	40Ω Typical

### NOTES:

1. Typical values are for  $T_A = +25^\circ\text{C}$  and nominal supply voltage.

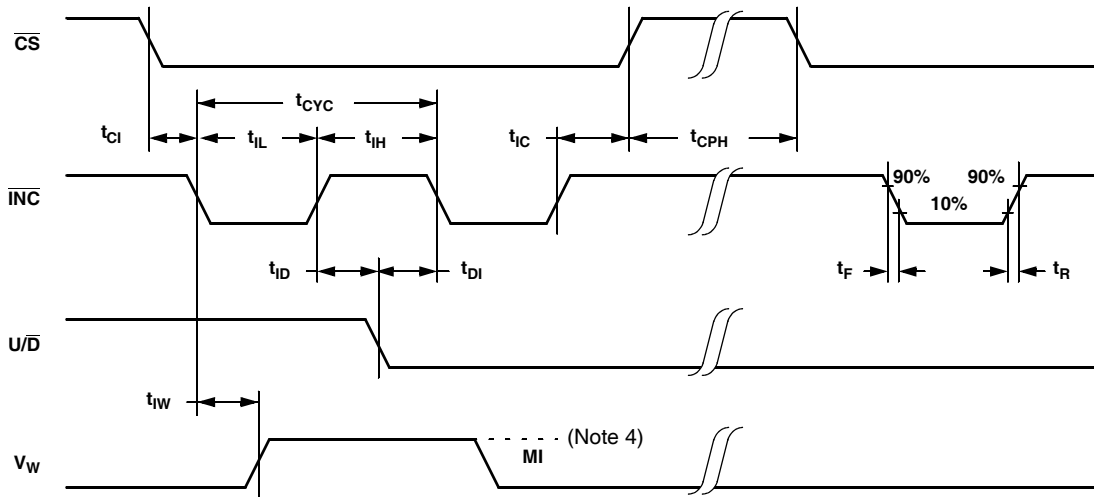
## A.C. Conditions of Test

Input pulse levels	0V to 3V
Input rise and fall times	10ns
Input reference levels	1.5V

## AC Electrical Specifications Over recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP (Note 2)	MAX	
$t_{CI}$	$\overline{CS}$ to $\overline{INC}$ Set-up	100			ns
$t_{ID}$	$\overline{INC}$ HIGH to $U/\overline{D}$ Change	100			ns
$t_{DI}$	$U/\overline{D}$ to $\overline{INC}$ Set-up	2.9			μs
$t_{IL}$	$\overline{INC}$ LOW Period	1			μs
$t_{IH}$	$\overline{INC}$ HIGH Period	1			μs
$t_{IC}$	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1			μs
$t_{CPH}$	$\overline{CS}$ Deselect Time	20			ms
$t_{IW}$ (Note 3)	$\overline{INC}$ to $V_W$ Change		100		μs
$t_{CYC}$	$\overline{INC}$ Cycle Time	2			μs
$t_R, t_F$ (Note 3)	$\overline{INC}$ Input Rise and Fall Time			500	ns
$t_{PU}$ (Note 3)	Power-up to Wiper Stable		500		μs
$t_{R V_{CC}}$ (Note 3)	$V_{CC}$ Power-up Rate	0.2		50	mV/μs

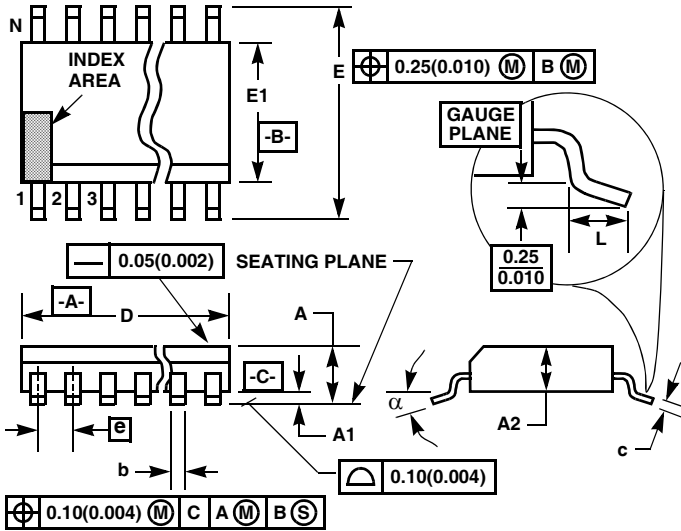
**A.C. Timing**



NOTES:

2. Typical values are for  $T_A = +25^\circ\text{C}$  and nominal supply voltage.
3. This parameter is not 100% tested.
4. MI in the A.C. timing diagram refers to the minimum incremental change in the  $V_w$  output due to a change in the wiper position.

**Thin Shrink Small Outline Plastic Packages (TSSOP)**



**M8.173**

**8 LEAD THIN SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	8		8		7
α	0°	8°	0°	8°	-

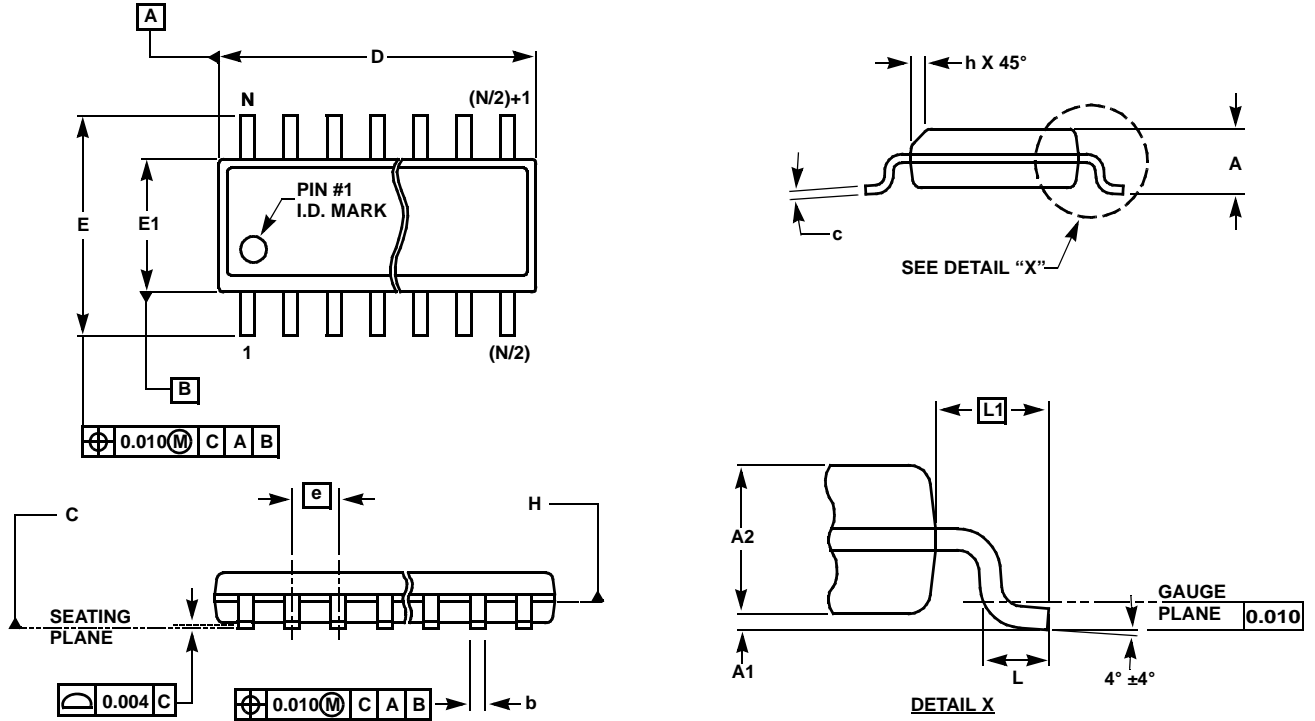
**NOTES:**

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

Rev. 1 12/00



**Small Outline Package Family (SO)**



**MDP0027**

**SMALL OUTLINE PACKAGE FAMILY (SO)**

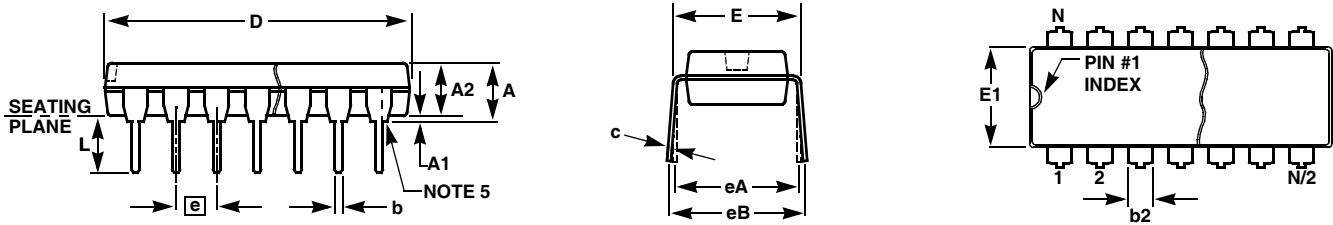
SYMBOL	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	TOLERANCE	NOTES
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. L 2/01

**NOTES:**

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

**Plastic Dual-In-Line Packages (PDIP)**



**MDP0031**

**PLASTIC DUAL-IN-LINE PACKAGE**

SYMBOL	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20	TOLERANCE	NOTES
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

Rev. B 2/99

**NOTES:**

1. Plastic or metal protrusions of 0.010" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.  
Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

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