

# XC25BS3 Series



PLL Clock Generator ICs with Built-In Divider/Multiplier Circuits

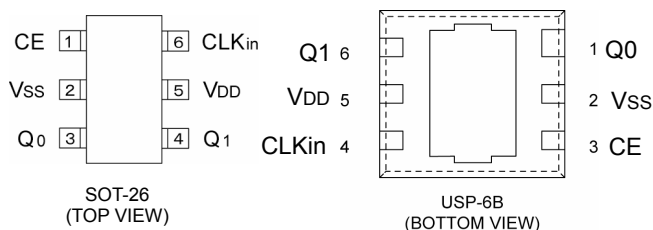
- ◆ CMOS Low Power Consumption
- ◆ Input Frequency : 14kHz ~ 35MHz
- ◆ Divider Ratio : 1~ 2047 Divisions  
(Laser Trimming)
- ◆ Multiplier Ratio : 20 ~ 2047 Multiplications  
(Laser Trimming)
- ◆ Comparative Frequency : 14kHz ~ 500kHz
- ◆ Output Frequency : 9MHz ~ 80MHz

## ■ GENERAL DESCRIPTION

The XC25BS3 series are high frequency, low power consumption PLL clock generator ICs with built-in crystal oscillator circuit, divider circuit & multiplier PLL circuit.

Laser trimming gives the option of being able to select from divider ratios (M) of 1 to 2047 and multiplier ratio (N) of 20 to 2047. Output frequency (Q0) is equal to reference oscillation (fCLKin) multiplied by N/M, within a range of 9MHz to 80MHz. Q1 output is selectable from input reference frequency (f0), Ground (GND), PLL output frequency/2 (Q0/2), and comparative frequency/2 (f0/M/2). Reference oscillation can input 14kHz to 35MHz of reference clock. Further, comparative frequency, within a range of 14kHz to 500kHz, can be obtained by dividing the reference oscillation. By halting oscillation via the CE pin, consumption current can be controlled. Output will be one of high impedance.

## ■ PIN CONFIGURATION



\*The dissipation pad for the USP-6B package should be solder-plated in recommended mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the VDD pin.

## ■ APPLICATIONS

- Crystal oscillation modules
- Microcontroller
- PDAs
- Portable audio systems
- Various system clocks

## ■ FEATURES

- Output Frequency** : 9MHz ~ 80MHz (Q0=fCLKin × N/M)
- Reference Oscillation (fCLKin)** : 14kHz ~ 35MHz
- Divider Ratio (M)** : Selectable from divisions of 1 ~ 2047
- Multiplier Ratio (N)** : Selectable from multiplications of 20 ~ 2047
- Output** : 3-State  
Q1 output selectable from reference oscillation, GND, PLL output frequency/2, comparative frequency/2.
- Operating Voltage Range**: 2.97V ~ 5.5V
- Low Power Consumption**: CMOS (stand-by function included)\*1
- Ultra Small Package** : SOT-26, USP-6B

\*1 High output impedance during stand-by

## ■ PIN ASSIGNMENT

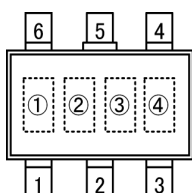
PIN NUMBER		PIN NAME	FUNCTION
SOT-26	USP-6B		
1	3	CE	Chip Enable
2	2	Vss	GND
3	1	Q0	PLL Output
4	6	Q1	Reference Oscillation, GND, Comparative Frequency/2, or PLL Output/2 Output *
5	5	VDD	Power Supply
6	4	CLKin	Reference Clock Input

\* Q1 Output is selectable from the above mentioned functions.



## MARKING RULE

### ●SOT-26



SOT-26  
(TOP VIEW)

①②Represents product series

MARK		PRODUCT SERIES
①	②	
B	3	XC25BS30xxMx

③Represents ② and ③ of product number as in ordering information

SYMBOL	②	③	PRODUCT SERIES	SYMBOL	②	③	PRODUCT SERIES
1	0	1	XC25BS3x01Mx	K	1	7	XC25BS3x17Mx
2	0	2	XC25BS3x02Mx	L	1	8	XC25BS3x18Mx
3	0	3	XC25BS3x03Mx	M	1	9	XC25BS3x19Mx
4	0	4	XC25BS3x04Mx	N	2	0	XC25BS3x20Mx
5	0	5	XC25BS3x05Mx	P	2	1	XC25BS3x21Mx
6	0	6	XC25BS3x06Mx	R	2	2	XC25BS3x22Mx
7	0	7	XC25BS3x07Mx	S	2	3	XC25BS3x23Mx
8	0	8	XC25BS3x08Mx	T	2	4	XC25BS3x24Mx
9	0	9	XC25BS3x09Mx	U	2	5	XC25BS3x25Mx
A	1	0	XC25BS3x10Mx	V	2	6	XC25BS3x26Mx
B	1	1	XC25BS3x11Mx	X	2	7	XC25BS3x27Mx
C	1	2	XC25BS3x12Mx	Y	2	8	XC25BS3x28Mx
D	1	3	XC25BS3x13Mx	Z	2	9	XC25BS3x29Mx
E	1	4	XC25BS3x14Mx	0	3	0*	XC25BS3x30Mx
F	1	5	XC25BS3x15Mx	1	3	1*	XC25BS3x31Mx
H	1	6	XC25BS3x16Mx	...	...	...	...

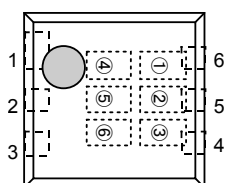
④Represents assembly lot number

0 to 9, A to Z, reverse character 0 to 9 and A to Z repeated.

(G, I, J, O, Q, W excepted.)

\* Character inversion is used.

### ●USP-6B



USP-6B  
(TOP VIEW)

①②③Represents product series

MARK			PRODUCT SERIES
①	②	③	
B	S	3	XC25BS30xxDx
S	3	S	XC25BS3SxxDx

④,⑤Represents ② and ③ of product number as in ordering information (ex)

MARK		PRODUCT SERIES
④	⑤	
0	7	XC25BS3007Dx
0	1	XC25BS3S01Dx

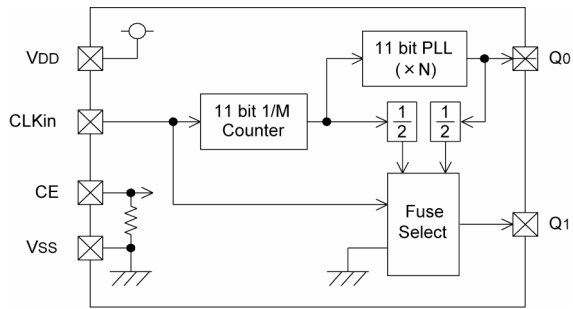
⑥Represents production lot number

0 to 9, A to Z repeated (G, I, J, O, Q, W excepted)

Note: No character inversion used.

# XC25BS3 Series

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

Ta = 25°C

PARAMETER	SYMBOL	CONDITIONS	UNITS
Supply Voltage	V <sub>DD</sub>	V <sub>SS</sub> -0.3~V <sub>SS</sub> +7.0	V
CLKin Pin Voltage	V <sub>CK</sub>	V <sub>SS</sub> -0.3~V <sub>DD</sub> +0.3	V
CE Pin Voltage	V <sub>CE</sub>	V <sub>SS</sub> -0.3~V <sub>DD</sub> +0.3	V
Q0 Pin Voltage	V <sub>Q0</sub>	V <sub>SS</sub> -0.3~V <sub>DD</sub> +0.3	V
Q1 Pin Voltage	V <sub>Q1</sub>	V <sub>SS</sub> -0.3~V <sub>DD</sub> +0.3	V
Q0 Output Current	I <sub>Q0</sub>	±50	mA
Q1 Output Current	I <sub>Q1</sub>	±50	mA
Power Dissipation	SOT-26	Pd	150
	USP-6B		100
Storage Temperature Range	T <sub>opr</sub>	-30~+80	°C
Operating Temperature Range	T <sub>stg</sub>	-40~+125	°C

## ■ ELECTRICAL CHARACTERISTICS

XC25BS30xxMR

### ● Set Value (example 1)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Input Frequency	fCLKin	13.000	—	20.000	MHz
Q0 Pin Output Multiplier Ratio	N/M	—	4.000	—	Multiplier
Output Frequency 1	fQ0	52.000	—	80.000	MHz
Output Frequency 2	Q1	fCLKin			—

### ● DC Characteristics

XC25BS30xxMR

fCLKin=20MHz, Q0 pin output multiplier ratio=4, Ta=25°C, No Load

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	VDD		2.97	3.30	3.63	V
Input Voltage "High"	VIH		2.7	—	—	V
Input Voltage "Low"	VIL		—	—	0.6	V
Input Current "High"	IiH	VCK=3.3V	—	—	3.0	μA
Input Current "Low"	IiL	VCK=0V	-3.0	—	—	μA
Output Voltage "High"	VOH	VDD=2.97V, IOH=-8mA	2.5	—	—	V
Output Voltage "Low"	VOL	VDD=2.97V, IOL=8mA	—	—	0.4	V
Supply Current 1	IDD1	CE=3.3V	—	5.5	11.0	mA
Supply Current 2	IDD2	CE=0V	—	—	5.0	μA
CE "High" Voltage	VCEH		2.70	—	—	V
CE "Low" Voltage	VCEL		—	—	0.45	V
CE Pull-Down Resistance 1	Rp1	CE=3.3V	0.5	1.5	2.5	MΩ
CE Pull-Down Resistance 2	Rp2	CE=0.3V	20.0	50.0	80.0	kΩ

### ● AC Characteristics

XC25BS30xxMR

fCLKin=20MHz, Q0 pin output multiplier ratio=4, Ta=25°C, CL=15pF

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise Time	TTLH	VDD=3.3V (20% to 80%) (*2)	—	5.0	—	ns
Output Fall Time	TTHL	VDD=3.3V (20% to 80%) (*2)	—	5.0	—	ns
Duty Ratio	DUTY		40	50	60	%
Output Start Time	Ton	(*2)	—	—	20	ms
PLL Output Jitter	Tj	1σ (*2)	—	60	—	ps

\*2 R&amp;D guarantee

## ■ ELECTRICAL CHARACTERISTICS (Continued)

XC25BS30xxMR (Continued)

### ● Set Value (example 2)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Input Frequency	fCLKin	10.000	—	16.000	MHz
Q0 Pin Output Multiplier Ratio	N/M	—	3.000	—	Multiplier
Output Frequency 1	fQ0	30.000	—	48.000	MHz
Output Frequency 2	Q1	GND			—

### ● DC Characteristics

XC25BS30xxMR

fCLKin=16MHz, Q0 pin output multiplier ratio=3, Ta=25°C, No Load

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	VDD		2.97	3.30	3.63	V
Input Voltage "High"	VIH		2.7	—	—	V
Input Voltage "Low"	VIL		—	—	0.6	V
Input Current "High"	IiH	VCK=3.3V	—	—	3.0	μA
Input Current "Low"	IiL	VCK=0V	-3.0	—	—	μA
Output Voltage "High"	VOH	VDD=2.97V, IOH=-8mA	2.5	—	—	V
Output Voltage "Low"	VOL	VDD=2.97V, IOL=8mA	—	—	0.4	V
Supply Current 1	IDD1	CE=3.3V	—	4.0	8.0	mA
Supply Current 2	IDD2	CE=0V	—	—	5.0	μA
CE "High" Voltage	VCEH		2.70	—	—	V
CE "Low" Voltage	VCEL		—	—	0.45	V
CE Pull-Down Resistance 1	Rp1	CE=3.3V	0.5	1.5	2.5	MΩ
CE Pull-Down Resistance 2	Rp2	CE=0.3V	20.0	50.0	80.0	kΩ

### ● AC Characteristics

XC25BS30xxMR

fCLKin=16MHz, Q0 pin output multiplier ratio=3, Ta=25°C, CL=15pF

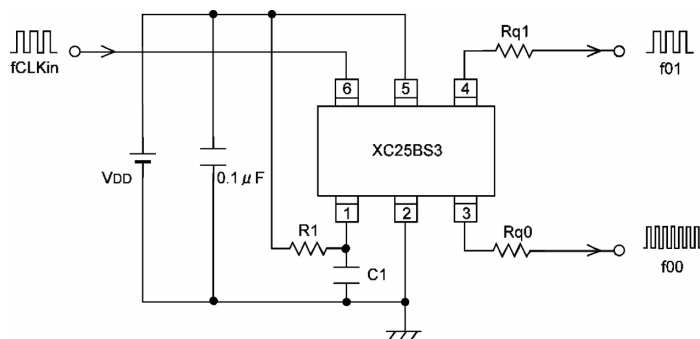
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise Time	TTLH	VDD=3.3V (20% to 80%) (*2)	—	5.0	—	ns
Output Fall Time	TTHL	VDD=3.3V (20% to 80%) (*2)	—	5.0	—	ns
Duty Ratio	DUTY		40	50	60	%
Output Start Time	Ton	(*2)	—	—	20	ms
PLL Output Jitter	Tj	1σ (*2)	—	60	—	ps

\*2 R&D guarantee

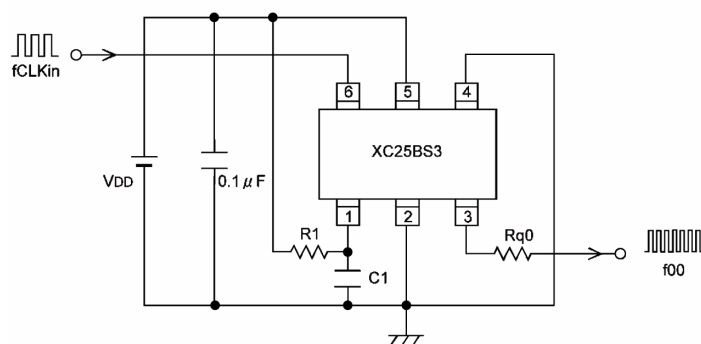
## ■ TYPICAL APPLICATION CIRCUITS

### ● Circuit Example

① Q1 Pin - reference oscillation, PLL output frequency/2, comparative frequency/2



② Q1 Pin - GND

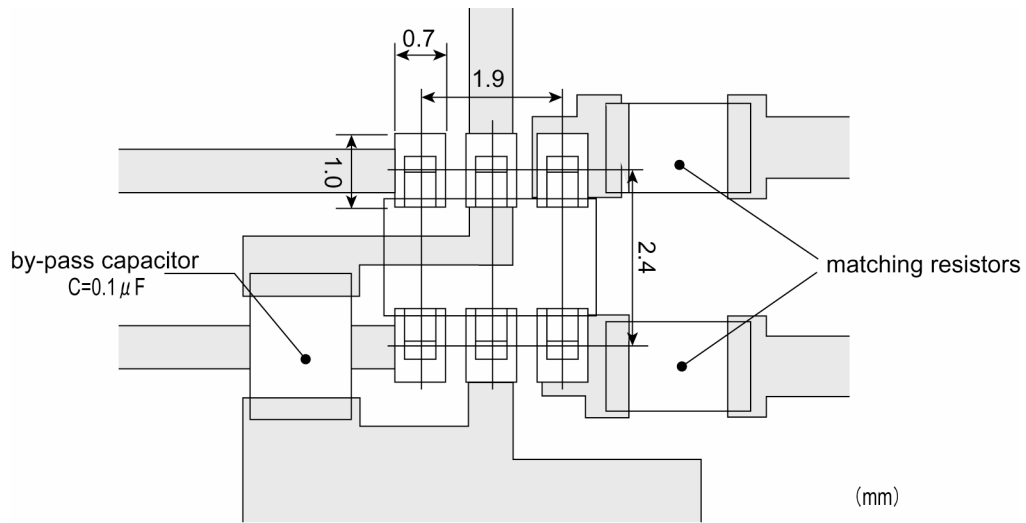


## ■ NOTES ON USE

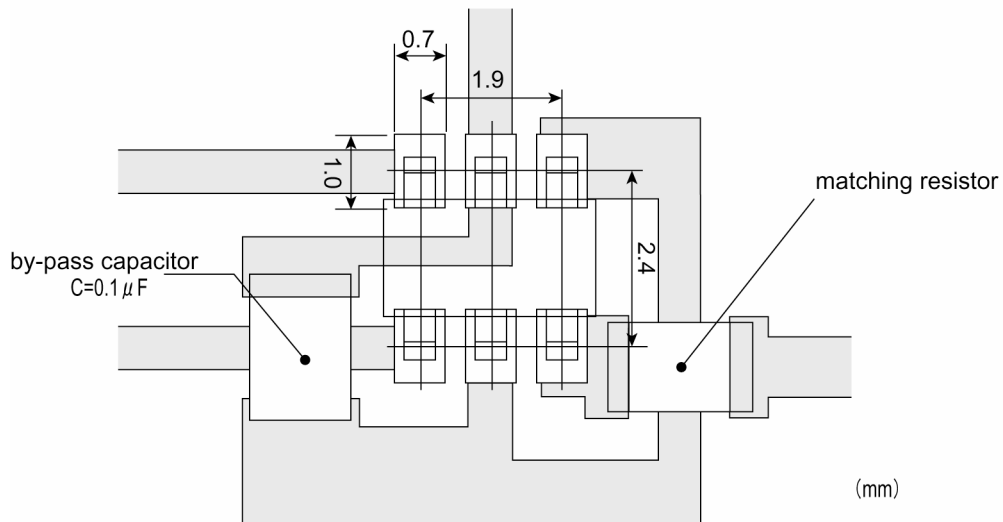
- (1) Please insert a by-pass capacitor of  $0.1 \mu\text{F}$ .
- (2) Rq0 and Rq1 are matching resistors. Their use is recommended in order to counter unwanted radiations.
- (3) Please place a by-pass capacitor and matching resistors as close to the IC as possible. The output may not be locked if the by-pass capacitor is not close enough to the IC. Further, there is a possibility of unwanted radiation occurrence between the resistor and the IC pin if the matching resistors are not close enough to the IC.
- (4) When selecting GND for the Q1 pin, although the IC will be connected to GND internally, it is also recommended that the PCB be connected to GND.
- (5) When the CE pin is not controlled by external signals, it is recommended that a time constant circuit of  $R1=1\text{k}\Omega \times C1=0.1 \mu\text{F}$  be added for stability.
- (6) With this IC, output is achieved by dividing and multiplying the reference oscillation by means of the PLL circuit. In cases where this output is further used as a reference oscillation of another PLL circuit, the final output signal's jitter may increase, so all necessary precautions should be taken to avoid this.
- (7) It is recommended that a low noise power supply, such as a series regulator, be used for the supply voltage. Using a power supply such as a switching regulator might lead to a larger jitter, which in turn may lead to an inability to lock due to the ripple of the switching regulator.
- (8) As for this IC, synchronization of input and output signal's edge is not guaranteed though the input frequency operates to the output frequency multiply.

## ■ REFERENCE LAND PATTERN

① Q1 Pin - reference oscillation, PLL output frequency/2, comparative frequency/2



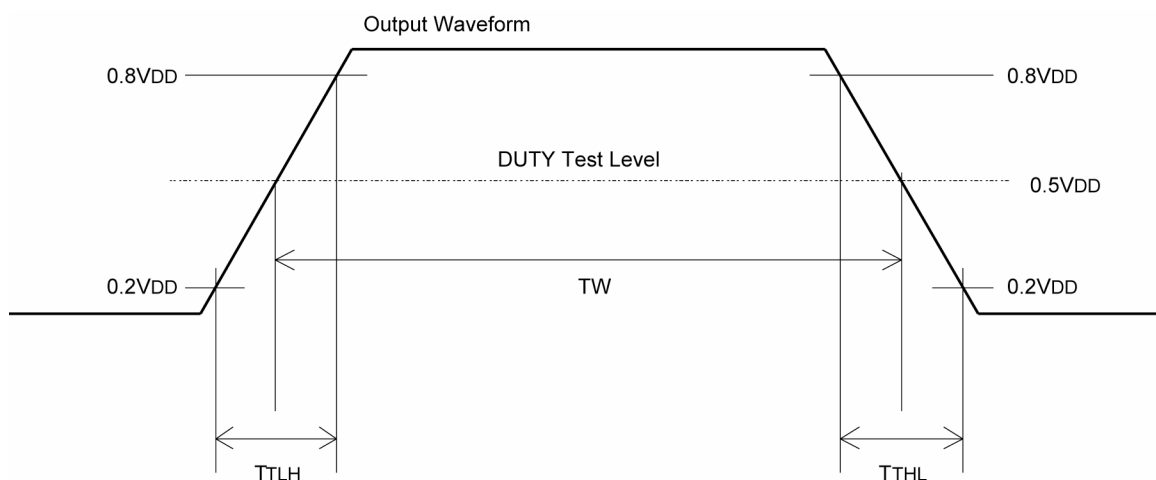
② Q1 Pin - GND



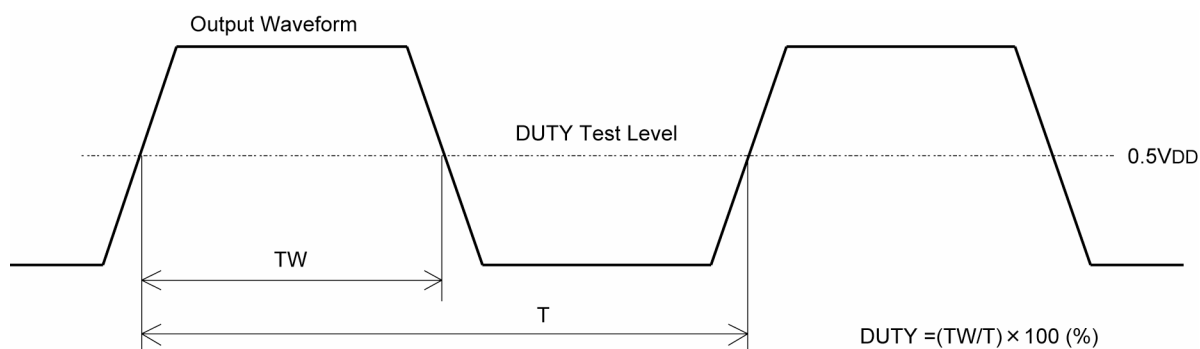


## ■ AC CHARACTERISTICS WAVEFORMS

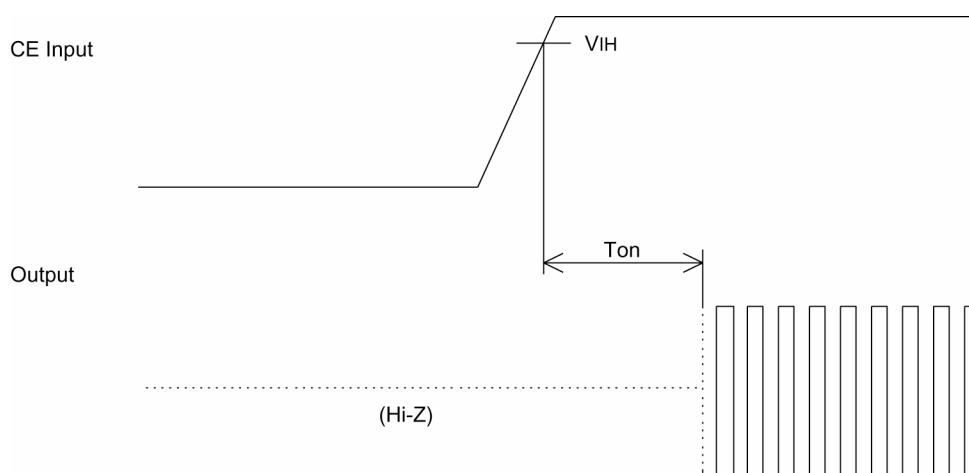
### 1) Output Rise Time / Output Fall Time



### 2) Duty Ratio



### 3) Output Start Time



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