XR68C92/192

DUAL UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

May 2000

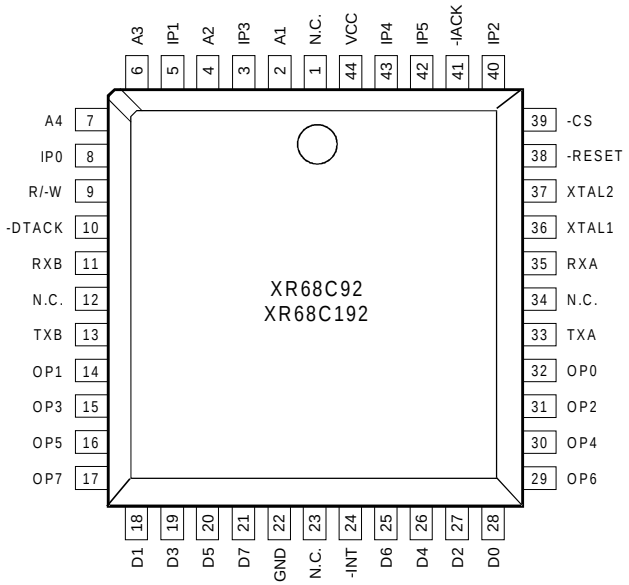
DESCRIPTION

The XR68C92/192 is a Dual Universal Asynchronous Receiver and Transmitter with 8 (XR68C92) or 16 (XR68C192) bytes of transmit and receive FIFOs. The XR68C92/192 is pin-to-pin and functionally compatible to the XR68C681 and Philips SCC68681 UART with additional features. The operating speed of the receiver and transmitter can be selected independently from a table of twenty four fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock input. The XR68C92/192 provides a power down mode in which the oscillator is stopped but the register contents are retained. The XR68C92/192 is fabricated in an advanced CMOS process to achieve low power and high speed requirements.

FEATURES

- Pin to pin and functionally compatible to XR68C681 and SCC68692
- Full duplex transmit and receive operation
- 8 bytes of transmit/receive FIFOs (XR68C92)
- 16 bytes of transmit/receive FIFOs (XR68C192)
- Programmable character lengths (5, 6, 7, 8)
- Parity, framing, and over run error detection
- Programmable 16-bit timer/counter
- On-chip crystal oscillator
- Single interrupt output with eight selectable interrupting conditions
- External 1X or 16X clock
- Data rate up to 1Mbps
- Independent transmit and receive baud rates from 50bps to 230.4kbps
- 6 General purpose inputs
- 8 General purpose outputs
- TTL compatible inputs, outputs
- 4 Transmit/receive trigger levels
- Watch dog timer
- Multi-drop mode compatible with 8051 nine bit mode
- 3.3 or 5 volts operation
- Loopback modes
- Power down mode

PLCC Package



ORDERING INFORMATION

Part number	Pins	Package	Operating temperature
XR68C92CP	40	PDIP	0° C to + 70° C
XR68C92CJ	44	PLCC	0° C to + 70° C
XR68C92CV	44	TQFP	0° C to + 70° C
XR68C92IP	40	PDIP	-40° C to + 85° C
XR68C92IJ	44	PLCC	-40° C to + 85° C
XR68C92IV	44	TQFP	-40° C to + 85° C

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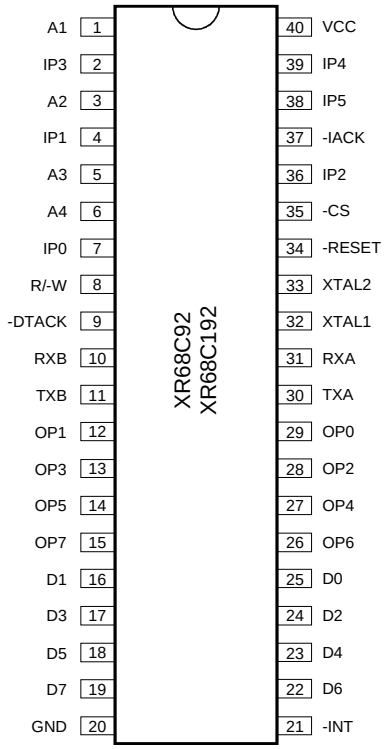
XR68C192CV	44	TQFP	0° C to + 70° C
XR68C192IP	40	PDIP	-40° C to + 85° C
XR68C192IJ	44	PLCC	-40° C to + 85° C
XR68C192IV	44	TQFP	-40° C to + 85° C

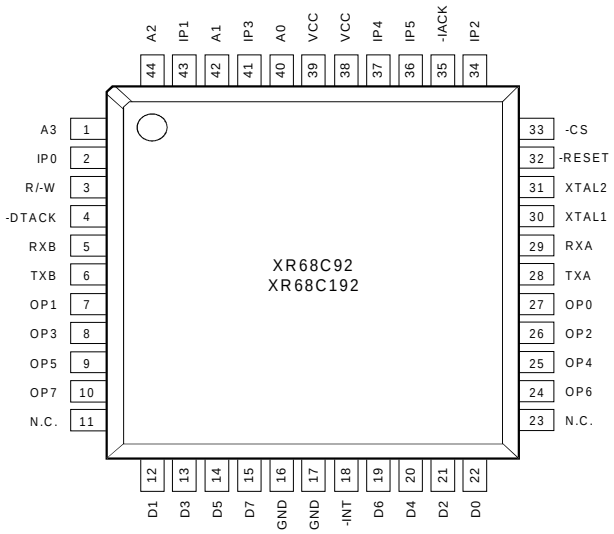
EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 • (510) 668-7000 • FAX (510) 668-7017

Package Description

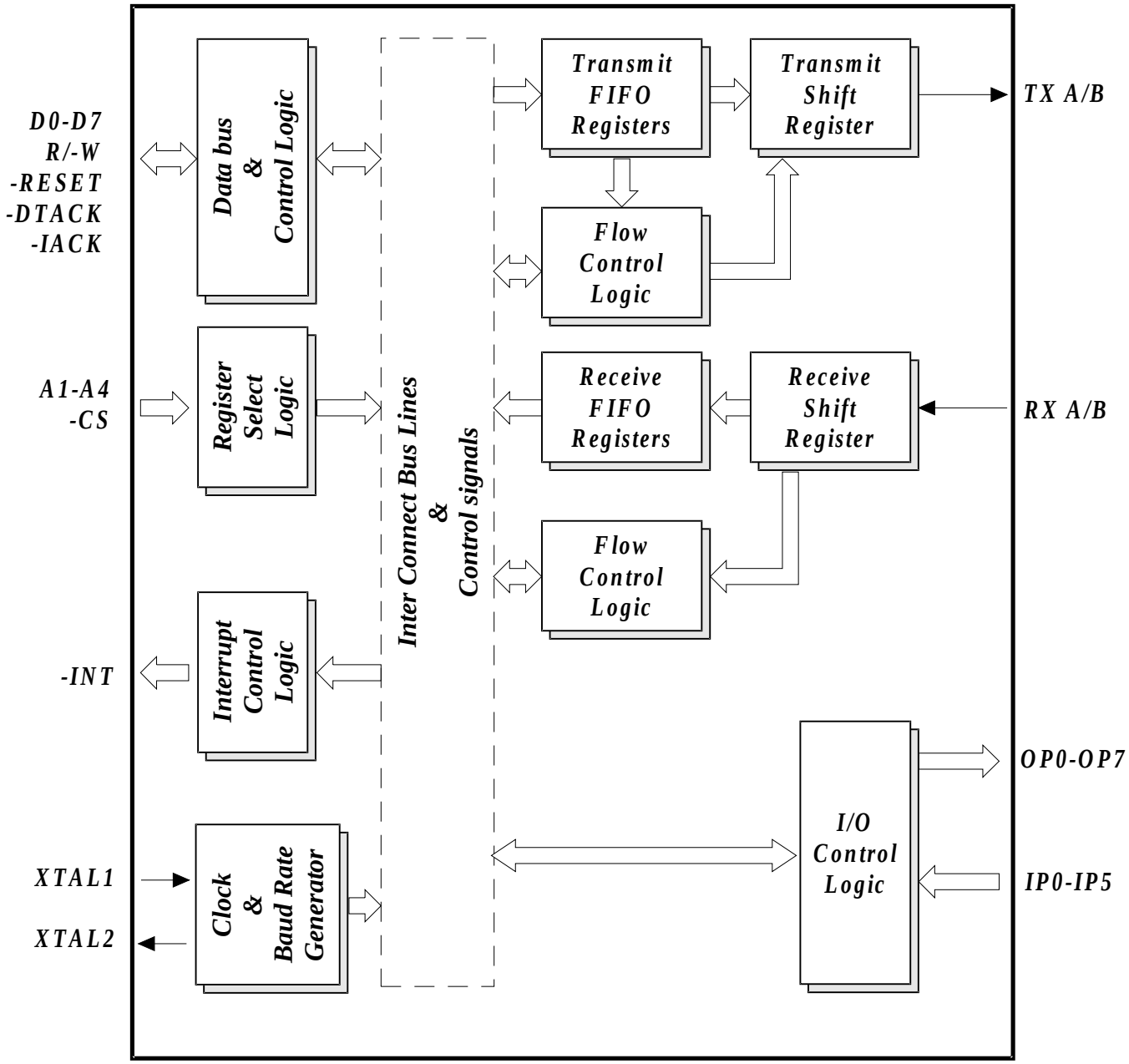
40 Pin DIP Package



44 Pin TQFP Package



Block Diagram



SYMBOL DESCRIPTION (* 44 TQFP Package)

Symbol	Pin 44	Pin 40	Pin 44*	Signal type	Pin Description
-DTACK	10	9	4	O	Data transfer acknowledge (three-state active low output). During Read, Write, or interrupt cycle goes low to indicate proper transfer of data between the CPU and XR68C92/192.
RX A/B	35,11	31,10	29,5	I	Serial data input. The serial information (data) received from serial port to XR68C92/192 receive input circuit. A mark (high) is logic one and a space (low) is logic zero.
TX A/B	33,13	30,11	28,6	O	Serial data output. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loop back mode or when the transmitter is disabled.
OP0	32	29	27	O	Multi-purpose output. General purpose output or Channel A Request-To-Send (-RTSA active low).
OP1	14	12	7	O	Multi-purpose output. General purpose output or Channel B Request-To-Send (-RTSB active low).
OP2	31	28	26	O	Multi-purpose output. General purpose output or one of the following functions can be selected for this output pin by programming the Output Port Configuration Register bits 1,0: **TxAClk1** -Transmit 1X clock. **TxAClk16** -Transmit 16X clock **RxAClk1** -Receive 1X clock
OP3	15	13	8	O	Multi-purpose output. General purpose output or one of the following functions can be selected for this output pin by programming the Output Port Configuration Register bits 3,2: **C/T** -Counter timer output (Open drain output) **TxBClk1** -Transmit 1X clock **RxBClk1** -Receive 1X clock
OP4	30	27	25	O	Multi-purpose output. General purpose output or one of the following functions can be selected for this output pin by programming the Output Port Configuration Register bit 4: -**RxARDY** -Receive ready signal (Open drain output) **-RxAFULL** - Receive FIFO full signal (Open drain output)

SYMBOL DESCRIPTION (* 44 TQFP Package)

Symbol	Pin 44	Pin 40	Pin 44*	Signal type	Pin Description
OP5	16	14	9	O	Multi-purpose output. General purpose output or one of the following functions can be selected for this output pin by programming the Output Port Configuration Register bit 5: -**RxBRDY** - Receive ready signal (Open drain output) **-RxBFULL** - Receive FIFO full signal (Open drain output)
OP6	29	26	24	O	Multi-purpose output. General purpose output or Transmit A holding register empty interrupt (**-TxARDY** Open drain output).
OP7	17	15	10	O	Multi-purpose output. General purpose output or Transmit B holding register empty interrupt (**-TxBRDY** Open drain output).
A1-A4	2,4, 6,7	1,3, 5,6	40,42, 44,1	I	Address select lines. To select internal registers.
XTAL1	36	32	30	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	37	33	31	O	Crystal input 2 or buffered clock output. See XTAL1.
-RESET	38	34	32	I	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
GND	22	20	16,17	Pwr	Signal and power ground.
-INT	24	21	18	O	Interrupt output (open drain active low) This pin goes low upon occurrence of one or more of eight maskable interrupt conditions (when enabled by the interrupt mask register) . CPU can read the interrupt status register to determine the interrupting condition(s). This output requires a pull-up resistor.
IP0	8	7	2	I	Multi-purpose input or Channel A Clear-To-Send (-CTSA active low).
IP1	5	4	43	I	Multi-purpose input or Channel B Clear-To-Send (-CTSB

SYMBOL DESCRIPTION (* 44 TQFP Package)

Symbol	Pin 44	Pin 40	Pin 44*	Signal type	Pin Description
					active low).
IP2	40	36	34	I	Multi-purpose input or Timer/Counter External clock input.
IP3	3	2	41	I	Multi-purpose input or Channel A transmit external clock input. The transmit data is clocked on the falling edge of the clock.
IP4	43	39	37	I	Multi-purpose input or Channel A receive external clock input. The received data is clocked on the rising edge of the clock.
IP5	42	38	36	I	Multi-purpose input or Channel B Transmit external clock input. The transmit data is clocked on the falling edge of the clock.
-IACK	41	37	35	I	Interrupt acknowledge (active low). Indicating an interrupt acknowledge cycle. XR68C92/192 will place the interrupt vector on the data bus and will set -DTACK low if it has a pending interrupt.
-CS	39	35	33	I	Chip select (active low). A low at this pin enables the serial port / CPU data transfer operation.
D0-D7	28,18 27,19 26,20 25,21	25,16 24,17 23,18 22,19	22,12 21,13 20,14 19,15	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
R/-W	9	8	3	I	Read/Write strobe. When -CS is asserted, a high level on this pin transfers the contents of the XR68C92/192 data bus to the CPU, and a low level on this pin will transfer the contents of the CPU data bus to the addressed register.
VCC	44	40	38,39	Pwr	Power supply input.
N.C.	1,12 23,34		11,23		No Connection.

INTERNAL CONTROL LOGIC

The internal control logic receives operation commands from the central processing unit (CPU) and generates appropriate signals to the internal sections to control device operation. The internal control logic allows access to the registers within the XR68C92/192 and performs various commands by decoding the four register-select lines (A1 through A4). Besides the four register-select lines, there are three other inputs to the internal control logic from the R/-W (Read/write), which allows read and write transfers between the CPU and XR68C92/192 via the data bus buffer, -CS (chip-select), which is the XR68C92/192 chip-select, and -RESET (reset), which initializes or resets. The -DTACK (data transfer acknowledge) signal, which is asserted during read, write, or interrupt-acknowledge cycles, is the internal control logic output. The -DTACK signal indicates to the CPU that data has been latched on a CPU write cycle or that valid data is present on the data bus during a CPU read cycle or -IACK (interrupt-acknowledge) cycle.

TIMING LOGIC

The timing logic consists of a crystal oscillator, a baud-rate generator (BRG), a programmable 16-bit counter/timer (C/T), and four clock selectors. The crystal oscillator operates directly from a 3.6864 MHz crystal connected across the XTAL1 and XTAL2 inputs or from an external clock of the appropriate frequency connected to XTAL1. The XTAL1 clock serves as the basic timing reference for the baud-rate generator, the C/T, and other internal circuits.

The baud-rate generator operates from the XTAL1 clock input and can generate 28 commonly used data communication baud rates ranging from 50 to 230.4k by producing internal clock outputs at 16 times the actual baud rate. The C/T can produce a 16X clock for other baud rates by counting down its programmed clock source. Other baud rates can also be derived by connecting 16X or 1X clocks to certain input port pins that have alternate functions as receiver or transmitter clock inputs. Four clock selectors allow the independent selection of any of these baud rates for each receiver and transmitter. Users can program the 16 bit C/T within the XR68C92/192 to use one of several clock sources as its input. The output of the C/T is available to the internal clock selectors and can also be programmed to appear at parallel output OP3. In the timer mode, the C/T acts as a programmable divider and can generate a square-wave output at OP3. In the counter mode, the C/T can be started and stopped under program control. When stopped, the CPU can read its contents. The counter counts down the number of pulses stored in the concatenation of the C/T upper register and C/T lower register and produces an interrupt. This is a system-oriented feature that can be used to record timeouts when implementing various application protocols.

INTERRUPT CONTROL LOGIC

The following registers are associated with the interrupt control logic:

- Interrupt Mask Register (IMR)
- Interrupt Status Register (ISR)
- Auxiliary Control Register (ACR)
- Interrupt Vector Register (IVR)

A single active-low interrupt output (-INT) can notify the processor that any of eight internal events has occurred. These eight events are described in the discussion of the interrupt status register (ISR). User can program the interrupt mask register (IMR) to allow only certain conditions to cause -INT to be asserted while the CPU can read the ISR to determine all currently active interrupting conditions. When an active-low interrupt acknowledge signal (-IACK) from the processor is asserted while the XR68C92/192 has an interrupt pending, the XR68C92/192 will place the contents of the interrupt vector register (IVR) on the data bus and assert the data transfer acknowledge signal (-DTACK). If the XR68C92/192 has no pending interrupt, it ignores -IACK cycles. In addition, users can program the interrupt outputs from the transmitters, the receivers, and the C/T to appear at the parallel output pins OP3 through OP7.

DATA BUS BUFFER

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the internal control logic to allow read and write data transfer operations to occur between the controlling CPU and XR68C92/192 via the eight parallel data lines (D0 through D7).

COMMUNICATION CHANNELS A AND B

Each communication channel includes a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and each transmitter can be selected independently from the baud-rate generator, the C/T, or from an external clock. The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits, and outputs a composite serial stream of data on the TX output pin. The receiver accepts serial data on the RX pin, converts this serial input to parallel format, checks for a start bit, stop bit, parity bit (if any), or break condition, and transfers an assembled character to the CPU during read operations.

INPUT PORT

The CPU reads the inputs to this 6-bit port (IP0 through IP5). High or low inputs to the input port result in the CPU reading a logic one or logic zero, respectively. Each input port bit also has an alternate control function capability. The alternate functions can be enabled/disabled on a bit-by-bit basis.

Four change-of-state detectors are associated with inputs IP0, IP1, IP2, and IP3. If a high-to-low or low-to-high transition occurs on any of these inputs and the new level is stable for more than 25 to 50 microseconds (best-to-worst case times), the corresponding bit in the input port change register (IPCR) will be set. The sampling clock of the change detectors is the XTAL1/96 tap of the baud-rate generator, which is 38.4kHz if XTAL1 is 3.6864MHz. A new input level must be sampled on two consecutive sample clocks to produce a change detect. Also, users can program the XR68C92/192 to allow a change of state to generate an interrupt to the CPU. The IPCR bits are cleared when the CPU reads the register.

OUTPUT PORT

The 8 output port pins can either be used as a general-purpose output port or can be controlled using internal registers to generate signals representing various conditions. Associated with the output port is an output port register (OPR) that can be bit-wise programmed. A bit is set (logical 1) by performing a write operation at address 0xE with the data having that bit-location to be 1 (0 means no change). Similarly, a bit is reset (logical 0) by performing a write operation at address 0xF with the data having that bit-location as 1 (0 means no change). However, it is to be noted that the outputs are complements of the data contained in the OPR (eg., 0x05 in OPR actually means 0xFA at the output pins).

Besides general-purpose outputs, the outputs can be individually assigned specific auxiliary functions serving the communication channels. The assignment is accomplished by appropriately programming the channel A and B mode registers (MR0A, MR0B, MR1A, MR1B, MR2A, and MR2B) and the output port configuration register (OPCR).

NOTE: The terms assertion and negation will be used extensively to avoid confusion when dealing with a mixture of "active low" and "active high" signals. The term assert or assertion indicates that a signal is active or true, independent of whether that level is represented by a high or low voltage. The term negate or negation indicates that a signal is inactive or false.

CRYSTAL INPUT (XTAL2)

If a crystal is used, it is connected between XTAL1 and this input, in which case a capacitor of approximately 15 to 33pF should be connected from this pin to ground. If an external CMOS-level clock is used, this pin must be left open.

-RESET (RESET)

The XR68C92/192 can be reset by asserting the -

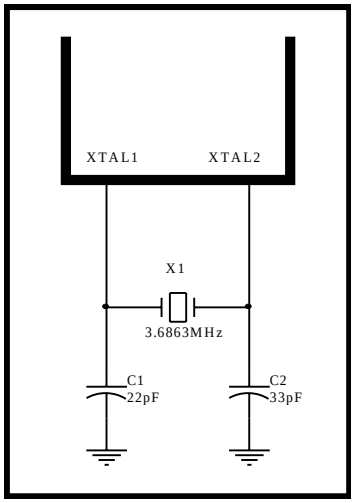


Figure 1: Crystal Connection

RESET signal or soft-reset by programming the appropriate command register. A hardware reset (assertion of RESET) clears the following registers:

- Status registers A and B (SRA and SRB)
- Interrupt mask register (IMR)
- Interrupt status register (ISR)
- Output port register (OPR)
- Output port configuration register (OPCR)

RESET performs the following operations:

- Initializes the interrupt vector register (IVR) to "0F" Hex
- Places parallel outputs OP0 through OP7 in the high state
- Places the counter/timer in timer mode
- Places channels A and B in the inactive state with the transmitter serial-data outputs (TXA and TXB) in the mark (high) state.

Software resets are not as encompassing and are achieved by appropriately programming the channel A and/or B command registers. Reset commands can be programmed through the command register to reset the receiver, transmitter, error status, or break-change interrupts for each channel

CHIP-SELECT (-CS)
This active-low input signal, when low, enables data transfers between the CPU and XR68C92/192 on the data lines (D0 through D7). These data transfers are controlled by read/write (R/-W) and the register-select inputs (A1 through A4). When chip-select is high, the D0 through D7 data lines are placed in the high-impedance state.

READ/WRITE (R/-W)
When high, this input indicates a read cycle, when low, it indicates a write cycle. Assertion of the chip-select input initiates a cycle.

DATA TRANSFER ACKOWLEDGE (-DTACK)
This three-state active low output is asserted in read, write, or interrupt-acknowledge (-IACK) cycles to indicate the proper transfer of data between the CPU and XR68C92/192. If there is no pending interrupt on an -IACK cycle, -DTACK is not asserted. At the end of a transfer, it drives high momentarily, then is three-stated so that it can be "wire-AND"-ed with other -DTACK sources, like an open-drain signal.

INTERUPT ACKOWLEDGE (-IACK)
This active-low input indicates an interrupt-acknowledge cycle. If there is an interrupt pending (-INT asserted) and this pin is asserted, the XR68C92/192 responds by placing the interrupt vector on the data bus and then asserting -DTACK. If there is no interrupt pending (-INT negated), the XR68C92/192 ignores this signal.

REGISTER-SELECT BUS (A1–A4)
The register-select bus lines during read/write operations select the XR68C92/192 internal registers or ports.

INTERUPT REQUEST (-INT)
This active-low, open-drain output signals the CPU that one or more of the eight maskable interrupting conditions is true.

CHANNEL A/B TRANSMITTER SERIAL-DATA OUTPUT (TXA/TXB)
The independent transmitter serial-data outputs for channel A and B transmit the least-significant bit first. The output is held high (mark condition) when its associated transmitter is disabled, idle, or operating in the local loopback mode. ("Mark" is high and "space" is low). Data is shifted out from this pin on the falling edge of the programmed clock source.

CHANNEL A/B RECEIVER SERIAL-DATA INPUT (RXA/RXB)
The independent receiver serial-data inputs for channel A and B receive the least-significant bit first. Data on these pins is sampled on the rising edge of the programmed clock source.

INPUT PORTS (IP0–IP5)
The input ports can be used as general-purpose inputs. However, each pin also has an alternate function(s) described below:

IP0
This input can be used as the channel A clear-to-send active-low input (-CTSA). A change-of-state detector (Input Port Configuration Register bit-4) is also associated with this input.

IP1
This input can be used as the channel B clear-to-send active-low input (-CTSB). A change-of-state detector

(IPCR bit-5) is also associated with this input.

IP2
This input can be used as the channel B receiver external clock input (RxBClk1), or the counter/timer external clock input. When this input functions as the external clock to the receiver, the received data is sampled on the rising edge of the clock. A change-of-state detector (IPCR bit-6) is also associated with this input.

IP3
This input can serve as the channel A transmitter external clock input (TxAClk1). When this input functions as the external clock to the transmitter, the transmitted data is clocked on the falling edge of the clock. A change-of-state detector (IPCR bit-7) is also associated with this input.

IP4
This input can be used as the channel A receiver external clock input (RxAClk1). When this input functions as the external clock to the receiver, the received data is sampled on the rising edge of the clock.

IP5
This input can serve as the channel B transmitter external clock (TxBClk1). When this input is used as the external clock to the transmitter, the transmitted data is clocked on the falling edge of the clock.

OUTPUT PORTS (OP0–OP7)
The output ports can be used as general-purpose outputs however, each pin also has an alternate function(s), described below.

OP0
This output can function as the channel A transmitter active-low request-to-send output, or as the channel A receiver active-low request-to-send (-RTSA) output. This pin, if asserted by programming the corresponding bit in OPCR, is used by the transmitter (MRA2 bit-5 = 1) to indicate end of transmission by negating it. This is useful because, even when a command to disable the transmitter is sent before the data is fully transmitted, the transmitter sends all the data, negates OP0 and then gets disabled. When used by the receiver (MRA1 bit-7 = 1), this pin is automatically negated and reasserted depending on the FIFO space available.

OP1
This output is identical to OP0 and is meant for channel B of the DUART.

OP2
This output can be programmed (bits 0 & 1 of OPCR) to represent the channel A transmitter 1X-clock or 16X-clock output or the channel A receiver 1X-clock output.

OP3
This output can be used (when bits 2 & 3 of OPCR are programmed) as the open-drain active-low counter-ready output, the open-drain timer output, the channel B transmitter 1X-clock output, or the channel B receiver 1X-clock output.

OP4
This output, when programmed using bit-4 of OPCR, can serve as the channel A open-drain active-low receiver-ready or buffer-full interrupt outputs (RxARDY/RxAFULL). One of RxARDY or RxAFULL can be selected using bit-6 of MRA1.

OP5
This output, when programmed using bit-5 of OPCR can be used as the channel B open-drain active-low receiver-ready or buffer-full interrupt outputs (RxRDYB/RxBFULL). One of RxBRDY or RxBFULL can be selected using bit-6 of MRB1.

OP6
This output can function as the channel A open-drain active-low transmitter-ready interrupt output (TxARDY).

OP7
This output can serve as the channel B open-drain active-low transmitter-ready interrupt output (TxBRDY).

TRANSMITTER
The channel A and B transmitters are enabled for data transmission through their respective command registers. The XR68C92/192 signals the CPU that it is ready to accept a character by setting the transmitter-ready bit in the channel's status register. Users can program this condition to generate an interrupt request on the -INT output, an interrupt request for channel A's transmitter on parallel output OP6, or for channel B's transmitter on parallel output OP7. When a character is loaded into the transmit buffer, the above condition

for the respective channel is negated. Data is transferred from the transmit holding register to the transmit shift register when the shift register is idle or has completed transmission of the previous character. The transmitter ready conditions are then reasserted, providing one full character time of buffering. Characters cannot be loaded into the transmit buffer while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the transmitter serial-data output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least-significant bit is sent first. Data is shifted out the transmit serial data output pin on the falling edge of the programmed clock source. After the transmission of the stop bits, and a new character is not available in the transmit holding register, the transmitter serial-data output remains high and the transmitter-empty bit in the status register (SRA and SRB) will be set to one. Transmission resumes and the transmitter-empty bit is cleared when the CPU loads a new character into the transmit buffer. If the transmitter receives a disable command, it will continue operating until the character in the transmit shift register is completely sent out. Other characters in the holding register are neither sent nor discarded, but will be sent when the transmitter is re-enabled. Users can program the transmitter to automatically negate the request-to-send (RTS) output (alternate function of OP0 and OP1) on completion of a message transmission. If the transmitter is programmed to operate in this manner, the RTS output must be manually asserted before each message is transmitted. If OP0 (or OP1) is programmed in automatic RTS mode, the RTS output will be automatically negated when the transmitter is disabled and the transmit-shift register and holding register are both empty. In automatic RTS mode, a character in the holding register is not held back by a disable, but no more characters can be written to the holding register after the transmitter is disabled.

If clear-to-send (CTS) operation is enabled, the CTS input (alternate function of IP0 or IP1) must be low in order for the character to be transmitted. If it goes high in the middle of a transmission, the character in the shift register is transmitted and TX then remains in the marking state until CTS again goes low. The transmitter can also be forced to send a continuous low condition by issuing a send-break command. The state of CTS is ignored by the transmitter when it is set to send break. A send break is deferred as long as the transmitter has characters to send, but if normal character transmission is inhibited by CTS, the send-break will proceed. The send-break must be terminated by a stop-break, disable, or reset before normal character transmission can resume.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and must be enabled through the command register before resuming operation. Reset also discards any character in the holding register.

RECEIVER

The channel A and B receivers are enabled for data reception through the respective channels command register. The channels receiver looks for the high-to-low (mark-to-space) transition of a start bit on the receiver serial-data input pin. If operating in 16X clock mode, the serial input data is re-sampled on the next 7 clocks. If the receiver serial data is sampled high, the start bit is invalid and the search for a valid start bit begins again. If receiver serial data is still low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals (at the theoretical center of the bit) until the proper number of data bits and the parity bit (if any) have been assembled and one stop bit has been detected. Data on the receiver serial data input pin is sampled on the rising edge of the programmed clock source.

During this process, the least-significant bit is received first. The data is then transferred to a receive holding register (RHR) and the receiver-ready bit in the status register (SRA or SRB) is set to one. This condition can be programmed to generate an interrupt request on the -INT output, an interrupt request for channel A receiver on output pin(OP4), or an interrupt request for channel B receiver on output pin (OP5). If the character length is less than eight bits, the most significant unused bits in the receive holding register (RHR) are set to zero.

If the stop bit is sampled as a 1, the receiver will immediately look for the next start bit. However, if the stop bit is sampled as a 0, either a framing error or a received break has occurred. If the stop bit is 0 and the data and parity (if any) are not all zero, it is a framing

error, the damaged character is transferred to a holding register with the framing error flag set. If the receiver serial data remains low for one-half of the bit period after the stop bit was sampled, the receiver operates as if a new start bit transition has been detected. If the stop bit is 0 and the data and parity (if any) are also all zero, it is a break. A character consisting of all zeros will be loaded into a receive holding register (RHR) with the received-break bit (but not the framing error bit) set to one. The receiver serial-data input must return to a high condition for at least one-half bit time before a search for the next start bit begins.

The receiver can detect a break that starts in the middle of a character provided the break persists completely through the next character time or longer. When the break begins in the middle of a character, the receiver will place the damaged character in a holding register with the framing error bit set. Then, provided the break persists through the next character time, the receiver will also place an all-zero character in the next holding register with the received-break bit set. The parity error, framing error, overrun error, and received-break conditions (if any) set error and break flags in the status register at the received character boundary and are valid only when the receiver-ready bit (RxRDY) in the status register is set. A first-in first-out (FIFO) stack is used in each channels receive buffer logic and consists of 8 (16 for XR68C192) receive holding registers.

The receiver buffer is composed of the FIFO and a receive shift register connected to the receiver serial-data input. Data is assembled in the shift register and loaded into the top most empty FIFO receive holding register position. The receiver-ready bit in the status register (SRA or SRB) is set whenever one or more characters are available to be read. A read of the receiver buffer produces an output of data from the top of the FIFO stack. After the read cycle, the data at the top of the FIFO stack and its associated status bits are “popped” and new data can be added at the bottom of the stack by the receive shift register. The FIFO-full status bit is set if all eight stack positions are filled with data. Either the receiver-ready or the FIFO-full status bits can be selected to cause an interrupt. In addition to the data byte, three status bits (parity error, framing error, and received break) are appended to each data character in the FIFO (overrun is not). By programming the error-mode control bit in the mode register, status can be provided for “character” or “block” modes.

In the “character” mode, the status register (SRA or SRB) is updated on a character-by-character basis and applies only to the character at the top of the FIFO. Thus, the status must be read before the character is read. Reading the character pops it and its error flags off the FIFO. In the “block” mode, the status provided in the status register for the parity error, framing error, and received-break conditions are the logical OR of these respective bits, for all characters coming to the top of the FIFO stack since the last reset error command was issued. That is, starting at the last reset-error command, a continuous logical-OR function of corresponding status bits is produced in the status register as each character comes to the top of the FIFO stack.

The block mode is useful in applications requiring the exchange of blocks of information where the software overhead of checking each characters error flags cannot be tolerated. In this mode, entire messages can be received and only one data integrity check is performed at the end of each message. Although data reception in this manner has speed advantages, there are also disadvantages. Because each character is not individually checked for error conditions by the software, if an error occurs within a message the error will not be recognized until the final check is performed. Also, there is no indication of which character(s) is in error within the message.

Reading the status register (SR) does not affect the FIFO. The FIFO is “popped” only when the receive buffer is read. If all 8/16 of the FIFOs receive holding registers are full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected, but the character previously in the shift register is lost and the overrun-error status bit will be set upon receipt of the start bit of the new overrunning character.

To support flow control, a receiver can automatically negate and reassert the request-to-send (RTS) output (alternate function of output ports OP0 and OP1). The request-to-send output will automatically be negated by the receiver when a valid start bit is received and the FIFO stack is full. When a FIFO position becomes available, the request-to-send output will be reasserted

automatically by the receiver. Connecting the request-to-send output to the clear-to-send (CTS) input of a transmitting device, prevents overrun errors in the receiver. The RTS output must be manually asserted the first time. Thereafter, the receiver will control the RTS output.

If the FIFO stack contains characters and the receiver is then disabled, the characters in the stack can still be read but no additional characters can be received until the receiver is again enabled. If the receiver is disabled while receiving a character, or while there is a character in the shift register waiting for a FIFO opening, these characters are lost. If the receiver is reset, the FIFO stack and all of the receiver status bits, the corresponding output ports, and the interrupt request are reset. No additional characters can be received until the receiver is again enabled.

LOOPBACK MODES

Besides the normal operation mode in which the receiver and transmitter operate independently, each XR68C92/192 channel can be configured to operate in various looping modes that are useful for local and remote system diagnostic functions.

AUTOMATIC ECHO MODE

In this mode, the channel automatically retransmits the received data on a bit-by-bit basis. The local CPU-to-receiver communication continues normally but the CPU-to-transmitter link is disabled.

LOCAL LOOPBACK MODE

In this mode, the transmitter output is internally connected to the receiver input. The external TX pin is held in the mark (high) state in this mode. This mode is useful for testing the operation of a local XR68C92/192 channel. By sending data to the transmitter and checking that the data assembled by the receiver is the same data that was sent, proper channel operation can be ensured. In this mode the CPU-to-transmitter and CPU-to-receiver communications continue normally.

REMOTE LOOPBACK MODE

In this mode, the channel automatically retransmits the received data on a bit-by-bit basis. The local CPU-to-receiver and CPU-to-transmitter links are disabled. This mode is useful in testing the receiver and transmitter operation of a remote channel. This mode requires the remote channel receiver to be enabled.

MULTIDROP MODE

Users can program the channel to operate in a wake-up mode for Multidrop applications. This mode is selected by setting bits 3 & 4 in Mode Register 1 (MR1). In this mode of operation, a master station channel, connected to several slave stations (a maximum of 256 unique slave stations), transmits an address character followed by a block of data characters targeted for one or more of the slave stations. In this mode, the channel receivers within the slave stations are disabled, but they continuously monitor the data stream sent out from the master station. When the slave stations channel receivers detect any address character in the data stream, each receiver notifies its respective CPU by setting receiver ready (RXRDY) and generating an interrupt, if programmed to do so. Each slave station CPU then compares the received address to its station address and enables its receiver if it wants to receive the subsequent data from the master station.

Slave stations that are not addressed continue monitoring the data stream for the next address character. An address character flags the end of one block of data and the start of another. After receiving a block of data, the slave stations CPU may disable the channel receiver and re-initiate the process. A transmitted character from the master station consists of a start bit, the programmed number of data bits, an address/data (A/D) bit flag, and the programmed number of stop bits. The address/data bit identifies to the slave stations channel whether the character should be interpreted as an address character or a data character. The character is interpreted as an address character if the A/D bit is set to a one or interpreted as a data character if it is set to a zero. The polarity of the transmitted address/data bit is selected by programming bit two in Mode Register 1 (MR1) to a '1' for an address character and to a '0' for data characters. Users should program the mode register prior to loading the corresponding data or address characters into the transmit buffer.

In the Multidrop mode, the receiver continuously monitors the received data stream regardless of whether it is enabled or disabled. If the receiver is disabled, it sets the receiver ready status bit and loads the character into the FIFO receive holding register stack provided the received address/data bit is a one

(address tag). The received character is discarded if the received address/data bit is a zero (data tag). If the receiver is enabled, all received characters are transferred to the CPU by way of the receive holding register stack during read operations. In either case, the data bits are loaded into the data portion of the FIFO stack while the address/data bit is loaded into the status portion of the FIFO stack normally used for parity error (Status Register bit-5). Framing error, overrun error, and break-detection operate normally regardless of whether the receiver is enabled or disabled. The address/data bit takes the place of the parity bit and parity is neither calculated nor checked for characters in this mode.

COUNTER/TIMER

The 16-bit counter/timer (C/T) can operate in a counter mode or a timer mode. In either mode, users can program the C/T input (clock source) to come from several sources and program the C/T output to appear at output port pin OP3. The value (pre-load value) stored in the concatenation of the C/T upper register (CTUR) and the C/T lower register (CTLR) can be from 0x0001 through 0xFFFF and can be changed at any time. In counter mode, the CPU can start and stop the C/T. This mode allows the C/T to function as a system stopwatch, a real-time single interrupt generator, or a device watchdog. In timer mode, the C/T runs continuously, the CPU cannot start or stop it. Instead, the CPU only resets the C/T interrupt. This mode allows the C/T to be used as a programmable clock source for channels A and B, or periodic interrupt generator. At power-up and after reset, the C/T operates in timer mode.

COUNTER MODE

In counter mode, the C/T counts down from the pre-load value using the programmed counter clock source. The counter clock source can be the channel A transmitter clock, the channel B transmitter clock, the external clock on the XTAL1 pin divided by sixteen, or an external clock on the input port pin IP2. The CPU can start and stop the counter, and can read the count value (CUR:CLR) if the counter is stopped. When a read at the start counter command address is performed, the counter is initialized to the pre-load value and begins a countdown sequence. When the counter counts from 0x0001 to 0x0000 (terminal count), the C/T-ready bit in the interrupt status register (ISR Bit-3) is set.

Users can program the counter to generate an interrupt request for this condition on the -INT output or output pin OP3. After 0x0000 the counter counts to 0xFFFF, and continues counting down from there. If the CPU changes the pre-load value, the counter will not recognize the new value until it receives the next start counter command (and is reinitialized). When a read at the stop counter command address is performed, the counter stops the countdown sequence and clears ISR Bit-3. The count value should only be read while the counter is stopped because only one of the count registers (either CUR or CLR) can be read at a time. If the counter is running, a decrement of CLR that requires a borrow from the CUR could take place between the two reads.

TIMER MODE

In timer mode, the C/T generates a square-wave output derived from the programmed timer input (clock source). The timer clock source can be the external clock on the XTAL1 input pin divided by one or sixteen, or it can be an external input on input port pin IP2 divided by one or sixteen. The square wave generated by the timer has a period of 2X (pre-load value) X (period of clock source), is available as a clock source for both communications channels and can be programmed to appear on output pin OP3. The timer runs continuously, the CPU cannot stop it. Because the timer cannot be stopped, the count value (CUR:CLR) should not be read. When a read at the start counter command address is performed, the timer terminates the current countdown sequence, sets its output to 1 (appears un-inverted at OP3), is initialized to the pre-load value, and begins a new countdown sequence. When the counter counts from 0x0001 (terminal count), it inverts its output, is re-initialized to the pre-load value and repeats the countdown sequence.

After reaching terminal count a second time, the timer sets the C/T-ready bit in the interrupt status register (ISR Bit-3), inverts its output, is re-initialized again, and begins a new countdown sequence. Users can program the timer to generate an interrupt request for this condition (every second countdown cycle) on the -INT output. If the CPU changes the pre-load value, the timer will not recognize the new value until either (a) it reaches the next terminal count and is reinitialized automatically, or (b) it is forced to re-initialize by a start command. When a read at the stop counter command address is performed, the timer clears ISR Bit-3 but does not stop. Because in timer mode the C/T runs continuously, it should be completely configured (pre-

PROGRAMMING AND REGISTER DESCRIPTIONS

A3	A2	A1	A0	READ	WRITE
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock-Select Register A (CSRA)
0	0	1	0	Reserved	Command Register A (CRA)
0	0	1	1	Receiver Buffer A (RBA)	Transmitter Buffer A (TBA)
0	1	0	0	Input Port Change Register (IPCR)	Auxiliary Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer MSB (CUR)	Counter/ Timer Upper Register (CTUR)
0	1	1	1	Counter/Timer LSB(CLR)	Counter/ Timer Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock-Select Register B (CSRB)
1	0	1	0	Reserved	Command Register B (CRB)
1	0	1	1	Receiver Buffer B (RBB)	Transmitter Buffer B (TBB)
1	1	0	0	Interrupt-Vector Register (IVR)	Interrupt-Vector Register (IVR)
1	1	0	1	Input Port (IP)	Output Port Configuration Register (OPCR)
1	1	1	0	Start-Counter Command	Set Output Port Register (OPR) bits
1	1	1	1	Stop-Counter Command	Reset Output Port Register (OPR) bits

load value loaded and start counter command issued) before programming the timer output to appear on OP3. Use caution if the contents of a register are changed during receiver/ transmitter operation as certain changes can produce undesired results. For example, changing the number of bits per character while the transmitter is active can transmit an incorrect character. The contents of the clock-select register (CSR) and ACR Bit-7 should only be changed after the receiver(s) and transmitter(s) have been issued software RX and TX reset commands. Most bits of the mode registers should not be changed during receiver/transmitter operation, except that in Multidrop parity mode, the address/data parity type bit can be changed at any time.

Similarly, certain changes to the auxiliary control register (ACR Bits 4-6) should only be made while the counter/timer (C/T) is not used. Channel A mode registers MR1A and MR2A are accessed via an auxiliary pointer. The pointer is set to mode register one (MR1A) by RESET or by issuing a “reset pointer” command via the channel A command register. Any read or write of the mode register switches the pointer to mode register two (MR2A). All subsequent accesses will address MR2A unless the pointer is reset to MR1A as described above. The channel B mode registers MR1B and MR2B are accessed by an identical pointer independent of the channel A pointer. Mode, command, clock-select, and status registers are duplicated for each channel to allow independent operation and control (except that both channels are restricted to baud rates that are in the same set).

A3	A2	A1	A0	Register [Default]	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	0	MRA0 [00]	Watch dog timer	RX trigger level	TX trigger level	TX trigger level	Not used	Baud rate ext. 2	Not used	Baud rate ext. 1
1	0	0	0	MRB0[00]								
0	0	0	0	MRA1[00]	RX RTS control	RX trigger level	Error mode	Parity mode	Parity mode	Parity type	Word length	Word length
1	0	0	0	MRB1[00]								
0	0	0	0	MRA2[00]	Channel mode select	Channel mode select	TX RTS control	TX CTS control	Stop bit length	Stop bit length	Stop bit length	Stop bit length
1	0	0	0	MRB2[00]								
0	0	0	1	CSRA[00]	RX clock	RX clock	RX clock	RX clock	TX clock	TX clock	TX clock	TX clock
1	0	0	1	CSRB[00]								
0	0	0	1	SRA[00]	Received break	Framing error	Parity error	Overrun error	TX empty	TX ready	RX FIFO full	RX ready
1	0	0	1	SRB[00]								
0	0	1	0	CRA[00]	Misc. command	Misc. command	Misc. command	Misc. command	TX disable	TX enable	RX disable	RX enable
1	0	0	0	CRB[00]								
0	0	1	1	RHRA[XX]	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1	0	1	1	RHRB[XX]								
0	0	1	1	THRA[XX]	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1	0	1	1	THRB[XX]								
0	1	0	0	ACR[00]	Baud rate set select	C/T mode	C/T mode	C/T mode	Delta IP3 INT	Delta IP2 INT	Delta IP1 INT	Delta IP0 INT
0	1	0	0	IPCR[00]	Delta IP3	Delta IP2	Delta IP1	Delta IP0	IP3 input	IP2 input	IP1 input	IP0 input
0	1	0	1	ISR[00]	Input port change	Delta break B	RXB ready/ FIFO full	TXB ready	C/T ready	Delta break A	RXA ready/ FIFO full	TXA ready
0	1	0	1	IMR[00]	Input port change	Delta break B	RXB ready/ FIFO full	TXB ready	C/T ready	Delta break A	RXA ready/ FIFO full	TXA rdy
0	1	1	0	CTU[00]	Bit-15	Bit-14	Bit-13	Bit-12	Bit-11	Bit-10	Bit-9	Bit-8
0	1	1	1	CTL[00]	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1	1	0	1	IPR[XX]	Not Used	Not Used	IP5	IP4	IP3	IP2	IP1	IP0
1	1	0	1	OPCR[00]	OP7	OP6	OP5	OP4	OP3	OP3	OP2	OP2
1	1	1	0	STCC[XX]	X	X	X	X	X	X	X	X
1	1	1	0	SOPB[00]	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1	1	1	1	SPCC[XX]	X	X	X	X	X	X	X	X
1	1	1	1	ROPB	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0

MR0 A/B
Mode register 0. This register is accessed only when command is applied via CR A/B register. After reading or writing to MR0 A/B register, the pointer will point to MR1 A/B register.

MR0 A/B Bit-0.
Extended baud rate table selection.
0 = Normal baud rate tables
1 = Extend baud rate tables (1)

MR0 A/B Bit-1.
0 = Regular Operation
1 = Factory test mode

MR0 A/B Bit-2.
Extended baud rate table selection.
0 = Normal baud rate tables
1 = Extend baud rate tables (2)

MR0 A/B Bit-3.
Not used.

MR0 A/B Bits 5-4
Transmit trigger levels:

MR0 Bit-5	MR0 Bit-4	XR68C92
0	0	8 FIFO locations empty
0	1	4 FIFO locations empty
1	0	6 FIFO locations empty
1	1	1 FIFO location empty

MR0 Bit-5	MR0 Bit-4	XR68C192
0	0	16 FIFO locations empty
0	1	6 FIFO locations empty
1	0	12 FIFO locations empty
1	1	1 FIFO location empty

MR0 A/B Bit-6.
Receive trigger levels:

MR0 Bit-6	MR1 Bit-6	XR68C92
0	0	1 byte in FIFO
0	1	3 bytes in FIFO
1	0	6 bytes in FIFO
1	1	8 bytes in FIFO

MR0 Bit-6	MR1 Bit-6	XR68C192
0	0	1 byte in FIFO
0	1	6 bytes in FIFO
1	0	12 bytes in FIFO
1	1	16 bytes in FIFO

MR0 A/B Bit-7.
Receive time-out (watch dog timer).
0 = Disabled
1 = Enabled

MR1 A/B
Mode register 1. MR1 A/B are accessed after reset or by command applied via CR A/B register. After reading or writing to MR1 A/B register, the pointer will point to MR2 A/B register.

MR1 A/B Bits 1-0.
Character Length
0 0 = 5
0 1 = 6
1 0 = 7
1 1 = 8

MR1 A/B Bit-2.
Parity Type
0 = Even Parity
1 = Odd Parity

MR1 A/B Bit 4-3.
Parity mode
00 = With parity
01 = Force parity
10 = No parity
11 = Multidrop mode

MR1 A/B Bit-5.
Data error mode
0 = Single Character mode
1 = Block (FIFO) mode

MR1 A/B Bit-6.
Receive Interrupt mode select.
0 = Single character mode (RxRdy)
1 = FIFO Full mode (FFULL)

MR1 A/B Bit-7.
Auto RTS flow control.

0 = Normal. No RTS control function.
1 = Auto RTS control function

MR2 A/B
Mode register 2. This register is accessed after any read or write operation to MR1 A/B register is performed. Access to MR2 A/B does not change the pointer.

MR2 A/B Bits 3-0.
Stop bit length
0000 = 0.563
0001 = 0.625
0010 = 0.668
0011 = 0.750
0100 = 0.813
0101 = 0.875
0110 = 0.938
0111 = 1.000
1000 = 1.563
1001 = 1.625
1010 = 1.668
1011 = 1.750
1100 = 1.813
1101 = 1.875
1110 = 1.938
1111 = 2.000

MR2 A/B Bit-4.
Auto CTS flow control
0 = Normal. No CTS control function
1 = Auto CTS control function.

MR2 A/B Bit-5.
Transmit RTS control.
0 = Normal. No control function
1 = Transmit RTS function enable.

MR2 A/B Bit 7-6.
Channel Mode.
0 0 = Normal
0 1 = Automatic Echo
1 0 = Local Loopback
1 1 = Remote Loopback

CLOCK SELECT REGISTER-CSR A/B
Transmit / Receive baud rates can be selected via this register.

CSR A/B Bits 3-0.
Transmit clock select (see baud rate table)

CSR A/B Bits 7-4.
Receive clock select (see baud rate table)

MISCELLANEOUS COMMAND REGISTER CR A/B
CR A/B register is used to supply commands to A/B channels. Multiple commands can be specified in a single write to CR A/B as long as commands are non-conflicting.

CR A/B Bits 1-0.
Receiver Commands
0 0 = No Action, Stays in Present Mode
0 1 = Receiver Enabled
1 0 = Receiver Disabled
1 1 = Not Used

CR A/B Bits 3-2.
Transmitter Commands
0 0 = No Action, Stays in Present Mode
0 1 = Transmitter Enabled
1 0 = Transmitter Disabled
1 1 = Not Used

CR A/B Bits 7-4.
Miscellaneous Commands.
0 0 0 0 = No Command.
0 0 0 1 = Reset MR Pointer to MR1.
0 0 1 0 = Reset Receiver. Receiver is disabled and FIFO is flushed.
0 0 1 1 = Reset Transmitter. Transmitter is disabled and FIFO is flushed.
0 1 0 0 = Reset Error Status. Clears channel A/B, break, parity, and over-run error bits in the status register.
0 1 0 1 = Reset Channels Break-Change Interrupt. Clears channel A/B break detect change bit in the interrupt status register (ISR Bit-2).
0 1 1 0 = Start Break. Forces the transmitter output to go low and stay low. If transmitter is empty the start of the break condition will be delayed up to two bit times. If transmitter is active, the break begins when transmission of the character is completed. All contents of the FIFO has to be transmitted before break signal takes place. Transmitter must to be enabled for this command to be accepted.
0 1 1 1 = Stop Break. Transmit output will go high within two bit times.
1 0 0 0 = Set -RTS output to low.
1 0 0 1 = Reset -RTS output to high.

Baud Rate Table (based on a 3.6864MHz clock)

	MR0 Bits 2,0=0		MR0 Bit-0=1 (extended 1)		MR0 Bit-2=1 (extended 2)	
CSR A/B	**SET-1 ACR Bit-7=0**	**SET-2 ACR Bit-7=1**	**SET-1 ACR Bit-7=0**	**SET-2 ACR Bit-7=1**	**SET-1 ACR Bit-7=0**	**SET-2 ACR Bit-7=1**
0000	50	75	300	450	4800	7200
0001	110	110	110	110	680	680
0010	134.5	134.5	134.5	134.5	1076	1076
0011	200	150	1200	900	19.2k	14.4k
0100	300	300	1800	1800	28.8k	28.8k
0101	600	600	3600	3600	57.6k	57.6k
0110	1200	1200	7200	7200	115.2k	115.2k
0111	1050	2000	1050	2000	1050	2000
1000	2400	2400	14.4k	14.4k	57.6k	57.6k
1001	4800	4800	28.8k	28.8k	4800	4800
1010	7200	1800	7200	1800	57.6k	14.4k
1011	9600	9600	57.6k	57.6k	9600	9600
1100	38.4k	19.2k	230.4k	115.2k	38.4k	19.2k
1101	Timer	Timer	Timer	Timer	Timer	Timer
1110	IP4-16X	IP4-16X	IP4-16X	IP4-16X	IP4-16X	IP4-16X
1111	IP4-1X	IP4-1X	IP4-1X	IP4-1X	IP4-1X	IP4-1X

1 01 0 = Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the receive FIFO. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR Bit-3 is reset. (See also Watchdog timer description in the receiver section.)

1 0 1 1 = Set MR pointer to MR0.

1 1 0 0 = Disable Timeout Mode. This command returns control of the C/T to the regular Start/Stop counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a "Stop Counter" command should be issued to force a reset of the ISR Bit-3.

1 1 0 1 = Not used.

1 1 1 0 = Power Down Mode On. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a XTAL1. While in the power down mode, do not issue any commands to the CR A/B except the disable power down mode command. The contents of all registers will be saved while in this mode. It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. This command is in CRA only.

1 1 1 1 = Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR A/B. This command is in CRA only. For maximum power reduction input pins should be at GND or VCC.

STATUS REGISTER (SRA/SRB)

SR A/B Bit-0.
Receive Ready.
This bit indicates that one or more character(s) has been received and is waiting in the FIFO for the CPU to read it. It is set when the first character is transferred

from the receive shift register to the empty FIFO, and cleared when the CPU reads the receiver buffer, if there are no more characters in the FIFO after the read.

SR A/B Bit-1.
Receive FIFO Full.
This bit is set when a character is transferred from the receive shift register to the receiver FIFO and the transfer fills the FIFO. All eight FIFO holding register positions are occupied. It is cleared when the CPU reads the receiver buffer, unless a ninth character is in the receive shift register waiting for an empty FIFO slot.

SR A/B Bit-2.
Transmit Ready.
This bit (when set) indicates that the transmit holding register is empty and ready to be loaded with a character. Transmitter ready is set when the character is transferred to the transmit shift register. This bit is cleared when the CPU loads the transmit holding register, or when the transmitter is disabled.

SR A/B Bit-3.
Transmit Empty.
This bit will be set when the channel A/B transmitter under-runs (empty). Both the transmit holding register and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the transmit holding register awaiting transmission. It is cleared when the CPU loads the transmit holding register or when the transmitter is disabled.

SR A/B Bit-4.
Overrun Error.
This bit (when set) indicates one or more characters in the received data stream have been lost. It becomes set on receipt of a valid start bit when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error, and framing error status, if any) is lost. A reset error status command clears this bit.

SR A/B Bit-5.
Parity Error.
This bit becomes set when the “with parity” or “force parity” mode is programmed by mode register one and the corresponding character in the FIFO is received with incorrect parity. In the Multidrop mode, the parity error bit position stores the received address/data bit. This bit is valid only when the RxRDY bit is set (SR A/B Bit-0 = 1).

SR A/B Bit-6.
Framing Error.
This bit (when set) indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position. This bit is valid only when the RxRDY bit is set (SR A/B Bit-0 = 1). Framing error and break are exclusive: At least one data bit and/or the parity bit must have been a 1 to signal a framing error. After a framing error, the receiver does not wait for the line to return to the marking state (high), if the line remains low for 1/2 a bit time after the stop bit sample (that is, the nominal end of the first stop bit), the receiver treats it as the beginning of a new start bit.

SR A/B Bit-7.
Received Break.
This bit indicates an all-zero character of the programmed length has been received without a stop bit. This bit is valid only when the RxRDY bit is set (SR A/B Bit-0 = 1). Only a single FIFO position is occupied when a break is received, additional entries to the FIFO are inhibited until the channel A/B receiver serial data input line returns to the marking state. The break-detect circuitry can detect a break that starts in the middle of a received character, however, the break condition must persist completely through the end of the current character and the next character time to be recognized.

OUTPUT PORT CONFIGURATION REGISTER (OPCR)
This register selects following options for output ports. Alternate functions of OP1 and OP0 are controlled by the mode registers, not the OPCR. MR1A Bit-7 and MR2A Bit-5 control OP0, MR1B Bit-7 and MR2B Bit-5 control OP1.

OP2 output select
0 0 = The complement of OPR
0 1 = TxAClk16-Transmit A 16X clock
1 0 = TxAClk1-Transmit A 1X clock
1 1 = RxAClk1- Receive A 1X clock

OP3 output select
0 0 = The complement of OPR
0 1 = C/T Output 1
1 0 = TxBClk1-Transmit B 1X clock
1 1 = RxBClk1- Receive B 1X clock

If OP3 is to be used for the timer output, Users should program the counter/timer for timer mode (ACR Bit-6 = 1), initialize the counter/timer pre-load registers (CTUR and CTLR), and the start counter command issued before setting OPCR Bits 3-2 = 01.

OP4 output select
0 = The complement of OPR
1 = -RxARDY/-RxAFULL

OP5 output select
0 = The complement of OPR
1 = -RxBRDY/-RxBFULL

OP6 output select
0 = The complement of OPR
1 = -TxARDY

OP7 output select
0 = The complement of OPR
1 = -TxBRDY

Output Port Register (OPR)
All bits, unless programmed for alternate function, can be set high or low individually:
0 = Sets output port high
1 = Sets output port low
For example, setting bit-4 to 1 will set OP4 low.

AUXILIARY CONTROL REGISTER (ACR)

ACR Bits 3-0.
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR Bit-7) to be set.
0 = Disabled
1 = Enabled

ACR Bits 6-4.
Counter/Timer Mode and Clock Source. Should only be altered while the C/T is not in use (stopped if in counter mode, output and/or interrupt masked if in timer mode).

MODE	CLOCK	SOURCE
0 0 0	Counter	External (IP2)
0 0 1	Counter	TXAClk1-Transmit A 1X clock
0 1 0	Counter	TXBClk1-Transmit B 1X clock
0 1 1	Counter	Crystal or External Clock (XTAL1/Clk) Divided by 16
1 0 0	Timer	External (IP2)
1 0 1	Timer	External (IP2) Divided by 16
1 1 0	Timer	Crystal or External Clock (XTAL1/Clk)
1 1 1	Timer	Crystal or External Clock (XTAL1/Clk) Divided by 16

ACR Bit-7
Baud rate table Select. Should only be changed after both channels have been reset and are disabled.

0 = Set 1
1 = Set 2

INPUT PORT CHANGE REGISTER (IPCR)

IP Level Bits 3-0.
0 = Low
1 = High

IP Delta Bits 7-4.
0 = No
1 = Yes

INTERRUPT STATUS REGISTER (ISR)
This register provides the status of all potential interrupt sources. The contents of this register are logically “AND”-ed with the contents of the interrupt mask register, and the results are "NOR"-ed to produce the -INT output. All active interrupt sources are visible by reading the ISR, regardless of the contents of the interrupt mask register. Reading the ISR has no effect on any interrupt source. Each active interrupt source must be cleared in a source-specific fashion to clear the ISR. All interrupt sources are cleared when the XR68C92/192 is reset.

ISR Bit-0.
Transmit ready A. This bit is the channel A equivalent of ISR Bit-4.

ISR Bit-1.
Receive ready A or FIFO full. The function of this bit is

programmed by MR1A Bit-6. If programmed as receiver ready, it is a copy of the SRA Bit-0. If programmed as FIFO full, it is a copy of the SRA Bit-1.

ISR Bit-2.
Channel A change in break. This bit (when set) indicates that the channel A receiver has detected the beginning or the end of a break condition. It is reset when the CPU issues a channel A reset break change interrupt command.

ISR Bit-3.
Counter/Timer ready. In counter mode, this bit is set when the counter reaches terminal count. In timer mode, this bit is set each time the timer output switches from low to high.

ISR Bit-4.
Transmit ready B. This bit is a duplicate of the channel B status register transmitter ready bit.

ISR Bit-5.
Receive ready B or FIFO full. The function of this bit is programmed by MR1B Bit-6. If programmed as receiver ready, it is a copy of the SRB Bit-0. If programmed as FIFO full, it is a copy of the SRB Bit-1.

ISR Bit-6.
Channel B change in break. This bit (when set) indicates that the channel B receiver has detected the beginning or the end of a break condition. It is reset when the CPU issues a channel B reset break change interrupt command.

ISR Bit-7.
Input port change status. This bit is a “1” when a change of state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been enabled to cause an interrupt by the programming of ACR Bits 3-0. This bit is cleared when the CPU reads the input port change register.

INTERRUPT MASK REGISTER (IMR)
This register selects which bits in the interrupt status register can cause an interrupt output. If a bit in the interrupt status register is a “1” and the corresponding bit in this register is also a “1”, the -INT output will be asserted. If the corresponding bit in this register is a zero, the state of the bit in the interrupt status register has no effect on the -INT output. Note that the interrupt mask register does not mask the programmable interrupt outputs OP7 through OP3 or the value read from the interrupt status register.

IMR Bit-0.
0 = Normal, no interrupt.
1 = Enable channel A transmit ready interrupt.

IMR Bit-1.
0 = Normal, no interrupt.
1 = Enable channel A receive ready or FIFO full interrupt. RxRDY or FIFO-full is selected via MR1A Bit-6.

IMR Bit-2.
0 = Normal, no interrupt.
1 = Enable channel A received break signal interrupt.

IMR Bit-3.
0 = Normal, no interrupt.
1 = Enable Timer/Counter interrupt.

IMR Bit-4.
0 = Normal, no interrupt.
1 = Enable channel B transmit ready interrupt.

IMR Bit-5.
0 = Normal, no interrupt.
1 = Enable channel B receive ready or FIFO full interrupt. RxRDY or FIFO-full is selected via MR1B Bit-6.

IMR Bit-6.
0 = Normal, no interrupt.
1 = Enable channel B received break signal interrupt.

IMR Bit-7.
0 = Normal, no interrupt.
1 = Enable input port state change interrupt.

INPUT PORT REGISTER
State of the input ports (IP0-IP6) can be read via this register.

IPR Bit 0-6.
0 = Inputs are in low state.
1 = Inputs are in high state.

IPR Bit-7.
Not used and set to “0”.

COUNTER REGISTER (CUR and CLR)
The count upper register (CUR) and count lower register (CLR) hold the most-significant byte and the least-significant byte, respectively, of the current counter value. These registers should only be read when the C/T is in counter mode and the counter is stopped.

START COUNTER / TIMER REGISTER
Reading from this register will start Timer counter function. Returned data values should be ignored.

STOP COUNTER TIMER REGISTER
Reading from this register will issue a stop command to Timer counter function. Returned data values should be ignored.

SET OUTPUT PORT REGISTER
Output ports (OP0-OP7) can be set to low by writing a “1” to each individual bits. Outputs will change state only when OPCR register bits are assigned to general purpose output pins. When output is set to low, it can not change state to high unless reset output port command is issued.

SOPR Bit 0-7.
0 = No change.
1 = Set output port to low.

RESET OUTPUT PORT BITS REGISTER
Each output port bit can be changed to high state by writing a “1” to each individual bit.

SOPR Bit 0-7.
0 = No change.
1 = Reset output port to high.

INTERRUPT VECTOR REGISTER (IVR)
This register contains the interrupt vector. When the XR68C92 responds to a valid interrupt acknowledge (-IACK) cycle, the contents of this register are placed on the data bus. At reset, this register will contain “0F” hex, which is the M68000 exception vector assignment for un-initialized interrupt vectors.

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
T_{1w}, T_{2w}	Clock pulse duration	17		17		ns	
T_{3w}	Oscillator/Clock frequency		8		24	MHz	
T_{AS}	Address Valid to -CS Low	0		0		ns	
T_{AH}	-CS High to Address Invalid	0		0		ns	
T_{RWS}	R/-W Setup Time to -CS Low	0		0		ns	
T_{RWH}	R/-W Hold Time from -CS High	0		0		ns	
T_{DD}	-CS Low to Data Valid (Read)		51		32	ns	
T_{DS}	Data Valid to -CS High (Write)	20		10		ns	
T_{DH}	-CS High to Data Invalid (Write)	1		1		ns	
T_{DF}	-CS High to Data Hi-Z (Read)		30		20	ns	
T_{AKL}	-CS Low to -DACK Low		70		42	ns	
T_{AKH}	-CS High to -DACK High		45		27	ns	
T_{AKT}	-CS High to -DACK Hi-Z		70		43	ns	
T_{CSL}	-CS Low Pulse Width	100		70		ns	
T_{CSH}	-CS High Pulse Width	100		70		ns	
T_{9s}	Port input setup time	0		0		ns	
T_{9h}	Port input hold time	0		0		ns	
T_{10d}	Delay from R/-W to output		110		110	ns	
T_{11d}	Delay to reset interrupt from R/-W		100		100	ns	
T_R	Reset pulse width	2		2		clks	
N	Baud rate divisor	1	2^{16}-1	1	2^{16}-1	clks	

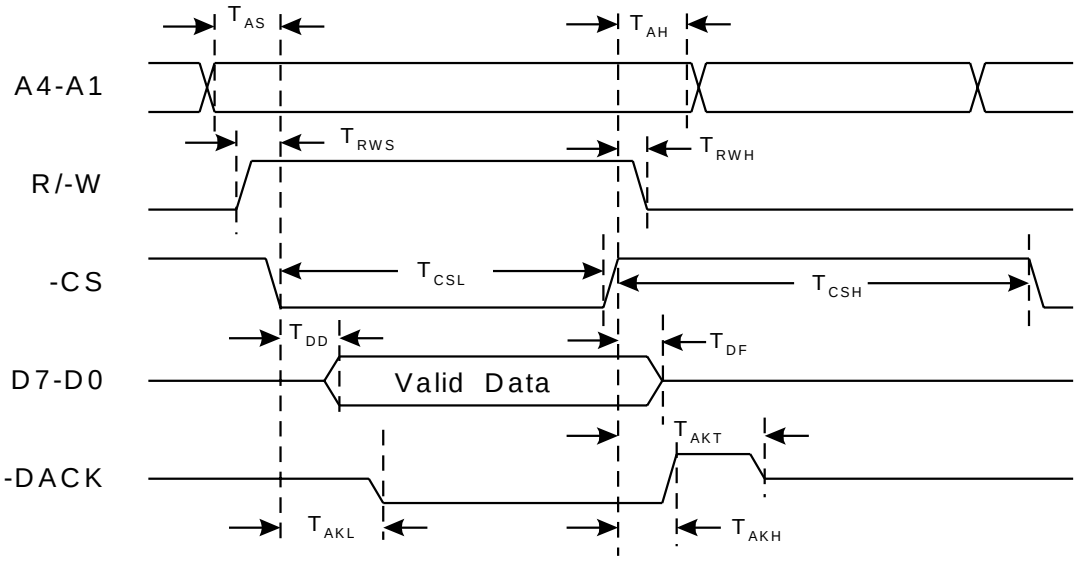
ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND - 0.3 V to VCC +0.3 V
Operating temperature	-40° C to +85° C
Storage temperature	-65° C to 150° C
Package dissipation	500 mW

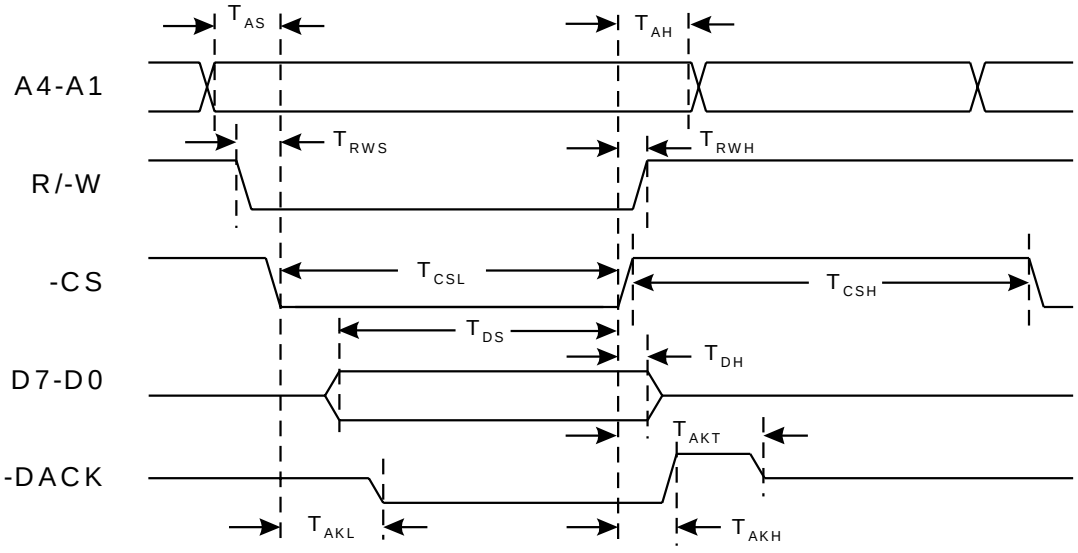
DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
V_{ILCK}	Clock input low level	-0.3	0.6	-0.5	0.6	V	
V_{IHCK}	Clock input high level	2.4	VCC	3.0	VCC	V	
V_{IL}	Input low level	-0.3	0.8	-0.5	0.8	V	
V_{IH}	Input high level	2.0		2.2	VCC	V	
V_{OL}	Output low level on all outputs				0.4	V	I_{OL}= 5 mA
V_{OL}	Output low level on all outputs		0.4			V	I_{OL}= 4 mA
V_{OH}	Output high level			2.4		V	I_{OH}= -5 mA
V_{OH}	Output high level	2.0				V	I_{OH}= -1 mA
I_{IL}	Input leakage		±10		±10	µA	
I_{CL}	Clock leakage		±10		±10	µA	
I_{CC}	Avg power supply current XR68C92		3		6	mA	
I_{SB}	Avg stand by supply current		100		150	µA	
	Typ.@25°C		50		70	µA	
	XR68C192						
I_{SB}	Avg stand by supply current		200		300	µA	
	Typ.@25°C		100		140	µA	
C_P	Input capacitance		5		5	pF	



Read Cycle Timing



Write Cycle Timing

Figure 2: Bus Timing (Read/Write cycle)

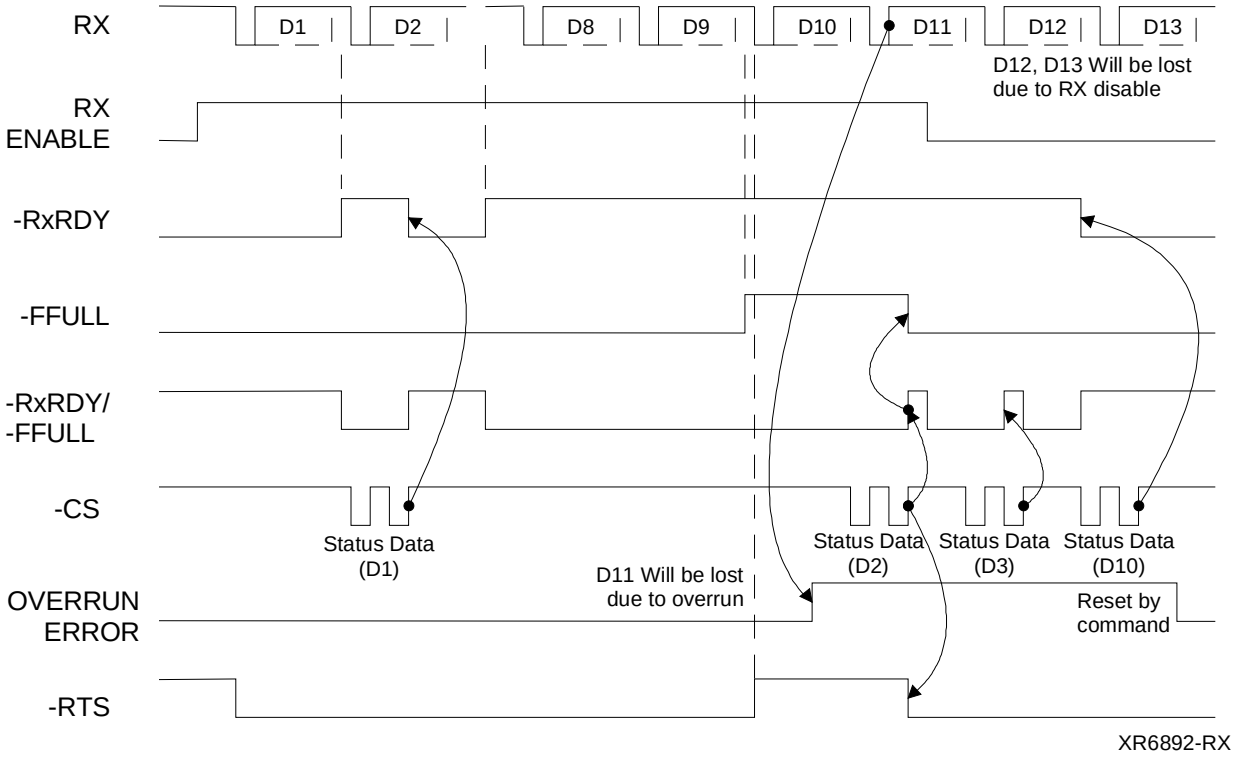


Figure 3: Receive Timing

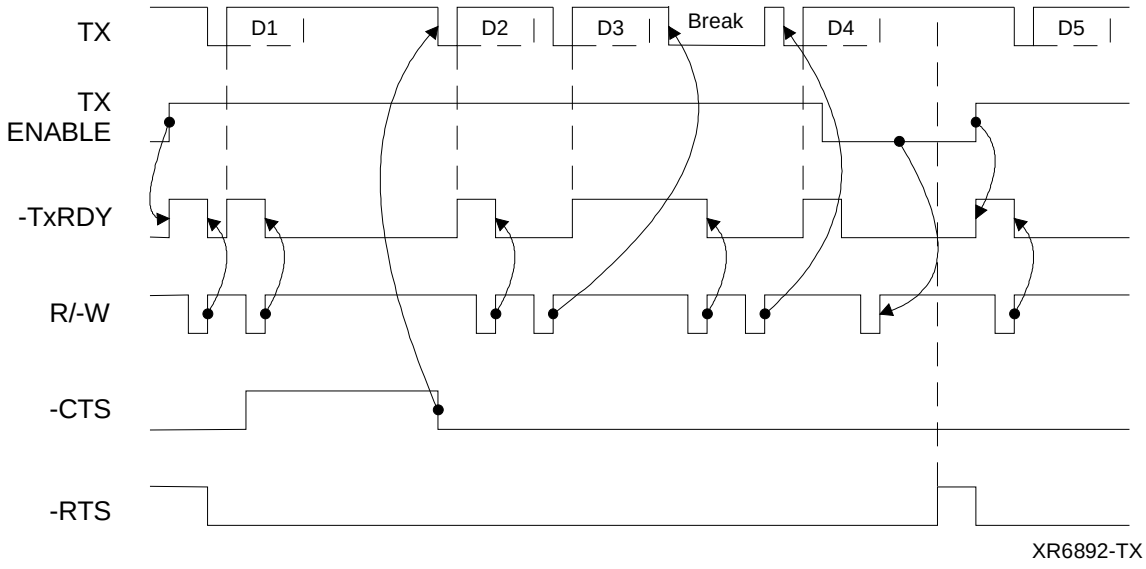


Figure 4: Transmit Timing

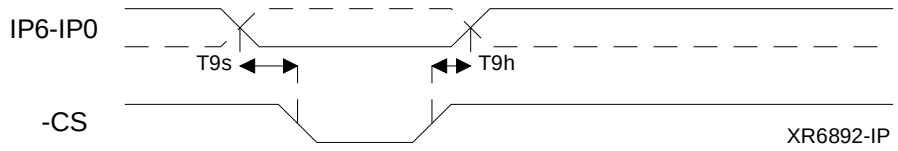


Figure 5: Input Port Timing

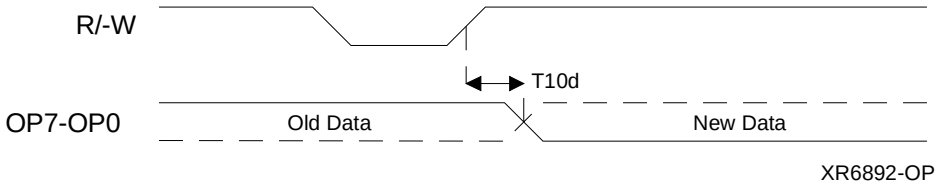


Figure 6: Output Port Timing

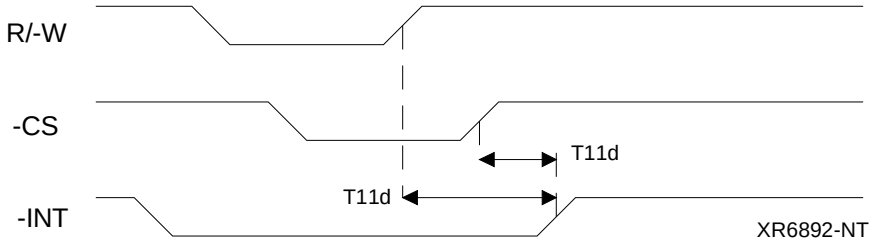


Figure 7: Interrupt Timing

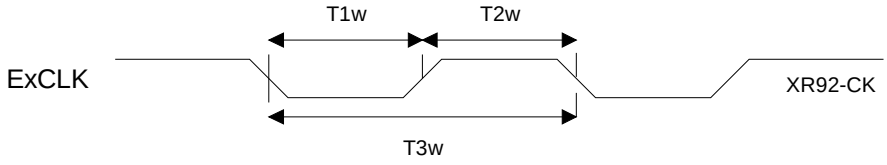
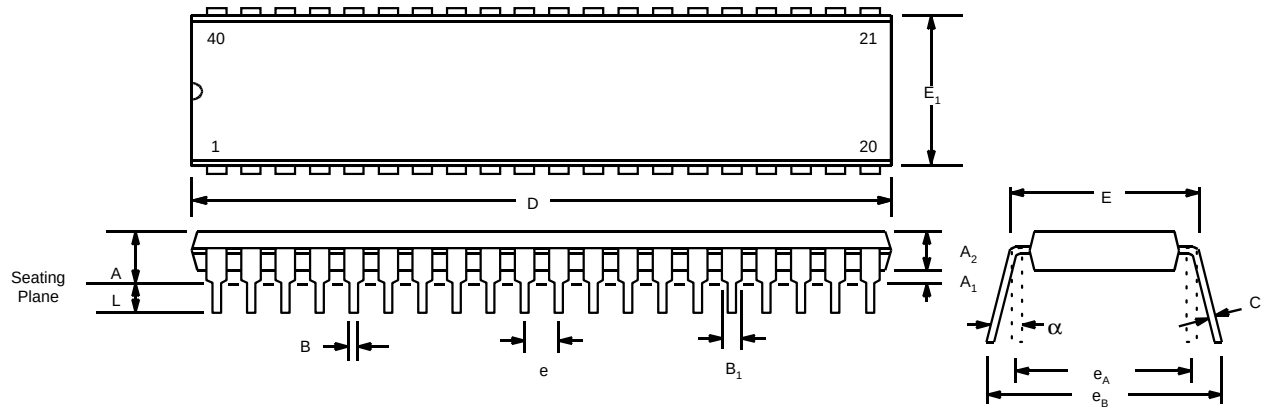


Figure 8: External clock Timing

40 LEAD PLASTIC DUAL-IN-LINE
(600 MIL PDIP)

Rev. 1.00

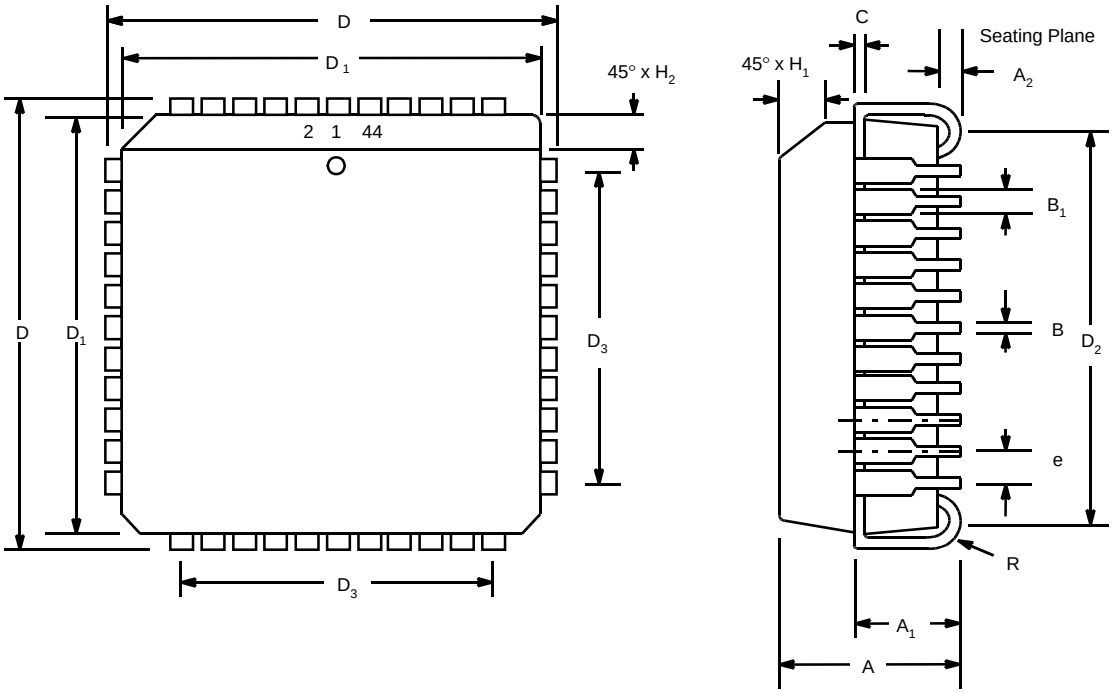


INCHES		MILLIMETERS		
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.16	0.25	4.06	6.35
A1	0.015	0.07	0.38	1.78
A2	0.125	0.195	3.18	4.95
B	0.014	0.024	0.36	0.56
B1	0.03	0.07	0.76	1.78
C	0.008	0.014	0.2	0.38
D	1.98	2.095	50.29	53.21
E	0.6	0.625	15.24	15.88
E1	0.485	0.58	12.32	14.73
e	0.100 BSC		2.54 BSC	
eA	0.600 BSC		15.24 BSC	
eB	0.6	0.7	15.24	17.78
L	0.115	0.2	2.92	5.08
a	0°	15°	0°	15°

Note: The control dimension is the inch column

44 LEAD PLASTIC LEADED CHIP CARRIER (PLCC)

Rev. 1.00

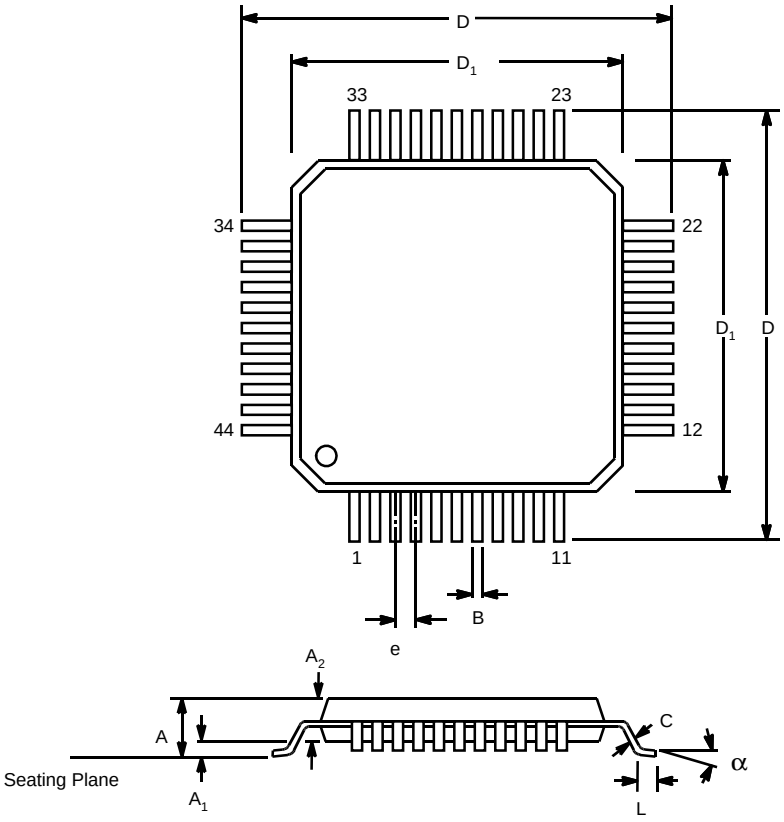


	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.165	0.18	4.19	4.57
A1	0.09	0.12	2.29	3.05
A2	0.02	---.	0.51	---
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.685	0.695	17.4	17.65
D1	0.65	0.656	16.51	16.66
D2	0.59	0.63	14.99	16
D3	0.500 typ.		12.70 typ.	
e	0.050 BSC		1.27 BSC	
H1	0.042	0.056	1.07	1.42
H2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

Note: The control dimension is the inch column

44 LEAD THIN QUAD FLAT PACK
(10 mm x 10 mm x 1.4 mm, TQFP)

Rev. 1.00



	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.055	0.063	1.4	1.6
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.012	0.018	0.3	0.45
C	0.004	0.008	0.09	0.2
D	0.465	0.48	11.8	12.2
D1	0.39	0.398	9.9	10.1
e	0.0315 BSC		0.80 BSC	
L	0.018	0.03	0.45	0.75
a	0°	7°	0°	7°

Note: The control dimension is the inch column

NOTICE

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