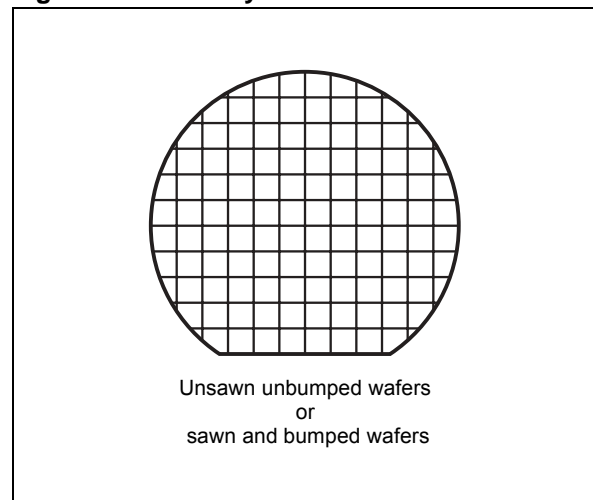


UHF, EPCglobal Class-1 Generation-2, Contactless Memory Chip 432 bit with Multi-session Protocol, Anti-collision and Kill functions

DATA BRIEF

Features summary

- EPCglobal Class-1 Generation-2 specification
- Passive Operation (no battery required)
- UHF Carrier Frequencies from 860 MHz to 960 MHz ISM Band which comply with:
 - North American regulations
 - European regulations
 - and other countries where similar regulations apply
- To the XRAG2:
 - Asynchronous 90% SSB-ASK, DSB-ASK or PR-ASK modulation using Pulse Interval Encoding (Up to 128 kbps)
- From the XRAG2:
 - Backscattered reflective answers using FMO or Miller bit coding (up to 640 kbps)
- 432-bit memory with two possible configurations:
 - 3 memory banks: 64-bit TID, 304-bit EPC and 64-bit RESERVED
 - 4 memory banks: 128-bit USER, 64-bit TID, 176-bit EPC and 64-bit RESERVED
- Multi-session protocol
- Anti-collision functionality
- Inventory, Read, Write and Erase features
- Kill command
- 100-ms Programming Time (max) for 288-bit programming (EPC code, Protocol Control bits and CRC16)
- More than 10,000 Write/Erase cycles
- Over 40 Year Data Retention

Figure 1. Delivery forms

1 Summary description

The XRAG2 is a full-featured, low-cost integrated circuit for use in Radio Frequency Identification (RFID) transponders (tags) operating at UHF frequencies. It is a 432-bit memory organized in 16-bit Words in 3 or 4 memory banks as shown in [Figure 3](#) and [Figure 4](#).

When connected to an antenna, the operating power is derived from RF energy produced by the RFID reader. Incoming data are demodulated and decoded from the received Double-Side Band Amplitude Shift Keying (DSB-ASK), Single-Side Band Amplitude Shift Keying (SSB-ASK) or Phase-Reversal Amplitude Shift Keying modulation signal. Outgoing data are generated by antenna reflectivity variations using either the FM0 or Miller bit coding principle (RFID reader parameter).

A Kill function is provided to permanently disable the tag.

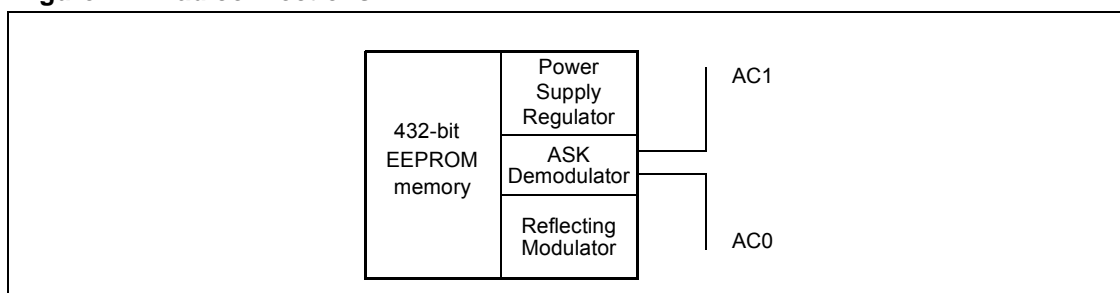
Anti-collision features enable the rapid inventorying of tag populations.

Communication between reader and tag are Half-duplex meaning that tags do not decode reader commands while backscattering.

The data transfer rate is defined by the local UHF frequency regulations.

The XRAG2 is fully compliant with the ePC Global Class-1 Generation-2 UHF RFID specification (Revision 1.0.9) for the radio-frequency power and signal interface.

Figure 2. Pad connections



The reader and the XRAG2 dialog through the following consecutive operations known as RTF (Reader Talk First) communication:

- Activation of the XRAG2 by the UHF operating field of the reader
- Transmission of a command by the reader
- Transmission of a response by the XRAG2

Table 1. Signal names

AC1	Antenna Pad
AC0	Antenna Pad (GND)

The XRAG2 is specifically designed for extended range applications that need automatic item identification. The XRAG2 provides a fast and flexible anti-collision protocol that is robust in noisy and unpredictable RF conditions typical of RFID applications. The XRAG2 EEPROM memory can be read and write which enable users to program the EPC code and USER memory at the point of application, if desired.

2 XRAG2 memory mapping

The XRAG2 is a 432-bit memory divided into a 3-memory bank (without USER memory) or 4-memory bank (with USER memory) configuration. Each bank is organized into 16-bit Words.

The reader can read part or all of each memory bank in single or multiple groups of 16-bit Words. Use the WRITE command to write to device memory using 16-bit Words. The BLOCKWRITE command enables readers to write up to four 16-bit Words to device memory at a single time. Erase multiple 16-bit Words (up to the complete memory bank) using the BLOCKERASE command.

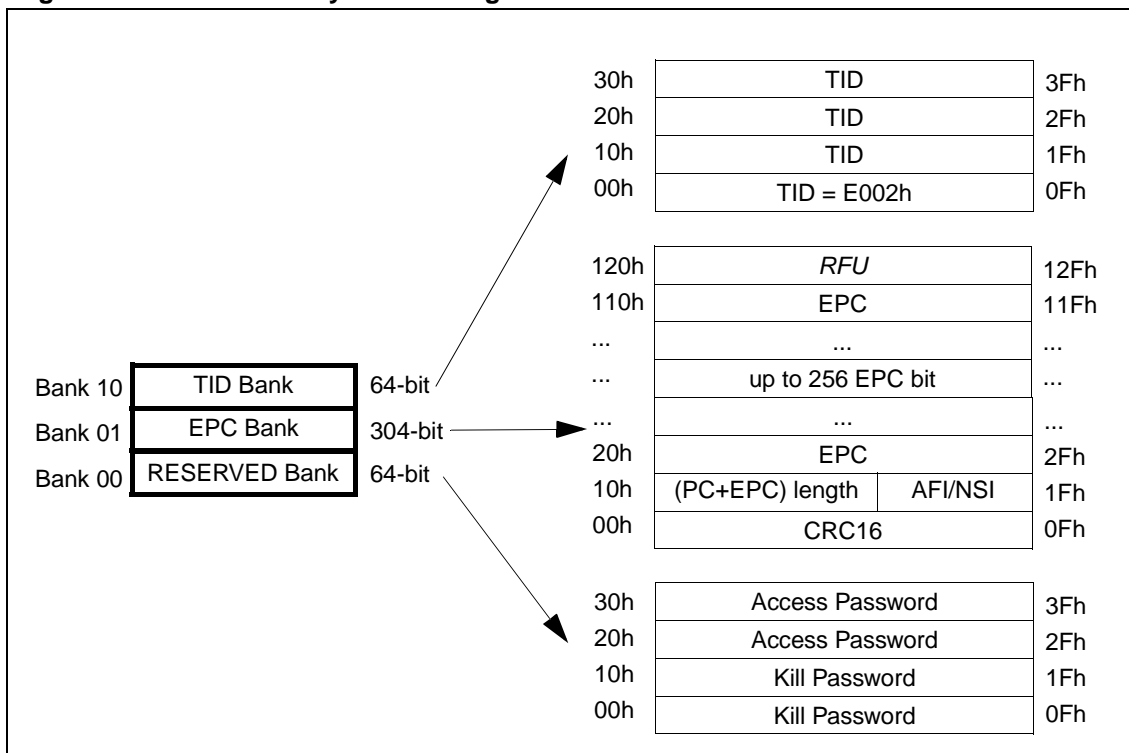
Table 2. Memory bank description

Memory Bank	Description
USER	User-specific data
TID (Tag-identification Data)	Manufacturer and custom information
EPC (Electronic Product Code)	CRC-16, Protocol Control and item identification code (EPC)
RESERVED	Kill and access passwords

Note: The 64-bit TID memory content is written by STMicroelectronics during the manufacturing process in compliance with the ISO 15963 Technical Report in order to comply with ISO 18000 recommendations.

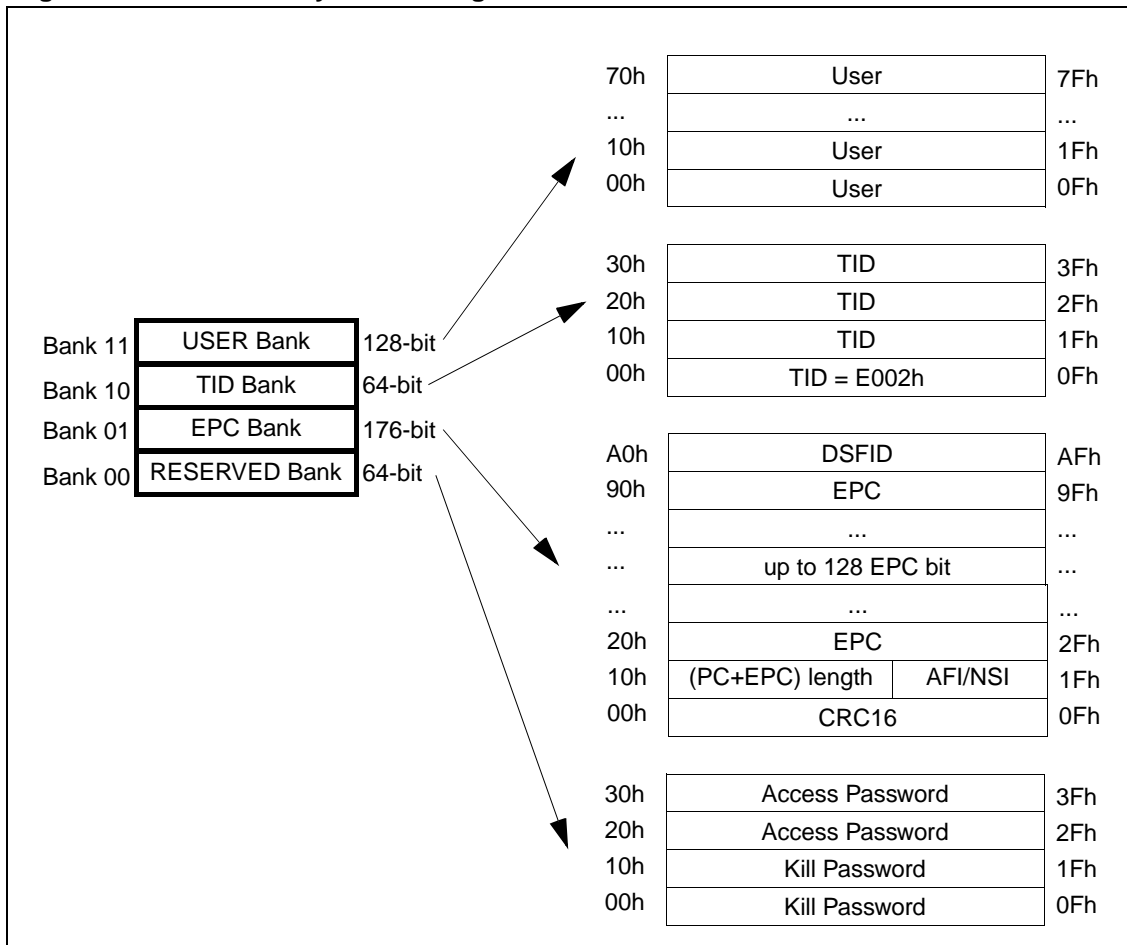
Figure 3 describes the three-memory bank configuration.

Figure 3. Three-memory bank configuration



The four-memory bank configuration is shown in [Figure 4](#).

Figure 4. Four-memory bank configuration



3 XRAG2 commands

The XRAG2 offers Select, Inventory, and Access commands sets supported as defined in ePCglobal Class-1 Generation-2 UHF RFID specifications (Revision 1.0.9).

Table 3. XRAG2 commands

Command Set	Available Commands
Select Command Set	SELECT
Inventory Command Set	QUERY, QUERYADJUST, QUERYREP, ACK and NAK
Access Command Set	REQ_RN, READ, WRITE, KILL, LOCK, ACCESS, BLOCKWRITE and BLOCKERASE

4 Part numbering

Table 4. Ordering information scheme

Example:	XRAG2	-	W4I	/	XXX
Device Type	XRAG2				
Delivery Form	W4I = 180µm ± 15µm UnsaWn Inkless Wafer SBN18I = 180 µm ± 15µm Bumped and Sawn Inkless Wafer on 8 inch frame				
Customer Code	XXX = Customer Code, given by STMicroelectronics				

Note: For further information on any aspect of this device, please contact your nearest ST Sales Office.

5 Revision history

Date	Revision	Changes
18-Jul-2005	1.0	Initial release.
17-Aug-2005	2.0	Replaced TID = E202h by TID = E002h in Figure 3 and Figure 4 .

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics.
All other names are the property of their respective owners

© 2005 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com