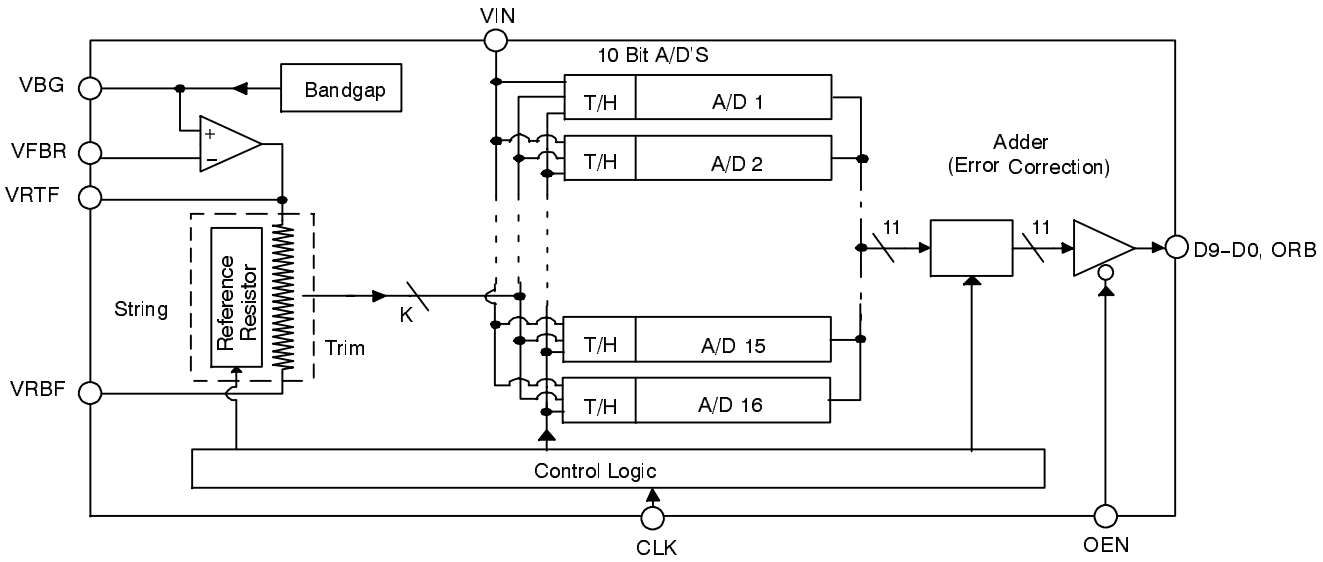
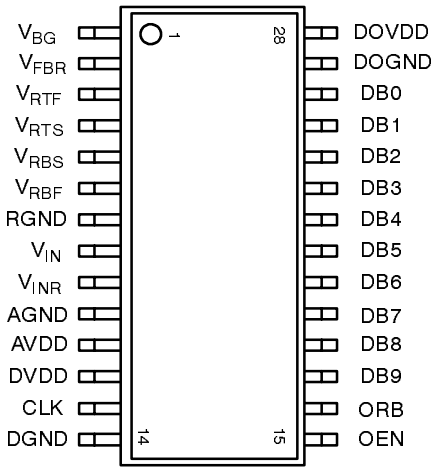


Figure 1. XRD6440 Simplified Block Diagram

PIN CONFIGURATION



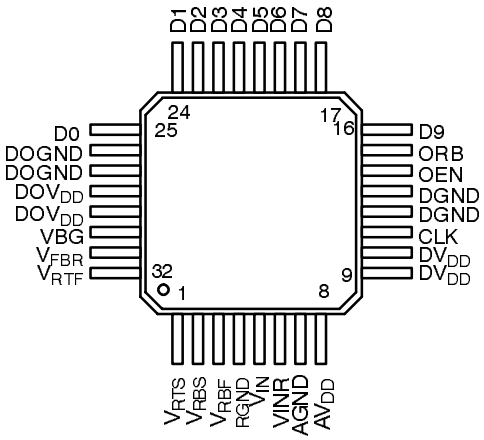
28 Lead SSOP Package

PIN DESCRIPTION (28-Lead SSOP Package)

Pin #	Symbol	Description
1	V_{BG}	Bandgap Voltage Output
2	V_{FBR}	Feedback for Internal Voltage Regulator
3	V_{RTF}	Top(+) Reference Voltage Force
4	V_{RTS}	Top(+) Reference Voltage Sense
5	V_{RBS}	Bottom(-) Reference Voltage Sense
6	V_{RBF}	Bottom(-) Reference Voltage Force
7	RGND	Analog Reference Ground
8	V_{IN}	Analog Voltage Input
9	V_{INR}	Analog Input Reference
10	AGND	Analog Ground
11	AVDD	Analog Power Supply
12	DVDD	Digital Power Supply
13	CLK	Clock Input
14	DGND	Digital Ground
15	OEN	Digital Output Enable (Tri-State Control), Low=Enable, High=Disable (Tri-State)
16	ORB	Over Range Digital Output Bit

PIN DESCRIPTION (CONT'D)

Pin #	Symbol	Description
17	DB9	MSB-Digital Output Data Bit 9
18	DB8	Digital Output Data Bit 8
19	DB7	Digital Output Data Bit 7
20	DB6	Digital Output Data Bit 6
21	DB5	Digital Output Data Bit 5
22	DB4	Digital Output Data Bit 4
23	DB3	Digital Output Data Bit 3
24	DB2	Digital Output Data Bit 2
25	DB1	Digital Output Data Bit 1
26	DB0	LSB- Digital Output Data Bit 0
27	DOGND	Digital Data Output Ground
28	DOVDD	Digital Data Output Power Supply



32 Lead TQFP Package

PIN DESCRIPTION (32-Lead TQFP Package)

Pin #	Symbol	Description
1	V_{RTS}	Top (+) Reference Voltage Sense
2	V_{RBS}	Bottom (-) Reference Voltage Sense
3	V_{RBF}	Bottom (-) Reference Voltage Force
4	RGND	Analog Reference Ground
5	V_{IN}	Analog Voltage Input
6	VINR	Analog Input Reference
7	AGND	Analog Ground
8	AV_{DD}	Analog Power Supply
9	DV_{DD}	Digital Power Supply
10	DV_{DD}	Digital Power Supply
11	CLK	Clock Input
12	DGND	Digital Ground
13	DGND	Digital Ground
14	OEN	Output Enable Control
15	ORB	Out of Range Digital Output
16	D9	Data Output Bit 9 (MSB)
17	D8	Data Output Bit 8
18	D7	Data Output Bit 7
19	D6	Data Output Bit 6
20	D5	Data Output Bit 5
21	D4	Data Output Bit 4
22	D3	Data Output Bit 3
23	D2	Data Output Bit 2
24	D1	Data Output Bit 1
25	D0	Data Output Bit 0 (LSB)

PIN DESCRIPTION(32-Lead TQFP Package)

Pin #	Symbol	Description
26	DOGND	Digital Data Output Ground
27	DOGND	Digital Data Output Ground
28	DOV_{DD}	Digital Data Output Power Supply
29	DOV_{DD}	Digital Data Output Power Supply
30	VBG	Bandgap Voltage Output
31	V_{FBR}	Feedback for Internal Voltage Regulator
32	V_{RTF}	Top (+) Reference Voltage Force

ELECTRICAL CHARACTERISTICS TABLE

Test Conditions (Unless Otherwise Specified):
Ta = 25°C AV_{DD} = DV_{DD} = +5V, V_{IN} = GND to +4V, V_{RBF} = GND, V_{RTF} = +4V and Fs = 40 MSPS, 50% Duty Cycle

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions/Comments
DC ACCURACY						
DNL	Differential Non-Linearity	-1.0	+/-0.7	1.0	LSB	
INL	Integral Non-Linearity		+/-1.1		LSB	
MON	Monotonicity					Guaranteed by Test
ZSE	Zero Scale Error		±20		mV	
ANALOG INPUT						
INVR	Input Voltage Range	AGND		VRTR	V	
INRES	Input Resistance		34		KΩ	
INCAP	Input Capacitance		5	8	pF	Guaranteed by Characterization
INBW	Input Bandwidth		400		MHz	-1dB Small Signal
REFERENCE INPUT						
RLAD	Ladder Resistance	400	500	600	Ω	Guaranteed by Characterization
RLADTCO	Ladder Resistance Tempco		+0.8		Ω/°C	
VRTR	Top(+) Reference Range	3.0		AVDD	V	
VRBR	Bottom(-) Reference Range	AGND		2.0	V	
ΔVRR	(VRT-VRB) Reference Range	1.0		AVDD	V	
INTERNAL BANDGAP REFERENCE AND REFERENCE BUFFER						
VBGVR	Bandgap Output Voltage Range		1.240		V	
VBVR	Buffer Output Voltage Range			4.5	V	
VBGTC	Bandgap Reference Tempco	-120	+36	120	ppm/°C	
BGPSRR	Bandgap PSRR		+6		mV/V	
CONVERSION and TIMING CHARACTERISTICS (C_L = 15pF)						
MAXCON	Maximum Conversion Rate	40	60		MSPS	
MINCON	Minimum Conversion Rate		100		KSPS	
PDEL	Pipeline Delay(Latency)		12		CLK	Clock Cycles Digital Data Delay
t_{ad}	Aperture Delay Time		4		ns	
APJT	Aperture Jitter Time		12		ps	Peak-to Peak
t_r	Digital Output Rise Time		10		ns	
t_f	Digital Output Fall Time		10		ns	
t_{pd}	Output Data Propagation Delay		10	14	ns	Guaranteed by Characterization
t_{den}	Output Data Enable Delay		10	14	ns	Guaranteed by Characterization
t_{dis}	Output Data Disable Delay		9		ns	
CLKDC	Clock Duty Cycle	30	50	70	%	Guaranteed by Characterization

ELECTRICAL CHARACTERISTICS TABLE (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions/Comments
DYNAMIC PERFORMANCE						
SNR	Signal-to-Noise Ratio					Not Including Harmonics
	Fin = 1.0 MHz	55	58		dB	
	fin = 3.6 MHz	55	58		dB	
	fin = 12.5 MHz		57		dB	
THD	Harmonic Distortion					
	fin = 1.0 MHz	--63	-66		dB	
	fin = 3.6 MHz	--61	-63		dB	
	fin = 12.5 MHz		-60		dB	
SINAD	Signal-to Noise and Distortion					
	fin = 1.0 MHz	54	57		dB	
	fin = 3.6 MHz	54	57		dB	
	fin = 12.5 MHz		55		dB	
ENOB	Effective Number of Bits					
	fin = 1.0 MHz		9.2		Bit	
	fin = 3.6 MHz		9.1		Bit	
	fin = 12.5 MHz		8.9		Bit	
SFDR	Spurious Free Dynamic Range		73		dBFS	fin=1MHz
DIFFPH	Differential Phase		0.1		°	Degree
DIFFG	Differential Gain		0.5		%	Percent
DIGITAL INPUTS						
DVINH	Digital Input High Voltage	4.0			V	
DVINL	Digital Input Low Voltage			0.8	V	
DIINH	Digital Input High Current	-5	0.05	5	nA	
DIINL	Digital Input Low Current	-5	0.05	5	nA	
DINC	Digital Input Capacitance		5	8	pF	
DIGITAL OUTPUTS (C_L = 15 pF)						
DOHV	Digital Output High Voltage	4.5	4.7		V	I_{OH} = 1.5 mA
DOLV	Digital Output Low Voltage		0.3	0.5	V	I_{OL} = 1.5 mA
IOZ	High-Z Leakage	-10	0.1	10	nA	

ELECTRICAL CHARACTERISTICS TABLE (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
POWER SUPPLIES						
AV_{DD}	Analog Power Supply Voltage	4.5	5.0	5.5	V	
DV_{DD}	Digital Power Supply Range		AV_{DD}		V	$DV_{DD} = AV_{DD}$
AI_{DD}	Analog Power Supply Current		27	35	mA	
DI_{DD}	Digital Power Supply Current		10	13	mA	
DOI_{DD}	DOUT Power Supply Current		6	8	mA	
PD	Power Dissipation		215	280	mW	C_L=10pF, AV_{DD} = 5.0V

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +7.0V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5V
V_{IN} ..... V_{DD} +0.5 to GND –0.5V
All Inputs ..... V_{DD} +0.5 to GND –0.5V
All Outputs ..... V_{DD} +0.5 to GND –0.5V
Storage Temperature ..... –65 to +150°C

Package Power Dissipation Rating to 75°C
TQFP 1000mW
Derates above 75°C ..... 18mW/°C
SSOP 500mW
Derates above 75°C ..... 20mW/°C
Lead Temperature (Soldering 10 seconds) .. +300°C

Notes:

1 *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*

2 *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.*

3 *V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.*

TIMING DIAGRAMS

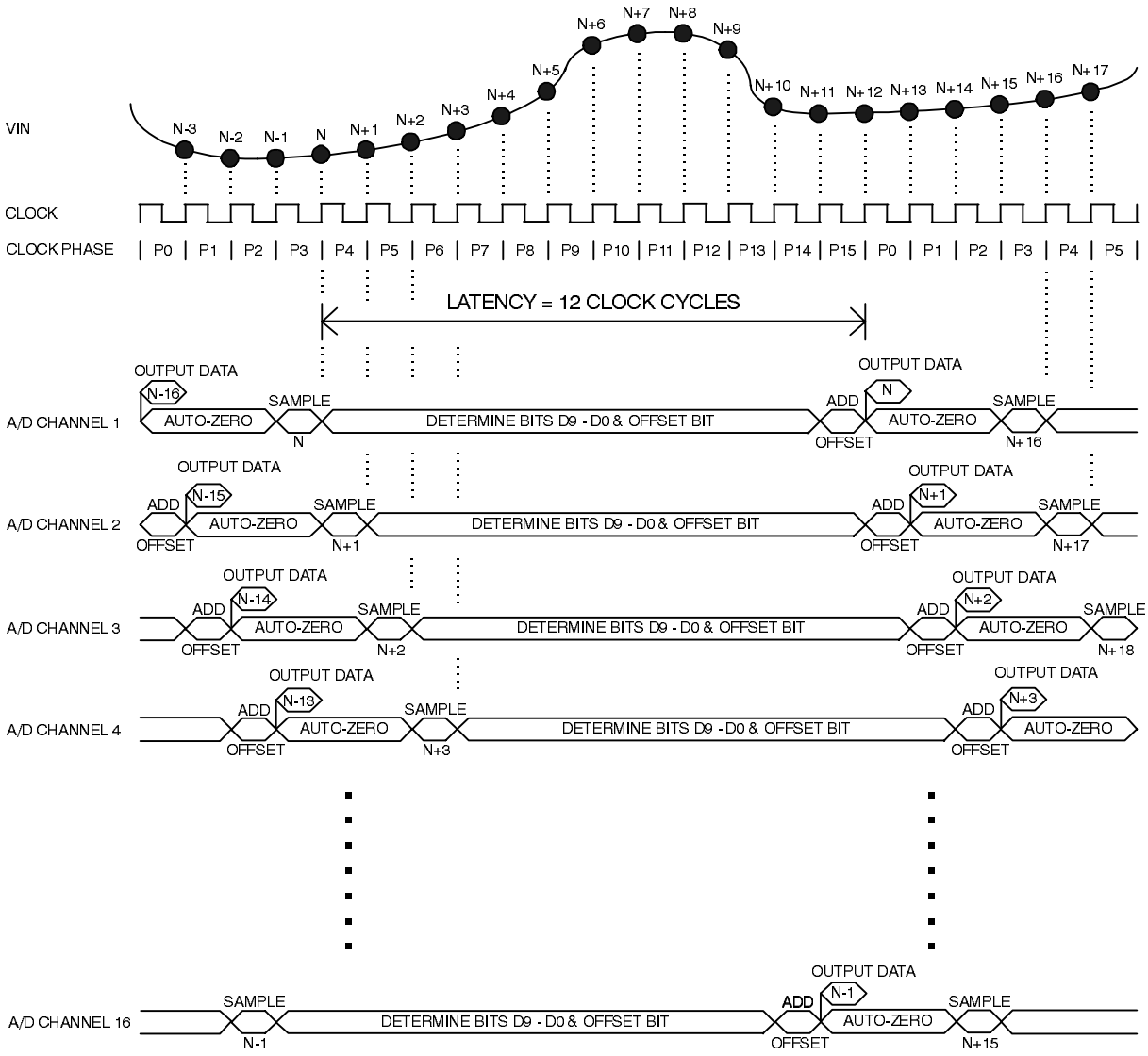


Figure 2. Timing Diagram

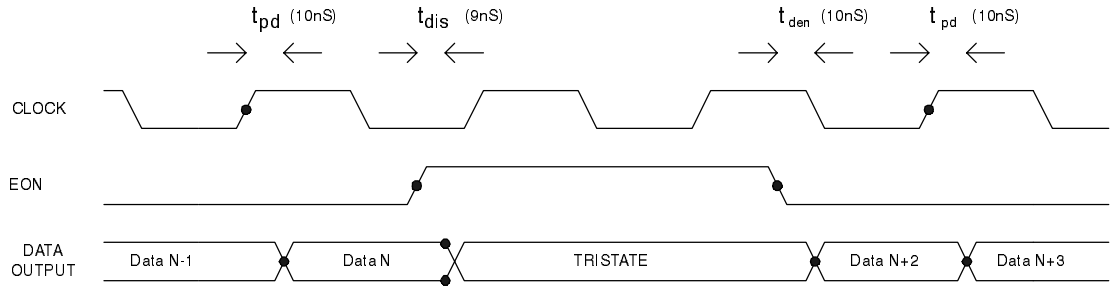


Figure 3. Clock-to-Output Data Relay

THEORY OF OPERATION

The XRD6440 is composed of 16 individual 10 bit successive approximation A/D converters operated in a time-interleaved fashion *(see Figure 1.)* A single resistor string with multiple taps generates reference voltages. This string is shared by all 16 converter channels, so any non-linearity (differential and integral) is common to all 16 channels.

Multiplexing of the 16 channels gives a 10 bit output every clock cycle, while changes in the input will take 13 clock edges to appear at the output (i.e. latency), much like a pipeline converter.

Each A/D channel is calibrated for offset and linearity just before it samples the input. In addition, the reference resistor string is continuously calibrated for linearity (differential and integral).

Successive Approximation A/D Conversion

N-bit successive approximation uses an N-bit digital-to-analog converter (DAC), a comparator, a sample-and-hold, and an N-bit successive approximation register (SAR) *(see Figure 4.)* After the input is sampled, the SAR sets all bits of the DAC to 0 except the MSB, which is set to 1 (output of the DAC is set to mid-scale). The comparator tells the SAR if the input is higher or lower than the DAC mid-scale. The MSB is set to 1 if the input is higher, 0 if it's lower. With the MSB set to it's new value, the SAR then sets the next most significant bit to 1. The comparator again tells the SAR if the input is higher or lower than the DAC output. The SAR sets the bit accordingly, and so on, until finally finishing with the LSB. Once the LSB has been determined, the conversion is finished and the next conversion may begin. A successive approximation converter needs one clock cycle for each bit, plus additional time to sample the input.

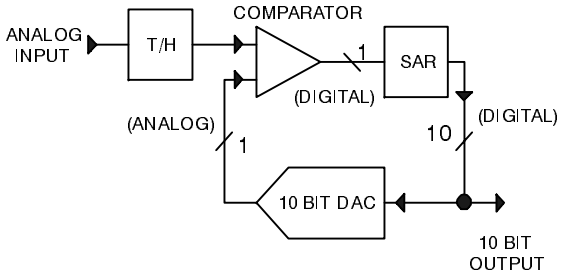


Figure 4. Successive Approximation (SAR) Architecture

Common DAC Shared by the 16 A/D Channels

For the XRD6440, each of the 16 A/D channels has its own S/H, comparator and SAR. The resistor string portion of the DAC, however, is shared by all 16 channels. The DAC analog switches are included in each channel, with all switches from all 16 channels going to the common resistor string. This gives the ability for each channel to access a different point on the resistor string simultaneously (refer to *Figure 5.* and *Figure 6.*).

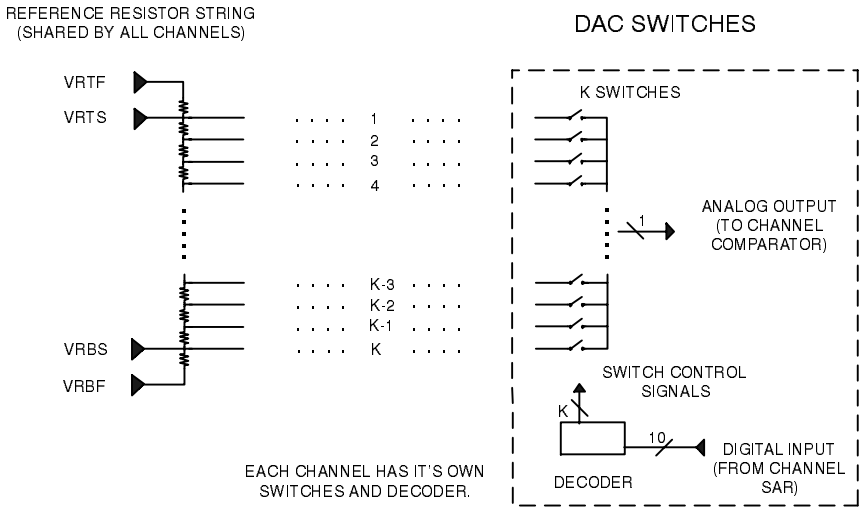


Figure 5. Simplified DAC Architecture

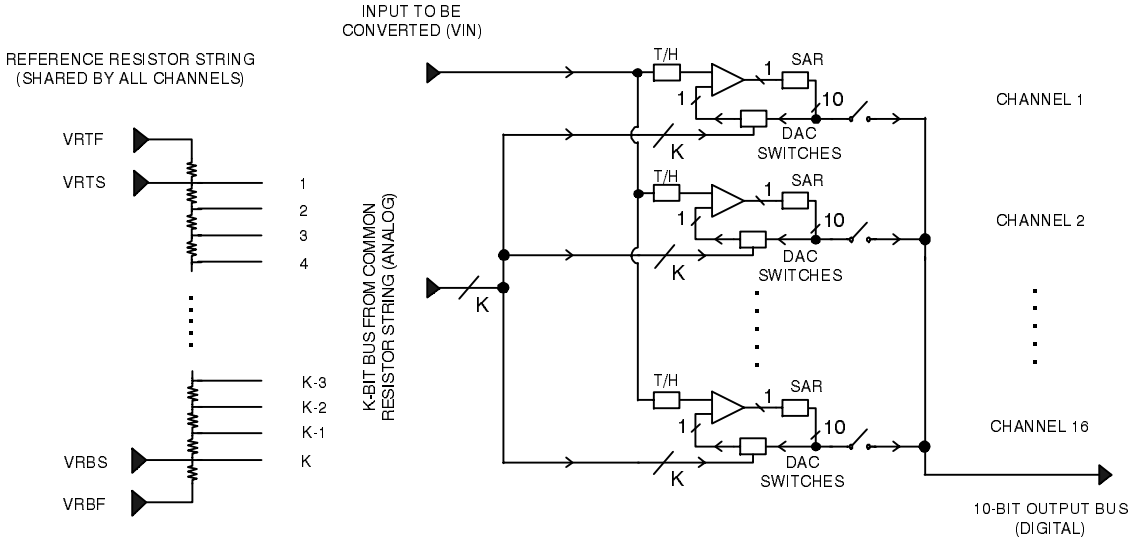


Figure 6. ADC Channel Multiplexing

Time-Interleaved Multiplexing of the A/D Converters

A 16 phase clock governs the chip timing. Each A/D channel is offset one clock phase from the previous A/D channel. For any given clock phase, one of the channels is sampling, and one of the channels is producing an output (refer to *Figure 2.*).

Digital Outputs

The circuits which supply the digital outputs (D0 - D9, and ORB) have their own supplies (DOVDD and DOGND). These supplies have no connection to the other supplies of the XRD6440, other than diode connections between DOGND and the other ground pins (AGND & DGND).

DOVDD can be at a lower voltage than AV_{DD} and DV_{DD}, allowing the A/D to send its data to a 3V system.

Output is normal binary. D9 is the MSB, and D0 is the LSB. Outputs change on the rising edge of the input clock *(see Figure 2. and Figure 3.)*

ORB is logic 1 if the input is out of range (i.e. too low or too high).

D0 - D9 and ORB outputs will become high impedance when OEN is high.

Automatic Calibration

Two types of continuous automatic calibrations are done - the reference resistor string itself and each of the A/D channels. Calibration removes both non-linearity in the reference resistor string (correcting differential and integral non-linearity) and individual offsets in each of the 16 A/D channels (such offsets would cause a repeating pattern of code variation as the channels are multiplexed). Calibration is done by storing correction voltages on internal storage capacitors. Only a small voltage change on each capacitor is possible each correction cycle, which ensures stable maintenance of the correction voltages. Initial calibration can take as long as 168,000 clock cycles.

Calibration will be maintained as long as the clock is running. If the clock is interrupted, leakage will eventually affect the trim voltages stored on the internal capacitors, and some or all of the initial calibration wait time will be required to restore proper trim.

Reference Resistor Ladder

The reference resistor ladder is continuously trimmed by looking at the 16 major segments of the common reference resistor ladder. The bottom segment is used as a standard, and the remaining 15 segments are tweaked to match the bottom segment. Calibration is done by means of voltage-controlled adjustable trim resistors in parallel with the 15 segments being trimmed (refer to Figure 7.)

Each round (phases 0 - 15) of clock phases adjusts one segment of the ladder. Since there are 15 segments to be trimmed, it takes 15 rounds to trim each of the 15 segments one time. There are 16 clocks in each round, so there are 240 clocks (=15x16) to trim the entire resistor ladder once. Since the permissible trim voltage changes are small, the user should allow for 168,000 clock cycles from the start-up to auto-calibrate the reference resistor ladder.

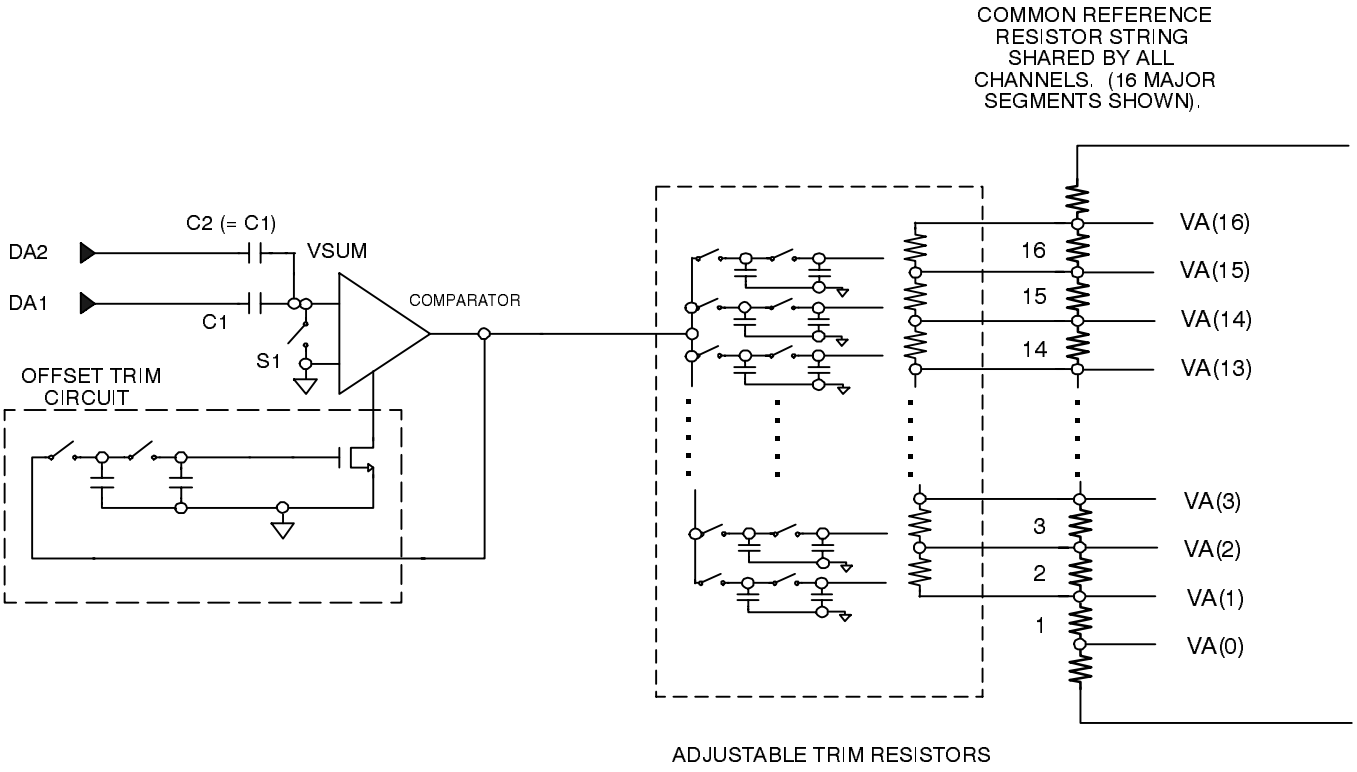


Figure 7. Simplified DAC Resistor Ladder Auto-Calibration Circuit

A/D Channels :

Each A/D channel comparator is trimmed for offset and sampling capacitor mismatch just before it samples the input using the circuitry shown in *Figure 8.* since the permissible trim voltage changes are small, initial calibration takes a rather long time. The comparator calibration is impacted by the resistor string which is being simultaneously calibrated, so theoretical determination of the required comparator initial calibration time is difficult. However, test results indicate that approximately 18,000 clock cycles are needed to begin producing recognizable outputs, and 42,000 clock cycles for more complete settling of the trim. After this time the reference resistor string is still undergoing initial trim, so integral non-linearities (INL) may still exist. This can create harmonics in the frequency domain and adversely impact SNR+distortion.

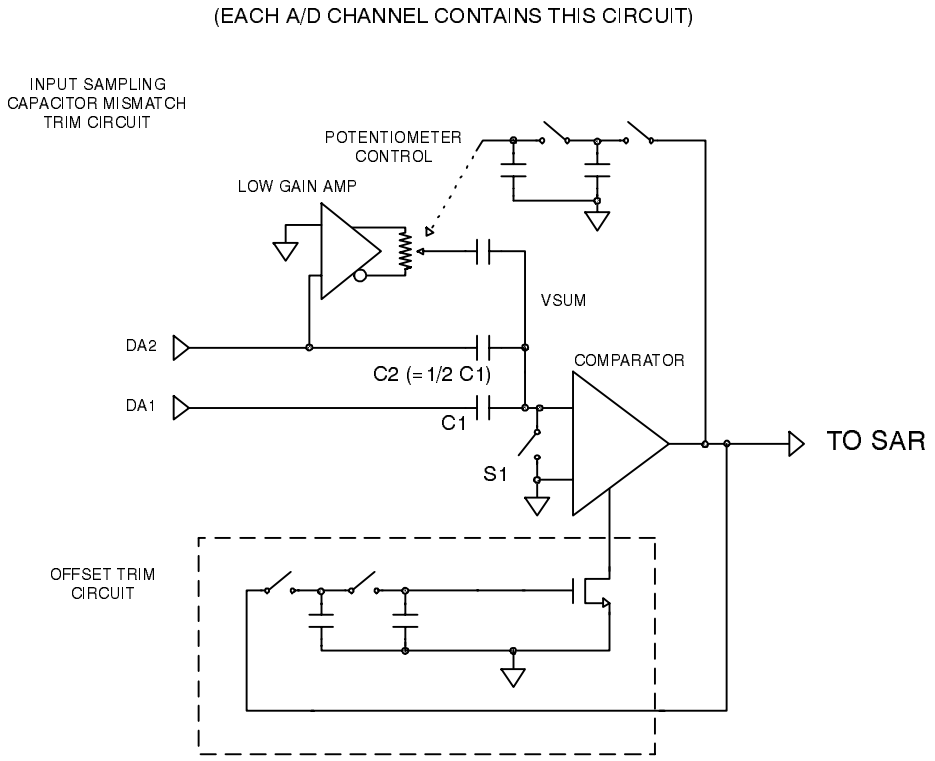


Figure 8. Simplified ADC Comparator Trimming Architecture

Input Sampling Circuit for the A/D Channels

Figure 9. shows a simplified version of the input sampling circuit in each A/D channel. When sampling, S1A and S1B are closed. S2A and S2B are connected to VIN and VINR, respectively. Sampling is completed when S1A and S1B open. When converting, S2B is connected to VRBS, and S2A is connected to the DAC, which is controlled by the SAR.

Normally, VRBF is set to ground, and VRTF is driven by the on-chip buffer. While the actual conversion from sampled input to digital output is done in a single-ended fashion, the input itself is sampled differentially - the difference between VIN and VINR is sampled. It is therefore theoretically possible to sample a differential signal, where both VIN and VINR are "active" (in that case VIN must be greater than VINR relative to ground, or an out of range condition will exist). However, best results are obtained if VINR is simply tied to VRBF (usually ground) or VRBS. This insures that the input common mode voltage of the A/D comparator will be proper (it's set during sampling through S1A and S1B).

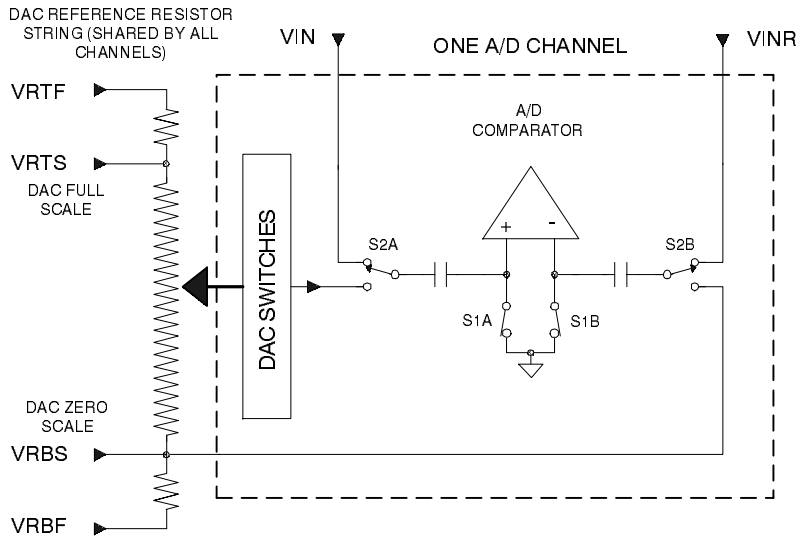


Figure 9. Simplified ADC Channel Input Sampling Circuit

If VINR is tied to ground, the XRD6440 will give an output of :

zero scale : all 0's when VIN = 0v

full scale : all 1's when VIN = (VRTS - VRBS)

If VINR is tied to VRBS, the XRD6440 will give an output of:

zero scale : all 0's when VIN = VRBS

full scale : all 1's when VIN = VRTS

Proper Setting of VRBF and VRTF Voltages

Proper setting of the voltages VRBF and VRTF is necessary to achieve full 10 bit dynamic range. VRTF can be set using either the internal voltage reference amplifier, or using an external buffer (*see Figure 10.* and *Figure 11.*) If using an external buffer, VRTS can be set more precisely by using VRTS as feedback to the external buffer. Likewise, VRBF can be forced with an external buffer, using VRBS as feedback. When not using the internal voltage reference amplifier, it must be disabled by connecting VFBR to V_{DD}. This will not cause a conflict between the internal amplifier and the external buffer - the internal amplifier's output will become high impedance when the voltage on VFBR is higher than on VBG.

VRTF

If VINR is tied to VRBS, VRTF should be set such that VRTS is equal to maximum VIN.

If VINR is tied to ground, VRTF should be set such that VRTS *minus VRBS* is equal to maximum VIN.

When using the internal amplifier, set VRTF to the desired value using the transfer function :

VRTF = VBG (1 + R2/R1) where VBG is nominally 1.24v

The values in *Figure 10.*, for example, would give VRTF = 3.968v = 1.24v x (1 + 11K/5K)

VRTS can be set more precisely by using an external buffer and known reference voltage VT (*see Figure 11.*)

VRBF

For minimum use of external components, VRBF can be tied to ground (*see Figure 10.*) However, if a more precise VRBS voltage is needed, or if the minimum expected voltage of VIN is not close to ground, then an external buffer and known reference voltage VB can be used (*see Figure 11.*) VINR can be tied to VRBS, and VRBS set with an external voltage source VB such that VRBS is at the expected minimum voltage of VIN.

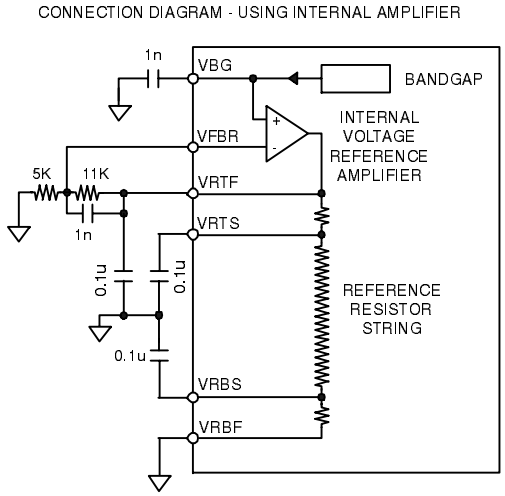


Figure 10. Circuit Diagram with Internal Amplifier

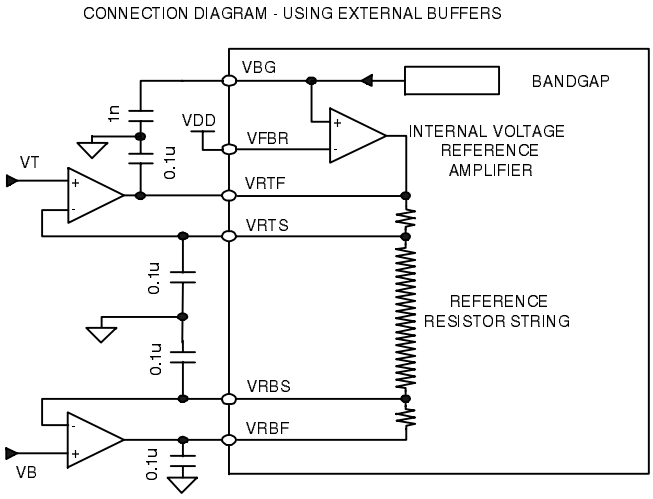


Figure 11. Circuit Diagram with External Amplifier

Typical values for VRTS and VRBS

VRBS - VRBF = 0.024 x (VRTF - VRBF) = 96mV if VRTF - VRBF = 4.0 volts

VRTF - VRTS = 0.014 x (VRTF - VRBF) = 56mV if VRTF - VRBF = 4.0 volts

External buffers must be capable of driving the 500 ohm reference resistor string. With 4 volts between VRTS and VRBS, the buffers must be able to sink and source 8 mA.

Board Layout Considerations

1) Sockets can degrade the A/D performance at these frequencies. Best results are obtained with the A/D soldered directly on the board.

2) Depending on the load seen by the output pins D0 - D9, it may be beneficial to latch the A/D output into digital latches placed fairly close to the A/D. D0 - D9 need only drive the inputs to the digital latches.

3) AGND and DGND pins for the A/D should be on the same ground plane. If digital output latches are used to buffer the A/D from load, they should be on a separate ground plane. Ground planes should be generous.

4) Place 0.1µF power supply filtering caps as close to the power supply pins on the XRD6440 as possible. The connection from the caps to the ground plane should also be as short as possible. The same holds true for the caps shown in *Figure 10.* and *Figure 11.*

5) Both the clock and VIN lines should be shielded if possible. VIN must be free of noise for good results. The clock line must be prevented from propagating noise elsewhere, but it must also be prevented from *picking up* noise, which could be seen by the A/D as clock jitter.

ANALOG INPUT

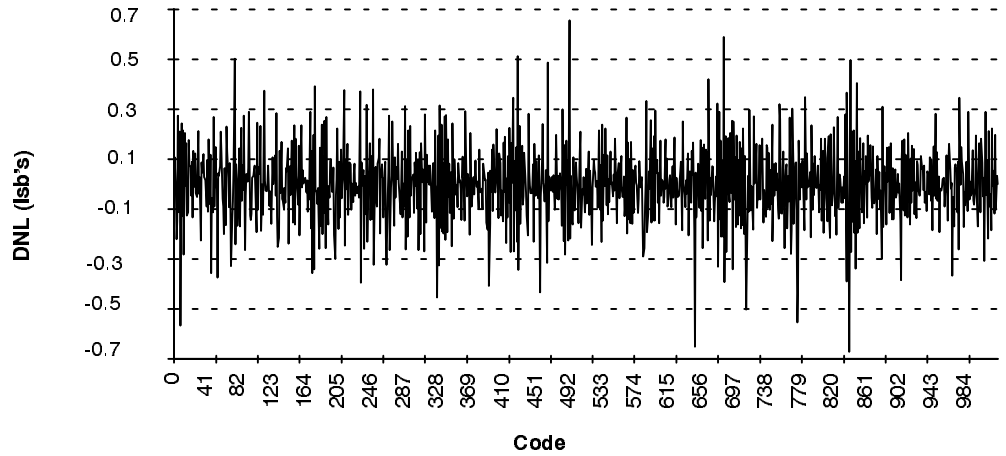
The operational range of the analog input, VIN, varies from VRT(+) to VRB(-) voltage references. Since these reference voltages set the full scale(all 1 code) and zero scale(all 0 code) of ADC, if VIN is driven above VRT(+) or bellow V_{RB}(-), output produces full scale or zero scale codes respectively.

The input drive requirements are minimal due to the low input capacitance (5pF-typ) and high input resistance (34 KΩ-typ) at this pin compared to the most other ADCs. This is made possible by the efficient design of sampling track-and-hold amplifiers(THAs) tied to this pin.

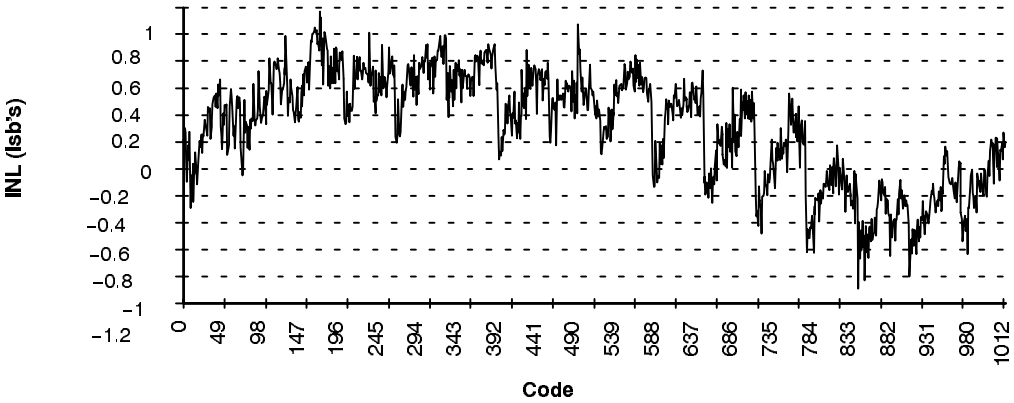
If this pin is to be driven above the analog power supply voltage(AV_{DD}), the input should be protected from a potential latch-up by using in series a 50Ω resistor and a clamping diode.

CALIBRATION CYCLE

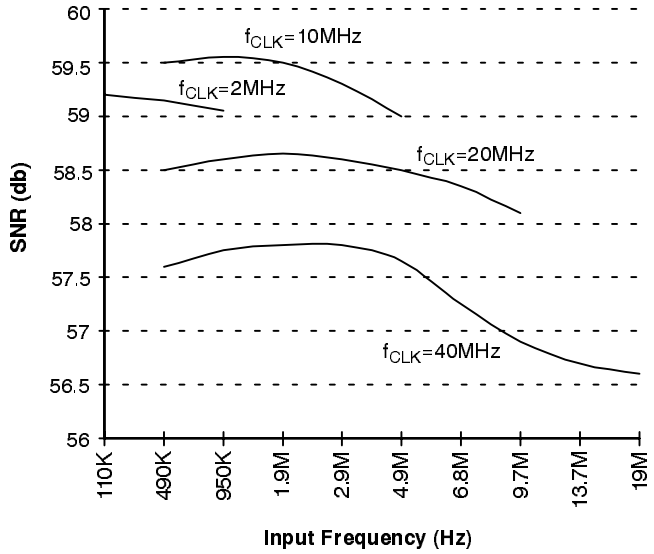
The XRD6440 incorporates a proprietary auto-calibration circuit which continuously adjusts the reference ladder, offset and gain of the sampling comparators. The auto-calibration algorithm is design to re-calibrate these errors by approximately 1/16 LSB per clock cycle to insure and maintain 10-bit accuracy over time and temperature changes.



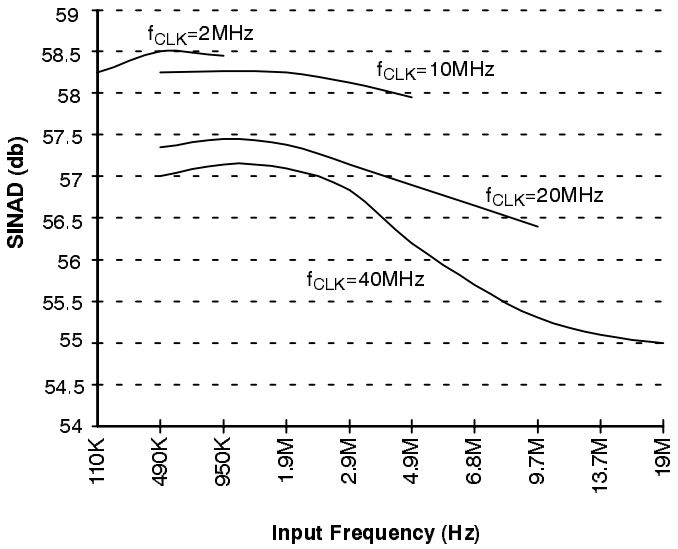
Graph 1. DNL
f_{SAMPLE} = 40MHz, f_{IN} = 490Khz



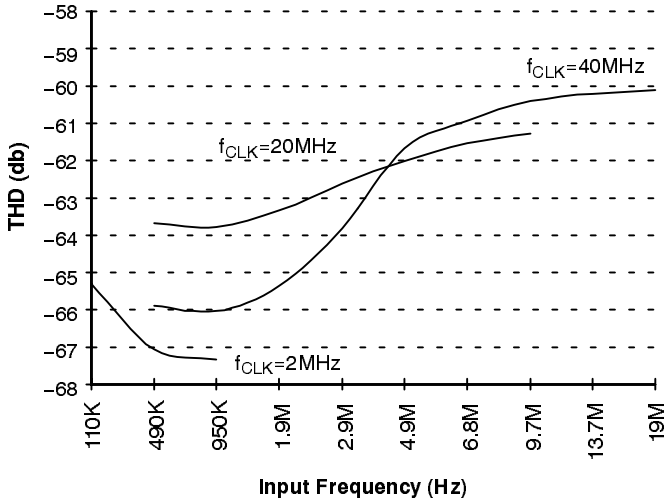
Graph 2. INL
f_{SAMPLE} = 40MHz, f_{IN} = 490Khz



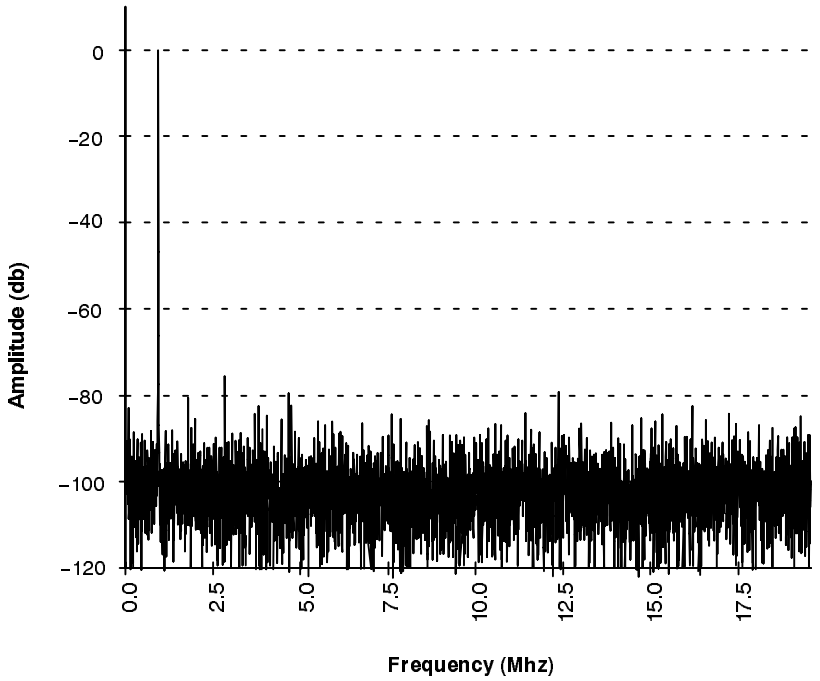
Graph 3.SNR vs. f_{IN}
f_{SAMPLE} = 2MHz, 10MHz, 20MHz, 40MHz



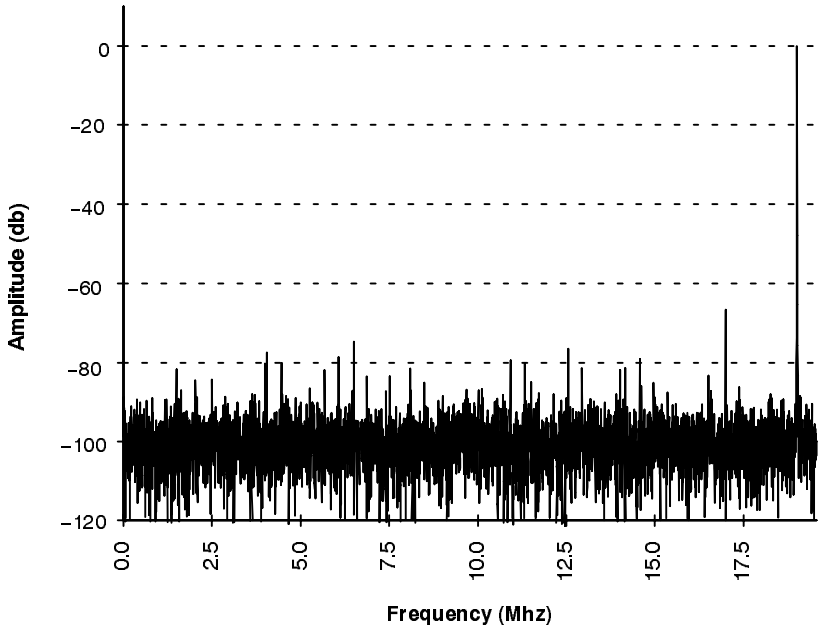
Graph 4.SINAD vs. f_{IN}
f_{SAMPLE} = 2MHz, 10MHz, 20MHz, 40MHz



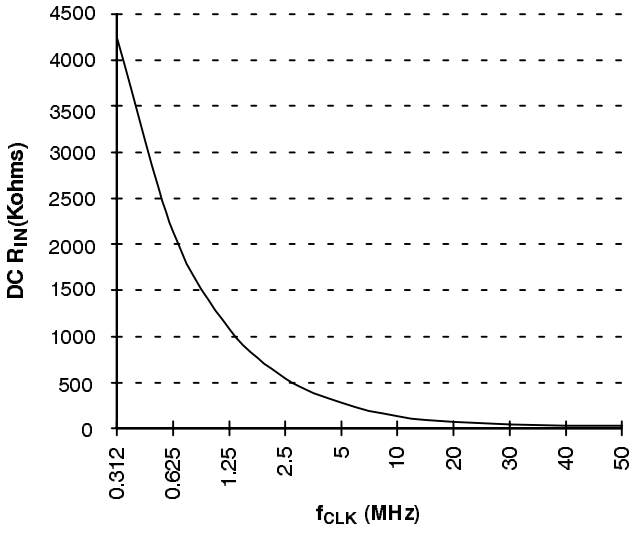
Graph 5.THD vs. f_{IN}
f_{SAMPLE} = 2MHz, 10MHz, 20MHz, 40MHz



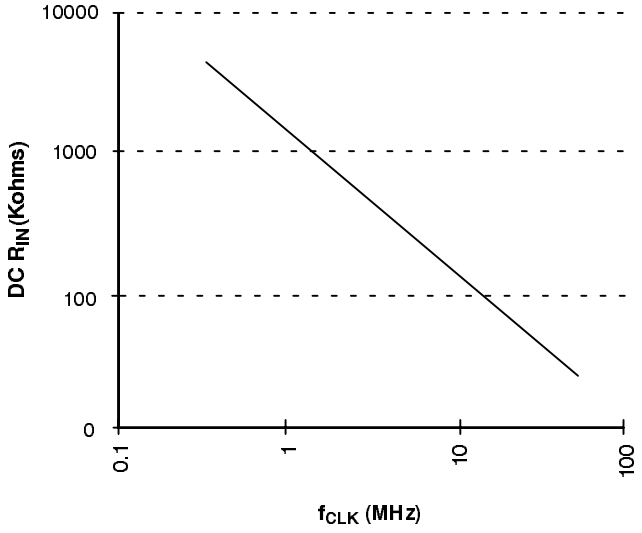
Graph 6.FFT
f_{SAMPLE} = 40MHz, f_{IN} = 950Khz



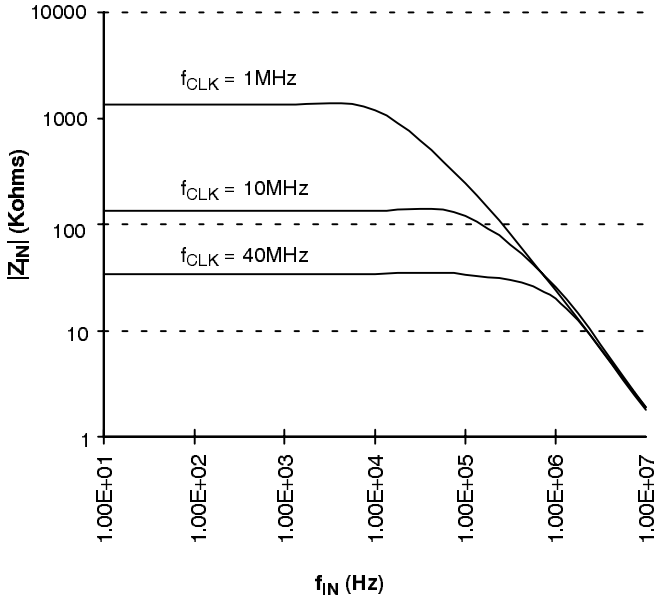
Graph 7.FFT
f_{SAMPLE} = 40MHz, f_{IN} = 19MHz



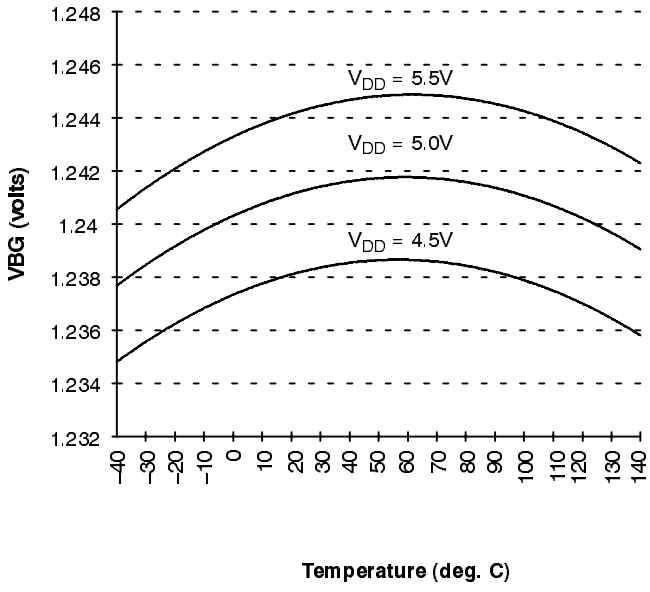
Graph 8.DC R_{IN} vs. f_{CLK}



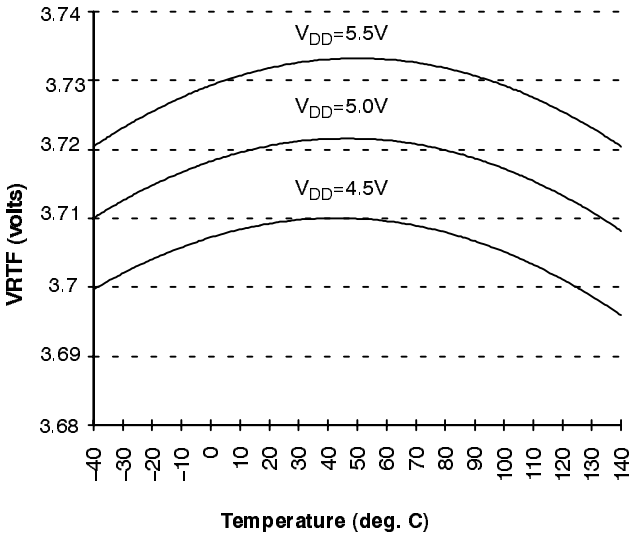
Graph 9.DC R_{IN} vs. f_{CLK}
Log - Log Scale



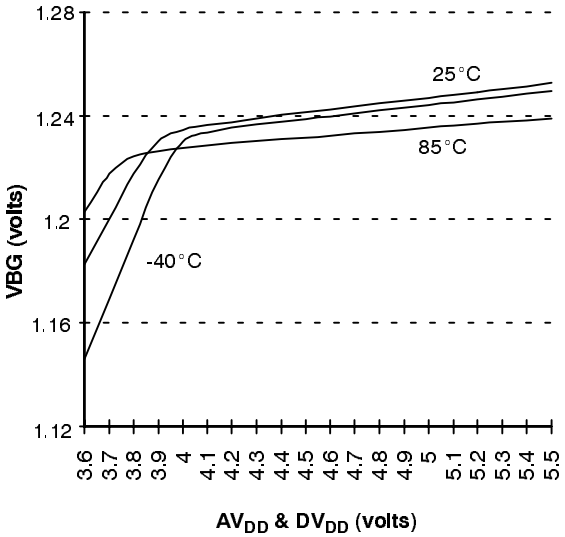
Graph 10.$|Z_{IN}|$ vs. f_{IN}
Log - Log Scale



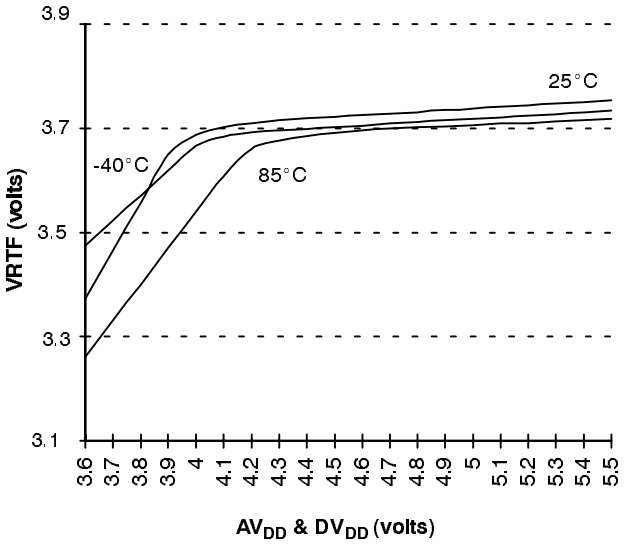
Graph 11.VBG vs. TEMP
V_{DD} = 4.5V, 5.5V



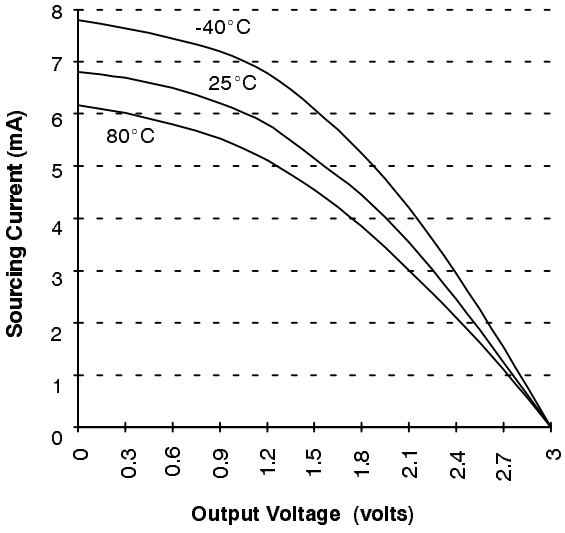
Graph 12.VRTF vs. TEMP
V_{DD} = 4.5V, 5.5V



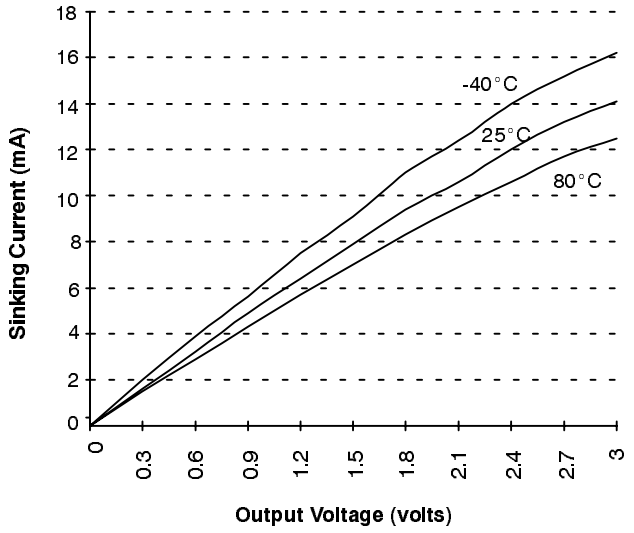
Graph 13.VBG vs. AV_{DD} (=DV_{DD})



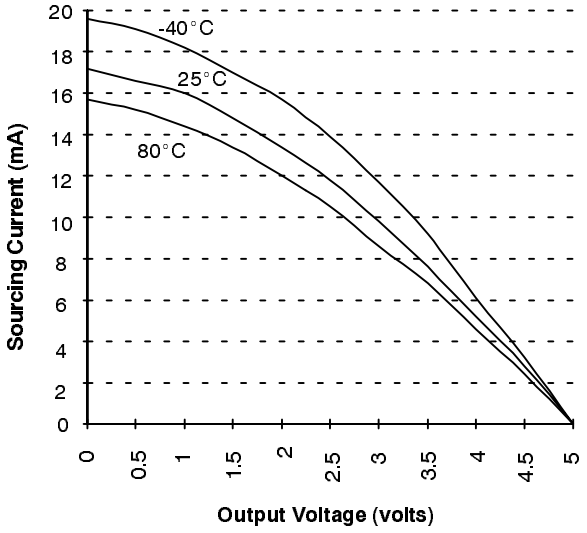
Graph 14.VTRF vs. AV_{DD} (=DV_{DD})
VRTF Set for 3.7V Using External 10K/5K



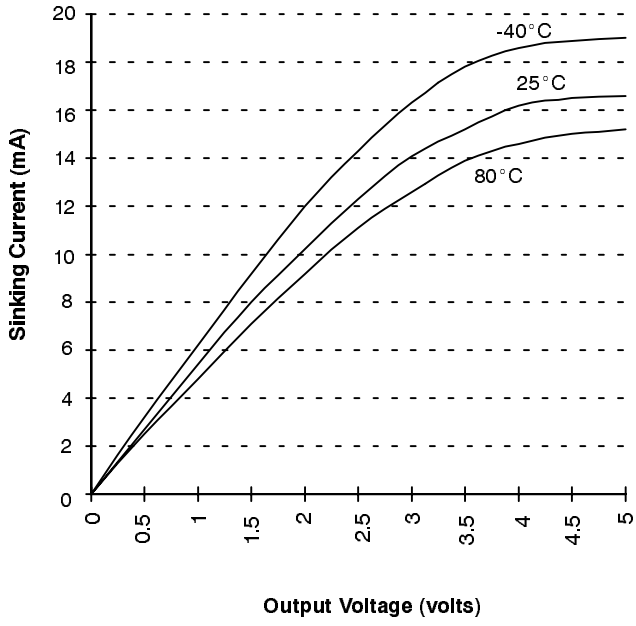
Graph 15.Digital Output Source Current
DOV_{DD} = 3.0V



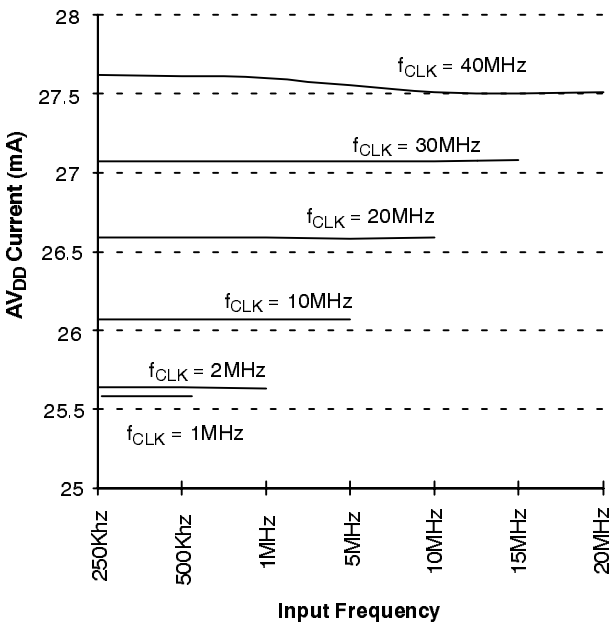
Graph 16.Digital Output Sink Current
DOV_{DD} = 3.0V



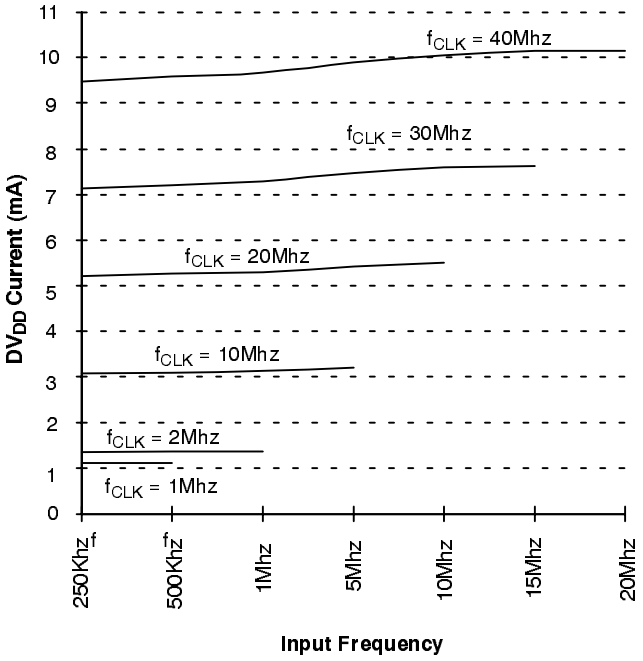
Graph 17.Digital Output Source Current
DOV_{DD} = 5.0V



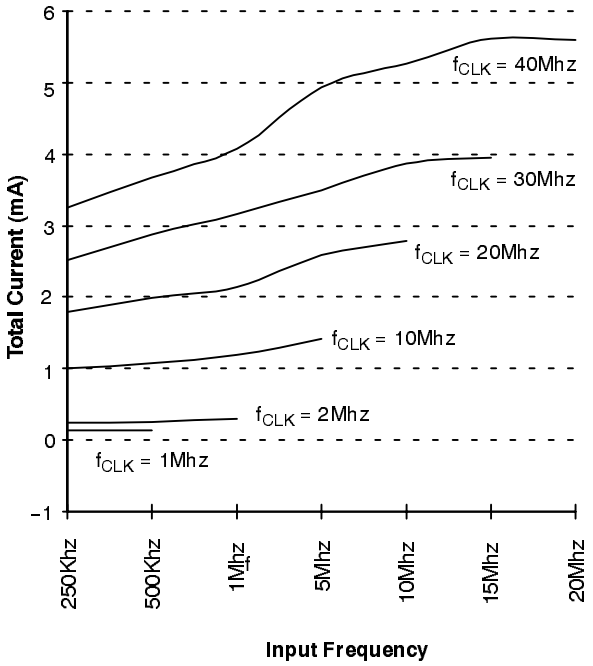
Graph 18.Digital Output Sink Current
DOV_{DD} = 5.0V



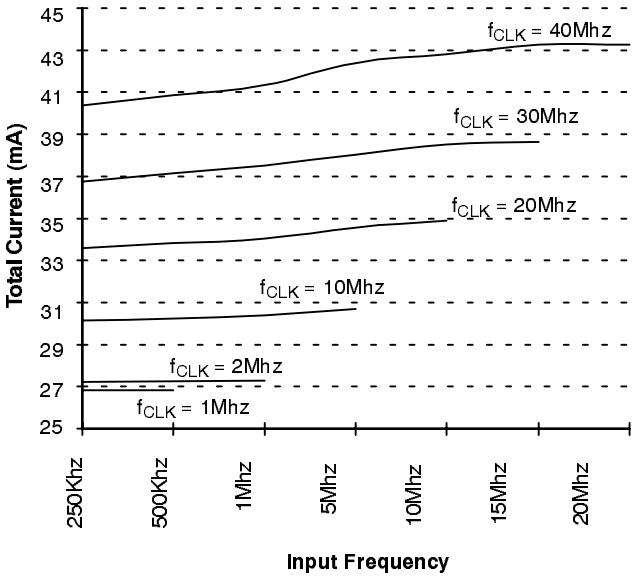
Graph 19.I(AV_{DD}) vs. f_{IN}
f_{IN} = 1, 2, 10, 20, 30, 40MHz



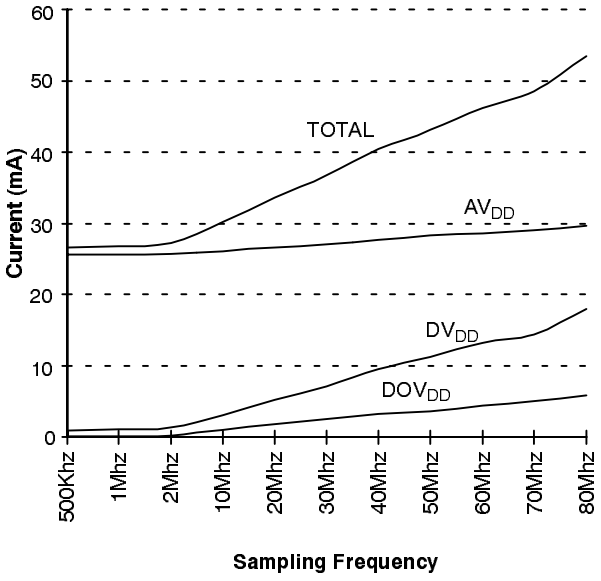
Graph 20.I(DV_{DD}) vs. f_{IN}
f_{IN} = 1, 2, 10, 20, 30, 40MHz



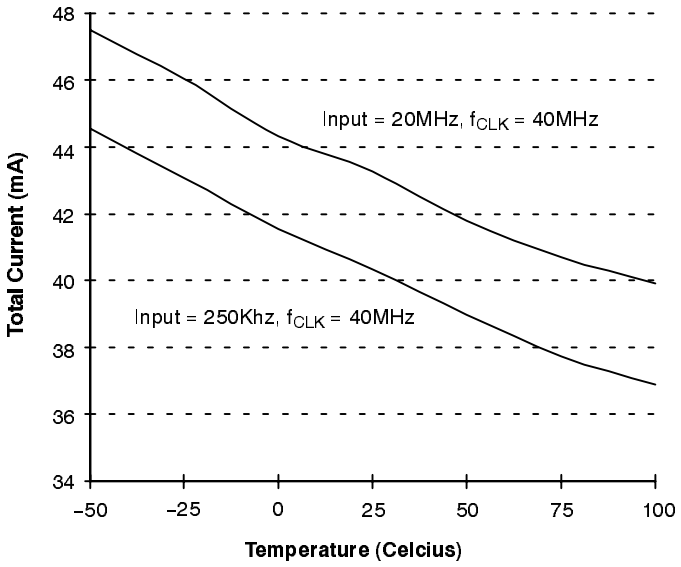
Graph 21.I(DOV_{DD}) vs. f_{IN}
f_{SAMPLE} = 1, 2, 10, 20, 30, 40MHz



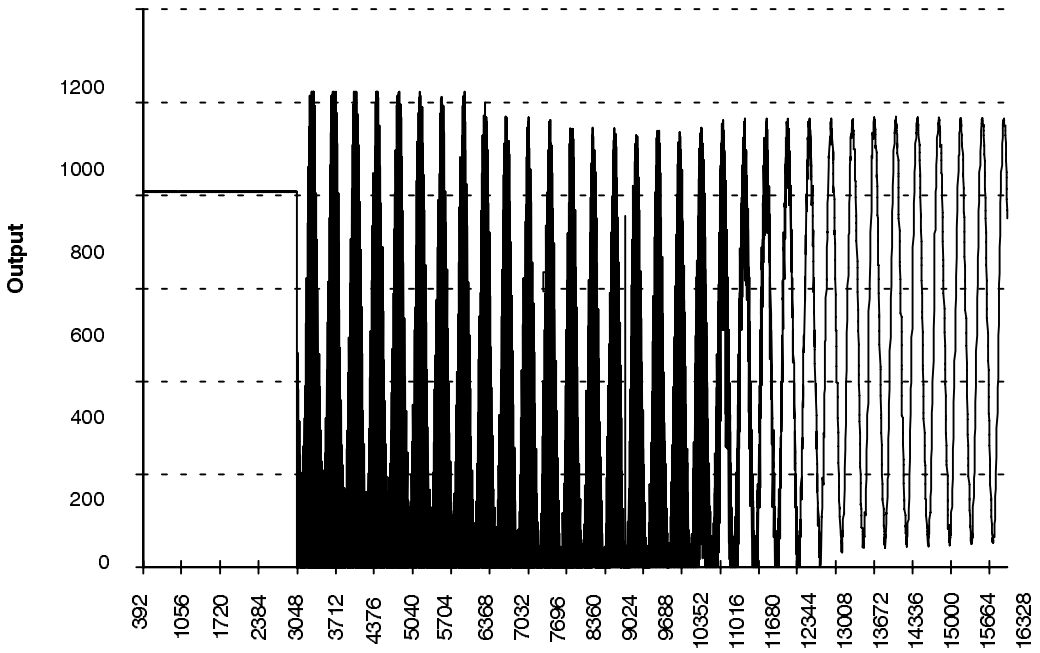
Graph 22.I(TOTAL) vs. f_{IN}
f_{SAMPLE} = 1, 2, 10, 20, 30, 40MHz



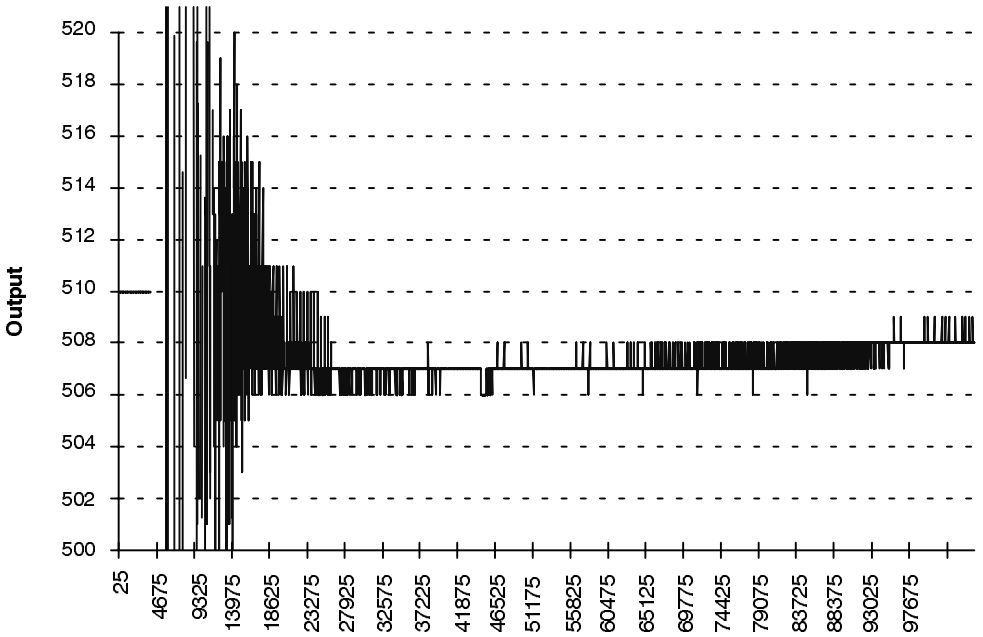
Graph 23.CURRENT vs. f_{SAMPLE}
f_{IN} = 250Khz



Graph 24.I(TOTAL) vs. Temperature
f_{IN} = 250Khz, 20MHz, f_{SAMPLE} = 40MHz



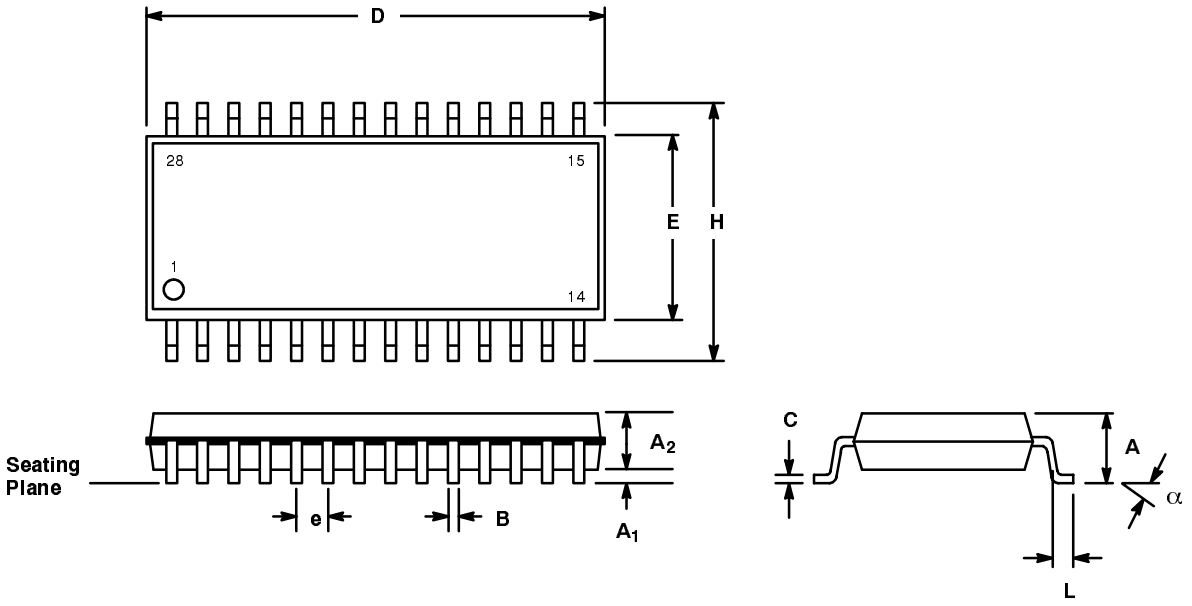
Graph 25.A/D During Initial Start-up
f_{SAMPLE} = 40MHz, f_{IN} = 100Khz Sine Wave



Graph 26.A/D During Initial Start-up
f_{SAMPLE} = 40MHz, f_{IN} = DC

28 LEAD SHRINK SMALL OUTLINE PACKAGE (5.3 mm SSOP)

Rev. 1.00

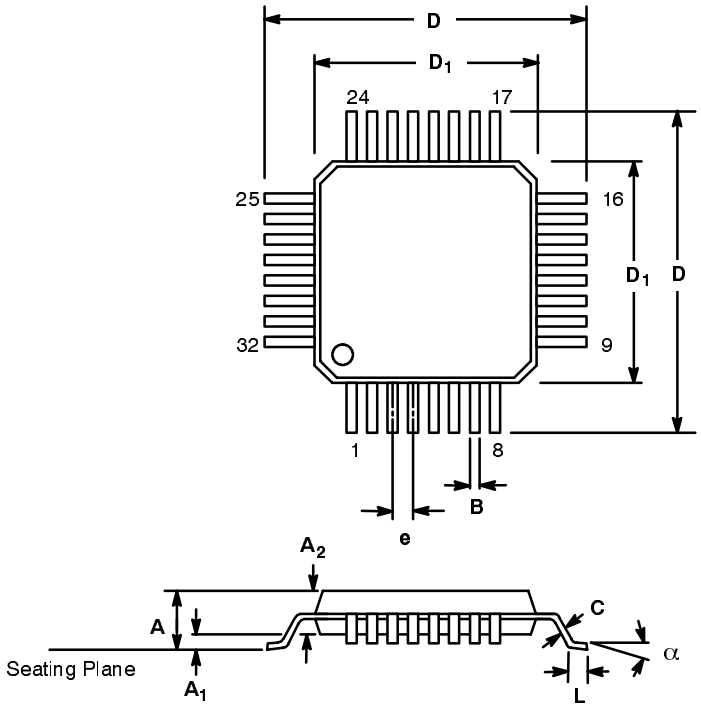


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.066	0.084	1.67	2.13
A_1	0.002	0.010	0.05	0.25
A_2	0.064	0.074	1.62	1.88
B	0.009	0.015	0.22	0.38
C	0.004	0.008	0.09	0.20
D	0.390	0.414	9.90	10.50
E	0.197	0.221	5.00	5.60
e	0.0256 BSC		0.65 BSC	
H	0.292	0.323	7.40	8.20
L	0.025	0.041	0.63	1.03
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

32 LEAD THIN QUAD FLAT PACK
(7 x 7 x 1.4 mm TQFP)

Rev. 2.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.012	0.018	0.30	0.45
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.0315 BSC		0.80 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

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Datasheet January 1999