YSS205B

KP
Karaoke Processor

■ OUTLINE

The YSS205B is an LSI to carry out audio signal processing needed for "karaoke" systems through digital processing. With one or two 256k pseudo-SRAM connected, this LSI executes signal processing such as Key Control, Digital Echo and Voice Cancel. As it has built-in A/D and D/A converters, it can handle input and output of analog audio signals in addition to digital audio signals. Also, the Digital Surround function integrated in it enables to enjoy all types of video and music software by using the same hardware.

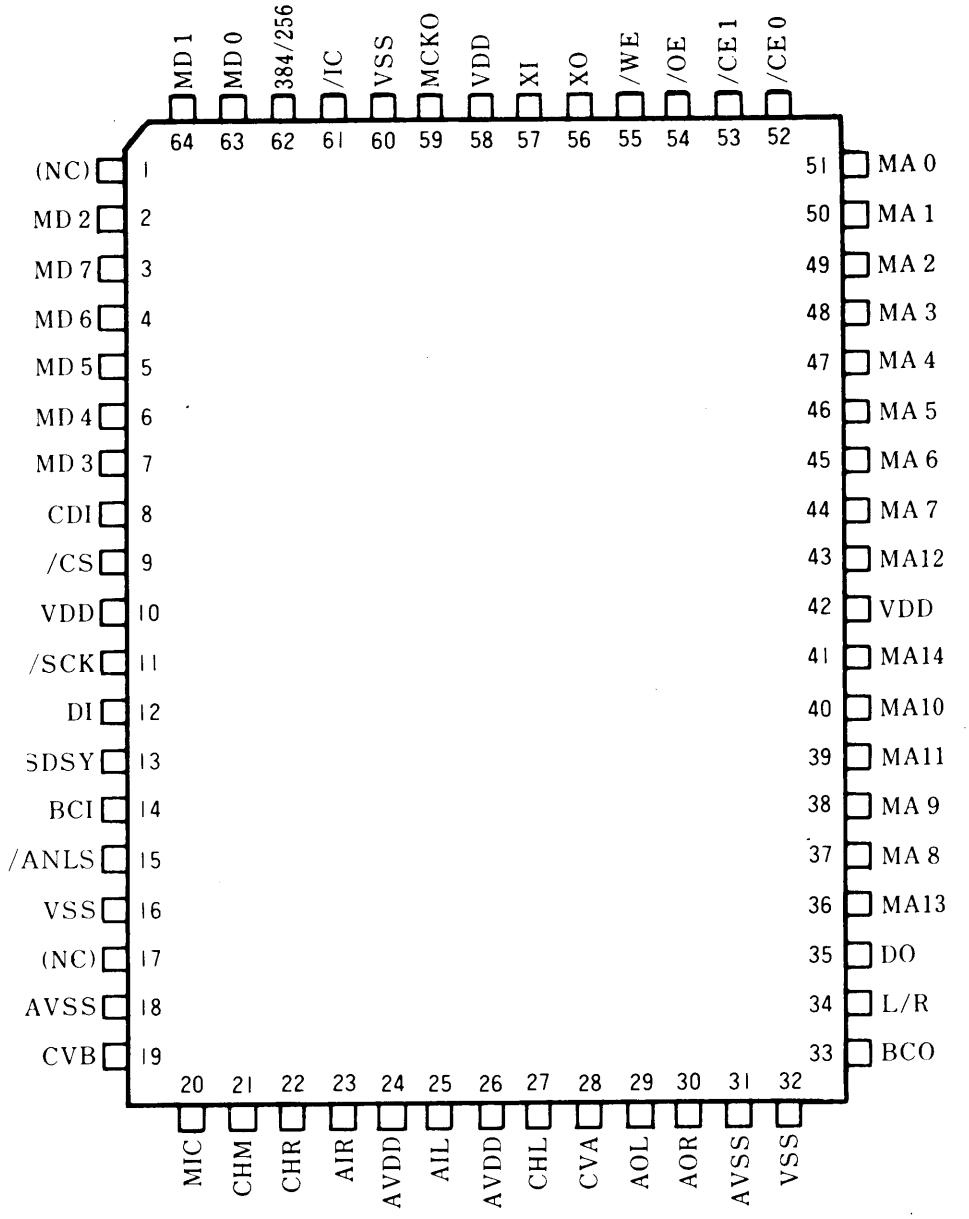
■ FEATURES

- 3 channels of 15-bit floating A/D converter and 2 channels of 15-bit floating D/A converter are integrated to handle audio signals from L and R channels and from the microphone.
- It is possible to input digital signals directly from CD or LD signal processing LSI's such and to output digital signals to the oversampling digital filter and the D/A converter.
- By using YM7110 interface, LD analog signals can be also digital processed.
- 5 operating modes to cope with necessary processing operations.
- Up to 370ms digital data can be stored (when one pseudo RAM at fs=44.1kHz is connected) and they are divided so that they are used for Key Control, Echo and Surround.
- Key Control function with a maximum variable range of ±1 octave
- High-quality digital Echo function by convoluting multiple taps
- Use of microprocessor serial interface for setting various parameters
- Up to two 256K(8 bit × 32k) pseudo-SRAM can be connected for external memory
- Either 384fs or 256fs can be selected for the master clock.
- +5V single power supply, silicon-gate CMOS process
- 64-pin plastic QFP(YSS205B-F)

YAMAHA CORPORATION

YSS222 CATALOG
CATALOG No. : LSI-4SS205B2
1996. 5

■ PIN CONFIGURATION



64QFP TOP VIEW

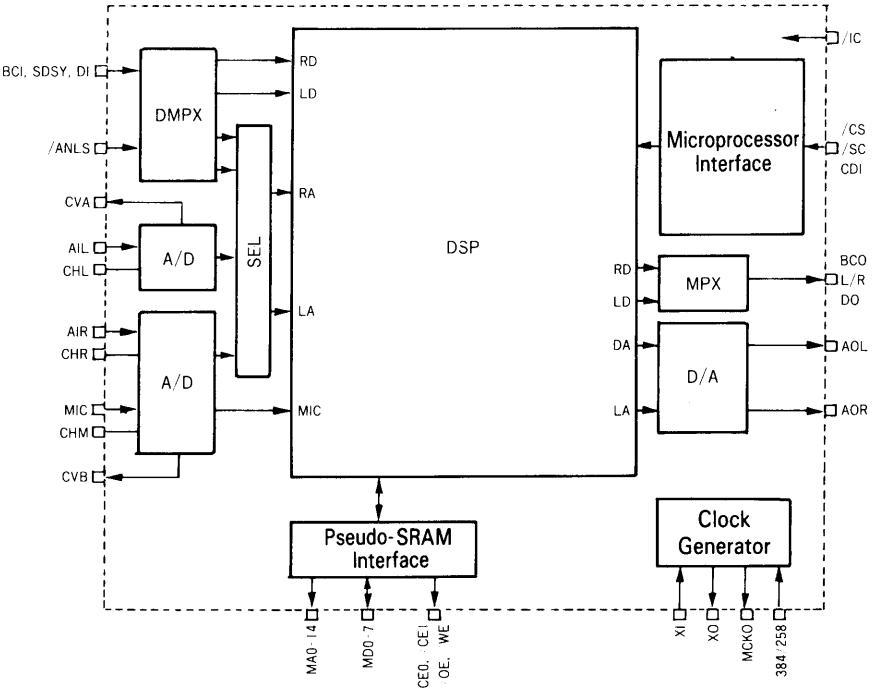
■ PIN DESCRIPTION

No.	Name	I/O	Function
1	(NC)		(Do not connect externally.)
2	MD2	I/O	External pseudo-SRAM interface data terminal
3	MD7	I/O	External pseudo-SRAM interface data terminal
4	MD6	I/O	External pseudo-SRAM interface data terminal
5	MD5	I/O	External pseudo-SRAM interface data terminal
6	MD4	I/O	External pseudo-SRAM interface data terminal
7	MD3	I/O	External pseudo-SRAM interface data terminal
8	CDI	I	Microprocessor interface serial data
9	/CS	I	Microprocessor interface chip select
10	VDD	—	+5V power supply (for digital block)
11	/SCK	I	Microprocessor interface serial clock
12	DI	I+	Digital audio signal input serial data
13	SDSY	I+	Digital audio signal input L/R clock
14	BCI	I+	Digital audio signal input bit clock
15	/ANLS	I+	YM7110 interface serial data
16	VSS	—	Ground (for digital block)
17	(NC)		(Do not connect externally.)
18	AVSS	A—	Ground (for A/D, D/A converters, Connect with VSS externally.)
19	CVB	A—	ADC center voltage for R and MIC channels
20	MIC	AI	Analog audio signal MIC channel ADC input
21	CHM	A—	Connecting terminal for MIC input sample/hold capacitor
22	CHR	A—	Connecting terminal for AIR input sample/hold capacitor
23	AIR	AI	Analog audio siganl R channel ADC input
24	AVDD	A—	+5V power supply (for A/D, D/A converters, Connect with VDD externally.)
25	AIL	AI	Analog audio signal L channel ADC input
26	AVDD	A—	+5V power supply (for A/D, D/A converters, Connect with VDD externally.)
27	CHL	A—	Connecting terminal for AIL input sample/hold capacitor
28	CVA	A—	ADC center voltage for L channel
29	AOL	AO	Analog audio signal L channel DAC output
30	AOR	AO	Analog audio signal R channel DAC output
31	AVSS	A—	Ground (for A/D, C/A converters, Connect with VSS externally.)
32	VSS	—	Ground (for digital block)
33	BCO	O	Digital audio signal output bit clock
34	L/R	O	Digital audio signal output L/R clock
35	DO	O	Digital audio signal output serial data
36	MA13	O	External pseudo-SRAM interface address terminal
37	MA8	O	External pseudo-SRAM interface address terminal
38	MA9	O	External pseudo-SRAM interface address terminal
39	MA11	O	External pseudo-SRAM interface address terminal
40	MA10	O	External pseudo-SRAM interface address terminal

No.	Name	I/O	Function
41	MA14	O	External pseudo-SRAM interface address terminal
42	VDD	—	GND (for digital block)
43	MA12	O	External pseudo-SRAM interface address terminal
44	MA7	O	External pseudo-SRAM interface address terminal
45	MA6	O	External pseudo-SRAM interface address terminal
46	MA5	O	External pseudo-SRAM interface address terminal
47	MA4	O	External pseudo-SRAM interface address terminal
48	MA3	O	External pseudo-SRAM interface address terminal
49	MA2	O	External pseudo-SRAM interface address terminal
50	MA1	O	External pseudo-SRAM interface address terminal
51	MA0	O	External pseudo-SRAM interface address terminal
52	/CE0	O	External pseudo-SRAM interface chip select #0
53	/CE1	O	External pseudo-SRAM interface chip select #1 (available when connecting two pseudo-SRAM)
54	/OE	O	External pseudo-SRAM interface OE terminal
55	/WE	O	External pseudo-SRAM interface WE terminal
56	XO	O	Connecting terminal for crystal oscillator
57	XI	I	Connecting terminal for crystal oscillator or external clock input terminal
58	VDD	—	+5V power supply (for digital block)
59	MCKO	O	Master clock (XI clock) output
60	VSS	—	Ground (for digital block)
61	/IC	I	Initial clear terminal
62	384/256	I+	Master clock rate switching ('H' = 384fs, 'L' = 256fs)
63	MD0	I/O	External pseudo-SRAM interface data terminal
64	MD1	I/O	External pseudo-SRAM interface data terminal

Note) +: Pulled-up terminal, A : Analog terminal

■ BLOCK DIAGRAM



■ FUNCTION DESCRIPTION

1. Clocks XI, XO, 384/256, MCKO

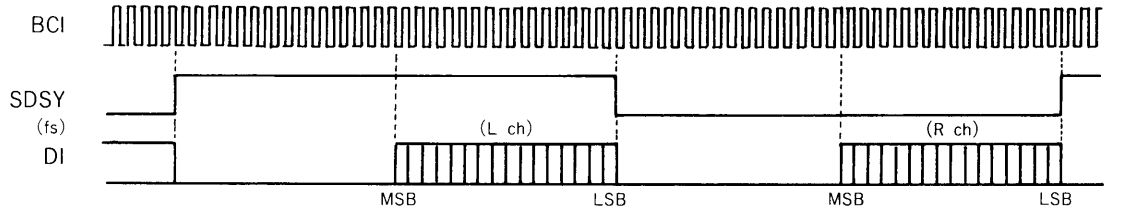
The crystal oscillator circuit is constructed with XI and XO terminals used.
The oscillation frequency should be 384fs when 384/256 terminal is at 'H' and 256fs when at 'L'.
The master clock is output through MCKO terminal.

2. ADCs, DACs AIL, AIR, MIC, CHL, CHR, CHM, CVA, CVB, AOL, AOR

Signals from L, R and MIC channels are input to AIL, AIR and MIC terminals respectively. Connect sample hold capacitors to CHL, CHR and CHM terminals. CVA and CVB are center voltage terminals; the former for R channel and the latter for L channel and MIC. Connect a stabilizing capacitor externally and bias inputs through AIL, AIR and MIC by using this voltage.
DAC outputs are voltage output from AOL and AOR terminals. Connect sample/hold capacitors and execute buffering by using operation amplifiers with high impedance input.

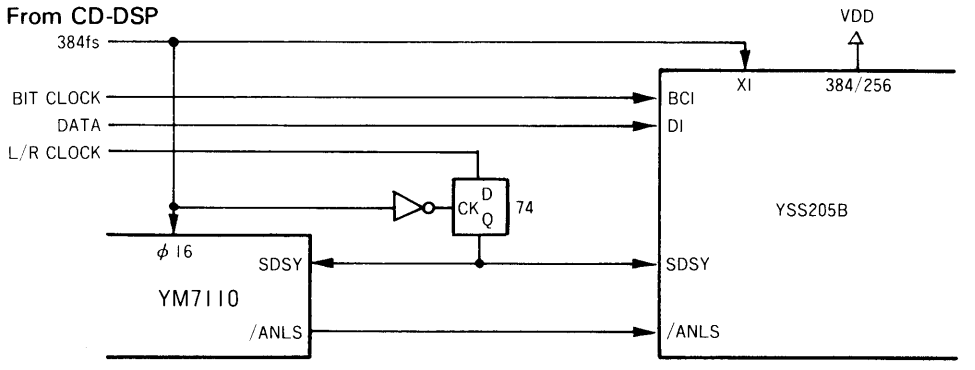
3. Digital inputs BCI, SDSY, DI, /ANLS

Digital signals are input through BCI, SDSY and DI terminals in the following format.



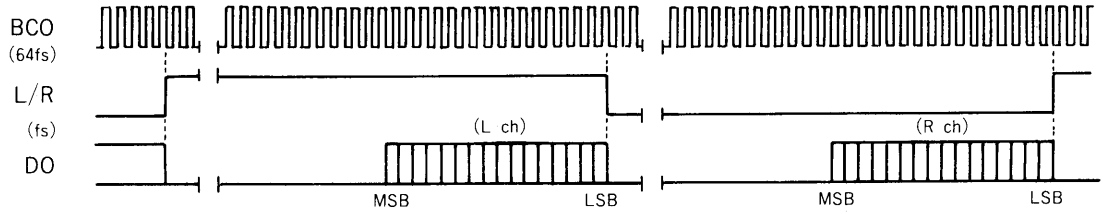
BCI, SDSI and DI must be synchronized with the master clock. BCI can be at any rate between 32fs and 96fs per cycle.
The signal input through SDSY must be of fs cycle. Note that if this cycle is disturbed even momentarily, the internal set data may be damaged.
When not using the digital audio data input, that is, when nothing is input through BCI and SDSY, set bit3 of OPR register to '1'.

Also, it is possible to input the digital data from YM7110 instead of analog L and R signals. Make connections as shown below and use the same master clock and fs clock.



4. Digital outputs BCO, L/R, DO

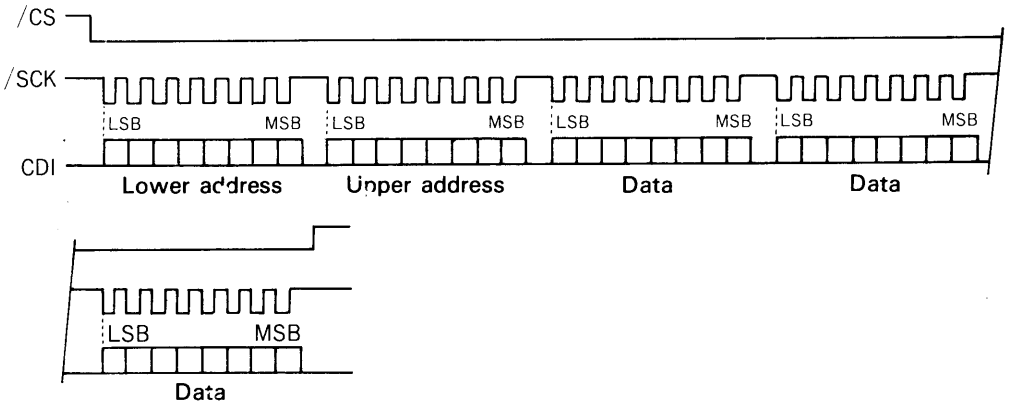
The digital audio signals are output from BCO, L/R and DO terminals in the following format.



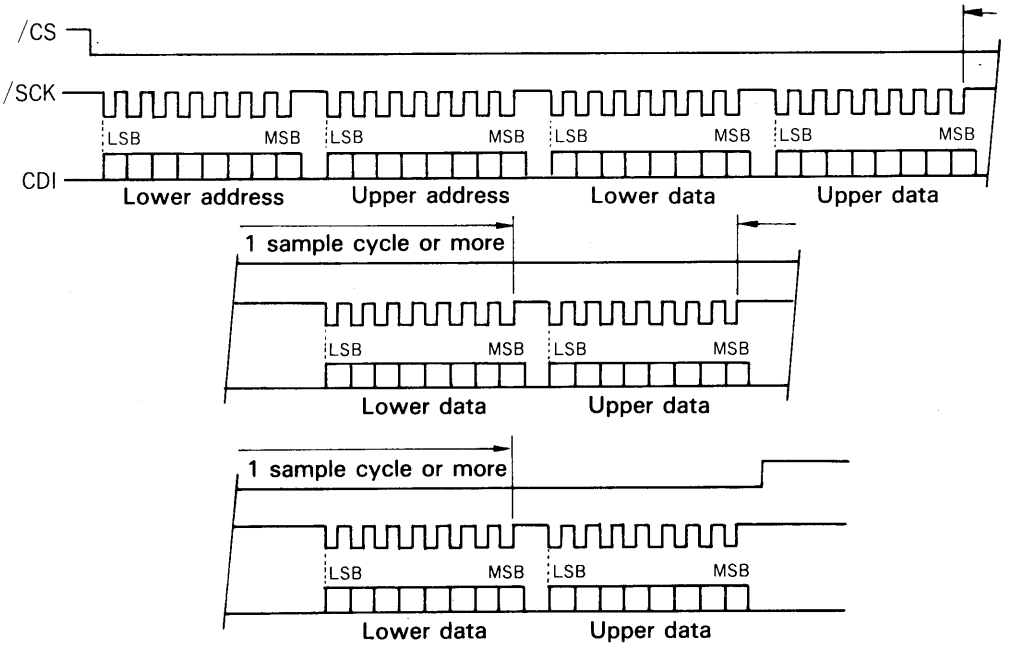
5. Microprocessor interface /CS, /SCK, CDI

Functions of this LSI are spedified by setting the data to the internal registers through the serial inteface.

a. For addresses 0000H to 0005H



b. For addresses 0040H and up



To the addresses specified by the 1st and 2nd bytes after /CS has become 'L', the data for the 3rd or later byte is written. At every 1-byte transmission, the address to which the data is written is increased, only the data can be transmitted continuously to continuous addresses. When transmitting the data of 0040H or higher address, set the lower byte LSB of the address to '0' (that is, the address is always even number). When sending the data continuously following transmission of the upper data, be sure to obtain 1 or more sampling cycle as an interval before completing lower data transmission.

6. **Pseudo-SRAM interface** **MA0-AM14, MD0-7, /CE0, /CE1, /WE, /OE**

Up to two 256k(8bit × 32k word) pseudo-static RAM's can be connected to this LSI. When connecting only one, use /CEO as a chip enable signal.

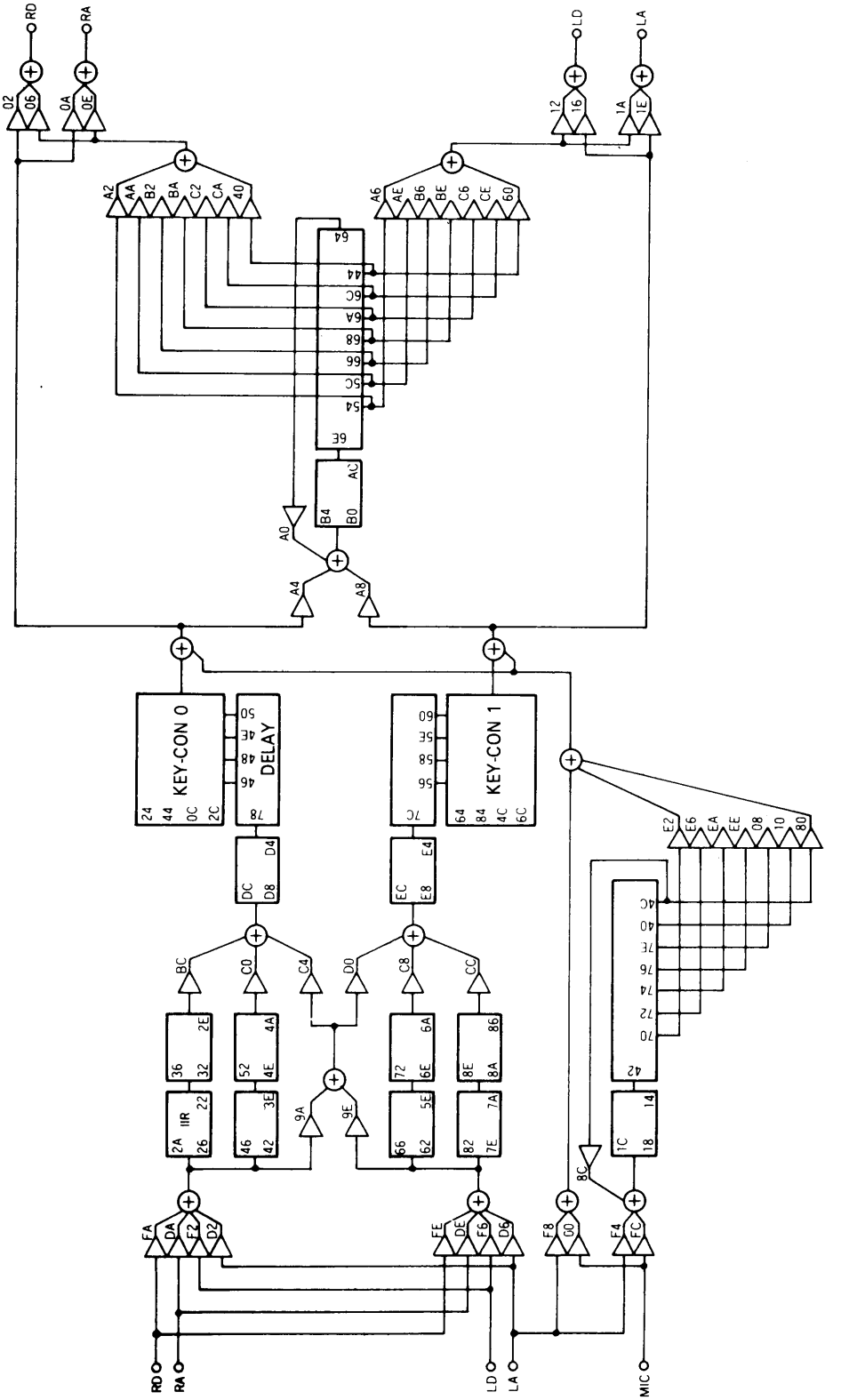
Switching operation of one or two connections is set by using the OPR register.

7. **Resetting** **/IC**

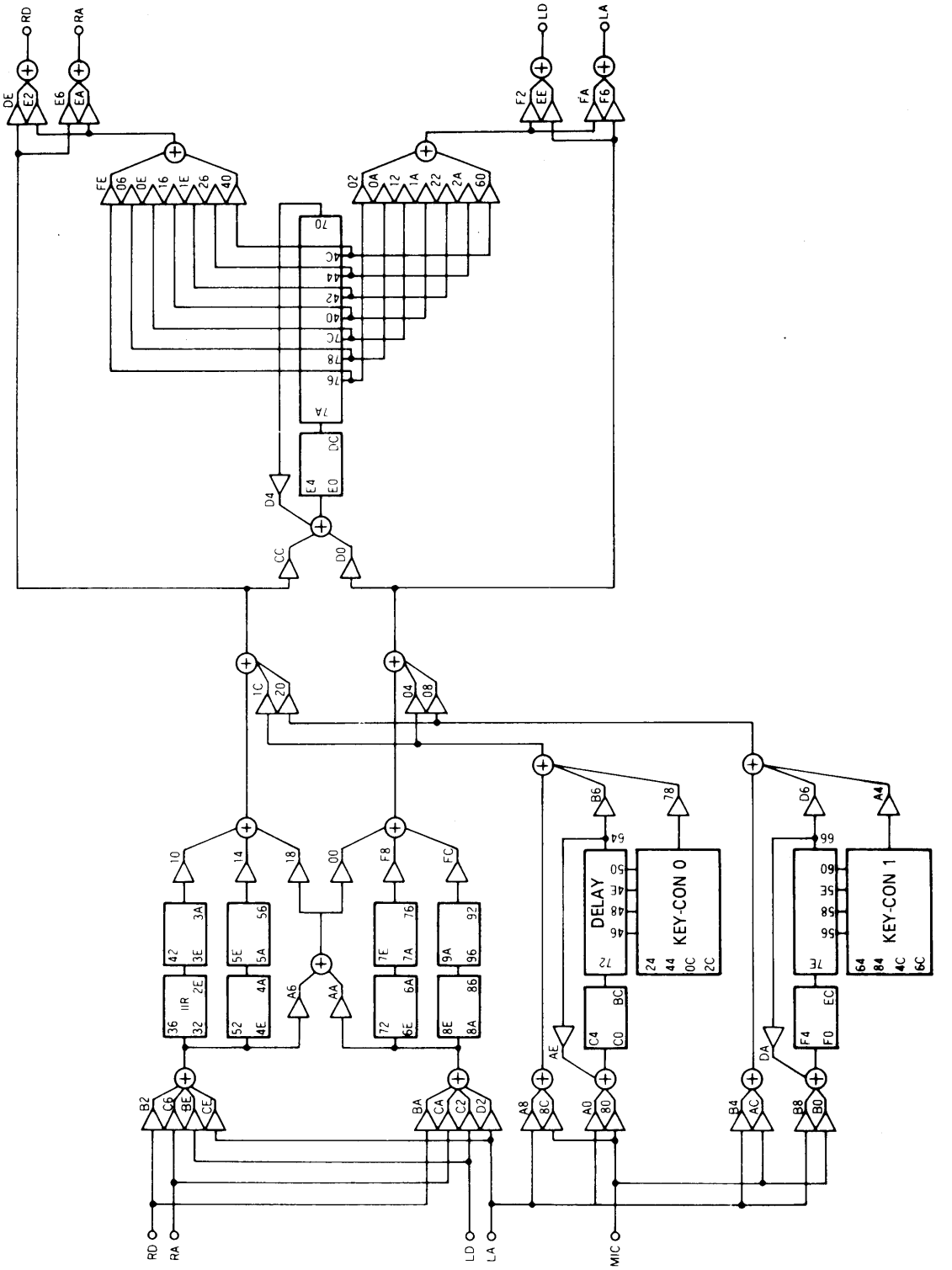
This LSI needs to be reset when turning on the power. Set /IC to 'L' for at least 1s.

■ DSP SIGNAL FLOW

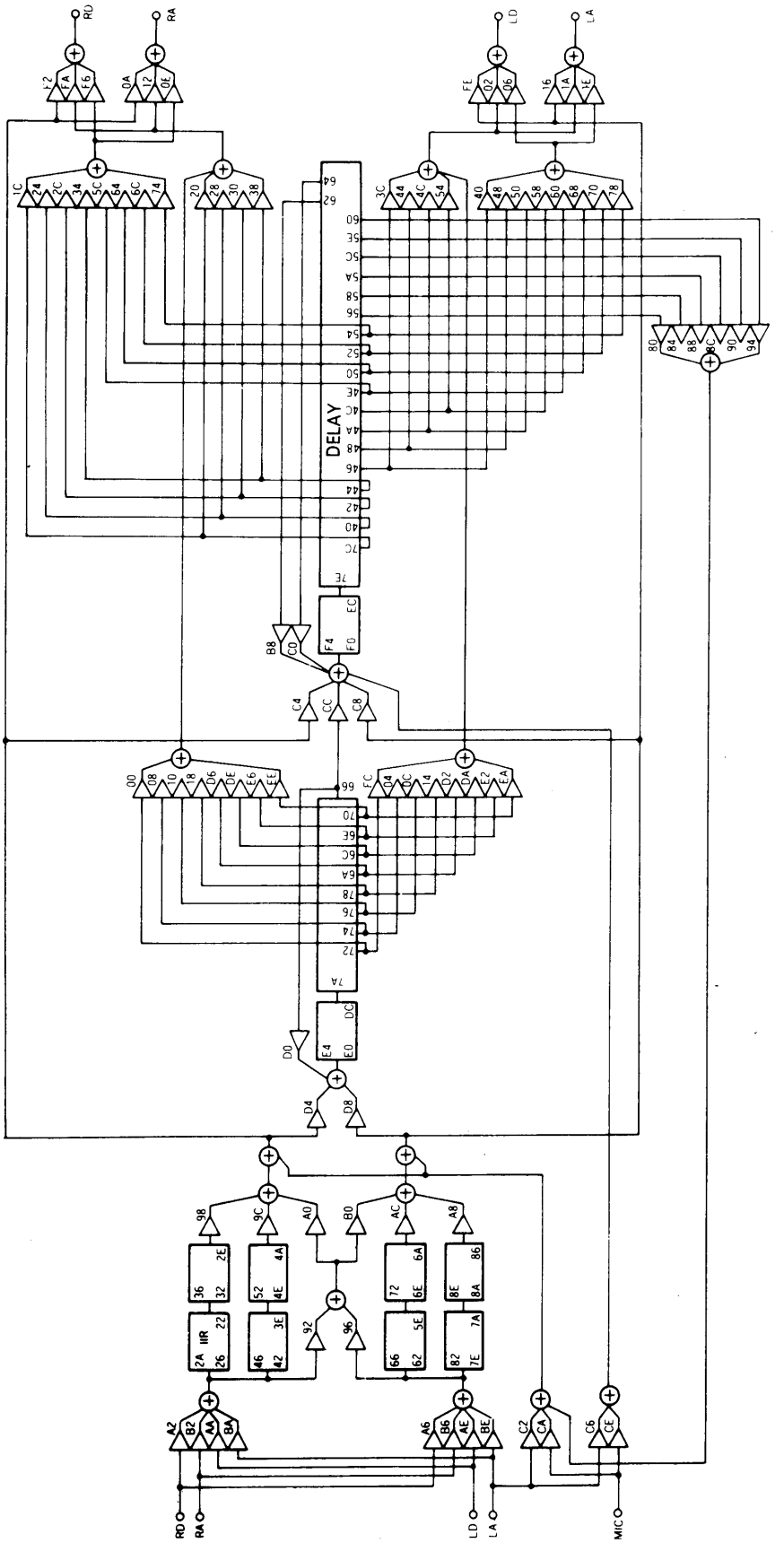
(1) MODE 0



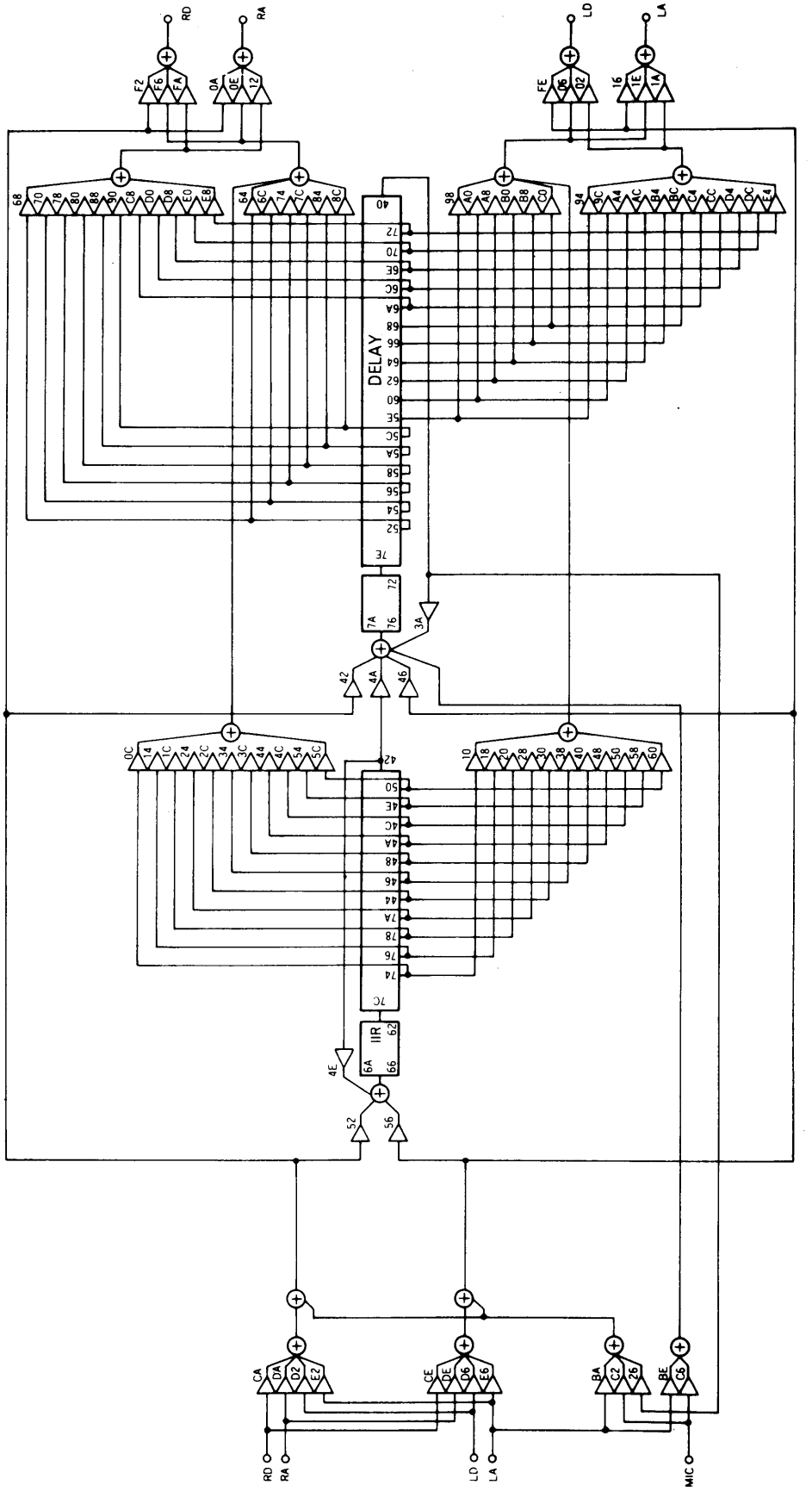
(2) MODE 1



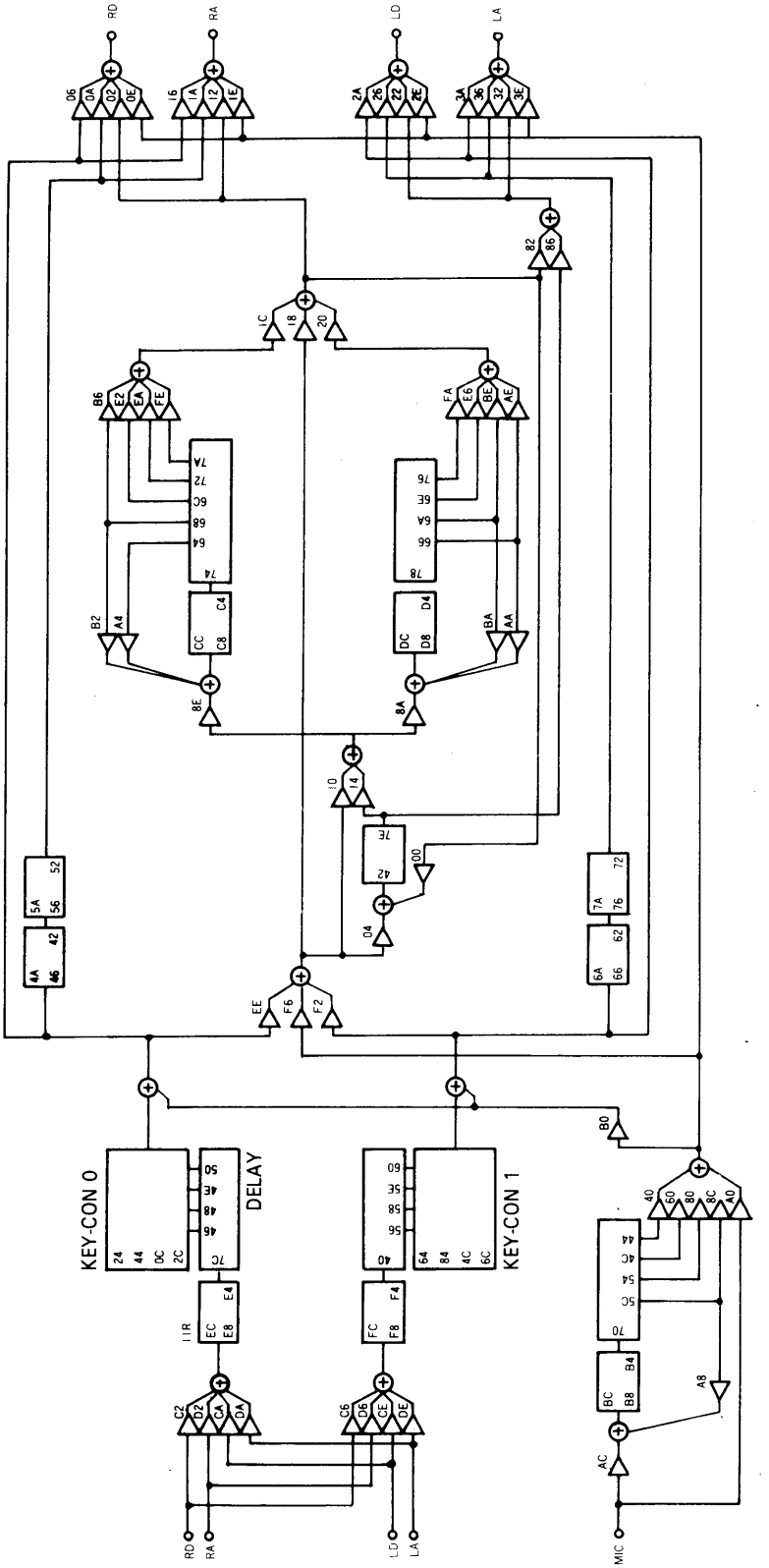
(3) MODE 2



(4) MODE 3



(5) MODE 4

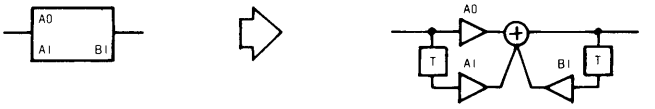


(6) Precautions for DSP signal flow

The number on the multiplier during signal flow indicates the lower byte of the address for the coefficient register. The number of the delay tap (shown in the different direction from the number on the multiplier for distinction) indicates the lower byte of the address for the memory pointer register.

- 1st order IIR filter

  In the diagram, the 1st order IIR filter is illustrated as a box with 3 coefficient register addresses. It should be noted that the coefficient of the IIR filter differs from that of the attenuator in data assignment.



T : 1 sample delay

- Coefficient registers requiring setting of fixed values

  For some coefficient registers, it is necessary to set fixed values for internal operation in each mode.

  For addresses listed below, be sure to set 0FFFH when changing the mode.

<Coefficient registers requiring 0FFFH setting>

Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
0104H	0134H	013AH	0122H	0108H
0120H	0138H	0156H	012AH	0134H
0134H	0146H	015AH	012EH	0138H
0138H	0154H	0176H	0132H	014EH
013AH	0158H	017CH	0136H	0154H
0154H	0162H	019AH	013EH	0158H
0156H	0166H	019EH	016EH	015EH
0158H	0174H	01A4H	017EH	016EH
015AH	0182H	01B4H	01ECH	0174H
0174H	0194H	01BCH	01F4H	0178H
0176H	0198H	01E8H		017EH
0178H	019EH	01F8H		0194H
0192H	01A2H			0198H
0194H	01C8H			01C0H
0196H	01E8H			01D0H
0198H				01E0H
01B8H				01F0H
01E0H				
01F0H				

- Dummy write tap for key control function

  In modes 0, 1 and 4 which use the key control function, memory pointer registers 004AH, 0052H, 005AH and 0062H become dummy write pointers. As indefinite data is written in memory addresses specified by these pointers, use care for pointer setting.

- Unspecified registers
  Any setting data can be used for memory pointer registers and coefficient registers of which nothing is indicated during signal flow and which are not listed above.

(7) DSP signal flow description

- MODE 0 :
  1. Key control of audio signals
  2. Voice cancel [to damp the center vocal]
  (L and R channels are equipped with 2 sets of 2-step, 1st order IIR filter respectively.)
  3. MIC echo
  4. Surround
  This mode with above functions is used for normal karaoke.

- MODE 1 :
  1. MIC echo + MIC key control (As there are 2 independent sets, this function can be used for stereo echo and harmony.)
  2. Voce cancel
  3. Surround
  This mode with above functions has improved production of MIC sounds.

- MODE 2 :
  1. Voice cancel
  2. Surround (There are 2 delays to produce early reflected sound and reverberation, and total of 20 taps are included.)
  This mode with above functions is intended for Surround.

- MODE 3 :
  1. Surround (There are 2 delays to produce early reflected sound and reverberation, and total of 28 taps are included.)
  This mode has emphasis on Surround for the AV source.

- MODE 4 :
  1. Key control of audio signals
  2. MIC echo
  3. Equalization (L and R channels are equipped with a 2-step,1st order IIR respectively.)
  4. Orchestra echo
  This mode with above functions is suitable for karaoke music source.

■ MICROPROCESSOR INTERFACE

(1) Register Map

ADDR	Name	Function
0000	OPR	Operation control register
0001	PSR	Program select register
0002 0003 0004 0005	KSR0L KSR0H KSR1L KSR1H	Key shift register
0040 ↕ 007F		Memory pointer register
0100 ↕ 01FF		Coefficient register

Note 1) Do not write data in any address other than those listed above.
Note 2) The data held by registers are indefinite at initial clear (except OPR).

(2) Data for setting

- Operation control register(OPR)

This register controls the internal operation. bit7 (MSB) to bit 4 have no meaning.

bit 0(LSB) : '0' = 2 external pseudo SRAM's connecting operation
'1' = 1 external pseudo SRAM connecting operation

bit 1 : '0' = Normal operation
'1' = External pseudo SRAM access prohibited

bit 2 : '0' = Normal operation
'1' = Output of internal accumulator zero clear

bit 3 : '0' = Use digital input terminals BCI, SDSY and DI (external synchronization)
'1' = Do not use digital input terminals BCI, SDSY and DI (internal synchronization)

When bit 3 has been reset from '1' to '0', avoid data transmission to the coefficient registers till falling of SDSY signals are input.

bit 0 to bit 3 are all set to '1' at initial clear.

- Program select register (PSR)
  This register is used to set the operation mode of the internal DSP.
  bit 0 (LSB) — bit 2 : operation mode setting

b2	b1	b0	Operation mode
0	0	0	Mode 0
0	0	1	Mode 1
0	1	0	Mode 2
0	1	1	Mode 3
1	0	0	Mode 4

bit 3 : YM7110 interface enable

'0' = To use built-in ADC(Connect built-in ADC input to DSP flow LA and RA.)

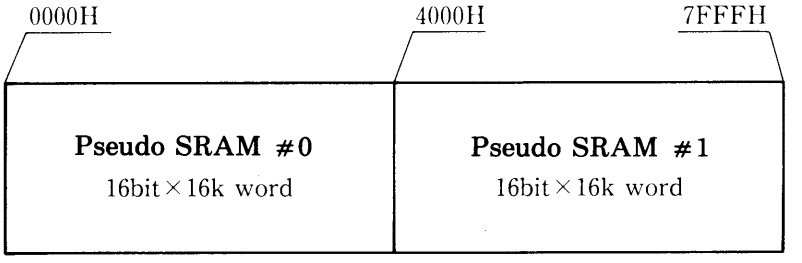
'1' = To use YM7110 (Connect input from /ANLS terminal to DSP flow LA and RA.)

Set all of bit 4 to bit 7 to '0'.

- Key shift registers (KSR0L, KSR0H, KSR1L, KSR1H)
  This register is used to set the key shift amount of the key control.
  KSR0L and KSR0H handle key controls of 0124H, 0144H, 010CH and 012CH.
  KSR1L and KSR1H handle key controls of 0164H, 0184H, 014CH and 016CH.
  Set the lower 8bits of the setting data(13 bits) to KSR0L/KSR1L and the upper 5 bits to KSR0H/KSR1H.
  As setting possible data are 0 to 4095, be sure to set MSB to '0'.

- Memory pointer register
  This register is used to specify the read and write pointers to external pseudo SRAM and control the delay time.
  The upper bytes of the memory pointer register address are 00H. The data written in that address and next address become access pointers of the memory map as shown below. The lower bytes of the memory pointer register address correspond to the delay tap number in the DSP signal flow.

  (Memory map)



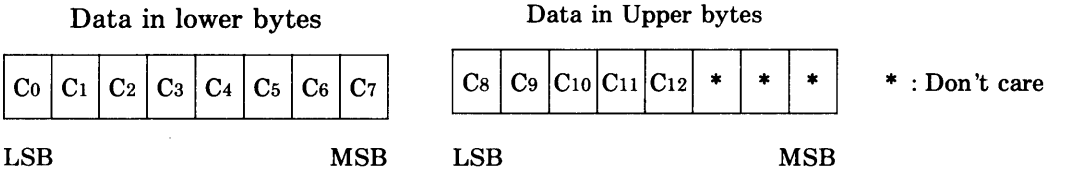
- The access ponter is expressed with 2 bytes. 0000H to 3FFFH are effective when one pseudo SRAM is connected and 0000H to 7FFFH become effective when two connections are made. The audio data is written in the memory address indicated by the write pointer and read out from the memory address indicated by the read pointer. The data in the memory shifts to the next address at every sampling period. The difference between the write pointer and the read pointer is the delay time, which is obtained by using the following equation.

  (Delay time) = [(Read pointer) − (write pointer)] × (1/fs) [s]
  fs : sampling frequency

- Coefficient register

This register is used to set the coefficient of the internal multiplier. the upper byte of the coefficient register address is 01H and the data written in that address and the next address become the coefficient value according to the assignment shown below. The lower bytes of the coefficient register address correspond to the multiplier number in the DSP signal flow.

(Coefficient data assignment)



The coefficient value of the attenuator is a 2's complement in 13 bits as expressed by the following equation.

$$\text{(Coefficient value)} = (-1) \times C_{12} + \sum_{N=0}^{11} C_N \times 2^{N-12}$$

The coefficient value of the IIR filter is doubled and so expressed as follows.

$$\text{(Coefficient value)} = [(-1) \times C_{12} + \sum_{N=0}^{11} C_N \times 2^{N-12}] \times 2$$

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 ~ 7.0	V
Input voltage	V_I	−0.3 ~ V_{DD}+0.5	V
Operating temperature	T_{op}	0 ~ 70	°C
Storage temperature	T_{stg}	−50 ~ 125	°C

2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	T_{op}	0	25	70	°C

3. DC characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current	P_{DD}	V_{DD}=5.0V			300	mW
Hight level input voltage (1)	V_{IH1}	*1	2.0			V
Low level input voltage (1)	V_{IL1}	*1			0.8	V
High level input voltage (2)	V_{IH2}	*2	3.5			V
Low level input voltage (2)	V_{IL2}	*2			0.8	V
Hight level output voltage	V_{OH1}	I_{OH}= −0.4mA	V_{DD} − 1.0			V
Low level output voltage	V_{OL}	I_{OL}=1.6mA			0.4	V
Input leakage current	I_{LI}		−10		10	μA
Input capcitance	C_I				10	pF
Output capacitance	C_O				10	pF

*1) Applicable to input terminals except XI and /IC
*2) Applicable to XI and /IC terminals

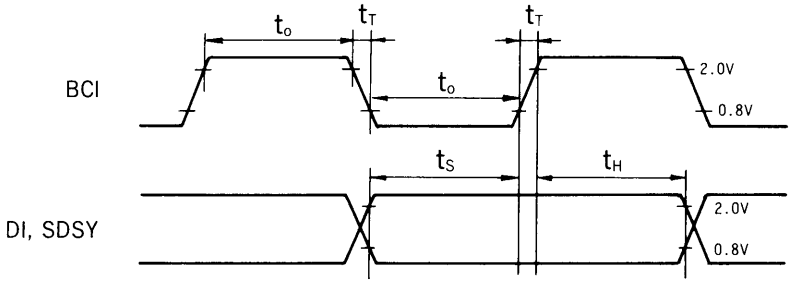
4. AC Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit
XI	input frequency (1) *1	f_{C1}	12.0	16.9344	19.0	MHz
	Input frequency (2) *2	f_{C2}	8.0	11.2896	13.0	MHz
	Duty	R_C		50		%
BCI	frequency	f_{BC}	1.0		4.3	MHz
	ON/OFF time	t_O	100			ns
	Transition time	t_T			20	ns
DI, SDSY	Setup time	t_S	100			ns
	hold time	t_H	100			ns
DO, L/R	Access time	t_D	−20		20	ns
/CS	Setup time	t_C	1/50fs			s
/SCK	ON/OFF time	t_{SO}	1/50fs			s
/CS, /SCK	Transition time	t_R			1/150fs	s
CDI	Setup time	t_{SS}	1/100fs			s
	hold time	t_{SH}	1/100fs			s

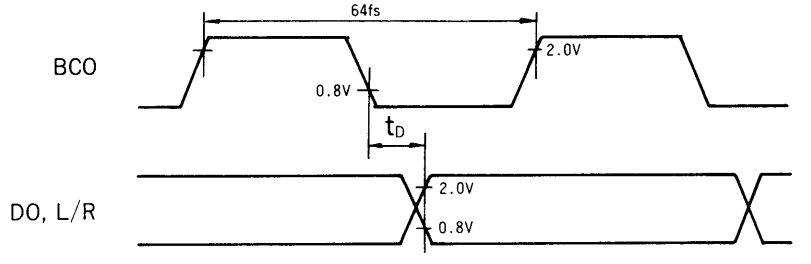
*1) When 386/256 = 'H'(fC1 = 384fs)

*2) When 384/256 = 'L'(fC2 = 256fs)

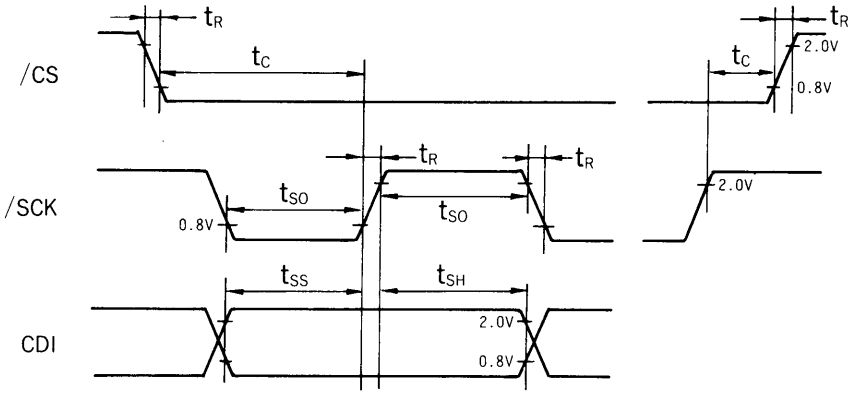
a. Audio data input timing



b. Audio data output timing



c. Microprocessor interface timing

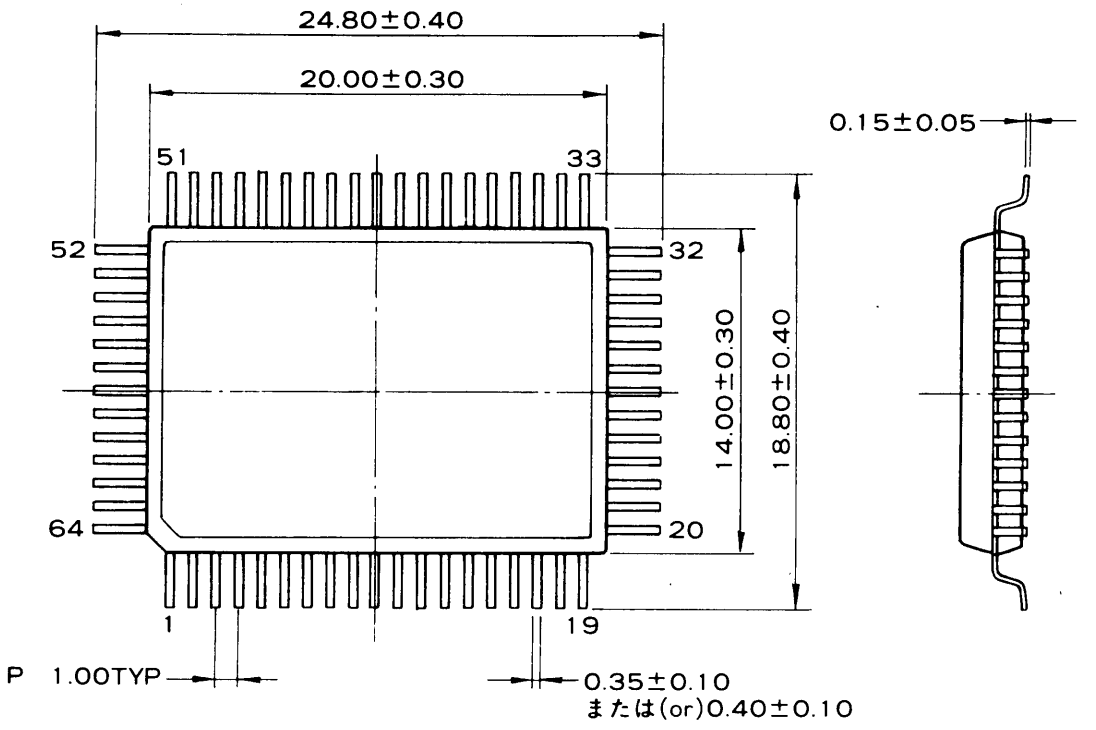


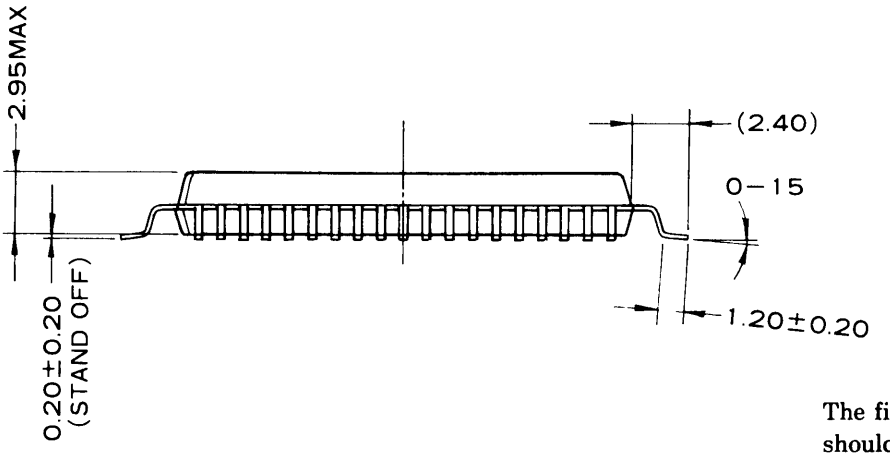
5. Analog Characteristics (Condition: V_{DD}=5.0V, Ta=25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog input voltage amplitude	VIA	AIL, AIR and MIC terminals		4.75		V
Analog output voltage amplitude	VOA	AOL, AOR and terminals		4.75		V
ADC center voltage	Vc	CVA, CVB terminals		2.5		V
Total harmonic distortion (1)	(THD+N) 1	1kHz,0dB, *1		0.5	1.0	%
Total harmonic distortion (2)	(THD+N) 2	1kHz, −30dB, *1		0.8	1.5	%
Signal-to-Noise ratio	S/N	S=0dB, *2	75	80		dB

*1) Use an LPF (fc=15kHz, 30dB/oct), 0dB=4,75Vpp and A/D → D/A through
*2) Use an IHF-A filter, 0dB=4.75Vpp and A/D → D/A through

■ EXTERNAL DIMENSIONS





The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

Note : The LSIs for surface mount need especial consideration on strage and soldering conditions. For detailed information, please contact your nearest agent of yamaha.

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