Z87200

SPREAD-SPECTRUM TRANSCEIVER

FEATURES

Device	Min PN Rate* (Mchips)	Max Data Rate* (Mbps)	Speed (MHz)	Package
Z87200	11	2.048	20/45	100-Pin PQFP

Note: *45 MHz only

- Complete Direct Sequence Spread-Spectrum Transceiver in a Single CMOS IC
- Programmable Functionality Supports Many Different Operational Modes
- Acquires Within One Symbol Duration Using Digital PN Matched Filter
- Two Independent PN Sequences, Each up to 64 Chips Long for Distinct Processing of the Acquisition/Preamble Symbol and Subsequent Data Symbols
- Power Management Features
- Optional Spectral Whitening Code Generation
- Full- or Half-Duplex Operation

Benefits

- High Performance and High Reliability for Reduced Manufacturing Costs
- Ideal for a Wide Range of Wireless Applications Including Data Acquisition Systems, Transaction Systems, and Wireless Local Area Networks (WLANs)
- Fast Response and Very Low Overhead when Operating in Burst Modes
- Allows High Processing Gain to Maximize the Acquisition Probability, then Reduced Code Length for Increased Data Rate
- Reduced Power Consumption
- Randomizes Data to Meet Regulatory Requirements
- Permits Dual Frequency (Frequency Division Duplex) or Single Frequency (Time Division Duplex) Operation
- Small Footprint, Surface Mount

GENERAL DESCRIPTION

The Z87200 is a programmable single-chip, spread-spectrum, direct-sequence transceiver. The Z87200 incorporates Stanford Telecom spread-spectrum and wireless technology and is identical to Stanford Telecom's STEL-2000A. By virtue of its fast acquisition capabilities and its ability to support a wide range of data rates and spread-spectrum parameters, the Z87200 spread-spectrum transceiver supports the implementation of a wide range of burst data communications applications.

Available in both 45- and 20-MHz versions, the Z87200 performs all the digital processing required to implement a fast-acquisition direct sequence (such as pseudonoise- or PN-modulated), spread-spectrum full- or half-duplex system. Differentially encoded BPSK and QPSK are fully supported. The receiver section can also handle differentially encoded pi/4 QPSK. A block diagram of the Z87200 is shown in Figure 1; its pin configuration is shown in Z87200 receive functions integrate the capabilities of a digital downconverter, PN matched filter, and DPSK demodulator, where the input signal is an analog-to-digital converted I.F. signal. Z87200 transmit functions include a differential BPSK/QPSK encoder, PN modulator (spreader), and BPSK/QPSK modulator, where the transmitter output is a sampled digitally modulated signal ready for external digi-

GENERAL DESCRIPTION (Continued)

tal-to-analog conversion (or, if preferred, the spread baseband signal may be output to an external modulator).

These transceiver functions have been designed and integrated for the transmission and reception of bursts of spread data. In particular, the PN Matched Filter has two distinct PN coefficient registers (rather than a single one) in order to speed and improve signal acquisition performance by automatically switching from one to the other upon signal acquisition. The Z87200 is thus optimized to provide reliable, high-speed wireless data communications.

Symbol-Synchronous PN Modulation

The Z87200 operates with symbol-synchronous PN modulation in both transmit and receive modes. Symbol-synchronous PN modulation refers to operation where the PN code is aligned with the symbol transitions and repeats once per symbol. By synchronizing a full PN code cycle over a symbol duration, acquisition of the PN code at the receiver simultaneously provides symbol synchronization, thereby significantly improving overall acquisition time.

As a result of the Z87200's symbol-synchronous PN modulation, the data rate is defined by the PN chip rate and length of the PN code; that is, by the number of chips per symbol, where a “chip” is a single “bit” of the PN code. The PN chip rate, R_c chips/second, is programmable to as much as 1/4 the rate of RXIFCLK, and the PN code length, N, can be programmed up to a value of 64. When operating with BPSK modulation, the data rate for a PN code of length N and PN chip rate R_C chips/sec is R_C/N bps. When operating with QPSK modulation (or $\pi/4$ QPSK with an external modulator), two bits of data are transmitted per symbol, and the data rate for a PN code of length N and PN chip rate R_c chips/sec is $2R_c/N$ bps. Conversely, for a given data rate R_b bps, the length N of the PN code defines the PN chip rate R_c as $N \times R_b$ chips/sec for BPSK or as $(N \times R_b)/2$ chips/sec for QPSK.

The data rate R_b and the PN code length N, however, cannot generally be arbitrarily chosen. United States FCC Part 15.247 regulations require a minimum processing gain of 10 dB for unlicensed operation in the Industrial, Scientific, and Medical (ISM) bands, implying that the value of N must be at least 10. To implement such a short code, a Barker code of length 11 would typically be used in order to obtain desirable auto- and cross-correlation properties, although compliance with FCC regulations depends upon the overall system implementation. The Z87200 further includes transmit and receive code overlay generators to insure that signals spread with such a short PN code length possess the spectral properties required by FCC regulations.

The receiver clock rate established by RXIFCLK must be at least four times the receive PN spreading rate and is limited to a maximum speed of 45.056 MHz in the 45 MHz Z87200 and 20.0 MHz in the 20 MHz Z87200. The ensuing discussion is in terms of the 45 MHz Z87200, but the numerical values may be scaled proportionately for the 20 MHz version. As a result of the maximum 45.056 MHz RXIFCLK, the maximum supported PN chip rate is 11.264 Mchips/second. When operating with BPSK modulation, the maximum data rate for a PN code of length N is 11.264/N Mbps. When operating with QPSK modulation (or $\pi/4$ QPSK with an external modulator), two bits of data are transmitted per symbol, and the data rate for a PN code of length N is 22.528/N Mbps. Conversely, for a given data rate R_b, the length N of the PN code employed must be such that the product of $N \times R_b$ is less than 11.264 Mchips/sec (for BPSK) or 22.528 Mchips/sec (for QPSK). For the 45 MHz Z87200, then, a PN code length of 11 implies that the maximum data rate that can be supported in compliance with the processing gain requirements of FCC regulations is 2.048 Mbps using differential QPSK. Note again, however, that FCC compliance using the Z87200 with a PN code of length 11 depends upon the overall system implementation.

Z87200 I.F. Interface

The Z87200 receiver circuitry employs an NCO and complex multiplier referenced to RXIFCLK to perform frequency downconversion, where the input I.F. sampling rate and the clock rate of RXIFCLK must be identical. In "complex input" or Quadrature Sampling Mode, external dual analog-to-digital converters (ADCs) sample quadrature I.F. signals so that the Z87200 can perform true full single sideband downconversion directly from I.F. to baseband. At PN chip rates less than one-eighth the value of RXIFCLK, downconversion may also be effected using a single ADC in "real input" or Direct I.F. Sampling Mode.

The input I.F. frequency is not limited by the capabilities of the Z87200. The highest frequency to which the NCO can be programmed is 50% of the I.F. sampling rate (the frequency of RXIFCLK); moreover, the signal bandwidth, NCO frequency, and I.F. sampling rate are all interrelated, as discussed in Higher I.F. frequencies, however, can be supported by using one of the aliases of the NCO frequency generated by the sampling process. For example, a spread signal presented to the Z87200's receiver ADCs at an I.F. frequency of $f_{I.F.}$, where $f_{RXIFCLK} < f_{I.F.} < 2 \times f_{RXIFCLK}$, can generally, as allowed by the signal's bandwidth, be supported by programming the Z87200's NCO to a frequency of ($f_{I.F.} - f_{RXIFCLK}$), as discussed in Appendix A of this product specification. The maximum I.F. frequency is then limited by the track-and-hold capabilities of the ADC(s) selected. Signals at I.F. frequencies up to about 100 MHz can be processed by currently available 8-bit ADCs, but the implementation cost as well as the performance can typically be improved by using an I.F. frequency of 30 MHz or lower. Downconversion to baseband is then accomplished digitally by the Z87200, with a programmable loop filter provided to establish a frequency tracking loop.

Burst and Continuous Data Modes

The Z87200 is designed to operate in either burst or continuous mode: in burst mode, built-in symbol counters allow bursts of up to 65,533 symbols to be automatically transmitted or received; in continuous mode, the data is simply treated as a burst of infinite length. The Z87200's use of a digital PN Matched Filter for code detection and despreading permits signal and symbol timing acquisition in just one symbol. The fast acquisition properties of this design are exploited by preceding each data burst with a single Acquisition/Preamble symbol, allowing different PN codes (at the same PN chip rate) to independently spread the Acquisition/Preamble and data symbols. In this way, a long PN code with high processing gain can be used for the Acquisition/Preamble symbol to maximize the probability of burst detection, and a shorter PN code can be used thereafter to permit a higher data rate.

To improve performance in the presence of high noise and interference levels, the Z87200 receiver's symbol timing recovery circuit incorporates a "flywheel circuit" to maximize the probability of correct symbol timing. This circuit will insert a symbol clock pulse if the correlation peak obtained by the PN Matched Filter fails to exceed the programmed detect threshold at the expected time during a given symbol. During each burst, a missed detect counter tallies each such event to monitor performance and allow a burst to be aborted in the presence of abnormally high interference. A timing gate circuit further minimizes the probability of false correlation peak detection and consequent false symbol clock generation due to noise or interference.

To minimize power consumption, individual sections of the device can be turned off when not in use. For example, the receiver circuitry can be turned off during transmission and, conversely, the transmitter circuitry can be turned off during reception when the Z87200 is operating in a half-duplex/time division duplex (TDD) system. If the NCO is not being used as the BPSK/QPSK modulator (that is, if an external modulator is being used), the NCO can also be turned off during transmission to conserve still more power.

Conclusion

The fast acquisition characteristics of the Z87200 make it ideal for use in applications where bursts are transmitted relatively infrequently. In such cases, the device can be controlled so that it is in full "sleep" mode with all receiver, transmitter, and NCO functions turned off over the majority of the burst cycle, thereby significantly reducing the aggregate power consumption. Since the multiply operations of the PN Matched Filter consume a major part of the overall power required during receiver operation, two independent power-saving techniques are also built into the PN Matched Filter to reduce consumption during operation by a significant factor for both short and long PN spreading codes.

The above features make the Z87200 an extremely versatile and useful device for spread-spectrum data communications. Operating at its highest rates, the Z87200 is suitable for use in wireless Local Area Network implementations, while its programmability allows it to be used in a variety of data acquisition, telemetry, and transaction system applications.

GENERAL DESCRIPTION (Continued)

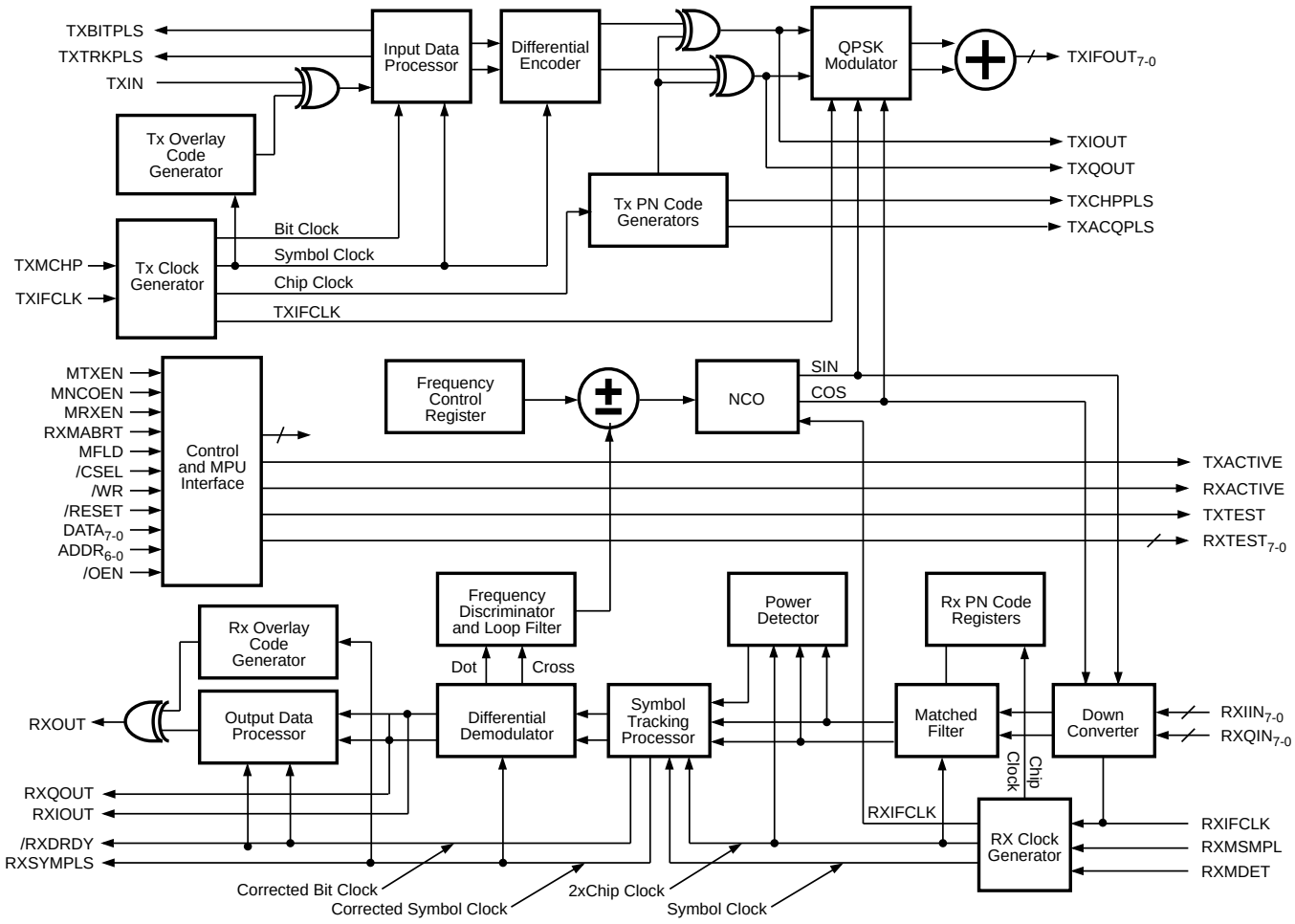
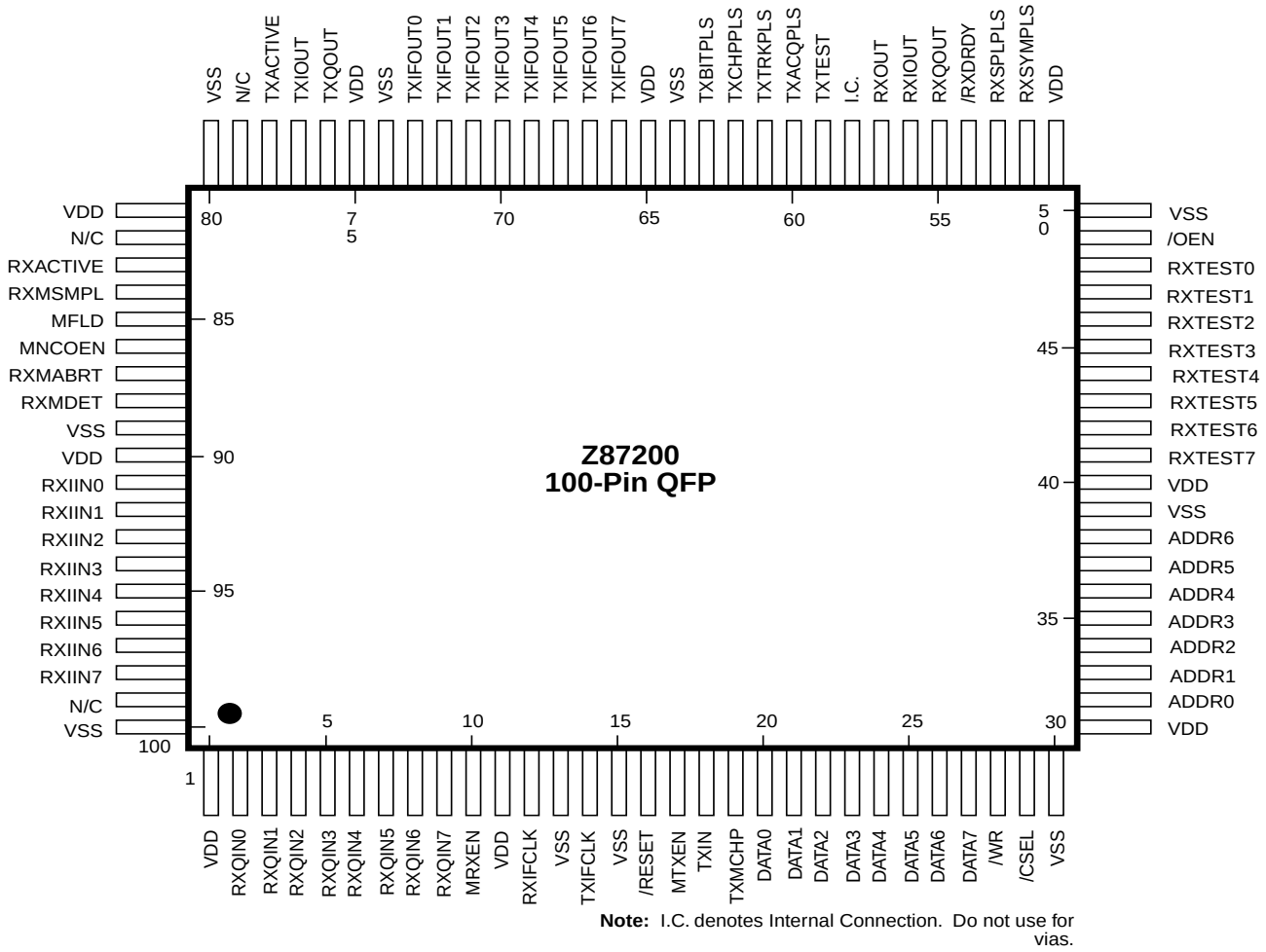


Figure 1. Z87200 Block Diagram

PIN DESCRIPTION



Note: I.C. denotes Internal Connection. Do not use for vias.

Figure 2. Z87200 100-Pin PQFP Pin Description

PIN DESCRIPTION (Continued)

Table 1. 100-Pin PQFP Pin Description

No	Symbol	Function
1,11,31,40,51,65,75,81,90	V_{DD}	Power Supply
2	RXQIN0	Rx Q-Channel Input (Bit 0; LSB)
3	RXQIN1	Rx Q-Channel Input (Bit 1)
4	RXQIN2	Rx Q-Channel Input (Bit 2)
5	RXQIN3	Rx Q-Channel Input (Bit 3)
6	RXQIN4	Rx Q-Channel Input (Bit 4)
7	RXQIN5	Rx Q-Channel Input (Bit 5)
8	RXQIN6	Rx Q-Channel Input (Bit 6)
9	RXQIN7	Rx Q-Channel Input (Bit 7; MSB)
10	RXXE	Manual Receiver Enable
12	RXIFCLK	Receiver I.F. Clock
13,15,30,39,50,64,74,80,89	V_{SS}	Ground
14	TXIFCLK	Transmitter I.F. Clock
16	/RESET	/Reset
17	MTXE	Manual Transmitter Enable
18	TXIN	Transmitter Input
19	TXMCHP	Transmitter Manual Chip Pulse
20	DATA0	Data Bus (Bit 0; LSB)
21	DATA1	Data Bus (Bit 1)
22	DATA2	Data Bus (Bit 2)
23	DATA3	Data Bus (Bit 3)
24	DATA4	Data Bus (Bit 4)
25	DATA5	Data Bus (Bit 5)
26	DATA6	Data Bus (Bit 6)
27	DATA7	Data Bus (Bit 7; MSB)
28	/WR	Write Bar
29	/CSEL	Chip Select Bar
32	ADDR0	Address Bus (Bit 0; LSB)
33	ADDR1	Address Bus (Bit 1)
34	ADDR2	Address Bus (Bit 2)
35	ADDR3	Address Bus (Bit 3)
36	ADDR4	Address Bus (Bit 4)
37	ADDR5	Address Bus (Bit 5)
38	ADDR6	Address Bus (Bit 6; MSB)
41	RXTEST7	Receiver Test Output (Bit 7)
42	RXTEST6	Receiver Test Output (Bit 6)
43	RXTEST5	Receiver Test Output (Bit 5)
44	RXTEST4	Receiver Test Output (Bit 4)
45	RXTEST3	Receiver Test Output (Bit 3)
46	RXTEST2	Receiver Test Output (Bit 2)
47	RXTEST1	Receiver Test Output (Bit 1)
48	RXTEST0	Receiver Test Output (Bit 0)
49	/OEN	Output Enable Bar
52	RXSYMPLS	Receiver Symbol Pulse
53	RXSPLPLS	Receiver Sample Pulse

Table 1. 100-Pin PQFP Pin Description

No	Symbol	Function
54	/RXDRDY	Receiver Data Ready Bar
55	RXQOUT	Receiver Q Channel Output
56	RXIOUT	Receiver I Channel Output
57	RXOUT	Receiver Output
58	I.C.	[Note]
59	TXTEST	Transmitter Test Output
60	TXACQPLS	Transmitter Acquisition Pulse
61	TXTRKPLS	Transmitter Data Track Pulse
62	TXCHPPLS	Transmitter Chip Pulse
63	TXBITPLS	Transmitter Bit Pulse
66	TXIFOUT7	Tx I.F. Output (Bit 7, MSB)
67	TXIFOUT6	Tx I.F. Output (Bit 6)
68	TXIFOUT5	Tx I.F. Output (Bit 5)
69	TXIFOUT4	Tx I.F. Output (Bit 4)
70	TXIFOUT3	Tx I.F. Output (Bit 3)
71	TXIFOUT2	Tx I.F. Output (Bit 2)
72	TXIFOUT1	Tx I.F. Output (Bit 1)
73	TXIFOUT0	Tx I.F. Output (Bit 0, LSB)
76	TXQOUT	Tx Q-Channel Output
77	TXIOUT	Tx I-Channel Output
78	TXACTIVE	Transmitter Active
79,82	N.C.	No Connection
83	RXACTIVE	Receiver Active
84	RXMSMPL	Receiver Manual Sample Clock
85	MFLD	Manual Frequency Load
86	MNCOEN	Manual NCO Enable
87	RXMABRT	Receiver Manual Abort
88	RXMDET	Receiver Manual Detect
91	RXIIN0	Rx I-Channel Input (Bit 0; LSB)
92	RXIIN1	Rx I-Channel Input (Bit 1)
93	RXIIN2	Rx I-Channel Input (Bit 2)
94	RXIIN3	Rx I-Channel Input (Bit 3)
95	RXIIN4	Rx I-Channel Input (Bit 4)
96	RXIIN5	Rx I-Channel Input (Bit 5)
97	RXIIN6	Rx I-Channel Input (Bit 6)
98	RXIIN7	Rx I-Channel Input (Bit 7; MSB)
99	N.C.	No Connection
100	V_{SS}	Ground

Note: I.C. denotes Internal Connection. Do not use for vias.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Range	Units
T_{STG}	Storage Temperature	–55 to +150	°C
V_{DD} (max)	Supply Voltage on V_{DD}	–0.3 to + 7	Volts
V_I(max)	Input Voltage	–0.3 to V_{DD}+0.3	Volts
I_I	DC Input Current	±10	mA
T_A	Operating Temperature (Ambient)	0 to +70	°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

D.C. CHARACTERISTICS

Operating Conditions: V_{DD} = 5.0V ±5%, V_{SS} = 0V

		T_A = 0° to +70°C		Typ		
Symbol	Parameter	Min	Max	@ 25°C	Units	Conditions
I_{DDQ}	Supply Current, Quiescent		1.0		mA	Static, no clock
I_{DD}	Supply Current, Operational		380 170	[Note]	mA mA	$f_{RXIFCLK}$ = 45.056 MHz $f_{RXIFCLK}$ = 20 MHz
V_{IH} (min)	High Level Input Voltage	0.7V_{DD}	V_{DD}+.3	2.6	Volts	Logic ‘1’
V_{IL}(min)	Low Level Input Voltage	V_{SS}–.3	0.2V_{DD}	1.5	Volts	Logic ‘0’
I_{IH} (min)	High Level Input Current		10		µA	All inputs, V_{IN} = V_{DD}
I_{IL} (max)	Low Level Input Current		–10		µA	TXIFCLK, RXIFCLK, /RESET only, V_{IN} = V_{SS}
I_{IL}(max)	Low Level Input Current	–130	–15	–45	µA	All other inputs, V_{IN} = V_{SS}
V_{OH}(min)	High Level Output Voltage	V_{DD}–0.4			Volts	I_O = –2.0 mA, all outputs
V_{OL}(max)	Low Level Output Voltage		0.4	0.1	Volts	I_O = +2.0 mA, all outputs
I_{OS}	Output Short Circuit Current	20	130	65	mA	V_{OUT} = V_{DD}, V_{DD} = max
C	Input Capacitance	2			pF	All inputs
C_{OUT}	Output Capacitance			4	pF	All outputs

Notes:

1. The operational supply current depends on how the Z87200 is configured. Typical current consumption can be approximated as follows:
2. I_{DD}=5x$f_{RXIFCLK}$ +13 x f_{CHIP} mA,
3. where $f_{RXIFCLK}$ is the frequency of RXIFCLK and f_{CHIP} is the PN chip rate, both in MHz.

A.C. CHARACTERISTICS

Operating Conditions: V_{DD} = 5.0V ±5%, V_{SS} = 0V

		T_A = 0° to +70°C			
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Conditions**
t_{SU}	/CSEL, ADDR, DBUS to WRITE Setup	5		ns	
t_{HD}	WRITE to CSEL, ADDR, DBUS Hold	5		ns	
t_W	WRITE Pulse Width	5		ns	

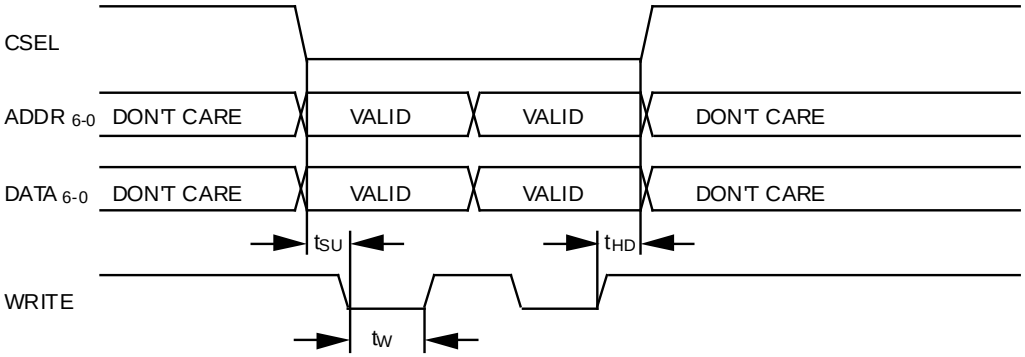


Figure 3. Microprocessor Interface Timing

A.C. CHARACTERISTICS - TRANSMITTER

Operating Conditions: V_{DD} = 5.0V ±5%, V_{SS} = 0V

		T_A 0°C to +70°C			
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Conditions**
$f_{TXIFCLK}$	TXIFCLK Frequency		45.056 20.0	MHz MHz	Z0200045FSC Z0200020FSC or if TXIFOUT is used
t_{CH}	TXIFCLK Pulse width, High	10		ns	
t_{CL}	TXIFCLK Pulse width, Low	10		ns	
t_{SU}	TXIN to TXIFCLK setup	3		ns	
t_{HD}	TXIN to TXIFCLK hold	5		ns	
t_{CT}	TXIFCLK to TXBITPLS, TXTRKPLS, XACQPLS, TXIOUT or TXQOUT delay		35	ns	

Notes:

1. The number of TXIFCLK cycles per cycle of TXCHPPLS is determined by the data stored in bits 5-0 of address 41_H. It is shown as 2 in Figure 8 but can be set from 2 to 64.
2. The width of the TXBITPLS, TXTRKPLS and TXACQPLS signal pulses is equal to the period of TXCHPPLS; that is, equal to the PN chip period.
3. In QPSK mode, the TXBITPLS signal pulses high twice during each symbol period, once during the center chip and once during the last chip. If the number of chips per symbol is even, the number of chip periods between the TXBITPLS pulse at the end of the previous symbol and the one in the center of the symbol will be one more than the number of chip periods between the TXBITPLS pulse in the center of the symbol and the one at the end. The falling edge of the second pulse corresponds to the end of the symbol period.
4. The TXTRKPLS signal pulses high once each symbol period, during the last chip period of that symbol. The falling edge corresponds to the end of the symbol period.
5. The TXACQPLS signal pulses high once each burst, transmission, during the last chip of the Acquisition/Preamble symbol. The falling edge corresponds to the end of this symbol period.

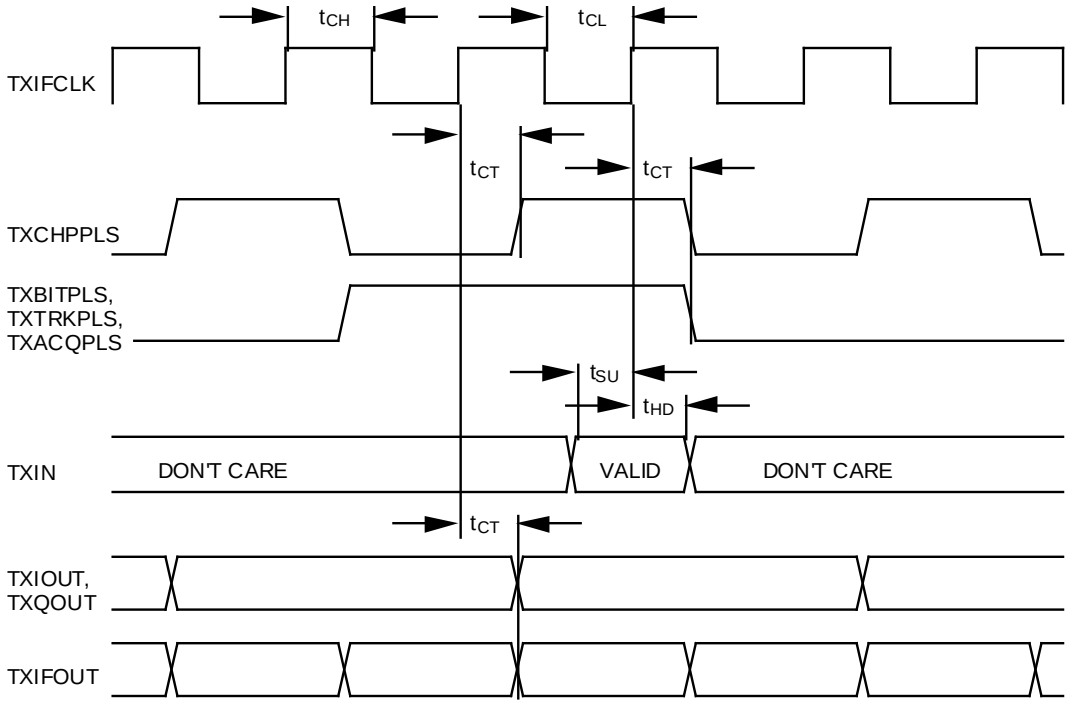


Figure 4. Transmitter Input/Output Timing

A.C. CHARACTERISTICS - RECEIVER

Operating Conditions: V_{DD} = 5.0V ±5%, V_{SS} = 0V

		T_A = 0° to +70°C			
Symbol	**Parameter**	**Min**	**Max.**	**Units**	**Conditions**
$f_{RXIFCLK}$	RXIFCLK Frequency		45.056 20.0	MHz MHz	Z8720045FSC Z8720020FSC
t_{CH}	RXIFCLK Pulse width, High	10		ns	
t_{CL}	RXIFCLK Pulse width, Low	10		ns	
t_{SU}	RXIIN or RXQIN to RXIFCLK setup	3		ns	
t_{HD}	RXIIN or RXQIN to RXIFCLK hold	7		ns	
t_{CR}	RXIFCLK to RXSPLPLS, RXSYMPLS, or /RXDRDY delay		35	ns	
t_{CD}	RXIFCLK to RXOUT, RXIOUT, or RXQOUT delay		35	ns	

Notes:

1. The number of RXIFCLK cycles per cycle of RXSPLPLS is determined by the data stored in bits 5-0 of address 02_H. It is shown as 2 in Figure 9, but can be set from 2 to 64.
2. The rising edge of /RXDRDY should be used to clock out the data (RXOUT, RXIOUT, or RXQOUT).

A.C. CHARACTERISTICS

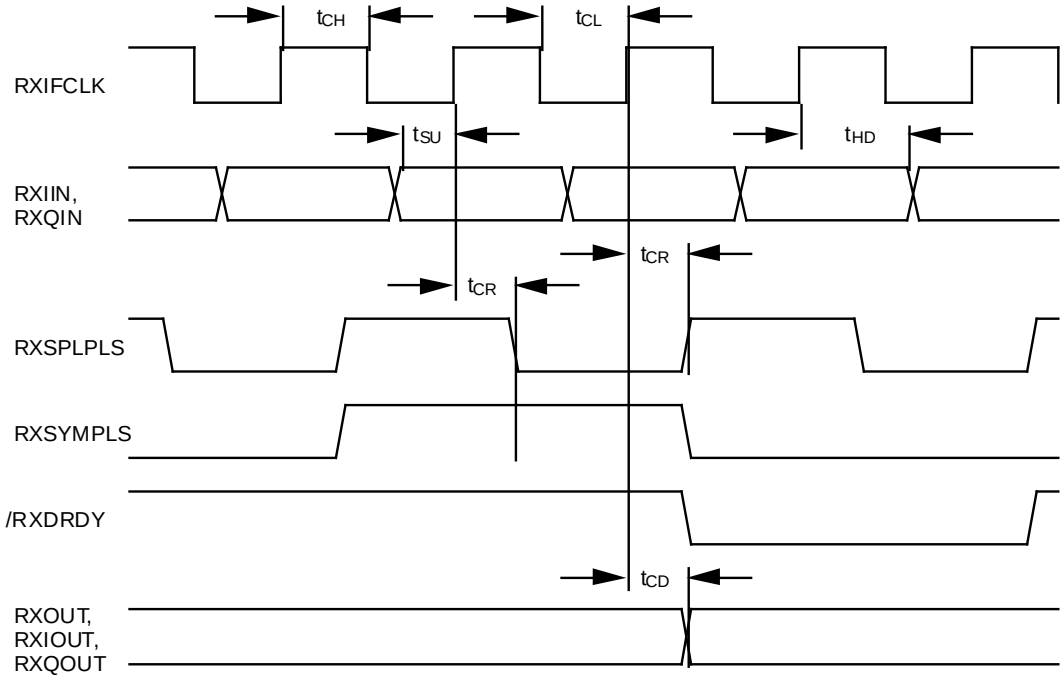


Figure 5. Receiver Input/Output

AC CHARACTERISTICS

Operating Conditions: V_{DD} = 5.0V ±5%, V_{SS} = 0V

		T_A = 0° to +70°C		
Symbol	**Parameter**	**Min**	**Max**	**Units**
t_{D1}	/OEN low to RXTEST $_{7-0}$ active	11		ns
t_{D2}	/OEN high to RXTEST $_{7-0}$ tri-state	7		ns

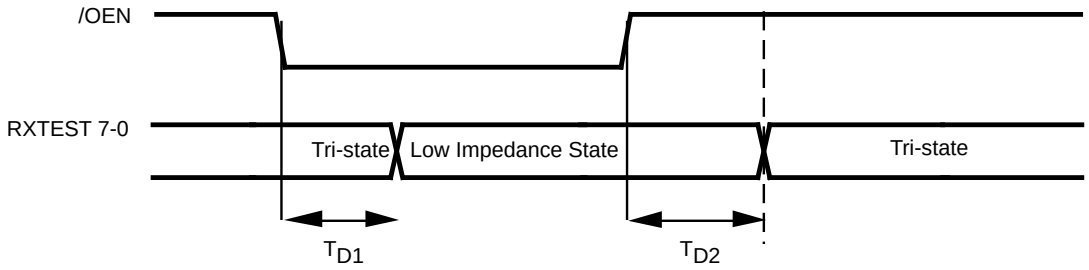


Figure 6. /OEN to RXTEST 7-0 Timing

FUNCTIONAL BLOCKS

Transmit and Receive Clock Generators

Timing in the transmitter and receiver sections of the Z87200 is controlled by the Transmit and Receive Clock Generator Blocks. These blocks are programmable dividers providing signals at the chip and symbol rates (as well as at multiples and sub-multiples of these frequencies) as programmed through the Z87200's control registers. If desired, the complete independence of the transmitter and receiver sections allows the transmit and receive clocks to be mutually asynchronous. Additionally, the Z87200 allows external signals to be provided as references for the transmit (TXMCHP) and receive (RXMSMPL) chip rates. Given the transmit PN chip rate, the PN-synchronous transmit symbol rate is then derived from the programmed number of PN chips per transmit symbol. At the receiver, symbol synchronization and the receive symbol rate are determined from processing of the PN matched filter output, or, if desired, can be provided from the programmed number of PN chips per receive symbol or an external symbol synch symbol, RXMDET. Burst control is achieved by means of the transmit and receive Symbols per Burst counters. These programmable 16-bit counters allow the Z87200 to operate automatically in burst mode, stopping at the end of each burst without the need of any external counters.

Input and Output Processors

When the transmitter and receiver are operating in QPSK mode, the data to be transmitted and the received data are processed in pairs of bits (dibits), one bit for the in-phase (I) channel and one for the quadrature (Q) channel. Dibits are transmitted and received as single differentially encoded QPSK symbols. Single-bit I/O data is converted to and from this format by the Input and Output Processors, accepting TXIN as the serial data to be transmitted and producing RXOUT as the serial data output. If desired, the received data is also available at the RXIOUT and RXQOUT pins in (I and Q) dibit format prior to dibit-to-serial conversion. While receive timing is derived by the Z87200 Symbol Tracking Processor, transmit timing is provided by the Input Processor. In BPSK mode, the Input Processor will generate the TXBITPLS signal once per symbol to request each bit of data, while in QPSK mode it will generate the TXBITPLS signal twice per symbol to request the two bits of data corresponding to each QPSK symbol.

Differential Encoder

Data to be transmitted is differentially encoded before being spread by the transmit PN code. Differential encoding of the signal is fundamental to operation of the Z87200's receiver: the Z87200's DPSK Demodulator computes "Dot" and "Cross" product functions of the current and previous symbols' downconverted I and Q signal components in order to perform differential decoding as an intrinsic part of DPSK demodulation.

The differential encoding scheme depends on whether the modulation format is to be BPSK or QPSK. For DBPSK, the encoding algorithm is straightforward: output bit(k) equals input bit(k) $\oplus$ output bit(k–1), where $\oplus$ represents the logical XOR function. For DQPSK, however, the differential encoding algorithm, as shown in Table 2, is more complex since there are now sixteen possible new states depending on the four possible previous output states and four possible new input states.

Table 2. QPSK Differential Encoder Sequence

New Input		**Previously Encoded OUT(I,Q)$_{K-1}$**							
IN(I,Q)$_K$		**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**
0	0	0	0	0	1	1	1	1	0
0	1	0	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0	0	1
1	0	1	0	0	0	0	1	1	1
Newly Encoded OUT (I,Q)K									

Transmitter PN Code Generation

When the Z87200 is used for burst signal operation, each burst is preceded by an Acquisition/Preamble symbol to facilitate acquisition. This Acquisition/Preamble symbol is automatically generated by the Z87200's transmitter before information data symbols are accepted for transmission. Two separate and independent PN codes may be employed: one for spreading the Acquisition/Preamble symbol, and one for the subsequent information data symbols. As a result, a much higher processing gain may be used for signal acquisition than for signal tracking in order to improve burst acquisition performance.

The Transmitter Acquisition/Preamble and Transmitter Data Symbol PN code lengths are completely independent of each other and can be up to 64 chips long. Transmit PN codes are programmed in the Z87200 as binary code values. The number of Transmitter Chips per Acquisition/Preamble Symbol is set by the value stored in bits 5-0 of address 43_H, and the Transmitter Acquisition/Preamble Symbol Code coefficient values are stored in addresses 44_H to $4B_H$. The number of Transmitter Chips per Data Symbol is set by the data stored in address 42_H, and the Transmitter Data Symbol Code coefficient values are stored in addresses $4C_H$ to 53_H.

A rising edge of the MTXEN input or of bit 1 of address 37_H causes the Z87200 to begin the transmit sequence by transmitting a single symbol using the Acquisition/Preamble PN code. The completion of transmission of the Acquisition/Preamble symbol is indicated with TXACQPLS, while the ongoing transmission of data symbols is signaled with TXTRKPLS. Data bits to be transmitted after the Acquisition/Preamble symbol are requested with TXBITPLS, where a single pulse requests data in BPSK mode and two pulses request data in QPSK mode. The user data symbols are then PN modulated using the Transmitter Data Symbol PN code.

The PN spreading codes are XORed with the data bits (in BPSK mode) or bit pairs (in QPSK mode) to transmit one complete code sequence for every Acquisition/Preamble and data symbol at all times. The resulting spread I and Q channel signals are brought out as the TXIOUT and TXQOUT signals for use by an external modulator and are also fed into the Z87200's internal on-chip modulator. In BPSK mode, only TXIOUT is used by the Z87200's modulator. If an external QPSK modulator is used, the carrier should be modulated as shown in Table 3 to be compatible with the Z87200 receiver.

Table 3. DQPSK Differential Encoder Sequence

I, Q BIts		Signal Quadrant	Quadrant Diagram	
0	0	First	2nd	1st
1	0	Second	3rd	4th
1	1	Third		
0	1	Fourth		

BPSK/QPSK Modulator

The Z87200 incorporates an on-chip BPSK/QPSK modulator which modulates the encoded and spread transmit signal with the sine and cosine outputs of the Z87200's NCO to generate a digitized I.F. output signal, $TXIFOUT_{7-0}$. Since the NCO operates at a rate defined by RXIFCLK, the BPSK/QPSK modulator output is also generated at this sampling rate, and, consequently, TXIFCLK must be held common with RXIFCLK to operate the Z87200's BPSK/QPSK Modulator. The digital modulator output signal can then be fed into an external 8-bit DAC (operating at RXIFCLK) to generate an analog I.F. transmit signal, where the chosen I.F. is the Z87200's programmed NCO frequency or one of its aliases with respect to the output sampling rate, RXIFCLK. Please note that operation of the BPSK/QPSK modulator is only specified to 20 MHz; that is, if RXIFCLK/TXIFCLK is greater than 20 MHz in the system design, it is recommended that the baseband transmit outputs of the Z87200 be used with an external BPSK/QPSK modulator.

When the Z87200 is set to transmit in BPSK mode (by setting bit 0 of address 40_H high), identical signals are applied to both the I and Q channels of the modulator so that the modulated output signal occupies only the first and third quadrants of the signal space defined in Note that the modulator itself cannot generate $\pi/4$ QPSK signals, but the Z87200 can receive such signals and can be used with an external modulator for their transmission.

FUNCTIONAL BLOCKS (Continued)

Frequency Control Register and NCO

The Z87200 incorporates a Numerically Controlled Oscillator (NCO) to synthesize a local oscillator signal for both the transmitter's modulator and receiver's downconverter. The NCO is clocked by the master receiver clock signal, RXIFCLK, and generates quadrature outputs with 32-bit frequency resolution. The NCO frequency is controlled by the value stored in the 32-bit Frequency Control Register, occupying 4 bytes at addresses 03_H to 06_H. To avoid destructive in-band aliasing, the NCO should not be programmed to be greater than 50% of RXIFCLK. As desired by the user, the output of the Z87200 receiver's Loop Filter can then be added or subtracted to adjust the NCO's frequency control word and create a closed-loop frequency tracking loop. If the receiver is disabled, either manually or automatically at the end of a burst, the Loop Filter output correcting the NCO's Frequency Control Word is disabled. When simultaneously operating both the transmitter and receiver, however, the receiver's frequency tracking loop affects the NCO signals to both the receive and transmit sides, a feature which can either be used to advantage in the overall system design or must be compensated in the programming of the Z87200 or in the system design.

Downconverter

The Z87200 incorporates a Quadrature (Single Sideband) Downconverter which digitally downconverts the sampled and digitized receive I.F. signal to baseband. Use of the Loop Filter and the NCO's built-in frequency tracking loop permits the received signal to be accurately downconverted to baseband.

The Downconverter includes a complex multiplier in which the 8-bit receiver input signal is multiplied by the sine and cosine signals generated by the NCO. In Quadrature Sampling Mode, two ADCs provide quadrature (complex) inputs I_{IN} and Q_{IN}, while, in Direct I.F. Sampling Mode, a single ADC provides I_{IN} as a real input. The input signals can be accepted in either two's complement or offset binary formats according to the setting of bit 3 of address 01_H. In Direct I.F. Sampling Mode, the unused RXQIN Q channel input (Q_{IN}) should be held to "zero" according to the ADC input format selected. The outputs of the Downconverter's complex multiplier are then:

$$I_{OUT} = I_{IN} \cdot \cos(\omega t) - Q_{IN} \cdot \sin(\omega t)$$

$$Q_{OUT} = I_{IN} \cdot \sin(\omega t) + Q_{IN} \cdot \cos(\omega t)$$

$$\text{where } \omega = 2\pi f_{nco}$$

These outputs are fed into the I and Q channel Integrate and Dump Filters. The Integrate and Dump Filters allow the samples from the complex multiplier (at the I.F. sampling rate, the frequency of RXIFCLK) to be integrated over a number of sample periods. The dump rate of these filters (the baseband sampling rate) can be controlled either by an internally generated dump clock or by an external input signal (RXMSMPL) according to the setting of bit 0 of address 01_H. Note that, while the receiver will extract exact PN and symbol timing information from the received signal, the baseband sampling rate must be twice the nominal PN chip rate for proper receiver operation and less than or equal to one-half the frequency of RXIFCLK. If twice the PN chip rate is a convenient integer sub-multiple of RXIFCLK, then an internal clock can be derived by frequency dividing RXIFCLK according to the divisor stored in bits 5-0 of address 02_H; otherwise, an external baseband sampling clock provided by RXMSMPL must be used.

The I.F. sampling rate, the baseband sampling rate, and the input signal levels determine the magnitudes of the Integrate and Dump Filters' accumulator outputs, and a programmable viewport is provided at the outputs of the Integrate and Dump Filters to select the appropriate output bits as the 3-bit inputs to the PN Matched Filter. The viewport circuitry here and elsewhere within the Z87200's receiver is designed with saturation protection so that extreme values above or below the selected range are limited to the correct maximum or minimum value for the selected viewport range. Both viewports for the I and Q channels of the Integrate and Dump Filters are controlled by the values stored in bits 7-4 of address 01_H.

Receiver PN Code Register and PN Matched Filter

As discussed for the Z87200 transmitter, the Z87200 receiver is designed for burst signal operation in which each burst begins with a single Acquisition/Preamble symbol and is then followed by data symbols for information transmittal. Complementing operation of the Z87200's transmitter, two separate and independent PN codes may be employed in the receiver's PN Matched Filter, one for despreading the Acquisition/Preamble symbol, and one for the information data symbols. The code lengths are completely independent of each other and can be each up to 64 chips long. A block diagram of the PN Matched Filter is shown in Figure 3.

The Z87200 contains a fully programmable 64-tap complex (dual I and Q channel) PN Matched Filter with coefficients which can be set to ±1 or zero according to the contents of either the Acquisition/Preamble or Data Symbol Code Coefficient Registers. By setting the coefficients of the end taps of the filter to zero, the effective length of the filter can be reduced for use with PN codes shorter than 64 bits. Power consumption may also be reduced by turning off those blocks of 7 taps for which all the coefficients are zero, using bits 6-0 of address 39H. Each ternary coefficient is stored as a 2-bit number so that a PN code of length N is stored as N 2-bit non-zero PN coefficients. Note that, as a convention, throughout this document the first PN Matched Filter tap encountered by the signal as it enters the I and Q channel tapped delay lines is referred to as “Tap 0.” Tap 63 is then the last tap of the PN Matched Filter.

The start of each burst is expected to be a single symbol PN-spread by the Acquisition/Preamble code. The receiver section of the Z87200 is automatically configured into acquisition mode so that the Matched Filter Acquisition/Preamble Coefficients stored in addresses 07_H to 16_H are used to despread the received signal. Provided that this symbol is successfully detected, the receiver will automatically switch from acquisition mode, and the Matched Filter Data Symbol Coefficients stored in addresses 17_H to 26_H will then be used to despread subsequent symbols.

To allow the system to sample the incoming signal asynchronously (at the I.F. sampling rate) with respect to the PN spreading rate, the PN Matched Filter is designed to operate with two signal samples (at the baseband sampling rate) per chip. A front end processor (FEP) operating on both the I and Q channels averages the incoming data over each chip period by adding each incoming baseband sample to the previous one:

$$FEP_{OUT} = FEP_{IN} (1 + z^{-1})$$

After the addition, the output of the FEP is rounded to a 3-bit offset 2’s complement word with an effective range of ±3.5 such that the rounding process does not introduce any bias to the data. The FEP can be disabled by setting bit 0 of address 27_H to 1, but for normal operation the FEP should be enabled.

The PN Matched Filter computes the cross-correlation between the I and Q channel signals and the locally stored PN code coefficients at the baseband sampling rate, which is twice per chip. The 3-bit signals from each tap in the PN Matched Filter are multiplied by the corresponding coefficient in two parallel tapped delay lines. Each delay line consists of 64 multipliers which multiply the delayed 3-bit signals by zero or ±1 according to the value of the tap coefficient. The products from the I and Q tapped delay lines are added together in the I and Q Adders to form the sums of the products, representing the complex cross-correlation factor. The correlation I and Q outputs are thus:

$$Output_{(I, Q)} = \sum_{n=0}^{n=63} Data_{n(I, Q)} * Coefficient_{n(I, Q)}$$

These I and Q channel PN Matched Filter outputs are 10-bit signals, with I and Q channel programmable viewports provided to select the appropriate output bits as the 8-bit inputs to the Power Detector and DPSK Demodulator blocks. Both I and Q channel viewports are jointly controlled by the data stored in bits 1-0 of address 28_H and are saturation protected.

Two power saving methods are used in the PN Matched Filter of the Z87200. As discussed previously, the first method allows power to be shut off in the unused taps of the PN Matched Filter when the filter length is configured to be less than 64 taps. The second method is a proprietary technique that (transparently to the user) shuts down the entire PN Matched Filter during portions of each symbol period.

FUNCTIONAL BLOCKS (Continued)

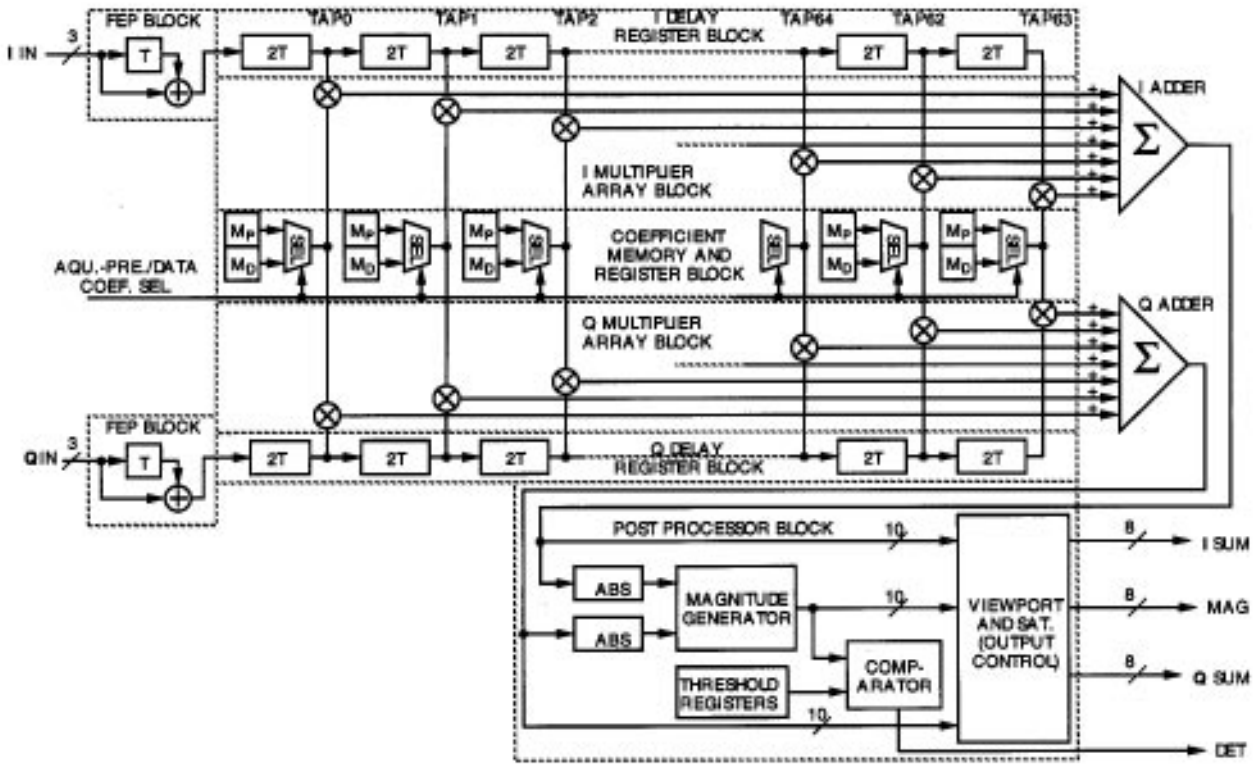


Figure 7. PN Matched Filter

Power Detector

The complex output of the PN Matched Filter is fed into a Power Detector which, for every cycle of the internal baseband sampling clock, computes the magnitude of the vector of the I and Q channel correlation sums,

$$\sqrt{I^2(K)+Q^2(k)}$$

, where the magnitude is approximated as

$$\text{Max}\{\text{Abs}(I),\text{Abs}(Q)\} + 1/2\ \text{Min}\{\text{Abs}(I), \text{Abs}(Q)\}.$$

This 10-bit value represents the power level of the correlated signal during each chip period and is used in the Symbol Tracking Processor.

Symbol Tracking Processor

The output of the Power Detector Block represents the signal power during each chip period. Ideally, this output will have a high peak value once per symbol (that is, once per PN code cycle) when the code sequence of the received signal in the PN Matched Filter is the same as (and is aligned in time with) the reference PN code used in the PN Matched Filter. At that instant, the I and Q channel outputs of the PN Matched Filter are, theoretically, the optimally despread I and Q symbols.

To detect this maximum correlation in each symbol period, the signal power value is compared against a 10-bit user-programmable threshold value. A symbol clock pulse is generated each time the power value exceeds the threshold value to indicate a symbol detect. Since the Acquisition/Preamble symbol and subsequent data symbols can have different PN codes with different peak correlation values (which depend on the PN code length and code properties), the Z87200 is equipped with two separate threshold registers to store the Acquisition/Preamble Threshold value (stored in addresses 29_H and $2A_H$) and the Data Symbol Threshold value (stored in addresses $2B_H$ and $2C_H$). The device will automatically use the appropriate value depending on whether it is in acquisition mode or not.

Since spread-spectrum receivers are frequently designed to operate under extremely adverse signal-to-noise ratio conditions, the Z87200 is equipped with a "flywheel circuit" to enhance the operation of the symbol tracking function by introducing memory to the PN Matched Filter operation. This circuit is designed to ignore false detects at inappropriate times in each symbol period and to insert a symbol clock pulse at the appropriate time if the symbol detection is missed. The flywheel circuit operates by its *a priori* knowledge of when the next detect pulse is expected. *A priori*, the expected pulse will occur one symbol period after the last correctly detected one, and a window of ±1 baseband sample time is therefore used to gate the detect pulse. Any detects generated outside this time window are ignored, while a symbol detect pulse will be inserted into the symbol clock stream if the power level does not exceed the threshold within the window, corresponding to a missed detect. An inserted symbol detect signal will be generated precisely one symbol after the last valid detect, the nominal symbol length being determined by the value of Rx Chips Per Data Symbol stored in address $2D_H$.

The cross-correlation characteristics of a noisy received signal with the noise-free local PN code used in the Z87200's PN Matched Filter may result in "smearing" of the peak power value over adjacent chip periods. Such smearing can result in two or three consecutive power values (typically, the on-time and one-sample early and late values) exceeding the threshold. A maximum power selector circuit is incorporated in the Z87200 to choose the highest of any three consecutive power levels each time this occurs, thereby enhancing the probability that the optimum symbol timing will be chosen in such cases. If desired, this function can be disabled by setting bit 3 of address 30_H high.

The Z87200 also includes a circuit to keep track of missed detects; that is, those cases where no peak power level exceeds the set threshold. An excessively high rate of missed detects is an indication of poor signal quality and can be used to abort the reception of a burst of data. The number of symbols expected in each receive burst, up to a maximum of 65,533, is stored in addresses $2E_H$ and 30_H. A counter is used to count the number of missed detects in each burst, and the system can be configured to automatically abort a burst and return to acquisition mode if this number exceeds the Missed Detects per Burst Threshold value stored in address $2F_H$. Under normal operating conditions, the Z87200 will automatically return to acquisition mode when the number of symbols processed in the burst is equal to the value of the data stored in address $2E_H$ and 30_H. To permit the processing of longer bursts or continuous data, this function can be disabled by setting bit 6 of address 30_H high.

Differential Demodulator

Both DPSK demodulation and carrier discrimination are supported in the Z87200 receiver by the calculation of "Dot" and "Cross" products using the despread I and Q channel information generated by the PN Matched Filter for the current and previous symbols. A block diagram of the DPSK Demodulator's I and Q channel processing is shown in Let I_k and Q_k represent the I and Q channel outputs, respectively, for the k^{th} symbol. The Dot and Cross products can then be defined as:

$$\text{Dot}(k) = I_k I_{k-1} + Q_k Q_{k-1}; \text{ and,}$$

$$\text{Cross}(k) = Q_k I_{k-1} - I_k Q_{k-1}.$$

Examination of these products in the complex plane reveals that the Dot and Cross products are the real and imaginary results, respectively, of complex multiplication of the current and previous symbols. The Dot product alone thus allows determination of the phase shift between successive BPSK symbols, while the Dot and Cross products together allow determination of the integer number of π/2 phase shifts between successive QPSK symbols. Differential encoding of the source data implies that an absolute phase reference is not required, and thus knowledge of the phase shift between successive symbols derived from the Dot and Cross products unambiguously permits correct demodulation.

Implementation of this approach is simplified if the polarities (the signs) alone of the Dot and Cross products provide the information required to make the correct symbol decision. For BPSK and π/4 QPSK signals, no modifications are needed: in BPSK, the sign of the Dot product fully captures the signal constellation, while, in π/4 QPSK, the signal constellation intrinsically includes the phase rotation needed to align the decision boundaries with the four possible combinations of the Dot and Cross product polarities. For QPSK signals, a fixed phase rotation of π/4 (45°) is introduced in the DPSK Demodulator to the previous symbol to simplify the decision algorithm. Rotation of the previous symbol is controlled by the settings of bits 0 and 1 of address 33_H, allowing the previous symbol to be rotated by 0° or ±45°. As noted, for BPSK or π/4 QPSK signals, a rotation of 0° should be programmed, but, for QPSK signals,

FUNCTIONAL BLOCKS (Continued)

a –45° signal rotation must be programmed to optimize the constellation boundaries in the comparison process between successive symbols. Note also that introduction of a ±45° rotation introduces a scaling factor of 1/√2 to the signal level in the system as discussed in Theory of Operation, where this factor should be taken into account when calculating optimum signal levels and viewport settings after the DPSK Demodulator

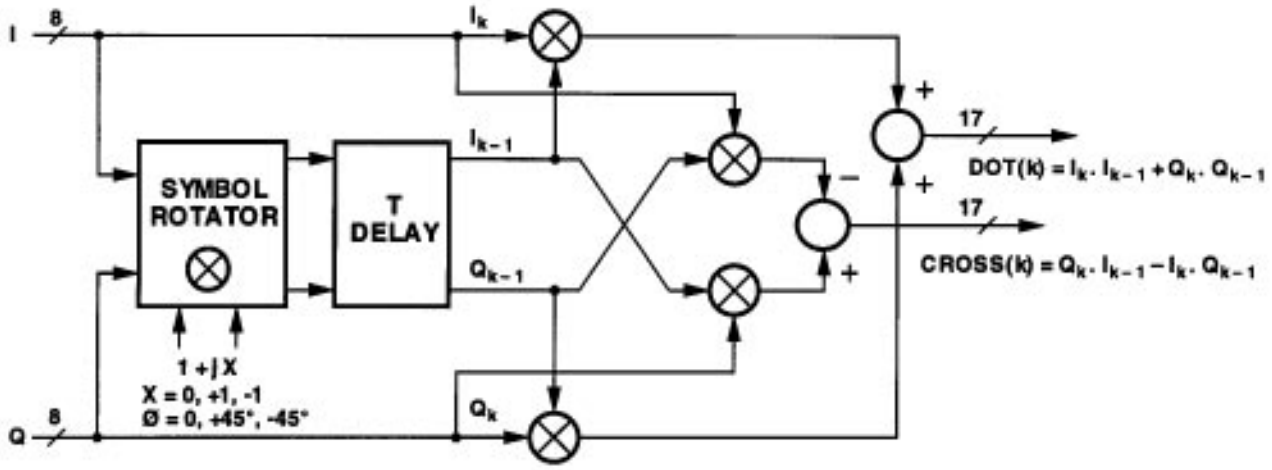


Figure 8. DPSK Demodulator I and Q Channel Processing

Frequency Discriminator and Loop Filter

The Frequency Discriminator uses the Dot and Cross products discussed above to generate the AFC signal for the frequency acquisition and tracking loop, as illustrated in The specific algorithm used depends on the signal modulation type and is controlled by the setting of bit 2 of address 33_H. When bit 2 is set low, the Frequency Discriminator circuit is in BPSK mode and the following algorithm is used to compute the Frequency Discriminator (FD) function:

FD = Cross x Sign[Dot],

where Sign[.] represents the polarity of the argument. When bit 2 is set high, the discriminator circuitry is in QPSK mode and the carrier discriminator function is instead calculated as:

FD = (Cross x Sign[Dot]) – (Dot x Sign[Cross]).

In both cases, the Frequency Discriminator function provides an error signal that reflects the change in phase between successive symbols. With the symbol period known, the error signal can equivalently be seen as a frequency error signal. As a practical matter, the computation of the Frequency Discriminator function results in a 17-bit signal, and a programmable saturation protected viewport is provided to select the desired output bits as the 8-bit input to the Loop Filter Block. The viewport is controlled by the value stored in bits 7-4 of address 33_H.

The Loop Filter is implemented with a direct gain (K1) path and an integrated or accumulated (K2) path to filter the Frequency Discriminator error signal and correct the frequency tracking of the Downconverter. The order of the Loop Filter transfer function can be set by enabling or disabling the K1 and K2 paths, and the coefficient values can be adjusted in powers of 2 from 2^0 to 2^{21}. The Loop Filter transfer function is:

Transfer Fn. = K1 + 1/4 K2

The factor of 1/4 results from truncation of the 2 LSBs of the signal in the integrator path of the loop so that, when added to the signal in the direct path, the LSBs of the signals are aligned. The coefficients K1 and K2 are defined by the data stored in bits 4-0 of addresses 35_H and 34_H, respectively. In addition, bit 5 of addresses 35_H and 34_H control whether the K1 and K2 paths, respectively, are enabled. These parameters thus give the user full control of the Loop Filter characteristics.

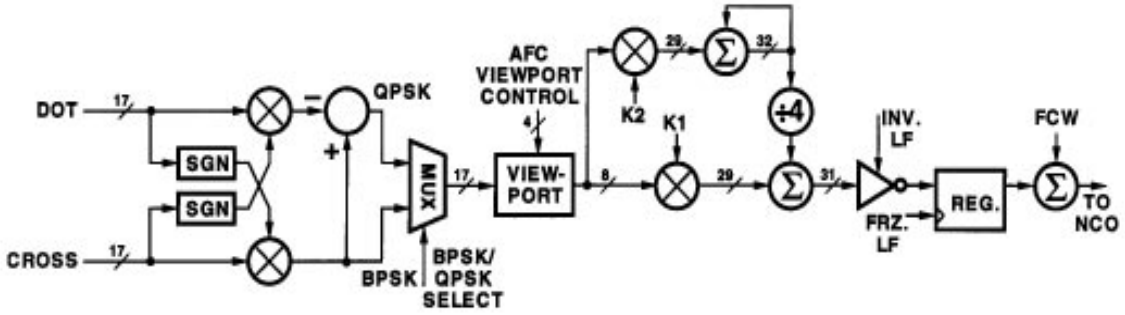


Figure 9. Frequency Discriminator and Loop Filter Detail

$RXIIN_{7-0}$ (Pins 91-98)

Receiver In-Phase Input. RXIIN is an 8-bit input port for in-phase data from external A/D converters. Data may be received in either two's complement or offset binary format as selected by bit 3 of address 01_H. The sampling rate of the RXIIN signals (the I.F. sampling rate of the A/Ds) may be independent of the baseband sampling rate (the Downconverter integrate and dump rate) and the PN chip rate, but must be equal to RXIFCLK and at least two times greater than the baseband sampling rate. Since the baseband sampling rate must be set at twice the PN chip rate, the I.F. sampling rate must thus be at least four times the PN chip rate. Data on the pins is latched and processed by RXIFCLK.

$RXQIN_{7-0}$ (Pins 2-9)

Receiver Quadrature-Phase Input. RXQIN is an 8-bit input port for quadrature-phase data from external A/D converters. Data may be received in either two's complement or offset binary format as selected by bit 3 of address 01_H. As with RXIIN, the sampling rate of the RXQIN signals may be independent of the baseband sampling and PN chip rates in the receiver, but must be at least two times greater than the baseband sample rate (or, equivalently, at least four times greater than the PN chip rate). Data on the pins is latched and processed by RXIFCLK.

FUNCTIONAL BLOCKS (Continued)

Note that if the Z87200 is to be used in Direct I.F. Sampling Mode, then the I.F. signal should be input to the RXIIN input port only. RXQIN must then be held to arithmetic zero according to the chosen ADC format as selected by bit 3 of address 01_H. In other words, to support Direct I.F. Sampling, RXQIN must be tied to a value of 127 or 128 if offset binary input format has been selected or to a value of 0 if two's complement input format has been selected.

RXMSMPL (Pin 84)
Receiver Manual Sample Clock. RXMSMPL enables the user to externally generate (independent of the I.F. sampling clock, RXIFCLK) the baseband sampling clock used for all processing after the digital downconverter, including the dump rate of the Integrate and Dump filters. This feature is useful in cases where a specific baseband sample rate is required that may not be derived by the internal sample rate timing generator which generates clock signals at integer sub-multiples of RXIFCLK. The signal is internally synchronized to RXIFCLK to avoid intrinsic race or hazard timing conditions. There must be at least two cycles of RXIFCLK to every cycle of RXMSMPL, and RXMSMPL should be set to twice the nominal receive PN chip rate.

When bit 0 of address 01_H is set high, a rising edge on RXMSMPL will initiate a baseband sampling clock pulse to the Integrate and Dump filters and subsequent circuitry (e.g., PN Matched Filter, DPSK Demodulator, Power Estimator, etc.). The rising edge of RXMSMPL is synchronized internally so that, on the second rising edge of RXIFCLK that follows the rising edge of RXMSMPL, a pulse is internally generated that clocks the circuitry that follows. On the third rising RXIFCLK edge, the contents of the Integrate and Dump Filters of the Downconverter are transferred to the PN Matched Filter. The extra one RXIFCLK delay before transfer of the contents of the filters enables the internally generated baseband sampling clock to be free of race conditions at the interface between the Downconverter and PN Matched Filter.

RXMDET (Pin 88)
Receiver Manual Detect. RXMDET enables the user to externally generate symbol timing, bypassing and overriding the internal symbol power estimation and tracking circuitry. This function may be useful when the dynamic characteristics of the transmission environment require unusual adjustments to the symbol timing.

When bit 0 of address 30_H is set high (Manual Detect Enable) and when bit 0 of address 31_H is set low, a rising edge of RXMDET will generate a symbol correlation detect pulse. The function can also be performed by means of bit 0 of address 31_H. The RXMDET input and bit 0 of address 31_H are logically ORed together so that, when either one is held low, a rising edge on the other triggers the manual detect function. The rising edge of RXMDET is synchronized internally so that, on the second rising edge of the baseband sampling clock that follows the rising edge of RXMDET, the correlated outputs of the PN Matched Filter I and Q channels will be transferred to the DPSK demodulator.

RXMABRT (Pin 87)
Receiver Manual Abort. RXMABRT enables the user to manually force the Z87200 to cease reception of the current burst of data symbols and prepare for acquisition of a new burst. This function can be used to reset the receiver and prepare to receive a priority transmission signal under precise timing control, giving the user the ability to control the current status of the receiver for reasons of priority, signal integrity, etc.

When bit 0 of address 32_H is set low, a rising edge on RXMABRT will execute the abort function. The function can also be performed under microprocessor control by means of bit 0 of address 32_H. The RXMABRT input and bit 0 of address 32_H are logically ORed together so that, when either one is held low, a rising edge on the other triggers the abort function. The second rising edge of the baseband sampling clock that follows a rising edge of RXMABRT will execute the abort and also clear the symbols-per-burst, samples-per-symbol, and missed-detects-per-burst counters. The counters will be reactivated on the detection of the next burst preamble or by a manual detect signal.

RXIFCLK (Pin 12)
Receiver I.F. Clock. RXIFCLK is the master clock of the NCO and all the receiver blocks. All clocks in the receiver section and the NCO, internal or external, are generated or synchronized internally to the rising edge of RXIFCLK. The frequency of RXIFCLK must be at least four times the PN chip rate of the received signal. When bit 0 of address 01_H is set low, the baseband sampling clock, required to be at twice the nominal PN chip rate, will be derived from RXIFCLK according to the setting of bits 5-0 of address 02_H.

MNCOEN (Pin 86)
Manual NCO Enable. MNCOEN allows the power consumed by the operation of the NCO circuitry to be minimized when the Z87200 is not receiving and not transmitting data. The NCO can also be disabled while the Z87200 is transmitting as long as the Z87200's on-chip BPSK/QPSK modulator is not being used. With the instantaneous acquisition properties of the PN Matched Filter, it is often desirable to shut down the receiver circuitry to reduce power consumption, resuming reception periodically until an Acquisition/Preamble symbol is acquired. Setting MNCOEN low holds the NCO in a reset state; setting MNCOEN high then reactivates the NCO, where it is necessary to then reload the frequency control word into the

NCO. Note that MNCOEN operates independently of MTXEN and MRXEN, where those pins have similar control over the transmit and receive circuitry, respectively.

MNCOEN performs the same function as bit 0 of address 37_H, and these two signals are logically ORed together to form the overall control function. When bit 0 of address 37_H is set low, MNCOEN controls the activity of the NCO circuitry; when MNCOEN is set low, bit 0 of address 37_H controls the activity of the NCO circuitry. When either bit 0 or MNCOEN (whichever is in control, as defined above) goes low, a reset sequence occurs on the following RXIFCLK cycle to effectively disable all of the NCO circuitry, although the user programmable control registers are not affected by this power down sequence.

Upon reactivation (when either MNCOEN or bit 0 of address 37_H return high), the NCO must be reloaded with frequency control information either by means of the MFLD input or by writing 01_H into address 00_H.

MTXEN (Pin 17)

Manual Transmitter Enable. A rising edge on MTXEN causes the transmit sequence to begin, where the Z87200 first transmits a single Acquisition/Preamble symbol followed by data symbols. MTXEN should be set low after the last symbol has been transmitted. When MTXEN is set low, power consumption of the transmitter circuit is minimized. MTXEN operates independently of MRXEN and MNCOEN, where these signals have similar control over the receive and NCO circuitry, respectively.

MTXEN performs the same function as bit 1 of address 37_H. and these two signals are logically ORed together to form the overall control function. When bit 1 of address 37_H is set low, MTXEN controls the activity of the transmitter circuitry, and, when MTXEN is set low, bit 1 of address 37H controls the activity of the transmitter circuitry. A rising edge on either MTXEN or bit 1 (whichever is in control, as defined above) initiates a transmit sequence. A falling edge initiates a reset sequence on the following TXIFCLK cycle to disable all of the transmitter data path, although the user programmable control registers are not affected by the power down sequence.

MRXEN (Pin 10)

Manual Receiver Enable. MRXEN allows power consumption of the Z87200 receiver circuitry to be minimized when the device is not receiving. With the instantaneous acquisition properties of the PN Matched Filter, it is often desirable to shut down the receiver circuitry to reduce power consumption, resuming reception periodically until an Acquisition/Preamble symbol is acquired. Setting MRXEN low reduces the power consumption substantially. When MRXEN is set high, the receiver will automatically power up in acquisition mode regardless of its prior state when it was powered down. MRXEN operates independently of MTXEN and MNCOEN, where these signals have similar control over the transmit and NCO circuitry, respectively.

MRXEN performs the same function as bit 2 of address 37_H, and these two signals are logically ORed together to form the overall control function. When bit 2 of address 37_H is set low, MRXEN controls the activity of the receiver circuitry and, when MRXEN is set low, bit 2 of address 37_H controls the activity of the receiver circuitry. When either MRXEN or bit 2 (whichever is in control, as defined above) goes low, a reset sequence begins on the following RXIFCLK cycle and continues through a total of six RXIFCLK cycles to virtually disable all of the receiver data paths. The user-programmable control registers are not affected by the power-down sequence, with the exception of $RXTEST_{7-0}$ Function Select (address 38_H), which is reset to 0. If the $RXTEST_{7-0}$ bus is being used to read any function other than the PN Matched Filter I and Q inputs, the value required must be rewritten after re-enabling the receiver.

TXIN (Pin 18)

Transmit Input. TXIN supports input of the information data to be transmitted by the Z87200. In BPSK mode, the transmitter requires one bit per symbol period; in QPSK mode, two bits are required per symbol period.

To initiate and enable transmission of the data, the user must raise MTXEN high. Data for transmission is requested with TXBITPLS, where one or two pulses per symbol are generated depending on whether the device is in BPSK or QPSK mode as set by bit 0 of address 40_H. To allow monitoring of the state of the transmitter, the Z87200 will pulse TXACQPLS after the initial Acquisition/Preamble symbol is transmitted; the transmission of each subsequent symbol is indicated by pulses of TXTRKPLS.

If programmed for BPSK mode, data is requested by the Z87200 by a rising edge of output signal TXBITPLS, where TKBITPLS is generated once per symbol, one chip period before the end of the current symbol. At the end of the symbol duration, the TXIN data is latched into the device. TXBITPLS falls low immediately following the rising edge of TXIFCLK, which latches the TXIN value, and is generated repeatedly at the symbol rate as long as the input signal MTXEN remains high.

In QPSK mode, data is requested by the Z87200 by a rising edge of output signal TXBITPLS, where this signal is generated twice per symbol, first one chip period before the middle of the symbol and then one chip period before the end of the symbol. TXBITPLS requests the data exactly one chip cycle before latching the TXIN data into the device. TXBITPLS falls low immediately following the rising edge of TXIFCLK, which latches the TXIN value.

FUNCTIONAL BLOCKS (Continued)

TXMCHP (Pin 19)

Transmit Manual Chip Pulse. TXMCHP enables the user to provide the PN chip rate clock pulses from an external source. This feature is useful in cases where a specific chip rate is required that cannot be derived by the internal clock generator which generates clocks of integer submultiples of TXIFCLK. The signal is internally synchronized to TXIFCLK to avoid intrinsic race or hazard timing conditions.

When bit 2 of address 40_H is set high, a rising edge on TXMCHP will generate the chip clock to the differential encoder and the following circuitry (Acquisition/Preamble and Data Symbol PN spreaders, etc.). The rising edge of TXMCHP is synchronized internally so that, on the third rising edge of TXIFCLK following the rising edge of TXMCHP, the PN code combined with the differentially encoded signal will change, generating the next chip.

TXIFCLK (Pin 14)

Transmitter I.F. Clock. TXIFCLK is the master clock of the transmitter. All transmitter clocks, internal or external, are generated or synchronized internally to the rising edge of TXIFCLK. The rate of TXIFCLK must be at least twice the transmit PN chip rate. It may be convenient to use the same external signal for both TXIFCLK and RXIFCLK, in which case the frequency of TXIFCLK will be at least four times the PN chip rate as required for RXIFCLK. Moreover, if the Z87200's on-chip BPSK/QPSK Modulator is to be used, TXIFCLK and RXIFCLK must be identical and should not exceed 20 MHz.

MFLD (Pin 85)

Manual Frequency Load. MFLD is used to load a frequency control value into the NCO. The NCO may be loaded in various ways, but MFLD provides a synchronized external method of updating the NCO, while the other methods involve setting bit 0 of address 00H or using the programmable loop filter timing circuitry. MFLD is internally synchronized to RXIFCLK to avoid internal race or hazard timing conditions.

The MFLD input and bit 0 of address 00H are logically ORed together so that, when either one is held low, a rising edge on the other triggers the frequency load function manually. The rising edge of MFLD is synchronized internally so that, on the sixth following rising edge of RXIFCLK, the frequency control word is completely registered into the NCO accumulator. The frequency load command must not be repeated until the six RXIFCLK cycle delay is completed.

/WR (Pin 28)

Write Bar. /WR is used to latch user-configurable information into the control registers. It is important to note that the control registers are transparent latches while /WR is set low. The information will be latched when /WR returns high. $DATA_{7-0}$ and $ADDR_{6-0}$ should be stable while /WR is set low in order to avoid undesirable effects.

$DATA_{7-0}$ (Pins 20-27)

Data Bus. $DATA_{7-0}$ is an 8-bit microprocessor interface bus that provides access to all internal control register inputs for programming. $DATA_{7-0}$ is used in conjunction with the $ADDR_{6-0}$ and /WR signals to set the values of the control registers.

$ADDR_{6-0}$ (Pins 32-38)

Address Bus. $ADDR_{6-0}$ is a 7-bit address bus that selects the control register location into which the information provided on the $DATA_{7-0}$ bus will be written. $ADDR_{6-0}$ is used in conjunction with /WR and $DATA_{7-0}$ to write the information into the registers.

/CSEL (Pin 29)

Chip Select Bar. /CSEL is provided to enable or disable the microprocessor operation of the Z87200. When /CSEL is set high, the $ADDR_{6-0}$ and /WR become disabled and have no effect on the device. When /CSEL is set low, the device is in its normal mode of operation and $ADDR_{6-0}$ and /WR are active.

/OEN (Pin 49)

Output Enable Bar. /OEN is provided to enable or disable the $RXTEST_{7-0}$ output bus. When /OEN is set high, the $RXTEST_{7-0}$ bus will have a high impedance, allowing it to be connected to other busses, such as $DATA_{7-0}$. When /OEN is set low, the $RXTEST_{7-0}$ bus will be active, allowing the RXTEST function selected to be accessed.

/RESET (Pin 16)

Reset Bar. /RESET is the master reset of the Z87200, clearing the control registers as well as the contents within the receiver, transmitter, and NCO data paths when it is set low. Setting /RESET high enables operation of the circuitry.

OUTPUT SIGNALS

TXIOUT (Pin 77)
Transmitter In-Phase Output. TXIOUT is the in-phase output transmission signal that has been differentially encoded and PN spread. TXIOUT changes on the rising edge of TXIFCLK following the falling edge of TXCHPPLS.

TXQOUT (Pin 76)
Transmitter Quadrature-Phase Output. TXQOUT is the quadrature-phase output transmission signal that has been differentially encoded and PN spread. TXQOUT changes on the rising edge of TXIFCLK following the falling edge of TXCHPPLS.

$TXIFOUT_{7-0}$ (Pins 66-73)
Transmitter I.F. Output. $TXIFOUT_{7-0}$ is the modulated transmit output signal from the on-chip BPSK/QPSK modulator. The signal is composed of the sum of the modulated TXIOUT and TXQOUT signals, modulated by the NCO cosine and sine outputs, respectively. Since the modulator is driven by the Z87200's NCO, $TXIFOUT_{7-0}$ changes on the rising edges of RXIFCLK, and operation of the BPSK/QPSK modulator requires that RXIFCLK and TXIFCLK be identical and their common frequency not exceed 20 MHz. $TXIFOUT_{7-0}$ may be in either two's complement or offset binary format according to the setting of bit 1 of address 40_H.

TXACQPLS (Pin 60)
Transmitter Acquisition Pulse. TXACQPLS is an output signal generated at the final chip of the Acquisition/Preamble symbol. The Acquisition/Preamble symbol is generated automatically by the Z87200 upon user command (either via bit 1 of address 37_H or MTXEN input) and immediately precedes transmission of user data. TXACQPLS is then provided to the user to indicate when the final chip of the Acquisition/Preamble symbol is being transmitted.

TXBITPLS (Pin 63)
Transmitter Bit Pulse. TXBITPLS is an output signal used to support transmission timing of user data for either BPSK or QPSK modes, as programmed by bit 0 of 40_H.

In BPSK mode, user-provided data is requested by the Z87200 by a rising edge of TXBITPLS once per symbol. TXBITPLS requests the data one chip period before the TXIN data is latched into the device, and TXBITPLS falls low immediately following the rising edge of TXIFCLK, where TXIFCLK latches the TXIN value.

In QPSK mode, user-provided data is requested by the Z87200 by a rising edge of output signal TXBITPLS which occurs twice per symbol, first one chip period before the middle of the symbol and then one chip period before the end of the symbol. TXBITPLS requests the data exactly one chip cycle period before the TXIN data is latched into the device. TXBITPLS falls low immediately following the rising edge of TXIFCLK, where TXIFCLK latches the TXIN value.

In both BPSK and QPSK modes, the data must be valid on the second rising edge of TXIFCLK after the rising edge of TXBITPLS.

TXCHPPLS (Pin 62)
Transmitter Chip Pulse. TXCHPPLS is an output signal used to support transmission timing for the device. TXCHPPLS pulses high for one TXIFCLK cycle at the PN chip rate defined by the user. The chip rate is set either by programming a value in bits 5-0 of address 41_H or through use of the external TXMCHP signal.

TXTRKPLS (Pin 61)
Transmitter Data Track Pulse. TXTRKPLS is an output signal that allows monitoring of data symbol transmissions. A rising edge of output signal TXTRKPLS occurs one chip period before the end of the current data symbol transmission. TXTRKPLS then falls low immediately following the rising edge of TXIFCLK.

TXACTIVE (Pin 78)
Transmitter Active. A high level on TXACTIVE indicates that the transmitter is sending data symbols. This signal will be set high at the end of the Acquisition/Preamble symbol, indicating the start of the first chip of the first data symbol at the TXIOUT and TXQOUT pins. It will be set low at the end of the last chip period of the last data symbol of the burst at the TXIOUT and TXQOUT pins.

RXOUT (Pin 57)
Receiver Output. RXOUT is the output data of the receiver following downconversion, despreading and demodulation. In BPSK mode, one data bit is provided per symbol; in QPSK mode, two data bits are provided per symbol with a half-symbol separation between the bits. Note that, when the Z87200 is operated in burst mode, the data will be invalid during the first symbol of each burst; that is, in BPSK mode the first bit will be invalid, and in QPSK mode the first two bits will be invalid.

RXIOUT (Pin 56)
Receiver I Channel Output. RXIOUT is the I channel output data before dibit-to-serial conversion. RXIOUT can be used in conjunction with the RXQOUT signal in applications where the QPSK output data is required as parallel bit pairs. Note that, when the Z87200 is operated in burst mode, the first bit of RXIOUT in each burst will be invalid RXQOUT (Pin 55).

Receiver Q Channel Output. RXQOUT is the Q channel output data before dibit-to-serial conversion. RXQOUT can be used in conjunction with the RXIOUT signal in applications where the QPSK data is required as parallel bit

OUTPUT SIGNALS (Continued)

pairs. Note that, when the Z87200 is operated in burst mode, the first bit of RXQOUT in each burst will be invalid.

/RXDRDY (Pin 54)
Receiver Data Ready Bar. /RXDRDY is provided as a receiver timing signal. /RXDRDY is normally set high and pulses low during the baseband sampling clock cycle when a new RXOUT signal is generated.

RXSPLPLS (Pin 53)
Receiver Sample Pulse. RXSPLPLS is an output timing signal that provides internal timing information to the user. RXSPLPLS is the internally generated baseband sampling clock, referenced either externally or internally according to the setting of bit 0 of address 01_H. All receiver functions, excluding those in the Downconverter, trigger internally on the rising edge of RXSPLPLS.

RXSYMPLS (Pin 52)
Receiver Symbol Pulse. RXSYMPLS is an output signal that provides the user internal timing information relative to the detection/correlation of symbols. Symbol information from the PN Matched Filter, DPSK Demodulator, and Output Processor is transferred on the rising edge of RXSPLPLS preceding the falling edge of RXSYMPLS.

RXACTIVE (Pin 83)
Receiver Active. A high level on RXACTIVE indicates that the receiver has detected an Acquisition/Preamble symbol and is currently receiving data symbols. RXACTIVE will be set high one bit period before the first rising edge of /RXDRDY, indicating that the first data bit is about to appear at the RXOUT, RXIOUT, and RXQOUT pins. RXACTIVE will be set low immediately following the last rising edge of /RXDRDY, indicating that the last data bit of the burst has been output at the RXOUT, RXIOUT, and RXQOUT pins. $RXTEST_{7-0}$ (Pins 41-48)

These pins provide access to 16 test points within the receiver as shown in The pin outputs are selected according to the value in bits 3-0 of address 38_H and the assignments shown in When one of these 4-bit values is written into address 38_H, the corresponding function becomes available at the $RXTEST_{7-0}$ outputs. The $RXTEST_{7-0}$ bus is a tri-state bus and is controlled by the OEN input. Note that the validity of the $RXTEST_{7-0}$ outputs at RXIFCLK speeds greater than 20 MHz is dependent on the output selected: outputs that change more rapidly than once per symbol may be indeterminate.

Table 4. Receiver Test Functions

	$RXTEST_{7-0}$ Output							
Bits 3-0 of 38_H	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0_H			MFQIN 2-0 Matched Filter Q Input			MFIN2-0 Matched Filter I Input		
1_H	$Pk\text{-}Power_{9-2}$ MF Peak Magnitude Output (Changes Once Per Symbol)							
2_H	COS_{7-0} Cosine Output of NCO (Changes Every Cycle of RXIFCLK)							
3_H	SIN_{7-0} Sine Output of NCO (Changes Every Cycle of RXIFCLK)							
4_H	$DCIOUT_{16-9}$ Downconverter I Channel Output (Changes at RXIFCLK Rate)							
5_H	$DCQOUT_{16-9}$ Downcounter Q Output (Changes at RXIFCLK Rate)							
6_H	$ISUM_{9-2}$ Matched Filter I Output (Changes Twice Per Chip)							
7_H	$QSUM_{9-2}$ Matched Filter Q Output (Changes Twice Per Chip)							
8_H	$POWER_{9-2}$ MF Magnitude Output (Changes Twice Per Chip)							
9_H	$ISUM_{7-0}$ MF Viewpoint I Output (Changes Twice Per Chip)							
A_H	$QSUM_{7-0}$ MF Viewpoint Q Output (Changes Twice Per Chip)							
B_H	$Pk\text{-}ISUM_{7-0}$ MF Peak I Channel Output (Changes Once Per Symbol)							
C_H	$Pk\text{-}QSUM_{7-0}$ MF Peak Q Channel Output (Changes Once Per Symbol)							
D_H	DOT_{16-9} Dot Product (Changes Once Per Symbol)							
E_H	$CROSS_{16-9}$ Cross Product (Changes Once Per Symbol)							
F_H	$TXFBK_{7-0}$ Loopback Test Output							

All signals available at this port, with one exception, are expressed as two's complement values, ranging from –128 to +127 (80_H to $7F_H$). The PN Matched Filter power output values, available when the value in bits 3-0 of address 38_H is set to either 1_H or 8_H, is an unsigned binary number, ranging from 0 to 255 (0_H to FF_H).

The reset sequence that occurs when the receiver is disabled will also reset the contents of address 38_H to a value of 0. If the $RXTEST_{7-0}$ bus is to be used to observe any function other than the PN Matched Filter I and Q inputs, then the appropriate value must be rewritten.

TXTEST (Pin 59)

Transmitter Test Output. TXTEST provides access to 3 test points within the transmitter as shown in The pin output is selected according to the state of the two least significant bits of the address line, $ADDR_{1-0}$ and the assignments shown in Table 5. Note that this method of accessing the transmitter test points is completely different than the method by which the receiver test points are accessed. The state of the other address lines does not affect this function, and this function is always enabled. The availability of TXTEST output signals is only supported for TXIFCLK speeds less than 20 MHz; output with clock speeds greater than 20 MHz will be indeterminate.

Table 5. Transmitter Test Functions

$ADDR_{1-0}$	TXTEST	Description
0_H	ISM	Unspread I Symbol
1_H	QSYM	Unspread Q Symbol
2_H	SCODE	Spreading Code

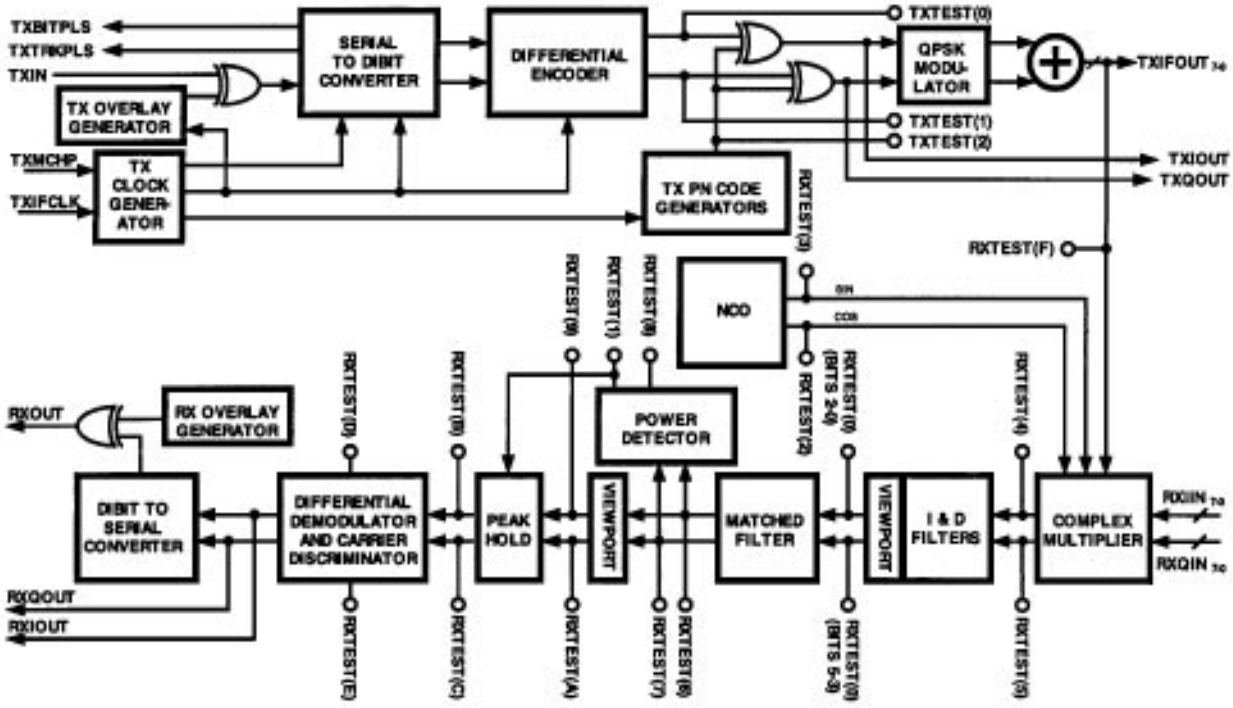


Figure 10. Transmitter and Receiver Test Points

CONTROL REGISTERS

Setting the Control Registers

The majority of the Z87200 control registers are completely independent and can be set or modified in any order. Two exceptions, however, exist:

- First, any time that the NCO is disabled, either through use of pin MNCOEN or bit 0 of address 37_H, the frequency control word must be reloaded, either through use of pin MFLD or bit 0 of address 00_H, once the NCO is re-enabled.
- Second, setting bit 2 of address 37_H to zero to disable the receiver will also cause the data in address 38_H to be set to zero, thereby possibly changing the receiver test point(s) that will be observed on the RXTEST pins. Address 38_H must be loaded with its desired value after bit 2 of address 37_H is again set to 1.

Downconverter Registers

Address 00_H:

Bit 0 — Frequency Control Word Load

This bit is used to load a frequency control value into the NCO, thereby changing its output frequency. The signal is internally synchronized to RXIFCLK to avoid intrinsic race or hazard timing conditions.

The loading of the NCO may be performed by various means. Setting this bit provides a synchronized internal means to control update of the NCO. Alternatively, the MFLD pin or the Z87200's programmable loop filter timing circuitry may be used.

The MFLD input and bit 0 of address 00_H are logically ORed together so that, when either one is held low, a rising edge on the other triggers the frequency load function manually. The rising edge of this bit is synchronized internally so that, on the following sixth rising edge of RXIFCLK, the frequency control word is completely registered into the NCO accumulator. The frequency load command must not be repeated until after a delay of six RXIFCLK cycles.

Address 01_H:

Bit 0 — Manual Sample Clock Enable

This bit selects the source of the internal baseband sampling clock, which should be at twice the nominal PN chip rate. The clock reference may be either supplied externally by RXMSMPL or generated internally from RXIFCLK.

When this bit is set high, the baseband sampling rate of the receiver is controlled by the external RXMSMPL signal. When it is set low, the sampling clock is generated internally (at a rate determined by the Sample Rate Control counter and set by bits 5-0 of address 02_H) and the RXMSMPL input is ignored.

Bit 1 — Invert Loop Filter Value

This bit allows the sign of the output signal from the loop filter to be inverted, thereby negating the value of the signal. The capability to invert the loop filter value permits the carrier frequency error component generated in the demodulator to be either added to or subtracted from the Frequency Control Word of the NCO. The correct setting will depend on several factors, including whether high-side or low-side downconversion is used.

When this bit is set low, the loop filter output is negated before being summed with the Frequency Control Word of the NCO and is thus subtracted from the FCW; when this bit is set high, the loop filter output is not negated and is added to the FCW.

Bit 2 — NCO Accumulator Carry In

This bit is primarily used as an internal test function and should be set low for normal operation. When this bit is set high, 1 LSB is added to the NCO accumulator each clock cycle. When it is set low, the NCO accumulator is not affected.

Bit 3 — Two's Complement Input

The $RXIIN_{7-0}$ and $RXQIN_{7-0}$ input signals can be in either two's complement or offset binary formats. Since all internal processing in the device operates with two's complement format signals, it is necessary to convert the $RXIIN_{7-0}$ and $RXQIN_{7-0}$ inputs in offset binary format to two's complement format by inverting the MSBs.

When this bit is set high, the device expects two's complement format inputs on $RXIIN_{7-0}$ and $RXQIN_{7-0}$. When it is set low, the device expects offset binary format on $RXIIN_{7-0}$ and $RXQIN_{7-0}$. In two's complement format, the 8-bit input values range from –128 to +127 (80_H to $7F_H$); in offset binary format, the values range from 0 to +255 (00_H to FF_H).

Bits 7-4 — Integrate and Dump Filter Viewport Control
The Z87200 incorporates viewport (data selector) circuitry to select any three consecutive bits from the 14-bit output of the Integrate and Dump (I & D) Filters in the Downconverter block as the 3-bit inputs to the dual-channel PN Matched Filter. The signal levels of the Integrate and Dump Filter I and Q outputs reflect the input signal levels and the number of samples integrated before the filter contents are "dumped," where the number of samples is determined by the baseband sampling rate (nominally, twice the PN chip rate) and the I.F. sampling rate (RXIFCLK). Setting the viewport thus effectively normalizes the I & D Filter outputs before further processing. The unsigned value, n, of bits 7-4 of address 01_H determines the 3-bit inputs to the PN Matched Filter as the14-bit I & D Filter outputs divided by 2^n. Equivalently, bits 7-4 control the viewport of the Integrate and Dump Filter outputs as shown in Note that viewport control affects both I and Q channels of the Integrate and Dump Filters.

Table 6. Integrate & Dump Filter Viewport Control

Bits 7-4	I & D Bits Output to Matched Filter
0_H	2-0
1_H	3-1
2_H	4-2
3_H	5-3
• • •	• • •
• • •	• • •
A_H	12-10
B_H	13-11

Saturation protection is implemented for those cases when the Integrate and Dump Filter output signal level overflows the scaled range selected for the PN Matched Filter. When the scaled value range is exceeded, the saturation protection limits the output word to the maximum or minimum value of the range according to whether the positive or negative boundary was exceeded.

Address 02_H:
Bits 5-0 — Receiver Baseband Sampling (Dump) Rate Control
The baseband sampling rate should be set to twice the nominal PN chip rate of the received signal and must be less than or equal to half the rate of RXIFCLK. When bit 0 of address 01_H is set low, the baseband sampling clock for the Integrate and Dump Filter and all subsequent receiver circuitry is referenced to RXIFCLK and generated internally. The receiver baseband sampling rate is then set to the frequency of RXIFCLK/(n+1), where n is the value stored in bits 5-0 and must range from 1 to 63. This feature is useful in cases where a specific sample rate is required that is an integer sub-multiple of $f_{RXIFCLK}$. In cases where a sample rate is required that is not an integer sub-multiple of $f_{RXIFCLK}$, an external baseband sampling rate can be provided by the RXMSMPL input.

Addresses 03_H through 06_H:
NCO Frequency Control Word
The Z87200's internal NCO is driven by a frequency control word that is the sum of the frequency discriminator error value (generated in the demodulator) and the 32-bit frequency control word (FCW) stored in this location. The four 8-bit registers at addresses 03_H to 06_H are used to store the 32-bit frequency control word as shown in The LSB of each byte is stored in bit 0 of each register.

Table 7. Integrate & Dump Filter Viewport Control

ADDR06H	ADDR 05H	ADDR04H	ADDR03H
Bits 31-24	Bits 23-16	Bits 15-8	Bits 7-0

The NCO frequency is then set by the FCW according to the following formula:

$$f_{NCO} = \frac{f_{RXIFCLK} \times FCW}{2^{32}}$$

In order to avoid in-band aliasing, f_{NCO} must not exceed 50% of $f_{RXIFCLK}$; normally, the FCW should be set so that f_{NCO} does not exceed ~35% of $f_{RXIFCLK}$. While this limitation may seem to restrict use of the NCO, higher I.F. transmit or receive frequencies can generally be achieved by using aliases resulting from digital sampling. The signal bandwidth with respect to $f_{RXIFCLK}$, the modulation type, and the use of Direct I.F. or Quadrature Sampling Mode also restrict the choice of NCO frequency, Theory of Operation.

PN Matched Filter Registers

Despreading of the received signal is accomplished in the Z87200 with a dual (I and Q channel) PN Matched Filter. Furthermore, the Z87200 is designed for burst signal operation, where each data burst begins with an Acquisition/Preamble symbol and is then followed by the actual information data symbols. Two separate and independent PN codes can be employed, one for the Acquisition/Preamble symbol, the other for the information symbols. Accordingly, the PN Matched Filter is supported by two PN code registers to independently allow the programming of two distinct codes up to 64 chips in length. The PN codes are represented as a sequence of ternary-valued tap coef-

CONTROL REGISTERS (Continued)

ficients, each requiring 2 bits of storage according to the mapping shown in Table 8.

Table 8. PN Matched Filter Tap Values

Tap Bits 1,0		Tap Coeff
X	0	0
0	1	+1
1	1	-1

As a convention, Tap 0 is the first tap as the received signal enters the PN Matched Filter, and Tap 63 is the last. All active taps of the PN Matched Filter, from Tap 0 up to Tap (N-1), where N is the length of the PN code, should be programmed with tap coefficient values of +1 or -1 according to the PN code sequence. Setting the end coefficients of the PN Matched Filter registers to zero values permits the effective length of the filter to be made shorter than 64 taps.

Addresses 07_H through 16_H:

Matched Filter Acquisition/Preamble Symbol Coefficients

Addresses 07_H to 16_H contain the 64 2-bit Acquisition/Preamble PN code coefficient values. The 128 bits of information are stored in 16 8-bit registers at addresses 07_H to 16_H as shown in Table 8.

Table 9. Acquisition/Preamble Coefficient Storage

Address 16_H			
Bits 7,6	Bits 5,4	Bits 3,2	Bits 1,0
Coeff. 63	Coeff. 62	Coeff. 61	Coeff. 60
Address 15_H			
Bits 7,6	Bits 5,4	Bits 3,2	Bits 1,0
Coeff. 59	Coeff. 58	Coeff. 57	Coeff. 56
- - -	- - -	- - -	- - -
- - -	- - -	- - -	- - -
Address 08_H			
Bits 7,6	Bits 5,4	Bits 3,2	Bits 1,0
Coeff. 7	Coeff. 6	Coeff. 5	Coeff. 4
Address 07_H			
Bits 7,6	Bits 5,4	Bits 3,2	Bits 1,0
Coeff. 3	Coeff. 2	Coeff. 1	Coeff. 0

Addresses 17_H through 26_H:

Matched Filter Data Symbol Coefficients

Addresses 17_H to 26_H contain the 64 2-bit Data Symbol PN code coefficient values. The 128 bits of information are stored in 16 8-bit registers at addresses 17_H to 26_H as shown in The contents of addresses 17_H to 26_H are independent of and not affected by the contents of addresses 07_H to 16_H.

Table 10. Data Symbol Coefficient Storage

Address 26_H			
Bits 7,6	Bits 5,4	Bits 3,2	Bits 1,0
Coeff. 63	Coeff. 62	Coeff. 61	Coeff. 60
Address 25_H			
Bits 7,6	Bits 5,4	Bits 3,2	Bits 1,0
Coeff. 59	Coeff. 58	Coeff. 57	Coeff. 56
- - -	- - -	- - -	- - -
- - -	- - -	- - -	- - -
Address 18_H			
Bits 7,6	Bits 5,4	Bits 3,2	Bits 1,0
Coeff. 7	Coeff. 6	Coeff. 5	Coeff. 4
Address 17_H			
Bits 7,6	Bits 5,4	Bits 3,2	Bits 1,0
Coeff. 3	Coeff. 2	Coeff. 1	Coeff. 0

Address 27_H:

Bit 0 — Front End Processor Disable

The Front End Processor (FEP) averages the two baseband samples per chip by adding consecutive pairs of samples. The function may be disabled for test purposes by using this bit: when set low, the FEP is enabled and in its normal mode of operation; when set high, the FEP is disabled.

Power Estimator Registers

Address 28_H:

Bits 1-0 — Matched Filter Viewport Control

The Z87200 incorporates viewport (data selector) circuitry to select any eight consecutive bits from the 10-bit outputs of the PN Matched Filter as the 8-bit inputs to the Power Estimator and DPSK Demodulator blocks. The Symbol Tracking Processor, however, operates on the full 10-bit PN Matched Filter outputs before the viewport is applied. The signal levels of the PN Matched Filter output reflect the number of chips per symbol and the signal-to-noise ratio of the signal. Setting the viewport thus effectively normalizes the PN Matched Filter outputs prior to further processing. The unsigned value, n, of bits 1-0 of address 28_H determines the 8-bit input to the Power Estimator and DPSK Demodulator blocks as the 10-bit PN Matched Filter output divided by 2^n. Equivalently, bits 1-0 control the viewport of the PN Matched Filter output as shown in Note

that viewport control affects both I and Q channels of the PN Matched Filter output.

Table 11. Matched Filter Viewport Control

Bits 1-0		ISUM, QSUM
0	0	Bits 7-0
0	1	Bits 8-1
1	X	Bits 9-2

Saturation protection is implemented for those cases when the PN Matched Filter output signal level overflows the scaled range selected for the Power Estimator and DPSK Demodulator. When the scaled value range is exceeded, the saturation protection limits the output word to the maximum or minimum value of the range according to whether the positive or negative boundary was exceeded.

Acquisition and Tracking Processor Registers

The Acquisition and Tracking Processor Registers allow the user to configure how the PN Matched Filter outputs for the Acquisition/Preamble symbol and the data symbols that follow thereafter are treated in the Symbol Tracking Processor. Since operation of the Z87200 receiver presumes symbol-synchronous PN modulation, processing of the PN Matched Filter outputs can be used for symbol synchronization prior to DPSK demodulation. The Acquisition/Preamble symbol and the data symbols may have different PN spreading codes, however, and so the PN Matched Filter outputs may exhibit different signal levels due to the different code lengths and auto-correlation properties. The control registers in this block allow such differences to be treated, as well as permitting specification of the number of receive data symbols per burst and other parameters associated with burst data communications.

The I and Q channel outputs of the PN Matched Filter are processed to estimate the correlation signal power at each baseband sampling instant. This estimated signal power is compared with the contents of the Acquisition/Preamble and Data Symbol Threshold registers, as appropriate, to determine whether “successful” correlation has been detected. Successful detection in acquisition mode immediately switches the receiver to despread and track the expected subsequent data symbols, while successful detection thereafter yields symbol synchronization. The threshold register values must be set by the user to satisfactorily detect the correlation peak in noise obtained when the received PN-spread signal is correlated against a local version of the PN code by the PN Matched Filter. Once the power estimation value exceeds the threshold register value, a successful correlation is assumed to have been detected. Further operations in the Symbol Tracking Processor then handle the possibility of multiple detects per symbol, missed detects, etc.

The choice of the threshold values will be determined by several factors. Arithmetically, the digital baseband samples of the received signal are multiplied by the PN Matched Filter tap coefficients each baseband sample clock cycle and the results are summed to provide a correlation value. The I and Q PN Matched Filter correlated output values are then used to estimate the signal power according to the following approximation:

$$\text{Max}\{\text{Abs}(I),\text{Abs}(Q)\}+1/2\ \text{Min}\{\text{Abs}(I), \text{Abs}(Q)\}.$$

The magnitude of the estimated power thus depends on several variables, including the setting of the Integrate and Dump Filter viewport, the PN code length and autocorrelation properties, and the magnitudes of the incoming $RXIIN_{7-0}$ and $RXQIN_{7-0}$ signals. The actual threshold values that should be programmed will therefore vary from application to application.

Addresses 29_H and $2A_H$: Acquisition/Preamble Threshold

Addresses 29_H and $2A_H$ contain the unsigned Acquisition/Preamble Threshold value, as shown in This value is used for comparison with the estimated signal power from the PN Matched Filter to determine whether a successful correlation has been detected in acquisition mode. The Acquisition/Preamble Threshold value must be set by the user to satisfactorily detect the correlation peak in noise obtained when the received PN-spread Acquisition/Preamble is correlated against a local version of the Acquisition/Preamble PN code by the PN Matched Filter. Once the power estimation value exceeds the threshold value, a successful correlation is assumed to have been detected. Note that the Symbol Tracking Processor does not insert missed detect pulses when the device is in acquisition mode.

Table 12. Acquisition/Preamble Threshold Storage

ADDR $2A_H$	ADDR 29_H
Bits 1-0	Bits 7-0
Acq. Thresh. Bits 9-8	Acq. Thresh. Bits 7-0

Addresses $2B_H$ and $2C_H$: Data Symbol Threshold

Addresses $2B_H$ and $2C_H$ contain the Data Symbol Threshold value, as shown in This value is used for comparison with the estimated signal power from the PN Matched Filter to determine whether a successful correlation has been detected for each data symbol. The Data Symbol Threshold value must be set by the user to satisfactorily detect the correlation peak in noise obtained when the received PN-spread data symbol is correlated against a local version of the data symbol PN code by the PN Matched Filter. Once the power estimation value exceeds the threshold value, a successful correlation is assumed to have been detected. If bit 2 of address 30_H is set low, then the Symbol Acquisi-

CONTROL REGISTERS (Continued)

tion Processor will insert a detect pulse at the appropriate time if a successful correlation is not detected as expected *a priori*.

Table 13. Data Symbol Threshold Storage

ADDR $2C_H$	ADDR $2B_H$
Bits 1-0	Bits 7-0
Data Thresh. Bits 9-8	Data Thresh. Bid 7-0

Address $2D_H$:

Bits 5-0 — Rx Chips per Data Symbol

The number of PN chips per data symbol in the receiver is controlled by address $2D_H$. The unsigned value must range from 1 to 63 (01_H to $3F_H$), where the number of chips per data symbol will be this value plus 1. The *a priori* number of PN chips per data symbol, where this value must be equal to the number of non-zero coefficients stored in the Data Symbol Coefficient Registers (addresses 17_H to 26_H) for the PN Matched Filter, is used to help control symbol timing in the receiver. Since acquisition is purely based on correlation of a single received Acquisition/Preamble symbol, the corresponding number of chips per Acquisition/Preamble symbol is not required and no similar register is provided for such use.

Address $2E_H$:

Receiver Data Symbols per Burst (bits 7-0)

The data stored as two bytes in addresses $2E_H$ (LS Byte) and $3A_H$ (MS Byte) define the number of data symbols per burst. This unsigned value must range from 3 to 65,535 (0003_H to $FFFF_H$), and the number of data symbols per burst will be this value minus 2, giving a range of 1 to 65,533. Note that the range is slightly different from that supported by the Z87200's transmitter. Once the number of received data symbols processed exceeds this number, the burst is assumed to have ended and the receiver immediately returns to acquisition mode, ready for the next burst.

Address $2F_H$:

Missed Detects per Burst Threshold

To monitor the reception quality of the received burst data symbols, the Z87200 incorporates a feature within its tracking algorithm that tallies the number of received data symbols whose PN Matched Filter correlation output did not exceed the Data Symbol Threshold value.

Whenever a "missed detect" occurs, the tracking algorithm will generate and insert a detect signal at the sample clock cycle corresponding to the expected correlation peak in order to maintain a continuous train of data symbols and symbol clocks. Simultaneously, a "missed detect" pulse will be generated internally and tallied for the current burst. When the accumulated number of missed detects is greater than the value stored in address $2F_H$, the device will terminate reception of the current burst and return to acquisition mode to await the next burst.

The unsigned value in address $2F_H$ must range from 1 to 255 (01_H to FF_H), where this value is the maximum number of missed detects per burst allowed before the burst terminates. This function can be disabled by setting bit 5 of address 30_H high.

Address 30_H:

Bit 0 — Manual Detect Enable

While the receiver is in acquisition mode, valid bursts may be ignored by setting this bit high. When it is set low (normal operation), the detection of a burst's Acquisition/Preamble symbol is enabled. Setting this bit high allows the user to force the device to ignore Acquisition/Preamble symbols that would normally be successfully acquired. This feature could be used, for example, in a system employing multiple receivers with identical PN codes in a Time Division Multiple Access scheme where time-synchronized device management could be supported through dynamic setting of this bit.

Acquisition and Tracking Processor Registers

Bit 1 — Manual Punctual

This bit enables the user to completely disable the internal tracking circuitry and force symbol information to be transferred to the demodulator punctually at the symbol rate determined by the number of chips per data symbol information programmed into address $2D_H$. This function overrides the symbol tracking algorithm, although the absence of a successful correlation will continue to be tallied as a missed detect and compared against the value stored in address $2F_H$ to monitor signal quality unless disabled by bit 5 of address 30_H. When bit 1 is set low, the Z87200 will operate in its normal mode with symbol timing derived from the symbol tracking processor; when set high, symbol timing is derived from the *a priori* number of chips per data symbol stored in bits 5-0 of address $2D_H$.

Bit 2 — Force Continuous Acquisition

This bit enables the user to force the receiver to remain in acquisition mode even after successful detection of the Acquisition/Preamble symbol. When so commanded, the receiver will continuously process only Acquisition/Preamble symbols and will not switch from acquisition mode. This function may be used under manual control to receive a series of repeated Acquisition/Preamble symbols in order to increase the confidence level of burst detection before beginning demodulation of the data symbol information.

When this bit is set high, the device will be locked in acquisition mode and the Symbol Tracking Processor will not in-

sert missed detect pulses; when set low, normal operation will be enabled whereby data symbols are automatically processed immediately following detection of an Acquisition/Preamble symbol.

Bit 3 — Bypass Max. Power Selector
The Z87200's receiver acquisition and tracking circuitry includes a function that continuously selects the highest estimated power level out of the three most recent consecutive estimated power levels from the PN Matched Filter. As the contents of the sliding 3-sample window change each cycle of the baseband sampling clock, a new determination of the highest power level is made from the current set of the three most recent power level values. The correlated I and Q channel values within the 3-sample window corresponding in time to the highest observed power level are then available to be processed in the demodulator.

This function assures that, within any 3-sample period, the I and Q channel values corresponding to the highest estimated power level will be selected over the two other pairs of correlated values even if the estimated power levels of the other pairs exceed the programmed threshold. The Maximum Power Selector is used in normal operation of the Z87200 so that the tracking algorithm discriminates by estimated power levels rather than exact timing intervals, thereby allowing the receiver to adjust to dynamic changes of the symbol phase. In cases where specific correlation values are desired regardless of their associated power level, bit 3 of address 30_H enables the 3-sample power discriminator to be bypassed, thereby making the outputs of the PN Matched Filter available directly to the demodulator.

When this bit is set high, the Maximum Power Selector is bypassed; when it is set low, the Selector is enabled, where this is the normal operating mode.

Bit 4 — Half Symbol Pulse Off
The Z87200 generates two bit clock pulses per symbol when operating in QPSK mode, one at the mid-point of each symbol and one at the end of each symbol. These clocks are used by the Output Processor to manage data flow.

When this bit is set high, the mid-point pulse is suppressed; when it is set low, the device operates in its normal mode. This function is primarily used for test purposes and should not normally be used.

Bit 5 — Missed Detects Per Burst Off
To monitor the quality of the received burst data symbols, the Symbol Tracking Processor keeps track of the cumulative number of received data symbols per burst whose estimated correlation power level did not exceed the specified Data Symbol Threshold value. When the accumulated number of missed detects equals the Missed Detects per Burst Threshold value stored in address $2F_H$, the device will terminate the reception of the current burst with the next missed detect and return to acquisition mode to await the next burst.

When bit 5 is set low, the "missed detect" function operates normally; when set high, this function is disabled, allowing the device to be operated until the end of the specified data burst even when the number of "missed detects" exceeds the Missed Detects per Burst Threshold.

Bit 6 — Receiver Symbols Per Burst Off
The data stored in addresses $2E_H$ and $3A_H$ defines the number of data symbols per burst that will be processed by the receiver. This unsigned value must range from 3 to 65,535 (0003_H to $FFFF_H$), and the number of data symbols per burst will be this value minus 2. Once the number of data symbols processed by the receiver exceeds this number, the burst is assumed to have ended and the receiver will immediately return to acquisition mode.

When bit 6 is set high, the function is disabled, providing an option to track data symbols under external control for bursts of more than 65,533 data symbols or indefinitely for continuous transmission; when set low, the function will operate normally as defined by the value stored in addresses $2E_H$ and $3A_H$.

Address 31_H:
Bit 0 — Manual Detect Pulse
This bit provides the user a means to externally generate symbol timing, bypassing and overriding the internal symbol power estimation and tracking circuitry. This function may be useful in applications where the dynamic characteristics of the transmission environment require unusual adjustments to the symbol timing.

When bit 0 of address 30_H is set high (Manual Detect Enable) and when RXMDET is low, a rising edge on this bit will generate a detect pulse. The function can also be performed by means of the RXMDET input signal. Bit 0 of address 31_H and the RXMDET input are logically ORed together so that, when either one is held low, a rising edge on the other triggers the manual detect function. The rising edge of this bit is synchronized internally so that on the second rising edge of the baseband sampling clock that follows, the rising edge of bit 0 will transfer the I and Q channel correlated output values of the PN Matched Filter to the DPSK Demodulator.

Address 32_H:
Bit 0 — Receiver Manual Abort
This bit enables the user to manually force the Z87200 to cease reception of the present burst of data symbols and prepare for acquisition of a new burst. This function can be used to reset the receiver and prepare to receive a priority transmission signal under precise timing control, giving the user the ability to control the current state of the receiver as needed.

CONTROL REGISTERS (Continued)

When RXMABRT is set low, a rising edge on bit 0 of address 32_H will execute the abort function. The function can also be performed by means of the RXMABRT input. The RXMABRT input and bit 0 of address 32_H are logically ORed together so that, when either one is held low, a rising edge on the other triggers the abort function. The second rising edge of the internal baseband sampling clock that follows a rising edge of this bit will execute the abort and also clear the symbols-per-burst, samples-per-symbol, and missed-detects-per-burst counters. The counters will be reactivated on the detection of the next Acquisition/Preamble symbol or by a manual detect signal.

Demodulator Registers

Address 33_H:

Bits 1-0 — Signal Rotation Control

These bits control the function of the Signal Rotation Block used in demodulation of the differentially encoded BPSK, QPSK, or $\pi/4$ QPSK signals. The previous symbol will be rotated in phase with respect to the current symbol as shown in Table 14, where I_{OUT} and Q_{OUT} are the I and Q channel outputs of the Signal Rotation Block and I_{IN} and Q_{IN} are the inputs. The normal settings are 0 X (no rotation) for BPSK and $\pi/4$ QPSK signals and 1 1 (–45° rotation) for conventional QPSK signals.

Table 14. Signal Rotation Control

Bits 1,0	I_{OUT}	Q_{OUT}	Resulting Rotation
0, X	I_{IN}	Q_{IN}	No rotation
1,0	I_{IN}-Q_{IN}	Q_{IN}+I_{IN}	+45° rotation
1,1	I_{IN} + Q_{IN}	Q_{IN}-I_{IN}	-45° rotation

Bit 2 — Not Used

Bit 2 of address 33_H is not used and must always be set low (0).

Bit 3 — Loop Clear Disable

The setting of this bit determines whether the Loop Filter's K2 accumulator is reset or not when the Z87200 receiver function is turned off when the input signal MRXEN is set low.

When bit 3 is set low, the Loop Filter's K2 accumulator will be reset to zero whenever MRXEN is set low to disable the receiver function. When bit 3 is set high, this function is disabled and the contents of the accumulator are not affected when MRXEN transitions from high to low. The optimum setting of this bit will depend on the stability of the oscillators used for carrier generation and frequency translation in the system and the length of the period between bursts. If the oscillators are stable and the period between bursts is not very long, the optimum setting of this bit will be low so that at the start of each burst the tracking loop will resume from its state at the end of the previous burst. If the oscillators are not stable or if the period between bursts is long with respect to the oscillators' stability, then the optimum setting may be high so that the tracking loop will restart from its initial state at the start of each burst.

Bits 7-4 — AFC Viewport Control

The Z87200 incorporates viewport (data selector) circuitry to select any eight consecutive bits from the 17-bit output of the Frequency Discriminator as the 8-bit input to the Loop Filter block to implement the Z87200's AFC function. The unsigned value, n, of bits 7-4 of address 33_H determines the 8-bit input to the Loop Filter as the 17-bit Frequency Discriminator output divided by 2^n. Equivalently, bits 7-4 control the viewport of the Frequency Discriminator output as shown in Table 14.

Table 15. AFC Viewport Control

Bits 7-4	Discrim. bits output to Loop Filter
0_H	7-0
1_H	8-1
2_H	9-2
3_H	10-3
• • •	• • •
• • •	• • •
8_H	15-8
9_H	16-9
A_H-F_H	Not used

Saturation protection is implemented for those cases when the Frequency Discriminator output signal level overflows the scaled range selected for the Loop Filter. When the scaled value range is exceeded, the saturation protection limits the output word to the maximum or minimum value of the range according to whether the positive or negative boundary was exceeded.

Address 34_H:

Bits 4-0 — K2 Gain Value

Bits 4-0 control the gain factor K2 within the Loop Filter. The gain factor multiplies the signal before the K2 accumulator by a value of 2^n, where n is the 5-bit K2 Gain Value. The value must range from 0 to 21 (15_H) as shown in Table 15.

Table 16. K2 Gain Values

Bits 4-0	Gain in K2 Path
00_H	2^0
01_H	2^1
• • •	• • •
• • •	• • •
14_H	2^{20}
15_H	2^{21}

Bit 5 — K2 On

This bit enables or disables the K2 path of the Loop Filter. Setting this bit low resets the K2 accumulator and keeps it reset; setting this bit high enables the path and turns on K2.

Bit 6 — Carry In One Half

When this bit is set high, the value of 1/2 of an LSB is added to the accumulator of the K2 path of the Loop Filter each symbol period. This function can be useful in cases where the scale and gain functions that precede the accumulator produce quantized values with significant error. In such cases, the processing of two's complement numbers by the accumulator will compound the error over time. Since truncation of two's complement numbers leads to a negative bias of 1/2 of an LSB when the error is random, adding 1/2 of an LSB per symbol can compensate by averaging the error to zero.

When bit 6 of address 34_H is set high, a value of 1/2 will be added to the accumulator input each symbol cycle; when it is low, a zero will be added.

Address 35_H:

Bits 4-0 — K1 Gain Value

Bits 4-0 control the gain factor K1 within the Loop Filter. The gain factor multiplies the signal by a value of 2^n, where n is the 5-bit K1 Gain Value. The value must range from 0 to 21 (15_H), as shown in Table 16.

Table 17. K1 Gain Values

Bits 4-0	Gain in K1 Path
00_H	20
01_H	21
•••••	•••••
•••••	•••••
14_H	2^{20}
15_H	2^{21}

Bit 5 — K1 On

This bit enables or disables the K1 path of the Loop Filter. Setting this bit low disables the K1 path; setting this bit high enables the path and turns on K1.

Bit 6 — Freeze Loop

This bit enables the Loop Filter to be held constant during symbol cycles, thereby fixing the output frequency of the NCO at the value established by the Loop Filter when bit 6 was set high. This function can be useful in cases where a carrier offset has been tracked by the Loop Filter and additional Doppler offsets are to be ignored.

When this bit is set high, it freezes the output of the Loop Filter; when it is set low, the Loop Filter is enabled and processes the frequency error information in the usual way.

CONTROL REGISTERS (Continued)

Output Processor Control Registers

Address 36_H:

Bit 0 — Reverse I and Q

In QPSK mode, the order in which the received I and Q bit information is output may be reversed by setting this bit high. This function has the effect of interchanging I and Q channels. Normally, when this bit is set low, the I-channel bit will precede the Q-channel bit in each symbol period. When bit 0 is set high, the Q-channel bit will precede the I-channel bit each symbol period.

Bit 1 — BPSK Enable

This bit configures the Output Processor to output either one bit per symbol (BPSK mode) or two bits per symbol (QPSK mode). In addition, it enables the user to output the I-channel information only or the Q-channel information only, depending on the value of bit 0. Table 18 shows the configuration of the output processor for all combinations of the values of bits 0 and 1.

Table 18. Output Processor Modes

Bit 1	Bit 0	Output Processor Mode
0	0	QPSK mode with I-Channel Bit Preceding Q-Channel Bit
0	1	QPSK mode with Q-Channel Bit Preceding I-Channel Bit
1	0	BPSK mode with I-Channel Information Output
1	1	BPSK mode with Q-Channel Information Output

Bit 1 also sets the Frequency Discriminator into either BPSK or QPSK mode. The Z87200 receiver uses Dot and Cross product results generated within the DPSK Demodulator to develop the error signal used to form a closed-loop AFC for carrier frequency acquisition and tracking.

When bit 1 is set high, the discriminator circuitry is in BPSK mode and the Frequency Discriminator function is calculated as:

$$Cross_{16\text{-}0} \times Dot_{MSB}.$$

When bit 1 is set low, the discriminator circuitry is in QPSK mode and the Frequency Discriminator function is calculated as:

$$(Cross_{16\text{-}0} \times Dot_{MSB}) - (Dot_{16\text{-}0} \times Cross_{MSB}).$$

Bit 2 – Invert Output

This bit inverts the output bits of both the I and Q Channels. The inversion will occur at the output pins RXOUT, RXIOUT, and RXQOUT.

When this bit is set low, the outputs are not inverted; when it is set high, the outputs are inverted.

Output Processor Control Registers

Address 37_H:

Bit 0 — NCO Enable

The function of this bit is to allow the power consumed by the operation of the NCO circuitry to be minimized when the Z87200 is not receiving. The NCO can also be disabled while the Z87200 is transmitting provided that the Z87200's on-chip BPSK/QPSK modulator is not being used. With the instantaneous acquisition properties of the PN Matched Filter, it is often desirable to shut down the receiver circuitry to reduce power consumption, resuming reception periodically until an Acquisition/Preamble symbol is acquired. Setting bit 0 low holds the NCO in a reset state; setting bit 0 high then reactivates the NCO, where it is necessary to reload the frequency control word into the NCO. Note that this bit operates independently of bits 1 (Transmitter Enable) and 2 (Receiver Enable), where those bits have similar control over the transmit and receive circuitry, respectively.

Bit 0 of address 37_H performs the same function as MNCOEN, and these two signals are logically ORed together to form the overall control function. When bit 0 is set low, MNCOEN controls the activity of the NCO circuitry and, when MNCOEN is set low, bit 0 controls the activity of the NCO circuitry. When either bit 0 or MNCOEN (whichever is in control, as defined above) goes low, a reset sequence occurs on the following RXIFCLK cycle to virtually disable all of the NCO circuitry, although the user programmable control registers are not affected by the power down sequence. Upon reactivation (when either MNCOEN or bit 0 of address 37_H return high), the NCO must be reloaded with frequency control information either by means of the MFLD input or by writing 01_H into address 00_H.

Bit 1 — Transmitter Enable

A rising edge on this bit causes the transmit sequence to begin so that the Z87200 first transmits a single Acquisition/Preamble symbol followed by data symbols. Bit 1 of address 37_H should be set low after the last symbol has been transmitted to minimize power consumption of the transmitter circuit. Bit 1 of address 37_H operates independently of bits 2 and 0, where those bits have similar control over the receive and NCO circuitry, respectively.

When input signal MTXEN is set low, bit 1 of address 37_H controls the activity of the transmit circuitry and, when MTXEN is set low, bit 1 controls this function. When either bit 1 or MTXEN (whichever is in control, as defined above) goes low, a reset sequence occurs on the following TXIFCLK cycle to virtually disable all of the transmitter data path, although the user programmable control registers are not affected by the power down sequence.

Bit 2 — Receiver Enable

The function of this bit is to allow power consumed by the operation of the receiver circuitry to be minimized when the device is not receiving. With the instantaneous acquisition properties of the PN Matched Filter, it is often desirable to shut down the receiver circuitry to reduce power consumption, resuming reception periodically until an Acquisition/Preamble symbol is acquired. Setting bit 2 low reduces the power consumption substantially. When bit 2 is set high, the receiver will automatically power up in acquisition mode regardless of its prior state when it was powered down. Bit 2 of address 37_H operates independently of bits 1 and 0 of address 37_H, where these signals have similar control over the transmit and NCO circuitry, respectively.

Bit 2 of address 37_H performs the same function as MRXEN, and these two signals are logically ORed together to form the overall control function. When bit 2 of address 37_H is set low, MRXEN controls the activity of the receiver circuitry and, when MRXEN is set low, bit 2 of address 37_H controls the activity of the receiver circuitry. When either bit 2 or MRXEN (whichever is in control, as defined above) goes low, a reset sequence begins on the following RXIFCLK cycle and continues through a total of six RXIFCLK cycles to virtually disable all of the receiver data paths. The user- programmable control registers are not affected by the power down sequence, with the exception of $RXTEST_{7-0}$ (address 38_H), which is reset to 0. If the $RXTEST_{7-0}$ bus is being used to read any function other than the PN Matched Filter I and Q inputs, the value must be rewritten.

Address 38_H:

Bits 3-0 — $RXTEST_{7-0}$ Function Select

The data stored in bits 3-0 of address 38_H selects the signal available at the $RXTEST_{7-0}$ bus (pins 41-48). These pins provide access to 16 test points within the receiver according to the data stored in bits 3-0 of address 38_H and the assignments shown in The validity of the $RXTEST_{7-0}$ outputs at RXIFCLK speeds greater than 20 MHz is dependent on the output selected: outputs that change more rapidly than once per symbol may be indeterminate.

Note that the reset sequence that occurs when the receiver is disabled will also reset the contents of address 38_H to a value of 0. If the RXTEST7-0 bus is to be used to observe any function other than the PN Matched Filter I and Q inputs, then the appropriate value must be rewritten.

Address 39_H:

Bits 6-0 — Matched Filter Power Saver

The data stored in bits 6-0 of address 39_H allows the unused sections of the PN Matched Filter to be turned off when the PN Matched Filter is configured to be less than 64 taps long for data symbols. All taps are always fully powered when the device is in acquisition mode.

The PN Matched Filter is split into seven 9-tap sections, and the power to each section is controlled by the settings of bits 6-0 of address 39_H, as shown in Table 19.

Table 19. Matched Filter Tap Power Control

Bit in Addr. 39_H	MF Taps Controlled
0	1-9
1	10-18
2	19-27
3	28-36
4	37-45
5	46-54
6	55-64

Power control is not provided for Tap 0, the first tap of the PN Matched Filter, since Tap 0 is always used no matter what the PN code length. Setting a bit high in bits 6-0 of address 39_H turns off the power to the corresponding block of taps of the PN Matched Filter. The power should only be turned off to those blocks of taps for which all the tap coefficients in that block have been set to zero

Address $3A_H$:

Receiver Data Symbols per Burst (bits 15-8)

The data stored as two bytes in addresses $2E_H$ (LS byte) and $3A_H$ (MS byte) defines the number of data symbols per burst. This unsigned value must range from 3 to 65,535 (0003_H to $FFFF_H$), and the number of data symbols per burst will be this value minus 2, giving a range of 1 to 65,533. Note that the range is slightly different from that in the transmitter. Once the number of received data symbols processed exceeds this number, the burst is assumed to have ended and the Z87200 immediately returns to acquisition mode to await the next burst.

CONTROL REGISTERS (Continued)

Address $3B_H$:

Bit 0 — Matched Filter Loopback Enable

The Z87200 incorporates a loopback capability that feeds the encoded and spread transmit signals TXIOUT and TXQOUT directly into the PN Matched Filter inputs. This test mode allows the baseband portion of the system to be tested independently of the BPSK/QPSK Modulator and Downconverter.

Setting bit 0 of address $3B_H$ high enables this loopback path; setting it low puts the device into its normal operating mode.

Bit 1 — I.F. Loopback Enable

The Z87200 incorporates a loopback capability that feeds the encoded, spread and modulated transmit signal $TXIFOUT_{7-0}$ directly into the receiver $RXIIN_{7-0}$ input. This test mode allows the entire digital portion of the system to be tested. Since only the I channel is provided as an input, I.F. loopback requires that the PN chip rate and RXIFCLK rate be consistent with Direct I.F. Sampling Mode.

Setting bit 1 of address $3B_H$ high enables this loopback path; setting it low puts the device into its normal operating mode.

Bits 3-2 — Receiver Overlay Select

The Z87200 incorporates programmable overlay code generators in both the transmitter and receiver. When enabled, the selected receiver overlay code is subtracted from the data symbols, one overlay bit per symbol in both BPSK and QPSK modes. No synchronization beyond the burst acquisition synchronization that is intrinsic to operation of the Z87200 is required since the overlay code generators in both the transmitter and the receiver are automatically reset at the start of each burst. The addition of the overlay code randomizes the transmitted data sequence to guarantee that the spectrum of the transmitted signal will be adequately whitened and will not contain a small number of spectral lines even when the data itself is not random.

Three transmit and receive overlay codes can be selected, where they are each maximal length sequences with lengths of 63, 511 and 1023 symbols. The receiver overlay codes are enabled and selected by the settings of bits 3-2 of address $3B_H$, as shown in Table 19.

Table 20. Receiver Overlay Code Select

Bits 3-2 in Addr. $3B_H$	Overlay Code Length and Polynomial
0	Overlay Code Disabled
1	63: $1 + x^{-2} + x^{-3} + x^{-5} + x^{-6}$
2	511: $1 + x^{-2} + x^{-3} + x^{-5} + x^{-9}$
3	1023: $1 + x^{-2} + x^{-3} + x^{-5} + x^{-10}$

Addresses $3C_H$ through $3F_H$: Unused

Transmit Control Registers

Address 40_H:

Bit 0 — Transmit BPSK

This bit configures the transmitter for either BPSK or QPSK mode transmission. and differential encoding.

If programmed for BPSK mode, data is requested by the Z87200 by a rising edge of output signal TXBITPLS, where TKBITPLS is generated once per symbol, one chip period before the end of the current symbol. At the end of the symbol duration, the TXIN data is latched into the device. TXBITPLS falls low immediately following the rising edge of TXIFCLK, which latches the TXIN value, and is generated repeatedly at the symbol rate as long as the input signal MTXEN remains high.

In QPSK mode, data is requested by the Z87200 by a rising edge of output signal TXBITPLS, where this signal is generated in this mode twice per symbol, first one chip period before the middle of the symbol and then one chip period before the end of the symbol. TXBITPLS requests the data exactly one chip cycle before latching the TXIN data into the device. TXBITPLS falls low immediately following the rising edge of TXIFCLK, which latches the TXIN value.

When bit 0 of address 40_H is set low, the transmitter is configured in QPSK mode; when it is set high, the transmitter is configured in BPSK mode.

Bit 1 — Offset Binary Output
The $TXIFOUT_{7-0}$ output signals can be in either two's complement or offset binary formats. Since all internal processing in the device uses two's complement format signals, the MSB of the two's complement modulated transmitter output must be inverted if the output is to be in offset binary format.

When this bit is set high, the $TXIFOUT_{7-0}$ output will be in offset binary format and, when it is set low, the signal will be in two's complement format. In two's complement format, the 8-bit output values range from –128 to +127 (80_H to $7F_H$); in offset binary format, the values range from 0 to +255 (00_H to FF_H).

Bit 2 — Manual Chip Clock Enable
This bit enables the PN chip rate to be controlled by either the internal chip rate clock generator or by the external input signal TXMCHP. The TXMCHP input allows the user to manually insert a single PN chip clock pulse or continuous stream of pulses. This feature is useful in cases where a specific chip rate is required that cannot be derived by the internal clock generator which generates clocks of integer sub-multiples of the frequency of TXIFCLK. The signal is internally synchronized to TXIFCLK to avoid race or hazard timing conditions.

When this bit is set high, TXMCHP will provide the PN chip rate clock; when it is set low, the clock will be provided by the internal chip rate clock generator controlled by bits 5-0 of address 41_H.

Bit 3 — Invert Symbol
This bit allows the user to invert the I and Q channel bits following differential encoding and before being spread by the PN code. This function has the same effect as inverting the PN code, which may be useful in some cases.

When this bit is set high, the encoded I and Q channel bits will be inverted; when it is set low, the I and Q channel bits will not be inverted.

Address 41_H:

Bits 5-0 — TXIFCLK Cycles per Chip
Bits 5-0 set the transmitter baseband PN chip rate to the frequency of TXIFCLK/(n+1), where n is the value stored in bits 5-0. The value of the data stored in bits 5-0 must range from 1 to 63 (01_H to $3F_H$). This feature is useful when the PN chip rate required is an integer sub-multiple of the frequency of TXIFCLK. In cases where a chip rate is required that is not an integer sub-multiple of the frequency of TXIFCLK, the rate may be controlled externally using TXMCHP.

Address 42_H:

Bits 5-0 — Tx Chips per Data Symbol
The number of chips per data symbol in the transmitter is stored in bits 5-0 of address 42_H. The unsigned value must range from 1 to 63 (01_H to $3F_H$), and the number of chips per data symbol will be this value plus 1. This value controls data symbol timing in the transmitter.

Address 43_H:

Bits 5-0 — Tx Chips per Acquisition/Preamble Symbol
The number of chips per Acquisition/Preamble symbol in the transmitter is stored in bits 5-0 of address 43_H. The unsigned value must range from 1 to 63 (01_H to $3F_H$), and the number of chips per data symbol will be this value plus 1. This value controls the Acquisition/Preamble symbol timing in the transmitter.

Addresses 44_H through $4B_H$:

Transmitter Acquisition/Preamble Symbol Code
Each Z87200 burst transmission begins with an Acquisition/Preamble symbol and is then followed by the actual information data symbols. Two separate and independent PN codes can be employed, one for the Acquisition/Preamble symbol, the other for the information symbols. Accordingly, the Z87200 Transmit PN Code Generators, like the receiver's PN Matched Filter, support independent PN codes up to 64 chips in length for the two modes. Addresses 44_H to $4B_H$ contain the binary Transmitter Acquisition/Preamble Symbol PN code chip values, where the configuration of the stored bits is as shown in Table 20.

Table 21. Acquisition/Preamble Symbol Codes

Addr $4B_H$, Bits 7-0 Code Bits 63-56
••••••••• •••••••••
Addr 45_H, Bits 7-0 Code Bits 15-8
Addr 44_H, Bits 7-0 Code Bits 7-0

The length, N, of the Acquisition/Preamble symbol code is set by the value of (N-1) stored in bits 5-0 of address 43_H. An internal counter begins the transmission with the PN code chip corresponding to that value. The last chip transmitted per symbol is then code chip 0. Note that this convention agrees with that used for the Z87200's PN Matched Filter: for a code of length N, code chip (N-1) will be the first chip transmitted and will first be processed by Tap 0 of the PN Matched Filter; the last chip per symbol to be transmitted, however, will be chip 0, and at that time chip (N-1) will be processed by Tap (N-1) and chip 0 by Tap 0 to achieve peak correlation. Operation with the subsequent data symbols is analogous.

CONTROL REGISTERS (Continued)

Address $4C_H$ through 53_H:

Data Symbol Code

Addresses $4C_H$ to 53_H contain the binary Data Symbol PN code sequence values. The storage capacity, assignments, and operation are similar to that of the Acquisition/Preamble PN code sequence values. The configuration of the bits stored is as shown in Table 22.

Table 22. Data Symbol Codes

Addr 53_H, Bits 7-0 Code Bits 63-56
••••••••• •••••••••
Addr $4D_H$, Bits 7-0 Code Bits 15-8
Addr $4C_H$, Bits 7-0 Code Bits 7-0

Transmit Control Registers

Address 54_H:

Bits 1-0 — Transmitter Overlay Select

The Z87200 incorporates programmable overlay code generators in both the transmitter and receiver. When enabled, the selected transmitter overlay code is subtracted from the data symbols, one overlay bit per symbol in both BPSK and QPSK modes. No synchronization is required since the codes in both the transmitter and the receiver are automatically synchronized by resetting the code generators at the start of each burst. The addition of the overlay codes randomizes the transmitted data sequence to guarantee that the spectrum of the transmitted signal will be adequately whitened and will not contain a small number of spectral lines even when the data itself is not random. Three transmit and receive overlay codes can be selected, where they are each maximal length sequences with lengths of 63, 511 and 1023 symbols. The transmitter overlay codes are enabled and selected by the settings of bits 1-0 of address 54_H, as shown in Table 23.

Table 23. Transmitter Overlay Code Select

Bits 1-0 in Addr. 54_H	Overlay Code Length and Polynomial
0	Overlay Code Disabled
1	63: $1+x^{-2}+x^{-3}+x^{-5}+x^{-6}$
2	511: $1+x^{-2}+x^{-3}+x^{-5}+x^{-9}$
3	1023: $1+x^{-2}+x^{-3}+x^{-5}+x^{-10}$

Bit 2 —Transmitter Symbols Per Burst Off

Bit 2 of address 54_H is not used and must always be set low (0).

Address 55_H through 56_H:

Transmitter Data Symbols per Burst (bits 15-0)

The data stored as two bytes in addresses 55_H (LS byte) and 56_H (MS byte) defines the number of data symbols per burst for the transmitter. This unsigned value must range from 1 to 65,535 (0001_H to $FFFF_H$), and the number of data symbols per burst will be this value plus 1. Note that the range is slightly different from that in the receiver. Once the number of transmitted data symbols exceeds this number, the burst is assumed to have ended and the transmitter is immediately turned off. If the data value is set to 0000_H, then the symbols per burst counter is disabled, permitting the Z87200 to be used for continuous transmission of data.

REGISTER SUMMARY

Table 24. Register Summary

	Contents							
Address	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
00_H								NCO Load
01_H	Integrate and Dump Filter Viewport Control				2's C. Input	NCO C'In	Inv. LF	RXMSMPL
02_H			Receiver Baseboard Sampling Rate Control					
$03\text{-}06_H$	NCO Frequency Control Word (32 bits)							
$07\text{-}16_H$	Matched Filter Acquisition/Preamble Symbol Coefficients							
27_H								FEP Disable
28_H							MF Viewport Control	
$29\text{-}2A_H$	Acquisition/Preamble Symbol Threshold, Bits 9-0							
$2B\text{-}2C_H$	Data Symbol Threshold, Bits 9-0							
$2D_H$			Receiver Chips Per Data Symbol					
$2E_H$	Receiver Data Symbols per Burst, Bits 7-0							
$2F_H$	Missed Detects Per Burst Threshold							
30_H		Rx Symb/ Burst Off	Missed Det. Per Bst. Off	Half Symb Pulse Off	Bypass Max Power Sel.	Force Cont. Acquis.	Manual Punctual	Man. Det. Enable
31_H								Man. Det.
32_H								Man. Abort
33_H	AFC Viewport Control				LF Clr. Dis.	Unused (0)	Signal Rotation Control	
34_H		Carry In 1/2	K2 On	K2 Gain Value				
35_H		L2 Freeze	K1 On	K2 Gain Value				
36_H						Inv. O/p	BPSK En.	Rev. I & Q
37_H						Rx. En.	Tx. En.	NCO En.
38_H					RXTEST7-0 Function Select			
39_H	Matched Filter Power Saver							
$3A_H$	Receiver Data Symbols per Burst, Bits 15-8							
$3B_H$					Receiver Overlay Sel		IF Lpbk En	MF Lpbk En
$3C\text{-}3F_H$								
40_H					Inv. Symb.	TXMXHP	O'Bin. O/p	TX BPSK
41_H			TXIFCLK Cycles per Chip					
42_H			Tx Chips per Data Symbol					
43_H			Tx Chips per Acquisition/Preamble Symbol					
$44\text{-}4B_H$	Transmitter Acquisition/Preamble Code (64 bits)							
$4C\text{-}53_H$	TransmitterData Symbol Code (64 bits)							
54_H							Unused (0)	Transmitter Overlay Select

THEORY OF OPERATION

The Z87200 receiver's downconverter circuitry allows use of two distinct modes, where the mode chosen will depend upon the application. In applications where the received PN chip rate is less than approximately 1/8 of the I.F. sample clock (RXIFCLK) rate, the Z87200 can be used with a single A/D converter (ADC) and operate in Direct I.F. Sampling Mode. For higher chip rate applications, it is necessary to use the Z87200 in the full Quadrature Sampling Mode; that is, using a quadrature signal source, two ADCs, and the on-chip NCO in its quadrature mode.

Using the Z87200 with a Single ADC in Direct I.F. Sample Mode

Direct I.F. Sampling Mode allows one rather than two ADCs to be used, as will be explained below. If appropriate for the application, use of Direct I.F. Sampling Mode can reduce the system cost since quadrature downconversion with its associated 90° signal separation and the second ADC used in Quadrature Sampling Mode are not required. The trade-off, however, is in the lower maximum PN chip rate that can be supported by the Z87200 in Direct I.F. Sampling Mode as compared to the maximum rate that can be supported by Quadrature Sampling Mode.

In Direct I.F. Sampling Mode, the sampled signal is presented as input to the receiver's I channel input (RXIIN) and the Q channel input (RXQIN) is held to zero (where "zero" is defined by the ADC input format). As a result, only two of the four multipliers in the Downconverter's complex multiplier are used and the device does not make a true single-sideband downconversion from I.F. to baseband. In Quadrature Sampling Mode, by contrast, quadrature inputs to two ADCs provide I and Q inputs to the Z87200 and the full complex multiplier is used. An illustration of the operation of Direct I.F. Sampling Mode is shown in the frequency domain in Figure 11, where the spectra have been drawn asymmetrically so that spectral inversions can be readily identified.

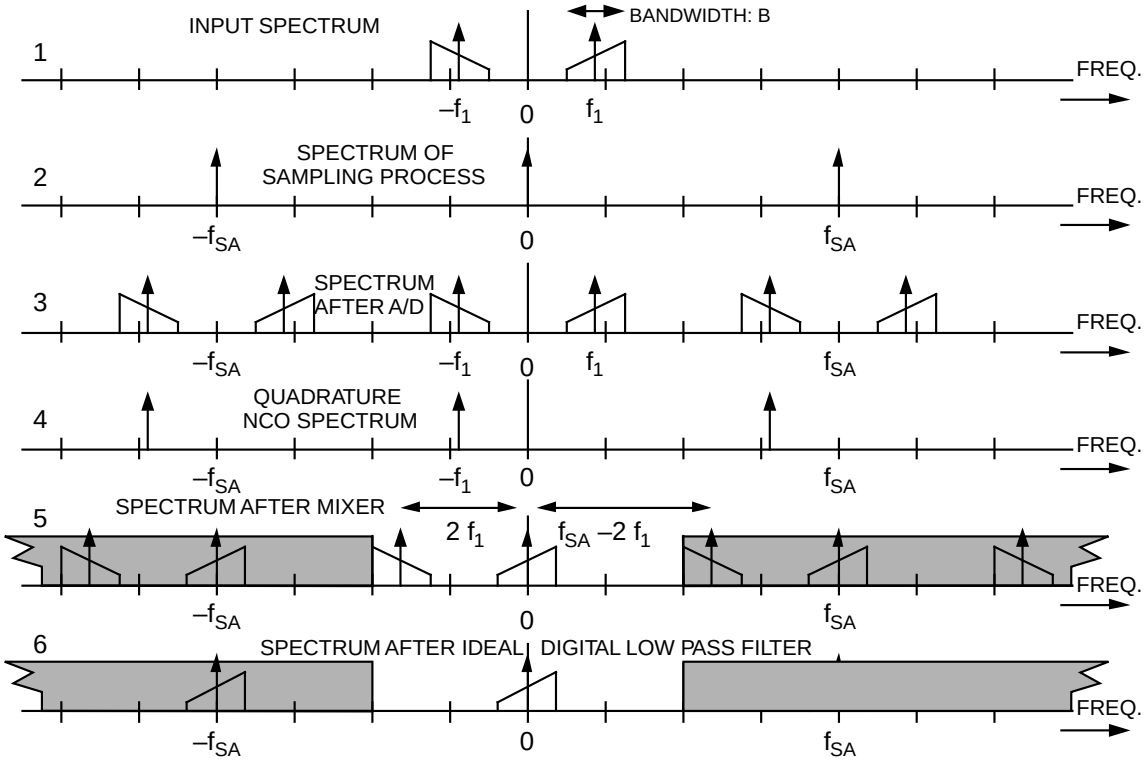


Figure 11. Spectra of Signals in Direct I.F. Sampling Mode

The spectrum of a real input signal with center (I.F.) frequency of f1 and signal bandwidth B is shown in line 1 of Figure 13. The bandwidth B is the two-sided bandwidth, corresponding to a PN chip rate of 1/2 B Mcps. Note that throughout this discussion it is assumed that the signal bandwidth does not exceed $1/2f_{SA}$; that is, $B < 1/2f_{SA}$. Otherwise, the mixing and sampling processes to be described will result in destructive in-band aliasing. Also, clearly, the I.F. frequency must be able to support the signal bandwidth; that is, 1/2B<f1.

The input signal is sampled at the frequency f_{SA}, where the sampling spectrum is shown in line 2 and the resulting spectrum is shown in line 3. As can be seen, the fundamental and harmonics of the sampling frequency result in images of the input signal spectrum at other frequencies, where here the images are centered about multiples of the sampling frequency. In other words, the spectrum of the sampled signal shown in line 3 contains aliases of the input signal at frequencies $f1 \pm n\ f_{SA}$, where n can assume both positive and negative integer values. Since the sampling process is linear, no spectral inversion occurs; that is, the original spectrum is translated along the frequency axis with no mirror reflections of the input spectrum created.

The Z87200's NCO provides a quadrature (sine and cosine) output that defines a complex signal. Line 4 shows its spectrum as an impulse at frequency -f1, where the minus sign reflects the signal's use in downconversion and the absence of a positive impulse at frequency +f1 results because the NCO output is truly complex. Aliases of this impulse are shown offset by integer multiples of f_{SA} to reflect the sampled nature of the NCO output. When the input sampled signal of line 3 is then modulated with the complex signal of the Z87200's quadrature NCO of line 4, the signal spectrum after mixing is as shown in line 5. The sections shown inside the shaded areas are the aliases of the baseband signal beyond the Nyquist frequency and are not of concern. The signals inside the primary baseband Nyquist region ($|f| < 1/2\ f_{SA}$) consist of the desired signal and a spectrally reversed or inverted image signal with center frequency separated from that of the desired signal by 2 f1, twice the I.F. frequency before sampling. This image signal can be removed by a subsequent ideal lowpass filter as shown in line 6.

In Figure 13, the input signal is shown at a low I.F. frequency such that $f1 < 1/2\ f_{SA}$; that is, the signal is only defined inside the primary Nyquist region. Provided, however, that $B < 1/2\ f_{SA}$, that condition need not be true as long as the input spectrum is only defined for frequencies within a non-primary Nyquist region; that is, defined only over frequencies f such that

$$(n-1/2)f_{SA} < |f| < (n+1/2)f_{SA}$$

for positive integer n.

Direct I.F. Sampling Mode with this type of signal is shown in Figure 14, where it can be seen that in line 3 the diagram's high frequency input has the same spectrum after sampling as does the low frequency input in Figure 11; consequently, all subsequent operations are identical to those in Figure 13.

This result stems from the periodic nature of sampling: sampling an input frequency f1 is theoretically indistinguishable from sampling an input frequency $(n\ f_{SA} + f1)$ for positive integer n and positive $f1 < 1/2\ f_{SA}$. A slightly different result obtains, however, when sampling an input frequency $(n\ f_{SA} - f1)$, again for positive integer n and positive $f1 < 1/2\ f_{SA}$. In this case, the positions of the spectrally inverted and spectrally correct aliases will be interchanged when compared with an input frequency of $(n\ f_{SA} + f1)$. As a consequence, the desired baseband signal after downconversion and filtering will also be spectrally inverted. This phenomenon is equivalent to high-side conversion; that is, downconversion of a signal by means of a local oscillator at a frequency higher than the carrier frequency. If the modulation type is QPSK, demodulation of a spectrally inverted signal will result in the inversion of the Q channel data (which can be readily corrected); if the modulation type is BPSK, there is no effect on the demodulated data.

THEORY OF OPERATION (Continued)

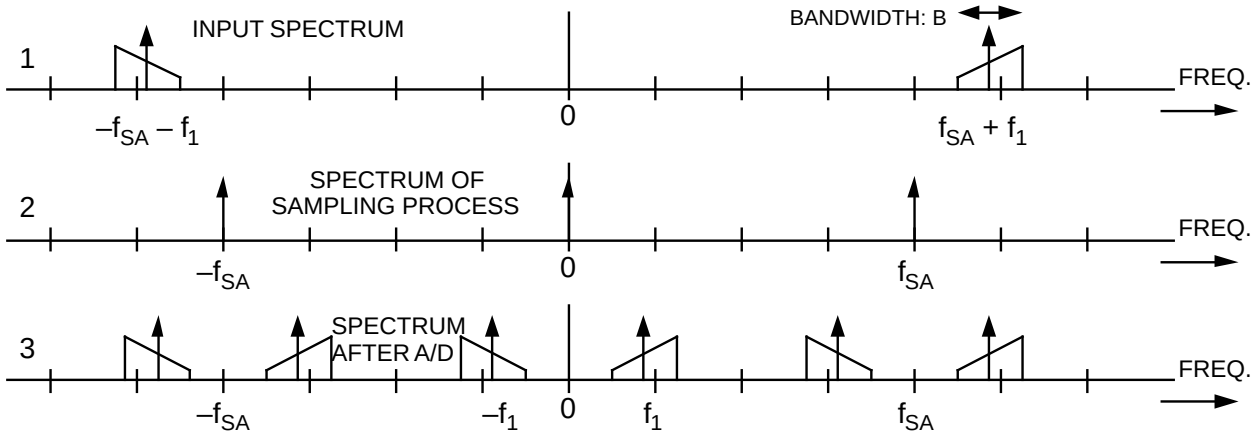


Figure 12. Direct I.F. Sampling Mode with I.F. Frequency ($f_{SA}+f_1$) > Sampling Frequency f_{SA}

The above discussion has assumed ideal low-pass filtering to recover the desired signal at baseband, but, in the Z87200's Downconverter, an ideal low-pass filter is not available. The quadrature Integrate and Dump filter of the Downconverter serves this purpose instead. The Downconverter's Integrate and Dump filter is a decimation filter, integrating input samples over a programmable number of sample periods, N, so that the output sampling rate is (1/N)th of the input sampling rate and the I.F. sampling rate fSA is decimated to the baseband sampling rate. Since the Z87200's PN Matched Filter requires two samples per chip, the baseband sampling rate must be at twice the PN chip rate and N must equal f_{SA}/B. When the sampling rate is much greater than the signal bandwidth (or, equivalently, the chip rate), the Integrate and Dump filter is most effective in attenuating the unwanted aliased image. This performance can be seen from the transfer function G(w) of a decimation filter, where:

$$G(w) = \sin(w')/w' \text{ and } w' = (2\pi Nf)/f_{SA}.$$

Figure 13 shows a plot of the gain of this transfer function as a function of the normalized frequency ($N f/F_{SA}$). To effect the desired low-pass filter and eliminate the aliased image in the baseband Nyquist region appearing in line 5 of Figure 11, the attenuation must be suitably high for frequencies greater than, in the worst case, 1/2 B. Given a defined signal bandwidth B, however, judicious choice of f1 and f_{SA} allows a higher break frequency to be chosen, as will be discussed.

As an extreme worst case, if $f1 = 1/4f_{SA}$ and $B=1/2f_{SA}$, corresponding to the highest chip rate that can be handled for a given value of f_{SA}, then the break frequency must be 1/2B (equal to $1/4f_{SA}$). In this example, then, $N = f_{SA}/B=2$ and the attenuation provided by the Integrate and Dump filter is given by the curve of Figure 13 for values of ($N f/f_{SA}$) greater than 1/2. As can be seen, the attenuation will be at least equal to the peak of the corresponding lobe or at least ~13 dB. This sidelobe peak is a worst case, and much of the alias energy outside the desired band will be attenuated by more than 13 dB. Nonetheless, the presence of unattenuated energy from the unwanted alias degrades performance. It is for this reason that Direct I.F. Sampling Mode is only recommended for received PN chip rates less than 1/8 f_{SA}; in other words, for $B<1/4\ f_{SA}$. The attenuation realized by the Integrate and Dump filter is then further determined by the choice of the I.F. frequency f_1 and the I.F. sampling rate f_{SA}.

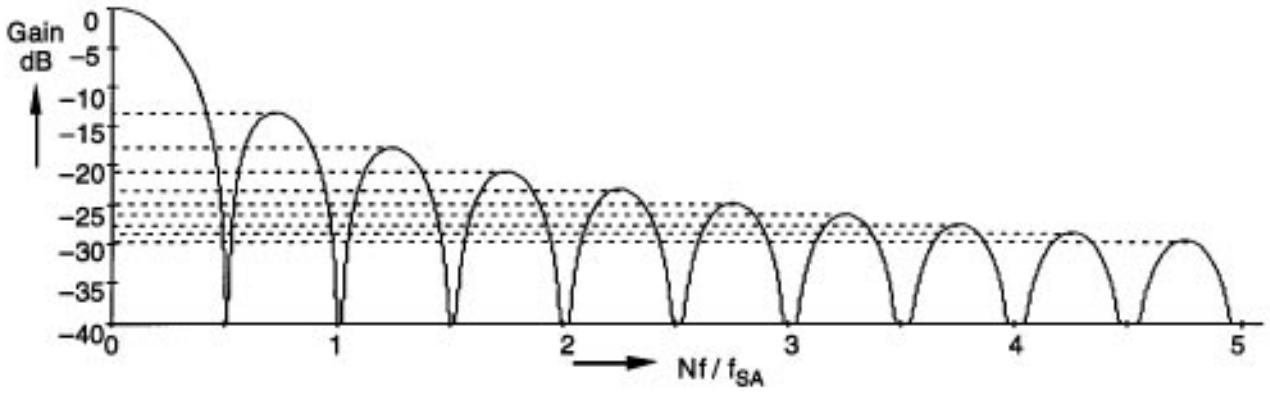


Figure 13. G(ω) = dom (ω')/ω', where ω' = (2πNf)/f_{SA}

The choice of the I.F. frequency and sampling rate is crucial so that the unwanted alias of the signal in the baseband Nyquist region lies as far as possible from the desired signal to permit maximum attenuation. The optimum separation of the desired signal and the unwanted alias occurs when the alias is centered at the bounds of the baseband Nyquist region, | f | =1/2 f_{SA} as shown in Figure 14. In this case, the desired signal is equally spaced from the unwanted aliases in both the positive and negative frequency domains and f1 = 1/4 f_{SA}. Consider, then, the worst case appropriate for Direct I.F. Sampling Mode. If B<1/4 f_{SA} as has been said to be appropriate for Direct I.F. Sampling Mode, then N=f_{SA}/B=4, the break frequency is 3 /8 f_{SA} or greater, and the attenuation provided by the Integrate and Dump filter is given by the curve of Figure 13 for values of (N f/f_{SA}) greater than 3/2. Here, the attenuation is at least ~21 dB, offering much better attenuation of the unwanted alias than in the previous worst case example. Further analysis shows that if the input SNR is 15 dB, then the alias attenuated by 21 dB will reduce the SNR by approximately 1 dB.

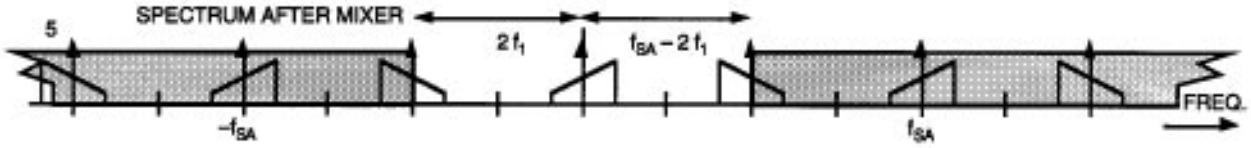


Figure 14. Optimum Condition for Bandpass Sampling

THEORY OF OPERATION (Continued)

The optimum choice of I.F. frequency discussed above can be extended beyond the primary Nyquist region. Since an I.F frequency of n f_{SA} + f1 produces exactly the same result for any value of n, the general condition for optimum separation of the desired signal and the unwanted alias is:

$$f1 = n\ f_{SA} + 1/4\ f_{SA} \text{ and } B < 1/2\ f_{SA}$$

for positive integer n and positive B and f_1.

And, if care is taken to handle the effect of high side conversion, the following I.F. frequencies also fulfill the optimum condition:

$$f1 = n\ f_{SA} 1/4\ f_{SA} \text{ and } B < 1/2\ f_{SA}$$

for positive integer n and positive B and f_1.

Using the Z87200 with Two ADCs in Quadrature Sampling Mode

Quadrature Sampling Mode requires that quadrature I and Q channel I.F. inputs are sampled by two ADCs and input to the Z87200's Downconverter. All four multipliers of the Downconverter's complex multiplier are then used to perform true single sideband downconversion to baseband. Quadrature inputs imply that the input signal is complex, and the input signal spectrum shown in line 1 of Figure 15 is thus only single-sided with no mirror image spectral component. As a result, the image alias within the primary Nyquist region associated with Direct I.F. Sampling Mode does not appear and does not have to be attenuated by the Integrate and Dump filter. As in the prior discussion, this analysis holds as long as B < 1/2 f_{SA}, 1/2 B < f1, and the input spectrum is only defined for frequencies within a single Nyquist region; that is, non-zero over frequencies f such that:

$$(n-1/2)f_{SA} < |f| < (n+1/2)f_{SA}$$

for positive integer n.

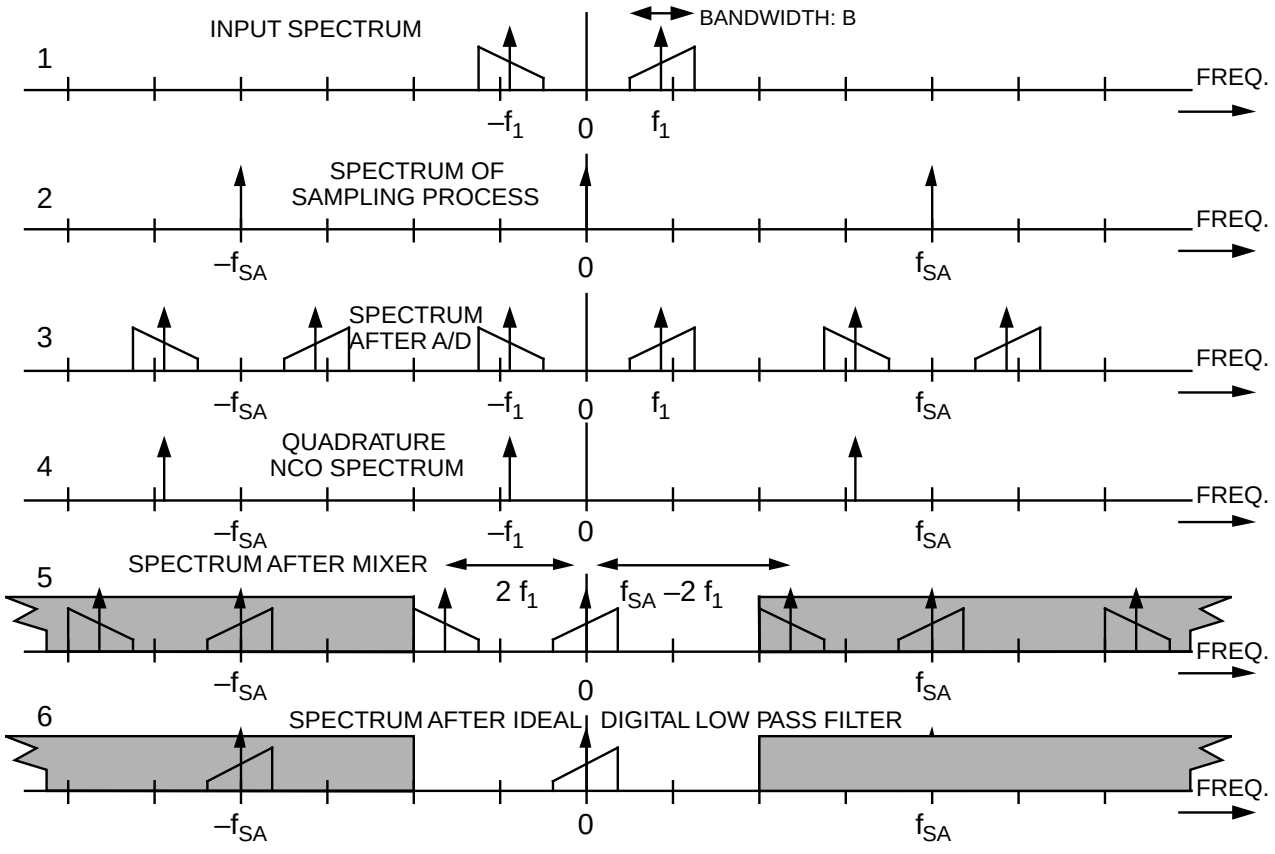


Figure 15. Spectra of Signals in Quadrature Sampling Mode

Differential Demodulation

As noted in the preceding text, computation of the "Dot" and "Cross" products is fundamental to operation of the DPSK Demodulator and Frequency Discriminator. Let I_k and Q_k represent the I and Q channel inputs, respectively, for the k^{th} symbol after downconversion and despreading. The Dot and Cross products can then be defined as:

$$Dot(k) = I_k\ I_{k-1} + Q_k\ Q_{k-1};\ \text{and,}$$

$$Cross(k) = Q_k\ I_{k-1} - I_k\ Q_{k-1}$$

In the complex domain, these products can be seen to have been defined to form the complex conjugate product between two input samples, one symbol apart. Let the k_{th} input sample, sin(k), be defined as:

$$s_{in}(k) = I(k) + j\ Q(k),$$

where I(k) and Q(k) are the 8-bit peak power PN Matched Filter I and Q channel outputs directed to the DPSK Demodulator. In polar form, $s_{in}(k)$ may be conveniently defined as:

$$s_{in}(k) = A(k)e^{\ j\varnothing(k)}$$

with

$$A(k)$$

$$\varnothing(k) = \arctan$$

Simple substitution then shows that the complex conjugate product between consecutive symbols (with an arbitrary phase shift introduced to the previous symbol value) may be expressed as:

$$s_{out}(k) = s_{in}(k)\ [s_{in}(k-1)\ .\ \omega_{fixed}]*$$

$$= Dot(k) + j\ Cross(k)$$

where

ω_{fixed} = arbitrary fixed phase rotation;

$Dot(k) = Re[s_{out}(k)]$; and,

$Cross(k) = Im[s_{out}(k)]*$

The fixed phase rotation ω_{fixed} has been introduced to later simplify the decision criteria. The ability to express real and imaginary parts of the complex conjugate product between consecutive symbols with the Dot and Cross products is the key to their use in DPSK demodulation.

DBPSK Demodulation

In DPSK, the phase difference between successive samples is due to the data modulation phase differences, $\Delta\varnothing$mod, plus any induced phase rotation between symbols, $\Delta\varnothing$rot, resulting from, for example, a frequency offset between the received signal's I.F. and that provided by the Downconverter. For DBPSK, the data modulation differences $\Delta\varnothing$mod can take only the values of 0° or 180°. Expressing the complex phase difference [Ø(k)-Ø(k-1)] in terms of these components, the decision can be seen to be based on:

$$Sout^{(k)} = A(k)\ A(k-1)\ e^{j\varnothing(k)*}e^{-j\varnothing(k-1)}$$

$$= A(k)*A(k1)*e^{j[\Delta\varnothing_{mod}(k)+\Delta\varnothing_{rot}(k)]}$$

For DBPSK, only the real part of sout(k), Dot(k), is needed to determine the modulated phase transition:

$$Dot(k) = A(k)*A(k-1)*\cos(\Delta\varnothing_{mod}(k)+\Delta\varnothing rot(k))$$

$$= \pm A(k)*A(k-1)*\cos(\Delta\varnothing_{rot}(k))$$

where the sign is determined by the transmitted data since $\cos[\Delta\varnothing_{mod}(k)] = \pm 1*$ As a result,

$$Dot(k) \approx \pm A^2(k)$$

if the amplitude of the signal is constant for consecutive symbols and if the phase rotation $\Delta\varnothing_{rot}(k)$ between symbols is small. The Z87200 DPSK Demodulator can thus use the sign of the Dot product in order to make DBPSK symbol decisions without the introduction of any fixed phase rotation.

THEORY OF OPERATION (Continued)

DQPSK Demodulation

For DQPSK modulation, the possible phase shifts between successive symbols due to the modulation are 0°, 90°, 180°, and 270°. Here, introduction of a phase shift (ω_{fixed}) of ±45° to the previous symbol in the calculation of the Dot and Cross products is desired in order shift the possible phase differences to 45°, 135°, 225°, or 315° so that the DQPSK decision boundaries coincide with the signs of the Dot and Cross products. In the Z87200 DPSK demodulator, phase rotation is accomplished in the signal rotation block by the following transformation of the I and Q channel values:

$$I_{rot}(k)=[\ I(k) - Q(k)]/2 \quad \text{for } 45^\circ \text{ rotation}$$

$$I_{rot}(k)=[\ I(k) + Q(k)]/2 \quad \text{for } -45^\circ \text{ rotation}$$

$$Q_{rot}(k)=[\ I(k) + Q(k)]/2 \quad \text{for } 45^\circ \text{ rotation}$$

$$Q_{rot}(k)=-[\ I(k) + Q(k)]/2 \quad \text{for } -45^\circ \text{ rotation}$$

The divide-by-2 is part of the signal rotation function. This transformation is equivalent to multiplying by $(1 \pm j)/2$ or $(1/\sqrt{2})e^{j\emptyset(fixed)}$ where $\emptyset_{fixed}$ is ±45°. In this case, $s_{out}(k)$ becomes:

$$s_{out}(k)=A(k).A(k-1)*e^{j\emptyset(k)*}e^{-j\emptyset(k-1)*}[\omega_{fixed}]*$$

$$=A(k).A(k-1)*e^{j[\Delta\emptyset_{mod}(k)+\Delta\emptyset_{rot}(k)]*}\ (1/\sqrt{2})e^{j\emptyset(fixed)}$$

$$\sqrt{I^2(K)+Q^2(k)}$$

$$\left(\frac{Q(k)}{I(k)}\right).$$

so that

$$Dot(k)\approx(1/\sqrt{2})A(k)*A(k-1)*\cos(\Delta\emptyset_{mod}(k) - \emptyset_{fixed})$$

$$Cross(k)\approx(1/\sqrt{2})A(k)*A(k-1)*\sin(\Delta\emptyset_{mod}(k) - \emptyset_{fixed})$$

where the phase rotation $\Delta\emptyset_{rot}(k)$ due to the frequency offset between symbols has been assumed negligible.

Assuming that the transmitted DQPSK modulation phasing is differentially encoded as defined in Table 3, the phase shift between consecutive symbols should always be set to –45°; that is, bits 1 and 0 of address 33_H should be set to 11. Similarly, when the transmission path from modulator to demodulator does not introduce a frequency (or phase direction) reversal, the "reverse I and Q" control function should be disabled; that is, bit 0 of address 36H should be set to 0. Note that, in the case of DBPSK, the phase increments are either 0 or 180° and frequency reversal has no impact.

If frequency reversal does take place, however, correct DQPSK demodulation can be achieved by enabling I and Q reversal; that is, the entry into bit 0 of address 36_H should be set to 1. Frequency reversal may occur in the up or down conversion process, depending on which mixing product is selected for further processing. No reversal occurs when the following conditions exist: when the mixing

A summary of the Dot(k) and Cross(k) products for the possible values of $\Delta\emptyset_{mod}(k)$ and $\emptyset_{fixed}$ is shown below, illustrating how the sign of the Dot and Cross products allow the symbol decision to be made:

	$\emptyset_{fixed}$ = -45°		$\emptyset_{fixed}$ = +45°		
$\Delta\emptyset_{mod}(k)$	Dot(k)	Cross (k)	$\Delta\emptyset_{mod}$ (k)	Dot(k)	Cross (k)
0°	$+A^2$	$+A^2$	0°	$+A^2$	$-A^2$
90°	$-A^2$	$+A^2$	90°	$+A^2$	$+A^2$
180°	$-A^2$	$-A^2$	180°	$-A^2$	$+A^2$
270°	$+A^2$	$-A^2$	270°	$-A^2$	$-A^2$

π/4 QPSK Demodulation

The Z87200 DPSK Demodulator decision logic is designed so that correct DQPSK decisions are made with a signal rotation of $\emptyset_{fixed}$= –45°. For π/4 QPSK modulation, however, the modulator itself inserts 45° between consecutive symbols, and the possible phase shifts between successive symbols due to modulation are 45°, 135°, 225°, and 315°. As a result, the DPSK Demodulator should be configured for π/4 QPSK with $\emptyset_{fixed}$=0°.

DQPSK Phasing and I/Q Channel Reversal

The Z87200 uses Differential BPSK and QPSK modulation and demodulation, meaning that the data is modulated on the carrier as phase changes. At the demodulator, the data is recovered by monitoring the phase change over a symbol period.

The Z87200 provides configuration control to specifically address DPSK phasing and I/Q channel reversal: the Signal Rotation control register, bits 0 and 1 of address 33_H, and the Reverse I and Q control register, bit 0 of address 36_H. The first register causes an insertion of ±45° in phase between consecutive symbols at the receiver, while the second register switches the I and Q channels presented to the DPSK demodulator. As discussed in the Z87200 appendix, the introduction of a phase shift between consecutive symbols changes the mapping of the input data with respect to the decision boundaries defined by the "Cross" and "Dot" product axes.

at the transmitter is performed by processing the sum frequency of the local oscillator and the modulator; when the mixing at the receiver is performed by subtracting the local oscillator from the incoming signal; and when the in-phase and quadrature inputs into the I and Q analog-to-digital converters are correctly connected such that the in-phase component leads the quadrature component by 90°. Under these conditions, bit 0 of address 36_H should be set to 0; otherwise, the I and Q channels may need to be reversed at the DPSK demodulator (by setting bit 0 of address 36_H to 1) in order to achieve proper demodulation.

Frequency Error Signal Generation

The frequency discriminator function or error signal is generated based on the Dot and Cross products. The objective is an error signal that is proportional to the sine of the phase difference between the present and prior symbol after correcting for the estimated phase increments due to data modulation. In the Z87200 Frequency Discriminator, the frequency error is calculated through a decision-directed cross-product algorithm and is then used with the Loop Filter to correct the NCO frequency. Assuming an input sin(k), where:

$$s_{in}(k) = I(k) + j\,Q(k),$$

the algorithm calculates the frequency discriminator function for DBPSK, $s_{AFC/BPSK}(k)$, as:

$S_{AFC/BPSK}(k)=SIGN[Dot(k)]*Cross(k)$

$=SIGN[Dot(k)]*A(k)*A(k-1)*sin(Ø(k)-Ø(k-1))$

$=SIGN[Dot(k)]*A(k)*A(k-1)*sin(\Delta Ømod(k) + \Delta Ørot(k))$

$\approx SIGN[Dot(k)]*A2(k)*cos[\Delta Ømod(k)]*sin[\Delta Ørot(k)]$

$\approx A2(k)*sin[\Delta Ørot(k)]*$

The final result assumes that the amplitude of the signal is constant over consecutive symbols and shows that the discriminator function is directly related to the change in phase between successive symbols. Since the interval between successive symbols is fixed, the discriminator function can be interpreted as a frequency error signal.

For DQPSK signals, the Z87200 computes the discriminator function $S_{AFC/QPSK}(k)$ as:

$S_{AFC/QPSK(}k)=SIGN[Dot(k)]$ Cross(k) - SIGN[Cross(k)] Dot(k),

where the above expression can be reduced to the same as for DBPSK,

$S_{AFC/QPSK}(k)\approx A2(k)*sin(\Delta Ørot(k))$.

BPSK/QPSK Modulation

The Z87200 incorporates a Direct Digital Synthesizer (DDS) to implement its on-chip BPSK/QPSK modulator. In the Z87200 design, the NCO and thus the sampling clock for the modulator is driven by fRXIFCLK; for this reason, both TXIFCLK and RXIFCLK must be common if the on-chip BPSK/QPSK modulator is to be used. The BPSK/QPSK modulator can then be used to generate the transmit output signal at a programmable IF frequency, thereby eliminating the need for an external modulator. Because it is a sampled data system like the Downconverter of the Z87200, however, care must be taken to ensure that the results of aliasing do not adversely affect the output transmit signal.

THEORY OF OPERATION (Continued)

In general, when a DDS is used to generate an unmodulated signal, the stepped sine wave generated by the DDS has spectral components at integer multiples of the DDS sampling clock. In other words, the Z87200's BPSK/QPSK modulator, when programmed to generate a signal at I.F. frequency f_{OUT}, will produce spectral components at $\pm f_{OUT}$ as well as at ($n_{RXIFCLK} \pm f_{OUT}$), where n is a positive or negative integer. Because of these aliases, one generally cannot program the NCO to provide an output frequency f_{OUT} greater than the Nyquist frequency $f_{RXIFCLK/2}$. When the I.F. frequency f_{OUT} is modulated, however, degradations to the output signal due to aliasing can result even when f_{OUT} is less than $f_{RXIFCLK/2}$.

In particular, the Z87200's PN modulation results in a transmit signal that has a power spectral density characterizable as a sinc function (sin(x)/x) centered about the I.F. frequency f_{OUT}. Nulls of the sinc function occur at integer multiples of the PN chip rate, and the null-to-null signal bandwidth of the Z87200's transmit signal about f_{OUT} is twice the transmit chip rate. The presence of modulation sidelobes and their interaction with aliases due to sampling, however, will result in distortion of the mainlobe of the baseband component centered at f_{OUT} unless attention is paid to the interaction of the chip rate, the I.F. frequency f_{OUT}, and the sampling rate fRXIFCLK.

In the example of Figure 18, the spectrum drawn in bold represents a signal where f_{OUT} has been programmed to be (0.4 x $f_{RXIFCLK}$) and has been PN-modulated at a chip rate of (0.1 x $f_{RXIFCLK}$). The first alias of the negative frequency version of this signal appears centered about (0.6 x $f_{RXIFCLK}$) and is shown as the lighter curve. As can be seen, energy of the second and third modulation sidelobes of the first alias is present within the mainlobe of the baseband component, resulting in distortion. One would typically filter the digital-to-analog converted output of the Z87200's BPSK/QPSK modulator to remove the energy outside the modulation mainlobe, but such filtering will not affect any aliasing distortion within the mainlobe as described here. Note that the nulls of the modulated signal aliases in this example coincide here only due to the choice of values for the I.F. frequency, sampling rate, and PN chip rate; in general, the nulls will not coincide. Note also that the filtering effect of sampling has been neglected in this discussion — in general, the aliases will be suppressed by a second sinc function, sin(f')/(f'), where f' = $\pi f/f_{RXIFCLK}$, but this effect is not very significant for the baseband component and first alias.

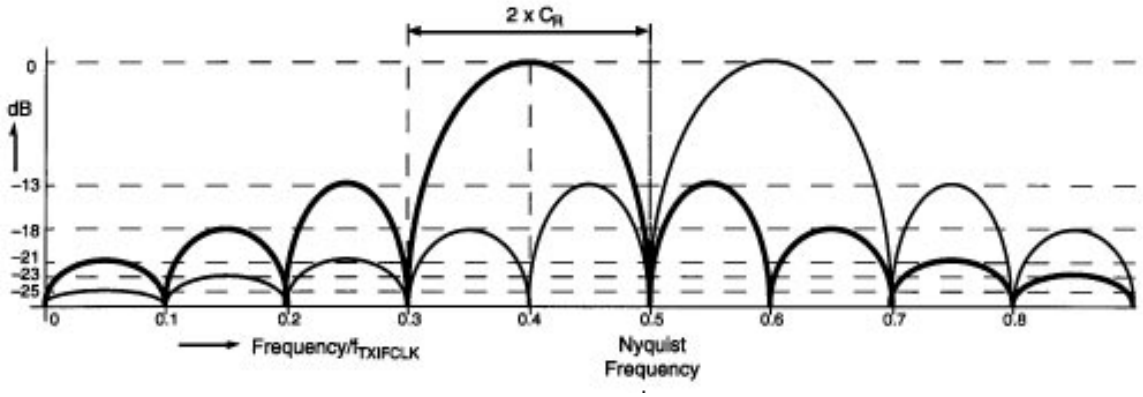


Figure 16. Spectrum of DDS modulated at 0.1 x $f_{RXIFCLK}$ when carrier frequency is set to 0.4 x $f_{RXIFCLK}$

The example of Figure 18 demonstrates that aliasing distortion of the BPSK/QPSK modulator output will result if significant energy of the baseband component's spectrum falls beyond the Nyquist frequency of $f_{RXIFCLK/2}$. The first alias will then shift that energy into the region below the Nyquist frequency and potentially interfere with the desired signal. In Figure 19 the second and third sidelobes of the first alias fall within the mainlobe of the baseband component, where the magnitude of this corrupting signal is approximately –13 dBc.

In Figure 20, by contrast, the level of distortion is considerably reduced by programming an I.F. frequency that increases the separation of the baseband mainlobe from the alias mainlobe. Here, the carrier frequency has been reduced to 0.25 x $f_{RXIFCLK}$, and now the fourth and fifth sidelobes of the first alias lie in the same part of the spectrum as the baseband mainlobe, reducing the distorting energy to approximately –23 dBc at the peak of the fourth sidelobe.

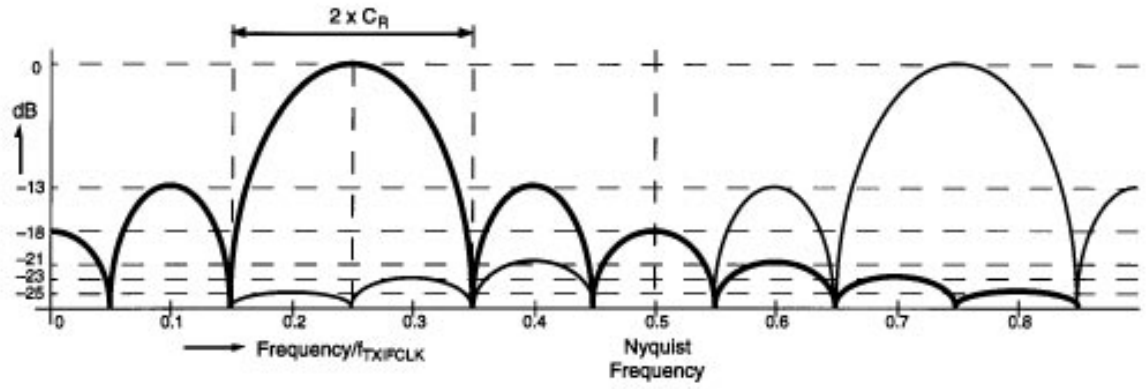


Figure 17. Spectrum of DDS modulated at 0.1 x $f_{RXIFCLK}$ when carrier frequency is set to 0.25 x $f_{RXIFCLK}$

THEORY OF OPERATION (Continued)

In both of the cases shown above, and especially the second, the level of the distortion is low enough so that the performance penalty would not be very great. And, of course, in a spread-spectrum system the effective distortion is reduced by the processing gain realized in despreading the signal at the receiver. In both of these examples, however, the PN chip rate is a very modest 10% of the frequency of the system clock; if the chip rate is increased to 40% of $f_{RXIFCLK}$, then the situation is very different, as shown in Figure 20.

In Figure 20, both the chip rate and the carrier frequency have been set at 40% of the clock frequency. As a result, the baseband mainlobe straddles the Nyquist frequency, and the first alias of the mainlobe overlaps the spectrum of the baseband mainlobe, thereby creating very significant aliasing distortion which cannot be eliminated by filtering. This level of distortion would severely affect the performance of the system and, in general, would be completely unacceptable.

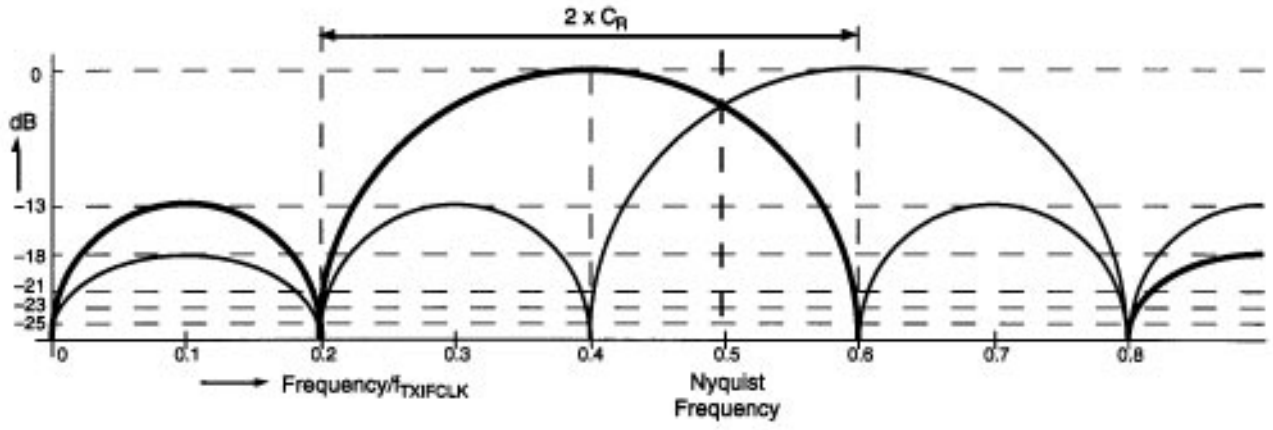


Figure 18. Spectrum of DDS Modulated at 0.4 x $f_{RXIFCLK}$ When Carrier Frequency is set to 0.4 x $f_{RXIFCLK}$

Reducing the carrier frequency to 25% of the clock frequency can reduce the distortion level, as shown in Figure 21. Although the distortion is still fairly severe, adequate performance may be obtainable as a result of the system's processing gain, but the performance would be many dB off the theoretical limit. As the PN chip rate of the system increases, then so, too, does the effect of aliasing distortion in the modulator, resulting in performance degradation. As a rule-of-thumb, one may restrict the I.F. frequency to 25% of the clock frequency, but, in general, each application and combination of PN chip rate, I.F. frequency, and TXIFCLK/RXIFCLK frequency is unique and should be evaluated before deciding whether to use the Z87200's internal BPSK/QPSK modulator.

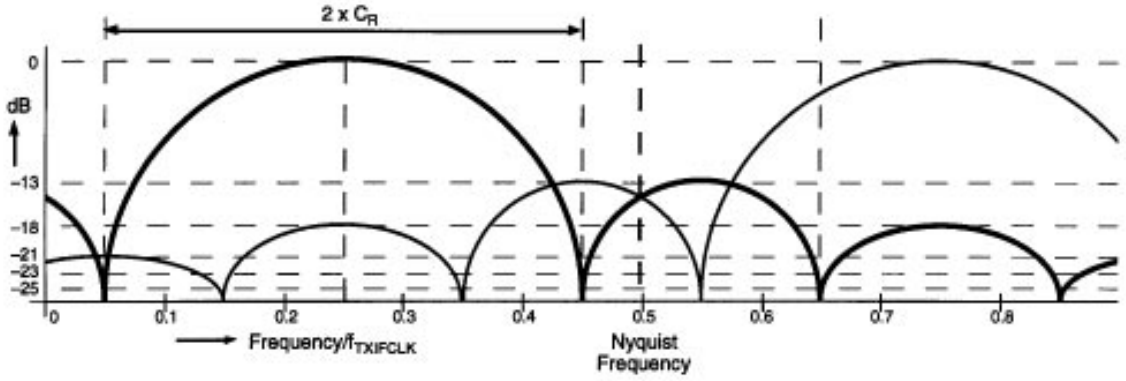


Figure 19. Spectrum of DDS Modulated at 0.4 x $f_{RXIFCLK}$ When Carrier Frequency is set to 0.25 x $f_{RXIFCLK}$