PRELIMINARY
CUSTOMER PROCUREMENT SPECIFICATION

Z89390

16-BIT DIGITAL
SIGNAL PROCESSOR

GENERAL DESCRIPTION

The Z89390 is a CMOS Digital Signal Processor (DSP). Single-cycle instruction execution and a Harvard bus structure promotes efficient algorithm execution. The processor contains 512 word data RAM and 64K word of external program address space is accessible. Six register pointers provide circular buffering capabilities and dual operand fetching. Three vectored interrupts are complemented by a six level stack. The CODEC interface enables high-speed transfer rates to accommodate digital audio and voice data. A dedicated Counter/Timer provides the necessary timing signals for the CODEC interface. An additional 13-bit timer is available for general-purpose use.

The Z89390 is optimized to accommodate intricate signal processing algorithms. The 20-MIP operating performance and efficient architecture provides real-time execution. Compression, filtering, frequency detection, audio, voice detection/synthesis and other available algorithms can all be accommodated. The on-board peripherals provide additional cost advantages.

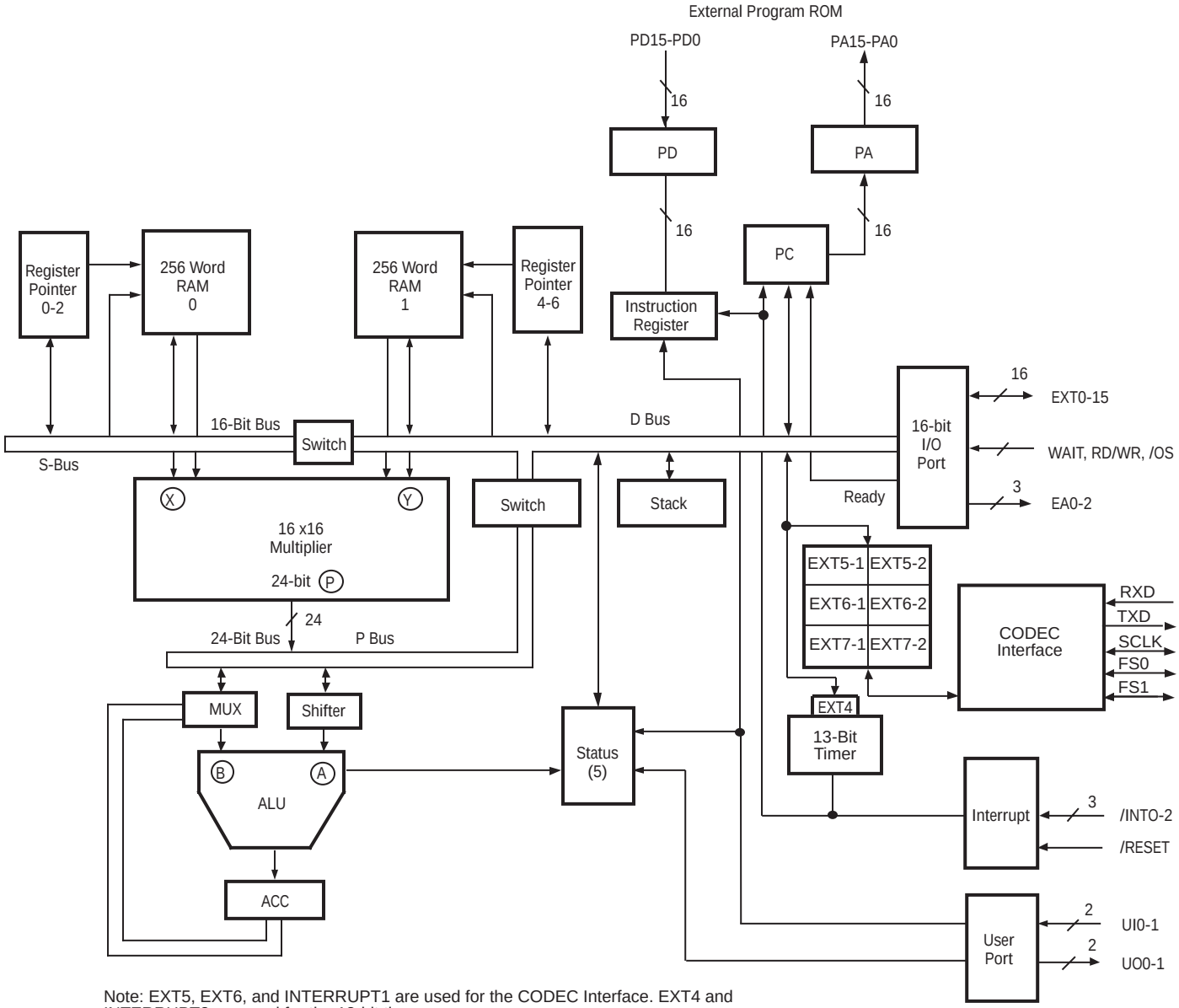
Development tools for the IBM PC include a relocatable assembler, a linker loader debugger.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

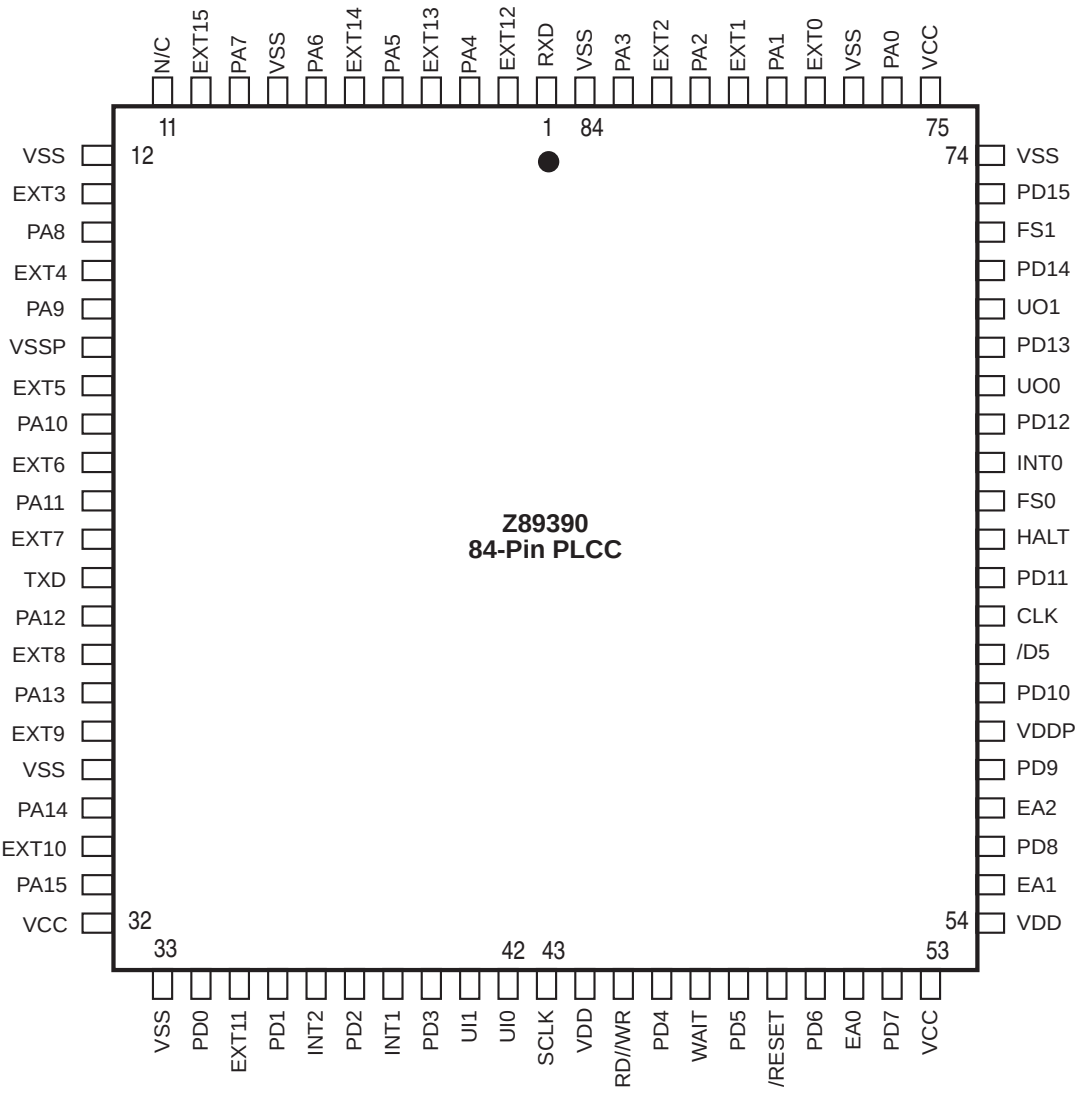
GENERAL DESCRIPTION (Continued)



Note: EXT5, EXT6, and INTERRUPT1 are used for the CODEC Interface. EXT4 and INTERRUPT2 are used for the 13-bit timer.

Z89391 Functional Block Diagram

PIN DESCRIPTION



84-Pin PLCC Pin Assignments

ABSOLUTE MAXIMUM RATINGS

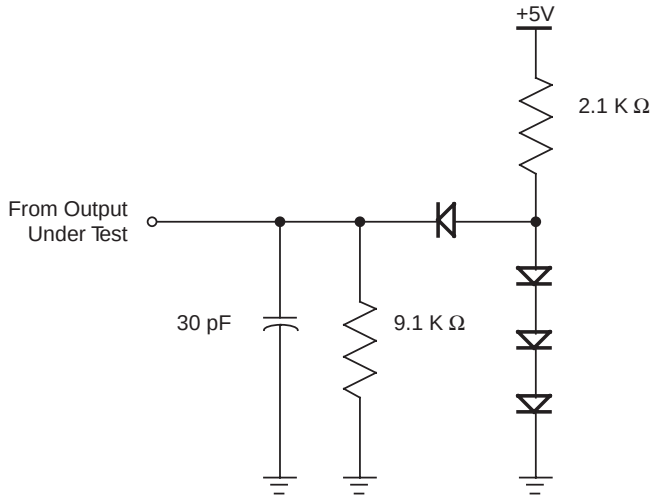
Symbol	Description	Min.	Max.	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp	–65°	+150°	C
T_A	Oper Ambient Temp		†	C

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to ground. Positive current flows into the referenced pin (Test Load).



. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

(V_{DD}= 5V ±10%, T_A = 0°C to +70°C unless otherwise specified)

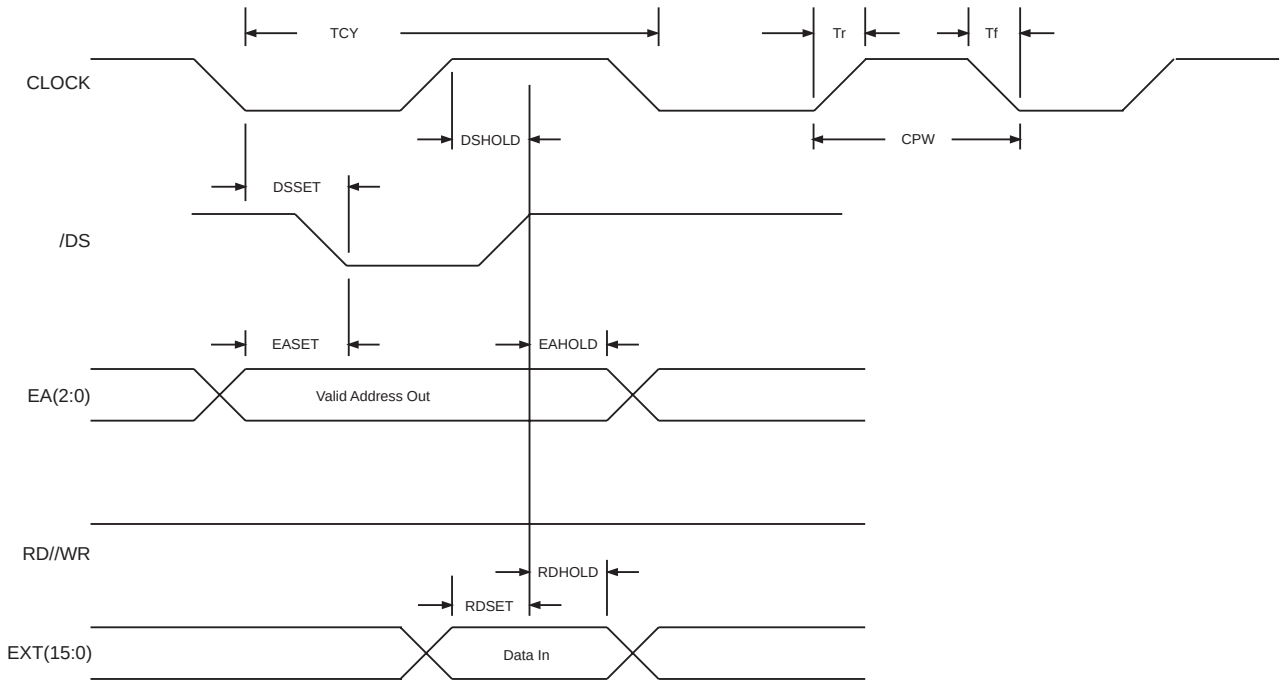
Symbol	Parameter	Condition	Min.	Max.	Typical	Units
I_{DD}	Supply Current	V_{DD} = 5.25V fclock = 20 MHz		80	70	mA
I_{DC}	DC Power Consumption	V_{DD} = 5.25V			5	mA
V_{IH}	Input High Level		2.5			V
V_{IL}	Input Low Level			0.8		V
IL	Input Leakage			10		µA
V_{OH}	Output High Voltage	I_{OH} = –100 µA	V_{DD}–0.2			V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.5		V
I_{FL}	Output Floating Leakage Current			5		µA

AC ELECTRICAL CHARACTERISTICS

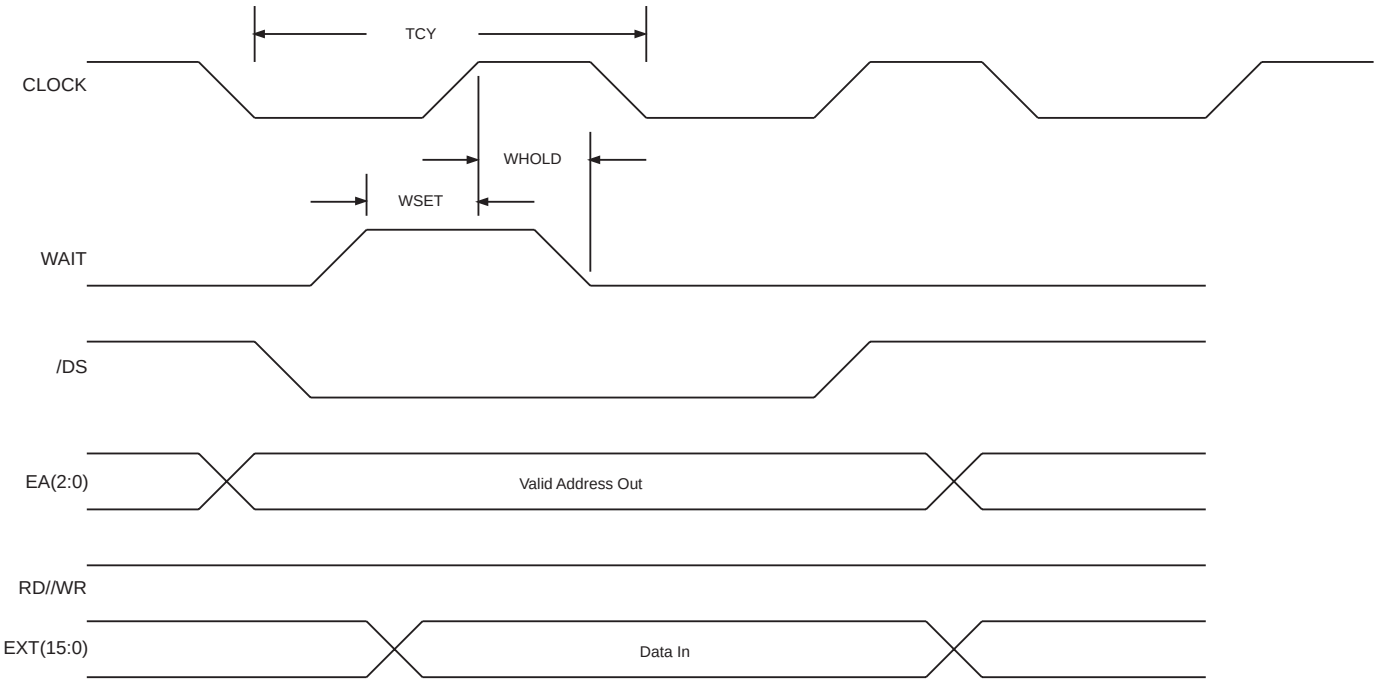
(V_{DD} = 5V 10%, T_A = 0°C to +70°C unless otherwise specified)

Symbol	Parameter	Min (ns)	Max (ns)
Clock			
TCY	Clock Cycle Time	50	
Tr	Clock Rise Time		2
Tf	Clock Fall Time		2
CPW	Clock Pulse Width	23	
I/O			
DSSET	/DS Setup Time from CLOCK Fall	0	15
DSHOLD	/DS Hold Time from CLOCK Rise	4	15
EASET	EA Setup Time to /DS Fall	12	
EAHOLD	EA Hold Time from /DS Rise	4	
RDSET	Data Read Setup Time to /DS Rise	14	
RDHOLD	Data Read Hold Time from /DS Rise	6	
WRSET	Data Write Setup Time to /DS Rise		18
WRHOLD	Data Write Hold Time from /DS Rise	5	
Interrupt			
INTSET	Interrupt Setup Time to CLOCK Fall	7	
INTWIDTH	Interrupt Low Pulse Width	1 TCY	
Codec Interface			
SSET	SCLK Setup Time from Clock Rise		15
FSSET	FSYNC Setup Time from SCLK Rise		6
TXSET	TXD Setup Time from SCLK Rise		7
RXSET	RXD Setup Time to SCLK Fall	7	
RXHOLD	RXD Hold Time from SCLK Fall	0	
Reset			
RRISE	Reset Rise Time		1000
RSET	Reset Setup Time to CLOCK Rise	15	
RWIDTH	Interrupt Low Pulse Width	2 TCY	
External Program Memory			
PASET	PA Setup Time from CLOCK Rise	5	
PDSET	PD Setup Time to CLOCK Rise	10	
PDHOLD	PD Hold Time from CLOCK Rise	10	
Wait State			
WSET	WAIT Setup Time to CLOCK Rise	23	
WHOLD	WAIT Hold Time from CLOCK Rise	1	
Halt			
HSET	Halt Setup Time to CLOCK Rise	3	
HHOLD	Halt Hold Time from CLOCK Rise	10	

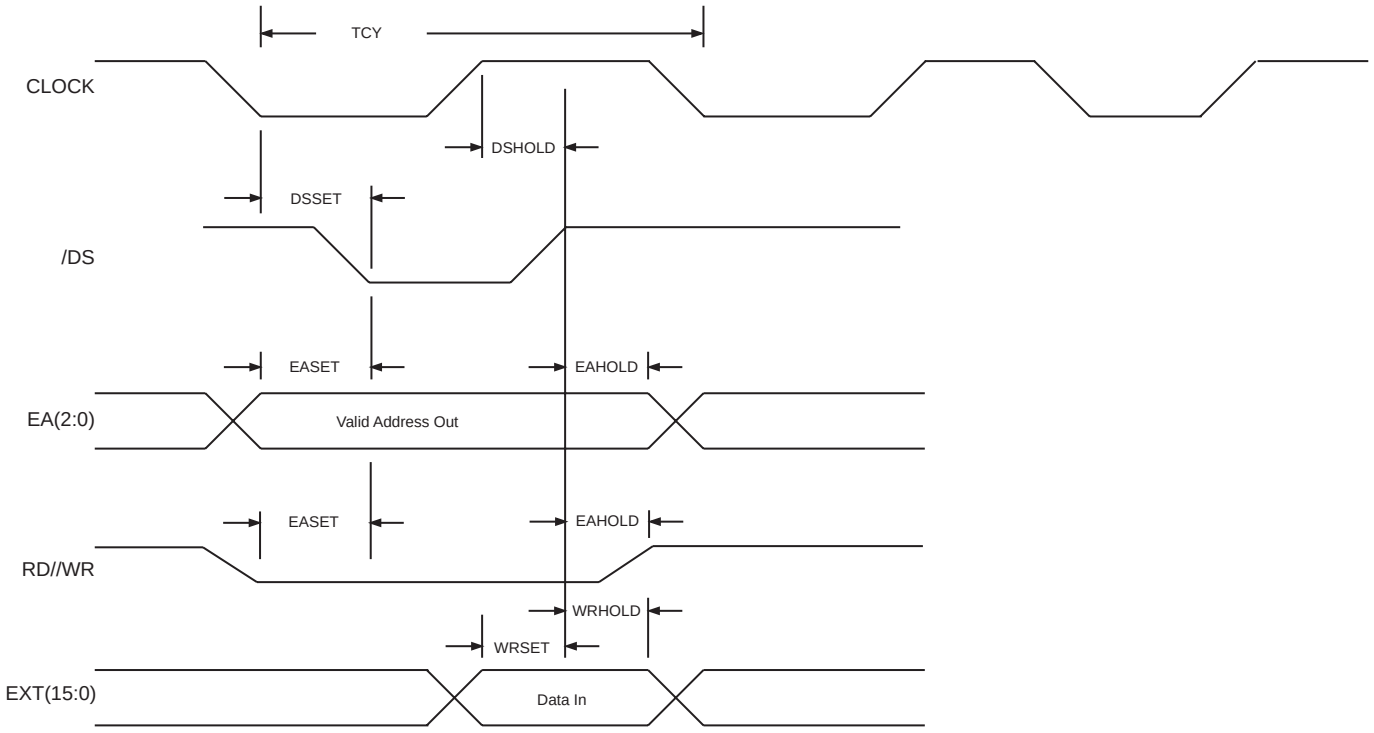
AC TIMING DIAGRAM



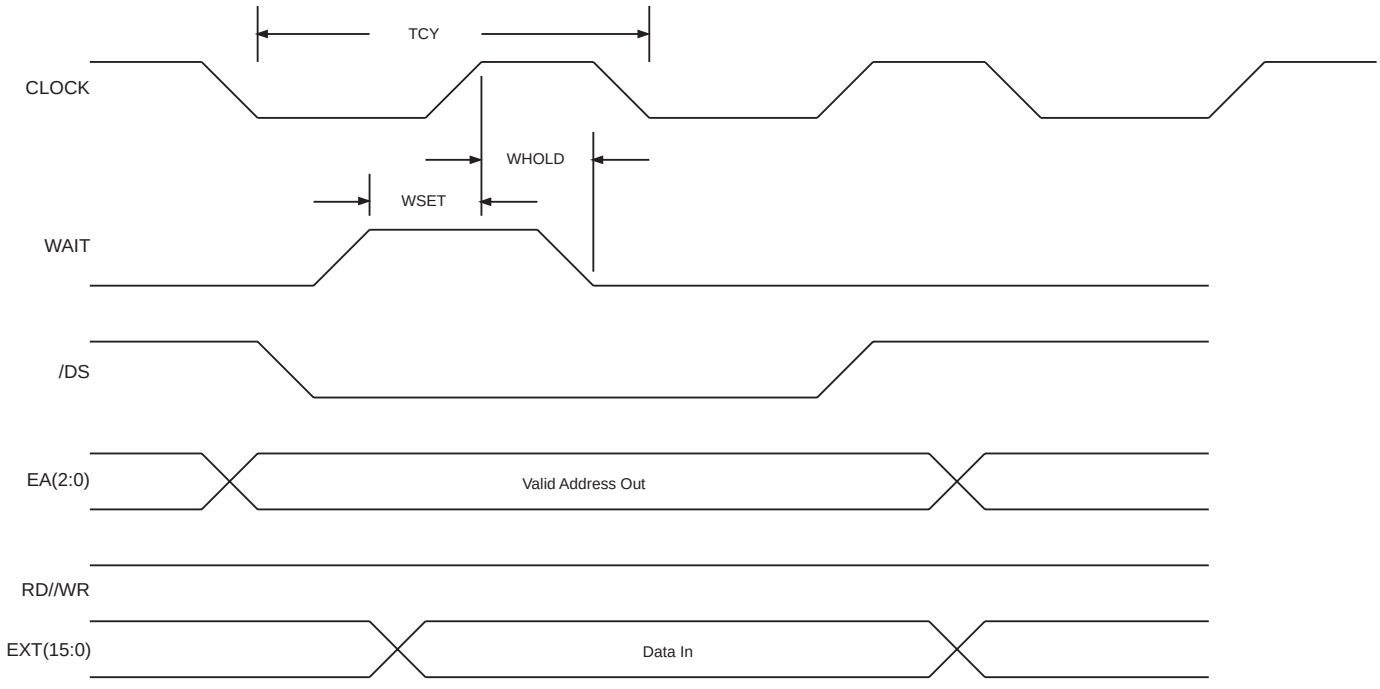
Read Timing Diagram



Read Timing Diagram Using WAIT Pin

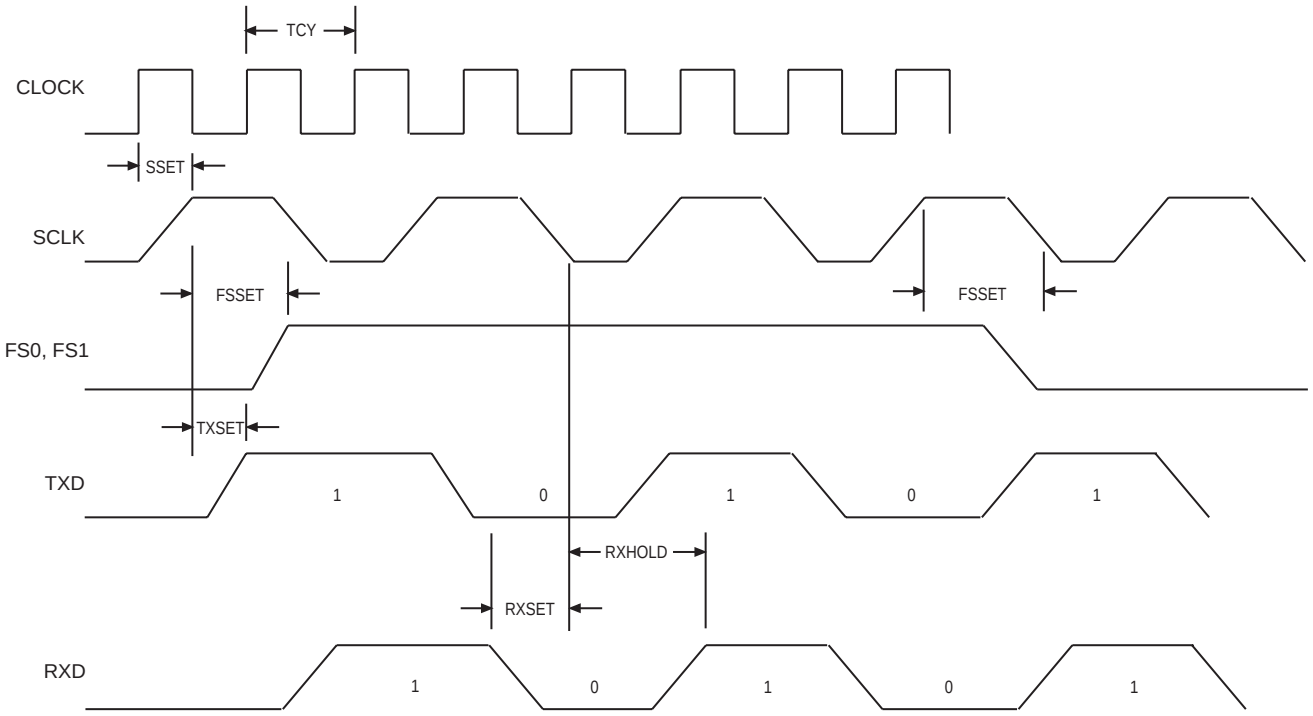


Write Timing Diagram



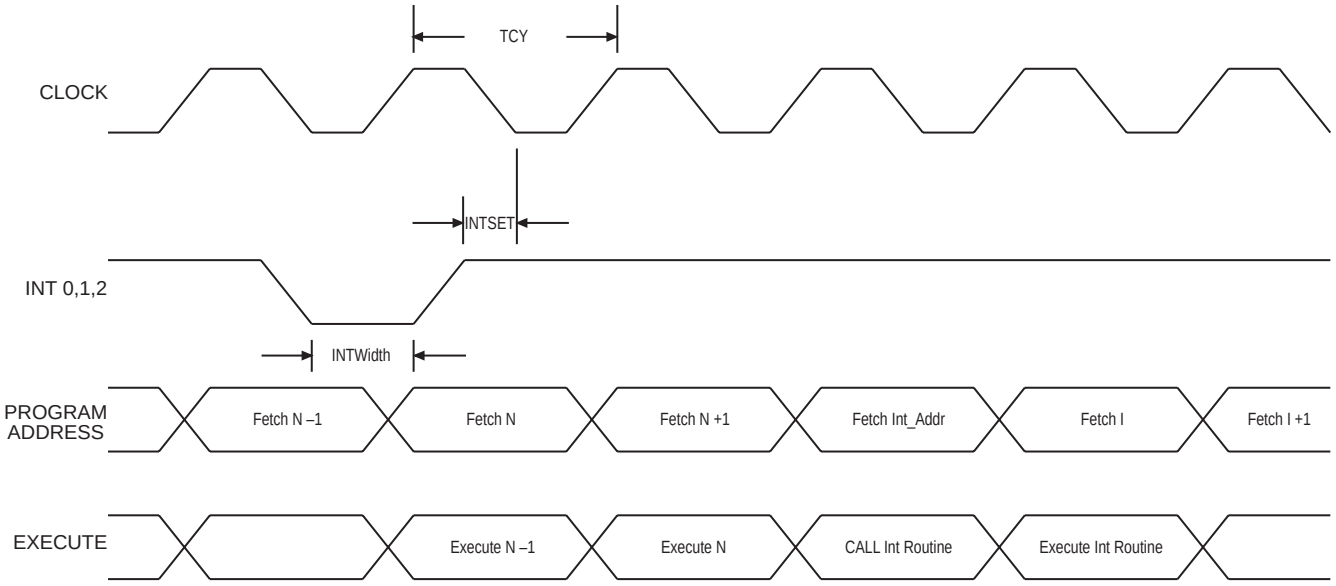
Write Timing Diagram Using WAIT Pin

AC TIMING (Continued)

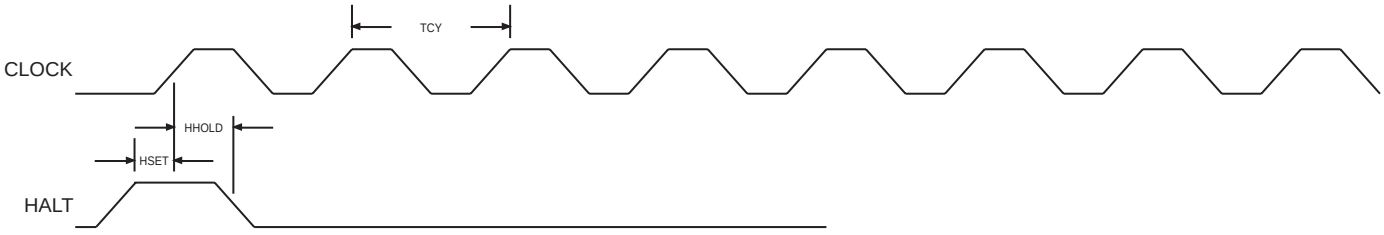


Codec Interface Timing Diagram

AC TIMING (Continued)

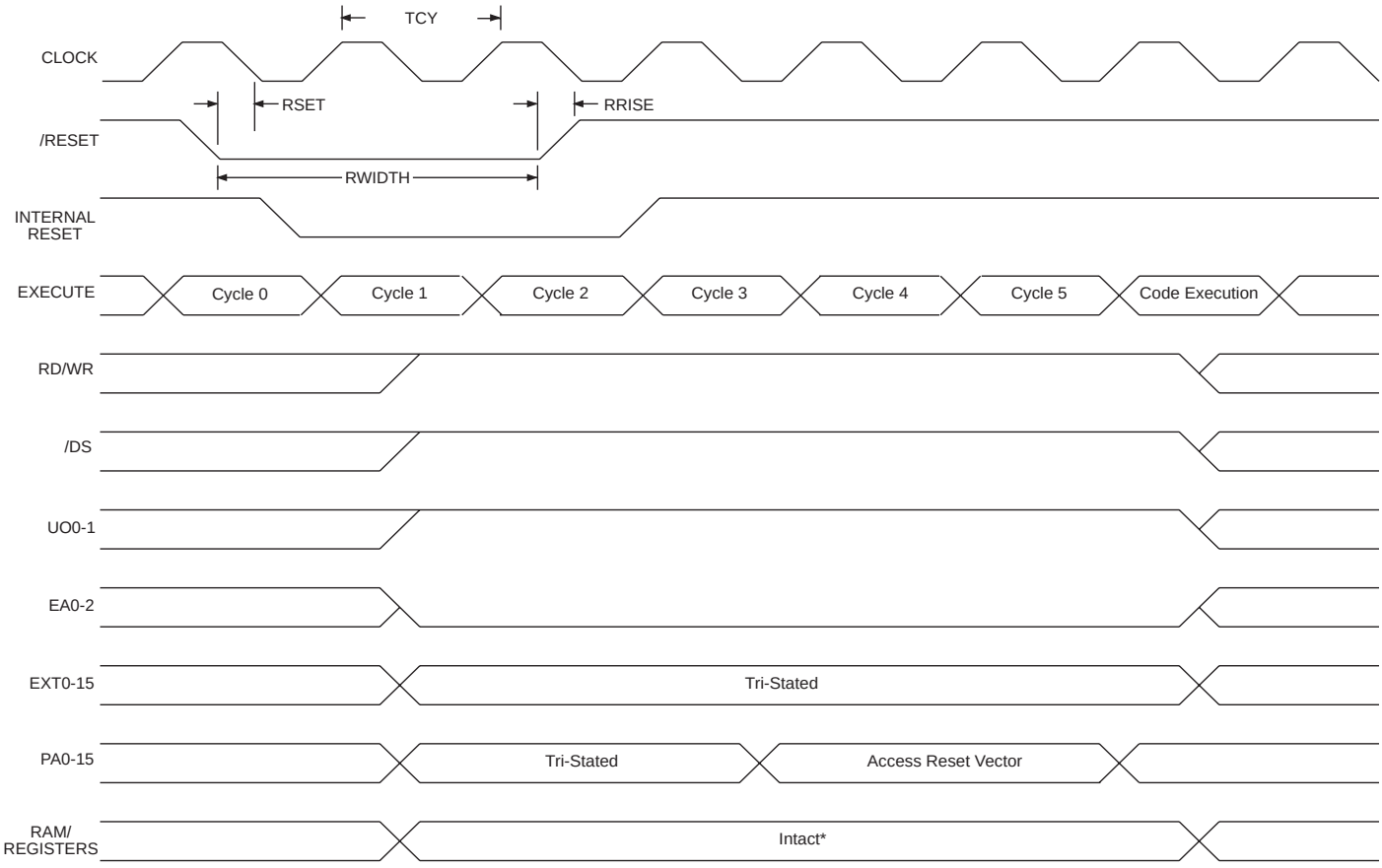


Interrupt Timing Diagram



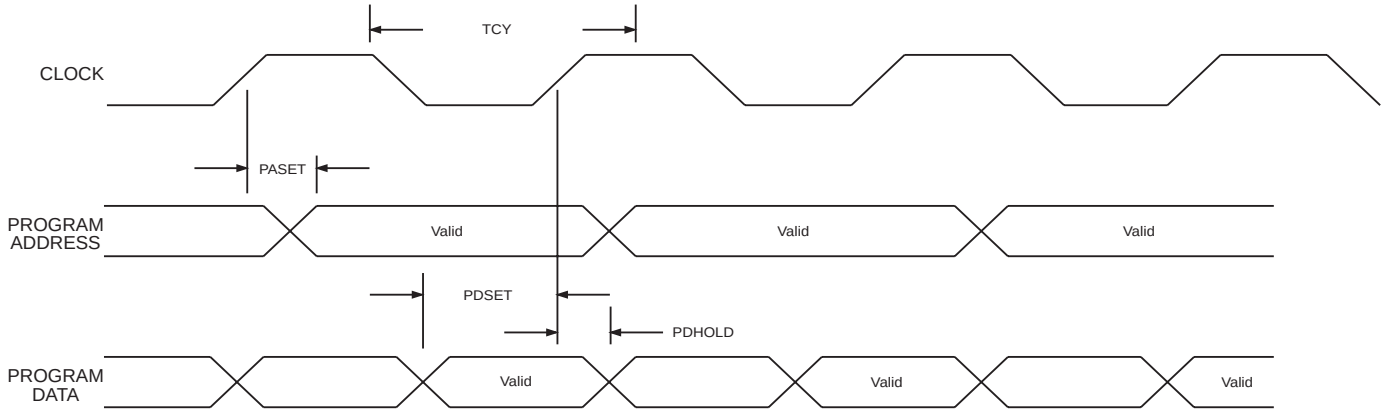
HALT Timing Diagram

AC TIMING (Continued)



* The RAM and hardware registers are left intact during a warm reset. A cold reset will produce random data in these locations. The status register is set to zeroes in both cases.

RESET Timing Diagram



External Memory Port Timing Diagram

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