

# P-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

## ZVP4105A

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### FEATURES

- \* 50 Volt  $V_{DS}$
- \*  $R_{DS(on)}=10\Omega$
- \* Low threshold



E-Line  
TO92 Compatible

### ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	$V_{DS}$	-50	V
Continuous Drain Current at $T_{amb}=25^{\circ}C$	$I_D$	-175	mA
Pulsed Drain Current	$I_{DM}$	-520	mA
Gate Source Voltage	$V_{GS}$	$\pm 20$	V
Power Dissipation at $T_{amb}=25^{\circ}C$	$P_{tot}$	625	mW
Operating and Storage Temperature Range	$T_j; T_{stg}$	-55 to +150	$^{\circ}C$

### ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}C$ unless otherwise stated).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	$BV_{DSS}$	-50		V	$I_D=-0.25mA, V_{GS}=0V$
Gate-Source Threshold Voltage	$V_{GS(th)}$	-0.8	-2.0	V	$I_D=-1mA, V_{DS}=V_{GS}$
Gate-Body Leakage	$I_{GSS}$		10	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Zero Gate Voltage Drain Current	$I_{DSS}$		-15 -60 -100	$\mu A$ $\mu A$ nA	$V_{DS}=-50V, V_{GS}=0V$ $V_{DS}=-50V, V_{GS}=0V, T=125^{\circ}C(2)$ $V_{DS}=-25V, V_{GS}=0V$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		10	$\Omega$	$V_{GS}=-5V, I_D=-100mA$
Forward Transconductance (1)(2)	$g_{fs}$	50		mS	$V_{DS}=-25V, I_D=-100mA$
Input Capacitance (2)(4)	$C_{iss}$		40	pF	$V_{DS}=-25V, V_{GS}=0V, f=1MHz$
Common Source Output Capacitance (2)(4)	$C_{oss}$		15	pF	
Reverse Transfer Capacitance (2)(4)	$C_{rss}$		6	pF	
Turn-On Delay Time (2)(3)(4)	$t_{d(on)}$		10	ns	$V_{DD}=-30V, I_D=-270mA$
Rise Time (2)(3)(4)	$t_r$		10	ns	
Turn-Off Delay Time (2)(3)(4)	$t_{d(off)}$		18	ns	
Fall Time (2)(3)(4)	$t_f$		25	ns	

(1) Measured under pulsed conditions. Width=300 $\mu s$ . Duty cycle  $\leq 2\%$

(2) Sample test.

(3) Switching times measured with 50 $\Omega$  source impedance and <5ns rise time on a pulse generator