SECTION 9

HARDWARE DESIGN TECHNIQUES

- Prototyping Analog Circuits
- Evaluation Boards
- Noise Reduction and Filtering for Switching Power Supplies
- Low Dropout References and Regulators
- EMI/RFI Considerations
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SECTION 9

HARDWARE DESIGN TECHNIQUES

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PROTOTYPING AND SIMULATING ANALOG CIRCUITS

Walt Kester, James Bryant

While there is no doubt that computer analysis is one of the most valuable tools that the analog designer has acquired in the last decade or so, there is equally no doubt that analog circuit models are not perfect and must be verified with hardware. If the initial test circuit or "breadboard" is not correctly constructed, it may suffer from malfunctions which are not the fault of the design but of the physical structure of the breadboard itself. This section considers the art of successful breadboarding of high performance analog circuits.

Real electronic circuits contain many "components" which were not present in the circuit diagram, but which are there because of the physical properties of conductors, circuit boards, IC packages, etc. These components are difficult, if not impossible, to incorporate into computer modeling software, and yet they have substantial effects on circuit performance at high resolutions, or high frequencies, or both.

It is therefore inadvisable to use SPICE modeling or similar software to predict the ultimate performance of such high performance analog circuits. After modeling is complete, the performance must be verified by experiment.

This is not to say that SPICE modeling is valueless - far from it. Most modern high performance analog circuits could never have been developed without the aid of SPICE and similar programs, but it must be remembered that such simulations are only as good as the models used, and these models are not perfect. We have seen the effects of parasitic components arising from the conductors, insulators and components on the PCB, but it is also necessary to appreciate that the models used within SPICE simulations are not perfect models.

Consider an operational amplifier. It contains some 20-40 transistors, almost as many resistors, and a few capacitors. A complete SPICE model will contain all these components, and probably a few of the more important parasitic capacitances and spurious diodes formed by the diffusions in the op-amp chip. This is the model that the designer will have used to evaluate the device during his design. In simulations, such a model will behave very like the actual op-amp, but not exactly.

SPICE MODELING

- **SPICE modeling is a powerful tool for predicting the performance of analog circuits.**
- **Analog Devices provides macromodels for over 450 ICs**

HOWEVER

- **Models omit real-life effects**
- **No model can simulate all the parasitic effects of discrete components and a PCB layout**

THEREFORE

- **Prototypes must be built and proven before production.**

Figure 9.1

However, this model is not published, as it contains too much information which would be of use to other semiconductor companies who might wish to copy or improve on the design. It would also take far too long for a simulation of a system containing such models of a number of op-amps to reach a useful result. For these, and other reasons, the SPICE models of analog circuits published by manufacturers or software companies are "macro" models, which simulate the major features of the component, but lack some of the fine detail. Consequently, SPICE modeling does not always reproduce the exact performance of a circuit and should always be verified experimentally.

The basic principle of a breadboard is that it is a *temporary* structure, designed to test the performance of a circuit or system, and must therefore be easy to modify.

There are many commercial breadboarding systems, but almost all of them are designed to facilitate the breadboarding of *digital* systems, where noise immunities are hundreds of millivolts or more. (We shall discuss the exception to this generality later.) Non copper-clad Matrix board (Vectorboard, etc.), wire-wrap, and plug-in breadboard systems (Bimboard, etc.) are, without exception, unsuitable for high performance or high frequency analog breadboarding. They have too high resistance, inductance, and capacitance. Even the use of standard IC sockets is inadvisable.

PRACTICAL BREADBOARDING TECHNIQUES

The most practical technique for analog breadboarding uses a copper-clad board as a ground plane. The ground pins of the components are soldered directly to the plane and the other components are wired together above it. This allows HF decoupling paths to be very short indeed. All lead lengths should be as short as possible, and signal routing should separate high-level and low-level signals. Ideally the layout should be similar to the layout to be used on the final PCB. This approach is often referred to as "deadbug" because the ICs are often mounted upside down with their

leads up in the air (with the exception of the ground pins, which are bent over and soldered directly to the ground plane). The upside-down ICs look liked deceased insects, hence the name.

Figure 9.2 shows a hand-wired breadboard based around two high speed op amps which gives excellent performance in spite of its lack of esthetic appeal. The IC op amps are mounted upside down on the copper board with the leads bent over. The signals are connected with short point-to-point wiring. The characteristic impedance of a wire over a ground plane is about 120ohms, although this may vary as much as ±40% depending on the distance from the plane. The decoupling capacitors are connected directly from the op amp power pins to the copper-clad ground. When working at frequencies of several hundred MHz, it is a good idea to use only one side of the board for ground. Many people drill holes in the board and connect both sides together with short pieces of wire soldered to both sides of the board. If care is not taken, however, this may result in unexpected ground loops between the two sides of the board, especially at RF frequencies.

"DEADBUG" PROTOTYPE TECHNIQUE

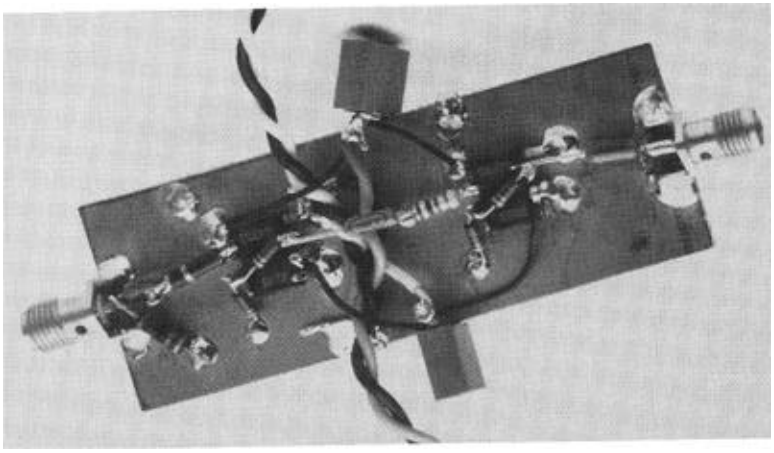

Figure 9.2

Pieces of copper-clad may be soldered at right angles to the main ground plane to provide screening, or circuitry may be constructed on both sides of the board (with connections through holes) with the board itself providing screening. In this case, the board will need legs to protect the components on the underside from being crushed.

When the components of a breadboard of this type are wired point-to-point in the air (a type of construction strongly advocated by Robert A. Pease of National Semiconductor (Reference 1) and sometimes known as "bird's nest" construction) there is always the risk of the circuitry being crushed and resulting short-circuits. Also if the circuitry rises high above the ground plane, the screening effect of the ground plane is diminished, and interaction between different parts of the circuit is more likely. Nevertheless the technique is very practical and widely used because the circuit may so easily be modified.

Another "deadbug" prototype is shown in Figure 9.3. The board is single-sided copper clad with holes pre-drilled on 0.1" centers. Power busses are at the top and bottom of the board. The decoupling capacitors are used on the power pins of each IC. Because of the loss of copper area due to the pre-drilled holes, this technique does not provide as low a ground impedance as a completely covered copper-clad board.

"DEADBUG" PROTOTYPE USING PRE-DRILLED SINGLE-SIDED COPPER-CLAD BOARD

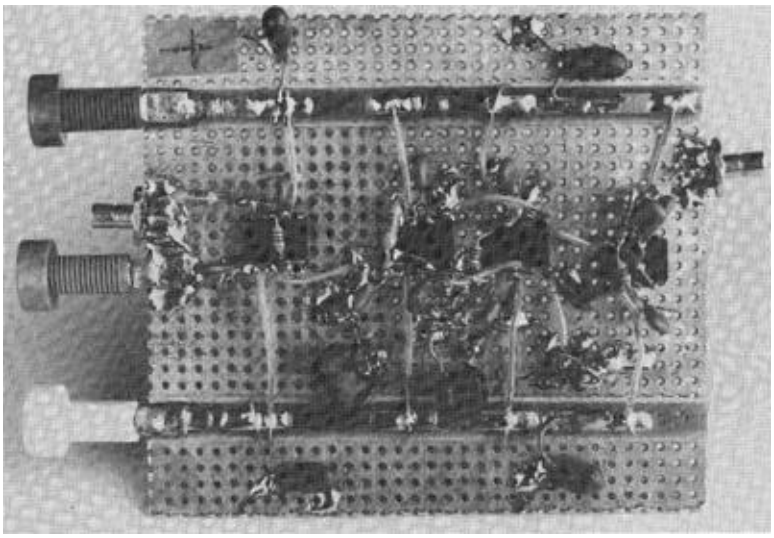

Figure 9.3

In a variation of this technique, the ICs and other components are mounted on the non-copper-clad side of the board. The holes are used as vias, and the point-to-point wiring is done on the copper-clad side of the board. The copper surrounding each hole used for a via must be drilled out so as to prevent shorting. This approach requires that all IC pins be on 0.1" centers. Low profile sockets can be used for low frequency circuits, and the socket pins allow easy point-to-point wiring.

IC sockets can degrade the performance of high speed or high precision analog ICs. Even "low-profile" sockets often introduce enough parasitic capacitance and inductance to degrade the performance of the circuit. If sockets must be used, an IC socket made of individual "pin sockets" (sometimes called "cage jacks") mounted in the ground plane board may be acceptable (clear the copper, on both sides of the board, for about 0.5mm around each ungrounded pin socket and solder the grounded ones to ground on both sides of the board. Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6, respectively).

PIN SOCKETS (CAGE JACKS) HAVE MINIMUM PARASITIC RESISTANCE, INDUCTANCE AND CAPACITANCE

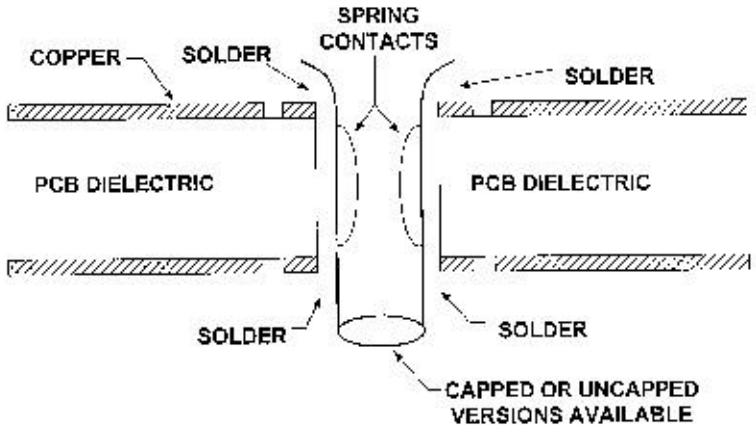

Figure 9.4

There is a commercial breadboarding system which has most of the advantages of "bird's nest over a ground plane, or deadbug" (robust ground, screening, ease of circuit alteration, low capacitance and low inductance) and several additional advantages:- it is rigid, components are close to the ground plane, and where necessary node capacitances and line impedances can be calculated easily. This system is made by Wainwright Instruments and is available in Europe as "Mini-Mount" and in the USA (where the trademark "Mini-Mount" is the property of another company) as "Solder-Mount"[Reference 2].

Solder-Mount consists of small pieces of PCB with etched patterns on one side and contact adhesive on the other. They are stuck to the ground plane, and components are soldered to them. They are available in a wide variety of patterns, including ready-made pads for IC packages of all sizes from 8-pin SOICs to 64-pin DILs, strips with solder pads at intervals (which intervals range from 0.040" to 0.25", the range includes strips with 0.1" pad spacing which may be used to mount DIL devices), strips with conductors of the correct width to form microstrip transmission lines (50ohms, 60ohms, 75ohms or 100ohms) when mounted on the ground plane, and a variety of pads for mounting various other components. A few of the many types of Solder-Mount building-block components are shown in Figure 9.5.

SAMPLES OF "SOLDER-MOUNT" COMPONENTS

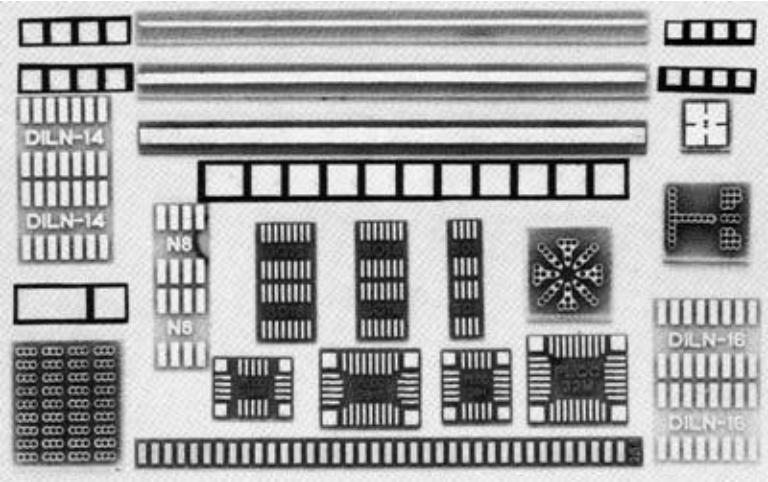

Figure 9.5

The main advantage of Solder-Mount construction over "bird's nest" or "deadbug" is that the resulting circuit is far more rigid, and, if desired, may be made far smaller (the latest Solder-Mounts are for surface-mount devices and allow the construction of breadboards scarcely larger than the final PCB, although it is generally more convenient if the prototype is somewhat larger). Solder-Mount is sufficiently durable that it may be used for small quantity production as well as prototyping.

Figure 9.6 shows an example of a 2.5GHz phase-locked-loop prototype built with Solder-Mount. This is a high speed circuit, but the technique is equally suitable for the construction of high resolution low frequency analog circuitry. A particularly convenient feature of Solder-Mount at VHF is the ease with which it is possible to make a transmission line.

"SOLDER-MOUNT" PROTOTYPE

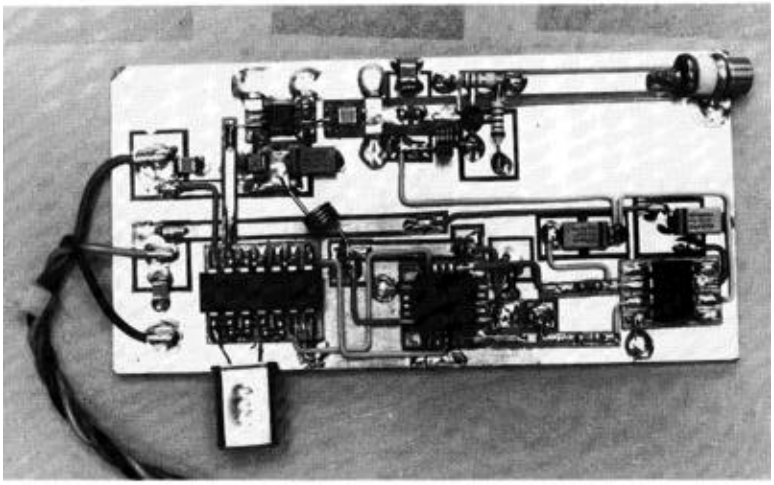

Figure 9.6

If a conductor runs over a ground plane it forms a microstrip transmission line. Solder-Mount has strips which form microstrip lines when mounted on a ground plane (they are available with impedances of 50ohms, 60ohms, 75ohms, and 100ohms). These strips may be used as transmission lines, for impedance matching, or simply as power buses. (Glass fiber/epoxy PCB is somewhat lossy at VHF and UHF, but the losses will probably be tolerable if microstrip runs are short.)

Both the "deadbug" and the "Solder-Mount" breadboarding techniques become tedious for complex circuits. Larger circuits are often better prototyped using more formal layout techniques.

An approach to prototyping more complex analog circuits is to actually lay out a double-sided board using CAD techniques. PC-based software layout packages offer ease of layout as well as schematic capture to verify connections. Although most layout software has some amount of auto-routing capability, this feature is best left to digital designs. After the components are placed in their approximate position, the interconnections should be routed manually following good analog layout guidelines. After the layout is complete, the software verifies the connections per the schematic diagram net list.

Many design engineers find that they can use CAD techniques (Reference 3) to lay out simple boards themselves, or work closely with a layout person who has experience in analog circuit boards. The result is a pattern-generation tape (or Gerber file) which would normally be sent to a PCB manufacturing facility where the final board is made. Rather than use a PC board manufacturer, however, automatic drilling and milling machines are available which accept the PG tape (Reference 4). These systems produce single and double-sided circuit boards directly by drilling all holes and using a milling technique to remove copper and create insulation paths and finally, the finished board. The result is a board very similar to the final manufactured double-sided PC board, the chief exception being that there

is no "plated-through" hole capability, and any "vias" between the two layers of the board must be wired and soldered on both sides. Minimum trace widths of 25 mils (1 mil = 0.001") and 12 mil spacing between traces are standard, although smaller trace widths can be achieved with care. The minimum spacing between lines is dictated by the size of the milling bit, typically 10 to 12 mils.

An example of such a prototype board is shown in Figure 9.7. This is a "daughter" board designed to interface an AD9562 Dual Pulse-Width Modulator in a 44-pin PLCC package to a "mother" board. The leads are on 50 mil centers, and the traces are approximately 25 mils wide.

"MILLED" PROTOTYPE PC BOARD

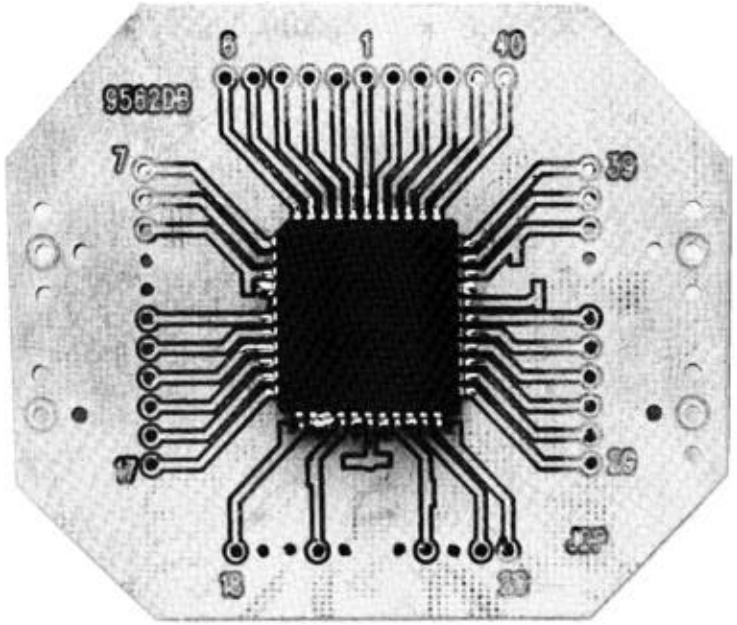

Figure 9.7

Multilayer PC boards do not easily lend themselves to standard prototyping techniques. One side of a double-sided board can be used for ground and the other side for power and signals. Point-to-point wiring can be used for additional runs which would normally be placed on the additional layers provided by a multi-layer board. However, it is difficult to control the impedance of the point-to-point wiring runs, and the high frequency performance of a circuit prototyped in this manner may differ significantly from the final multilayer board.

SUCCESSFUL PROTOTYPING

- **Always use a ground plane for precision or high frequency circuits**
- **Minimize parasitic resistance, capacitance, and inductance**
- **If sockets are required, use "pin sockets" ("cage jacks")**
- **Pay equal attention to signal routing, component placement, grounding, and decoupling in both the prototype and the final design**
- **Popular prototyping techiniques:**
  - **Freehand "deadbug" using point-to-point wiring**
  - **"Solder-Mount"**
  - **Milled PC board from CAD layout**
  - **Multilayer boards: Double-sided with additional point-to-point wiring**

Figure 9.8

EVALUATION BOARDS

Manufacturer's evaluation boards provide a convenient way of evaluating high-performance ICs without the need for constructing labor-intensive prototype boards. Analog Devices provides evaluation boards for almost all new high speed and precision products. The boards are designed with good layout, grounding, and decoupling techniques. They are completely tested, and artwork (including PG tape) is available to customers.

Because of the popularity of dual precision op amps in 8-pin DIPs, a universal evaluation board has been developed (see Figure 9.9). This board makes extensive use of pin sockets to allow resistors or jumpers to configure the two op amps in just about any conceivable feedback, input/output, and load condition. The inputs and outputs are convenient right-angle BNC connectors. Because of the use of sockets and the less-than-compact layout, this board is not useful for op amps having gain-bandwidth products much greater than 10MHz.

UNIVERSAL EVALUATION BOARD FOR DUAL PRECISION OP AMPS IN 8-PIN DIPs

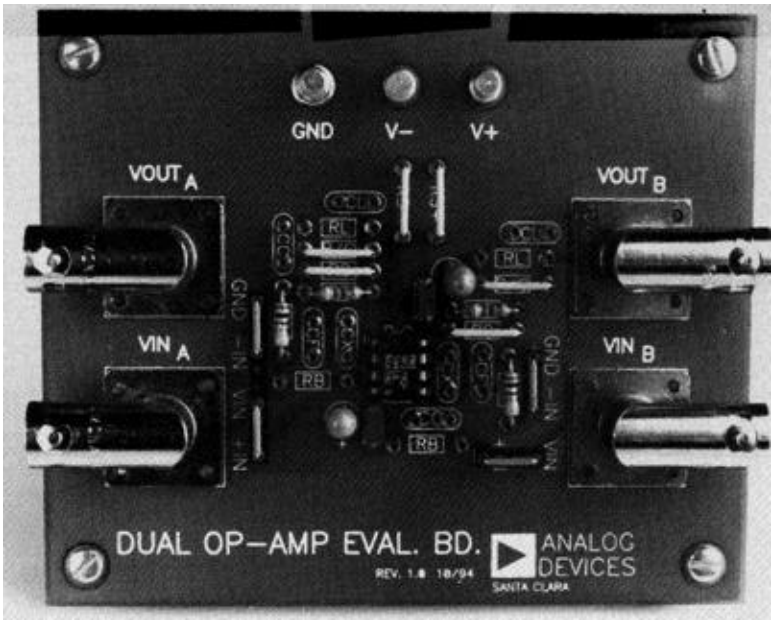

Figure 9.9

A schematic of the AD8001 800MHz 50mW current feedback op amp evaluation board for the 8-lead SOIC package is shown in Figure 9.10. The board is designed for a non-inverting gain of 2. (Boards for inverting and non-inverting modes are available for both the 8-lead SOIC and the DIP package).

Decoupling on both the + and – supplies consists of 1000pF and 0.01µF surface mount chip ceramic capacitors in addition to a 10µF/25V surface mount tantalum electrolytic. The top view of the PC board is shown in Figure 9.10, and the bottom view in Figure 9.12.

AD8001AR (SOIC) 800MHz OP AMP: NON-INVERTING MODE EVALUATION BOARD SCHEMATIC

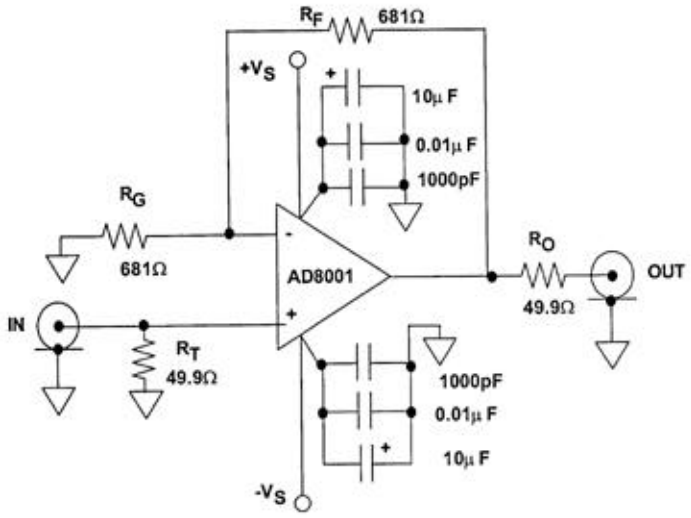

Figure 9.10

AD8001AR (SOIC) EVALUATION BOARD - TOP VIEW

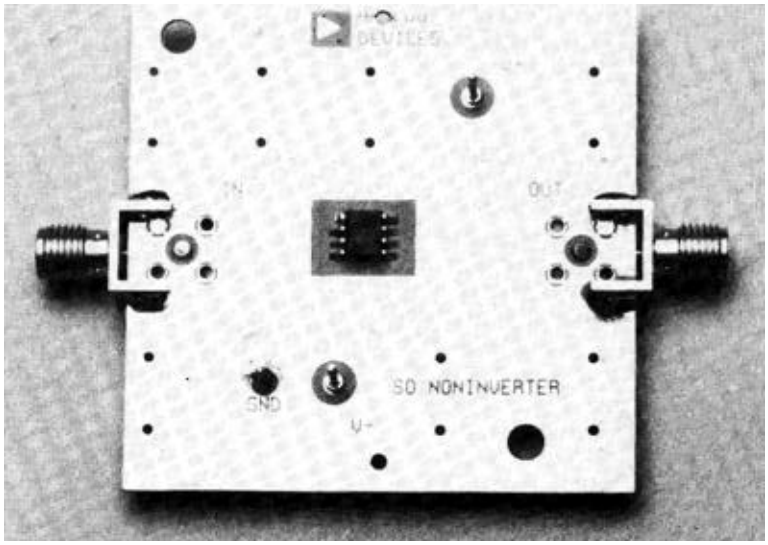

Figure 9.11

AD8001AR (SOIC) EVALUATION BOARD -BOTTOM VIEW

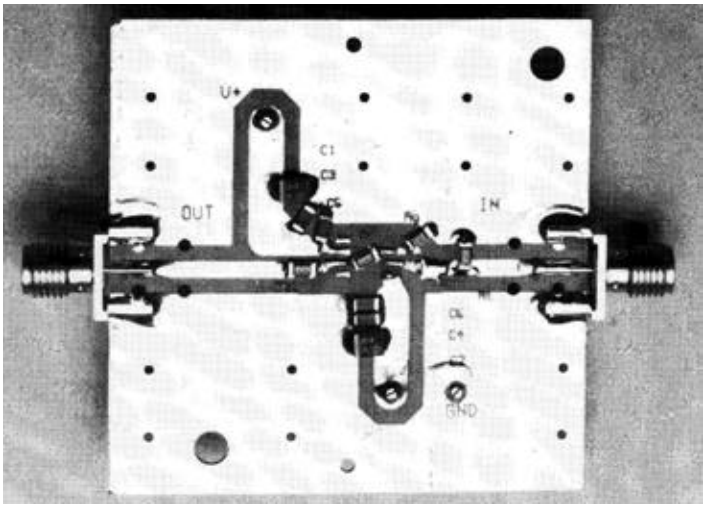

Figure 9.12

Figure 9.12 (bottom side of board) shows the surface mount resistors and capacitors. Notice that the ceramic chip capacitors are mounted as close as possible to the power pins as possible. The input and output runs are 50ohm transmission lines. The input from the SMA connector is terminated in a 50ohm chip resistor at the op amp, and the output has a 50ohm source termination for driving a 50ohm cable through the output SMA connector.

All resistors are surface mount film resistors. Notice that the ground plane is etched away from the area immediately surrounding the inputs of the op amp to minimize stray capacitance.

Slightly different resistor values are required to achieve optimum performance in the SOIC and the DIP packages (see Figure 9.13), because the SOIC package has slightly lower parasitic capacitance and inductance than the DIP. The criteria for selection of the components was maximum 0.1dB bandwidth.

OPTIMUM VALUES OF R_F AND R_G FOR AD8001 DIP AND SOIC PACKAGES (MAXIMUM 0.1dB BANDWIDTH)

AD8001AN (DIP) GAIN

Component	–1	+1	+2	+10	+100
R_F	649Ω	1050Ω	750Ω	470Ω	1000Ω
R_G	649Ω	-	750Ω	51Ω	10Ω
Small Signal BW	340MHz	880MHz	460MHz	260MHz	20MHz
0.1dB Flatness	105MHz	70MHz	105MHz	-	-

AD8001AR (SOIC) GAIN

Component	–1	+1	+2	+10	+100
R_F	604Ω	953Ω	681Ω	470Ω	1000Ω
R_G	604Ω	-	681Ω	51Ω	10Ω
Small Signal BW	370MHz	710MHz	440MHz	260MHz	20MHz
0.1dB Flatness	130MHz	100MHz	120MHz	-	-

Figure 9.13

ADC evaluation boards include more support circuitry than op amp boards. An example is the AD7714 (22-bit precision measurement sigma-delta ADC) evaluation board (see Figure 9.14 for a simplified block diagram). Included on the evaluation board are an AD780 precision reference, a 2.4576MHz crystal and digital buffers to buffer the signal to and from the edge connectors.

AD7714 ADC EVALUATION BOARD

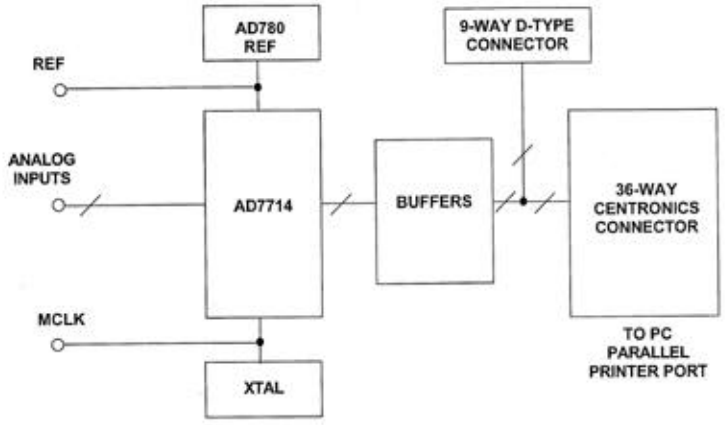

Figure 9.14

Interfacing to this board is provided either through a 36-Way Centronics connector or through a 9-Way D-type connector. The Centronics connector is intended for connection to the printer port of a PC. External sockets are provided for the analog inputs, an external reference input option, and an external master clock option.

Included in the evaluation board package is a PC-compatible DOS-based disk which contains software for controlling and evaluating the performance of the AD7714 using the printer port. There are two files on the disk, an executable file, and a "readme" text file which gives details of the functions available in the executable

program. The evaluation software is run by running the executable file. The program provides a number of different menu-type screens, each screen containing several function options.

The first menu gives options on the type of PC being used. The next menu in the sequence is the Main Menu which contains various options. These allow reading from the AD7714 Data Register, configuration of the Communications Register, file options (read and write data to files), noise analysis, printer port setup, and resetting the AD7714.

The Noise Menu allows the user to get statistical results from the data, to plot the raw data, plot a histogram of the data on the screen, or perform a rolling average of the data. A photograph of the AD7714 evaluation board is shown in Figure 9.15. Notice the parallel printer connector on the left and the use of low-profile sockets for convenience. It should be noted that although the use of sockets is discouraged, any sockets used on evaluation boards have been proven to cause minimal performance degradation.

AD7714 EVALUATION BOARD PHOTO

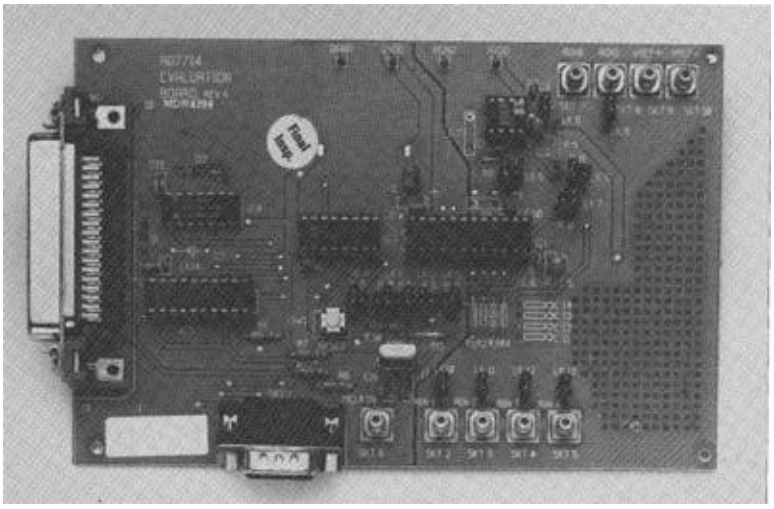

Figure 9.15

Evaluation boards for high speed sampling ADCs contain the required support circuitry for proper evaluation of the converter. Figure 9.16 shows a block diagram of the AD9026 (12-bit, 31MSPS) evaluation board. The analog input is connected directly to the ADC input via an SMA connector. The sampling clock (Encode Input) is conditioned by the low-jitter high-speed AD9698 dual comparator. The parallel digital outputs of the AD9026 are buffered by latches which drive the output connector as well as the AD9713 12-bit DAC. The DAC output is connected to an output SMA connector.

AD9026 12-BIT, 31MSPS ADC EVALUATION BOARD

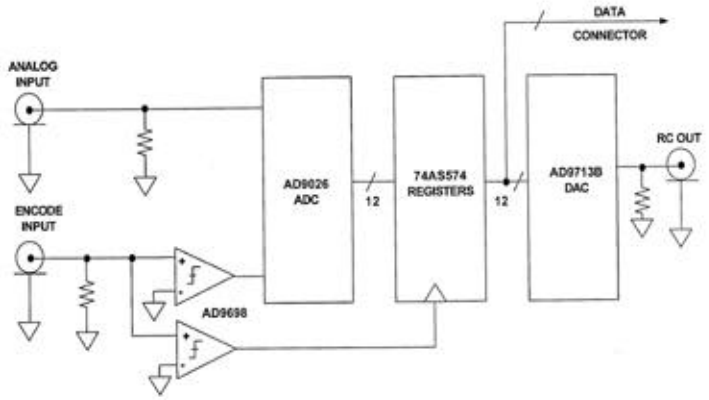

Figure 9.16

The output connector is designed for convenient interfacing to an external buffer memory or to a logic analyzer input (a very convenient high speed buffer memory). The top side of the board is shown in Figure 9.17. The board is a 3-layer board consisting of one ground plane (outer layer), one power/signal plane (inner layer), and an additional signal plane (outer layer). Pin sockets are used to mount the AD9026. Figure 9.18 shows the bottom side of the board and the surface mounted AD9698 SOIC comparator and the AD9713B PLCC DAC.

AD9026 EVALUATION BOARD - TOP VIEW

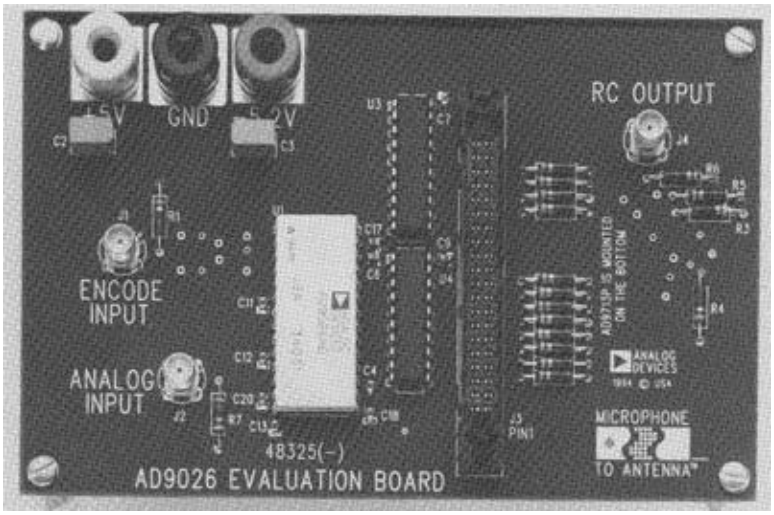

Figure 9.17

AD9026 EVALUATION BOARD - BOTTOM VIEW

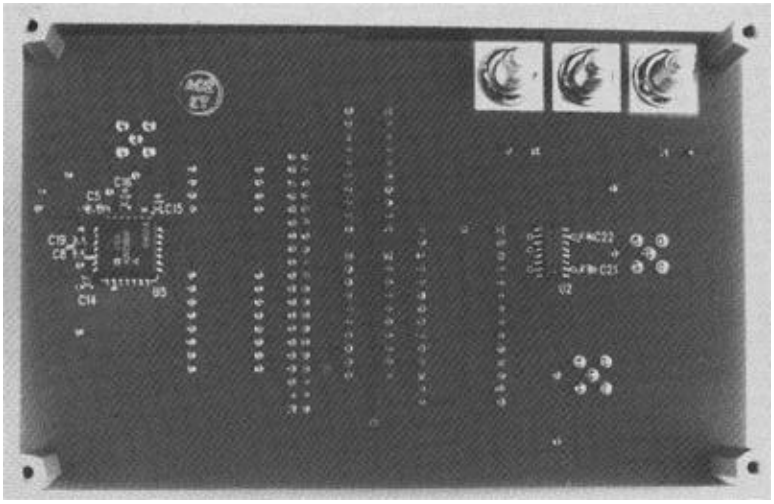

Figure 9.18

REFERENCES: PROTOTYPING AND EVALUATION BOARDS

1. Robert A. Pease, **Troubleshooting Analog Circuits**, Butterworth-Heinemann, 1991.

2. Wainwright Instruments Inc., 7770 Regents Rd., #113, Suite 371, San Diego, CA 92122, Tel. 619-558-1057, Fax. 619-558-1019.

   Wainwright Instruments GmbH, Widdersberger Strasse 14, DW-8138 Andechs-Frieding, Germany. Tel: +49-8152-3162, Fax: +49-8152-40525.

3. Schematic Capture and Layout Software:

   PADS Software, INC, 165 Forest St., Marlboro, MA, 01752

   ACCEL Technologies, Inc., 6825 Flanders Dr., San Diego, CA, 92121

4. Prototype Board Cutters:

   LPKF CAD/CAM Systems, Inc., 1800 NW 169th Place, Beaverton, OR, 97006

   T-Tech, Inc., 5591-B New Peachtree Road, Atlanta, GA, 34341

NOISE REDUCTION AND FILTERING FOR SWITCHING POWER SUPPLIES

Walt Jung and John McDonald

Precision analog circuitry has traditionally been powered from well regulated, low noise linear power supplies. During the last decade however, switching power supplies have become much more common in electronic systems. As a consequence, they also are being used for analog supplies. There are several good reasons for their popularity, including high efficiency, low temperature rise, small size, and light weight.

Switching power supplies, or more simply *switchers*, a category including switching regulators and switching converters, are by their nature efficient. Often this can be above 90%, and as a result, these power supply types use less power and generate less heat than do equivalent linear supplies.

A switcher can be as much as one third the size and weight of a linear supply delivering the same voltage and current. Switching frequencies can range from 20kHz to 1MHz, and as a result, relatively small components can be used in their design.

In spite of these benefits, switchers have their drawbacks, most notably high output noise. This noise generally extends over a broad band of frequencies, and occurs as both conducted and radiated noise, and unwanted electric and magnetic fields. Voltage output noise of switching supplies are short-duration voltage transients, or spikes. Although the fundamental switching frequency can range from 20kHz to 1MHz, the voltage spikes will contain frequency components extending easily to 100MHz or more.

Because of wide variation in the noise output characteristics of commercial switchers, they should always be purchased in accordance with a specification-control drawing. Although specifying switching supplies in terms of RMS noise is common vendor practice, as a user you should also specify the *peak* (or p-p) amplitudes of the switching spikes, with the output loading of your system. You should also insist that the switching-supply manufacturer inform you of any internal supply design changes that may alter the spike amplitudes, duration, or switching frequency. These changes may require corresponding changes in external filtering networks.

SWITCHING POWER SUPPLY CHARACTERISTICS

ADVANTAGES:

- **Efficient**
- **Small Size, Light Weight**
- **Low Operating Temperature Rise**
- **Isolation from Line Transients**
- **Wide Input/Output Range**

DISADVANTAGES:

- **Noise: LF, HF, Electric Field, Magnetic Field Conducted, Radiated**
- **DC regulation and accuracy can be poor**

Figure 9.19

This section discusses filter techniques for rendering a noisy switcher output *analog ready*, that is sufficiently quiet to power precision analog circuitry with relatively small loss of DC terminal voltage. These techniques include characterization of switcher output noise, identification of the frequency range of interference produced by the switching power supply, evaluation of passive components commonly used in external power supply filters, and the design and construction of a switching power supply filter. The filter solutions presented are generally applicable to all power supply types incorporating a switch element in their energy path. This includes various DC-DC converters, as well as the 5V PC type supply used in the example.

A TYPICAL 5V, 150W PC SWITCHING POWER SUPPLY

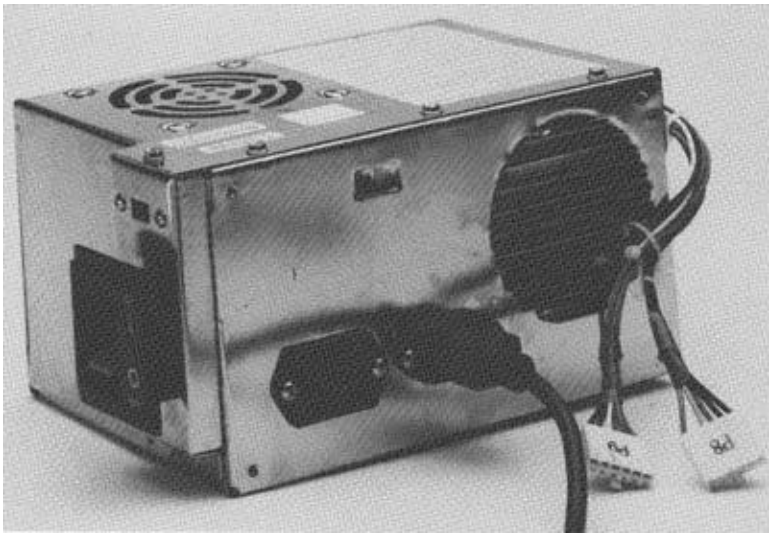

Figure 9.20

A typical 5V PC type switcher is shown in Figure 9.20, and typifies the style. A display of the 5V power buss of an operating desktop PC (Dell Dimension XPS P-90) using a similar (but not identical) supply is shown in Figure 9.21. The unfiltered output shown from this switcher exhibits a ~60mV p-p transient component at an 80kHz (roughly) switching frequency, as seen in the (A) left photo with the 5µs time base. The expanded scale photo for the same operating conditions of (B) right shows the detail of the switching glitches on a 100ns time base. The fast voltage spikes produce significant harmonics well into the high MHz range.

OUTPUT OF 5V PC SWITCHING POWER SUPPLY (UNFILTERED)

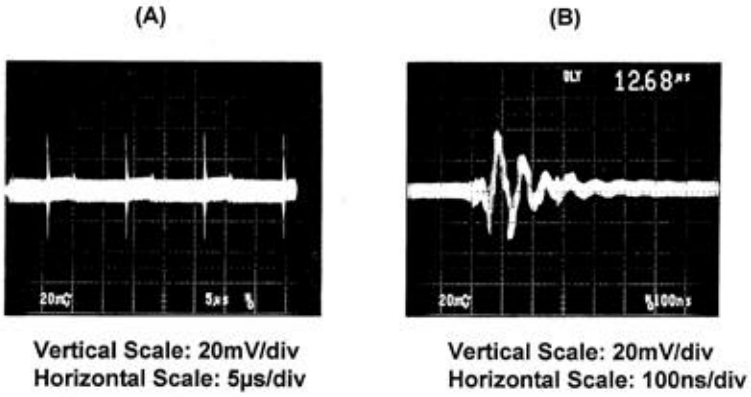

Figure 9.21

It is clear that this switcher is *not* analog ready, just as it is shown. Since many analog ICs show degraded power supply rejection at frequencies above a few kHz, some filtering is necessary. This will be particularly true for use with low power op amps, which can show PSRR degradation above a few hundred Hz. In general, all op amps, voltage references, DACs, and ADCs require clean supplies to meet their design accuracy. Switcher noise can prevent this happening, if left unchecked.

Before offering techniques to reduce switcher noise, a brief examination of switching supply architectures is helpful, and two popular ones are shown in Figure 9.22. Higher efficiency designs use a pulse width modulation technique for voltage regulation, while lower efficiency, lower noise designs use linear post regulators.

BASIC SWITCHING POWER SUPPLY TOPOLOGY

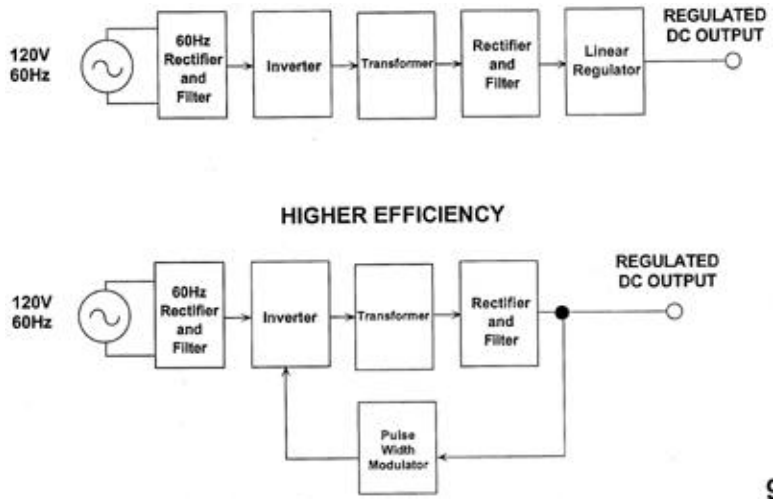

Figure 9.22

The raw AC line voltage is first rectified and filtered to a high DC level, then converted to a 30kHz (or higher) frequency square wave, which drives a transformer. The signal is again rectified, and filtered at the transformer output. Some switchers may use a linear regulator to form the final output voltage, as in the upper diagram. Others use pulse width regulation techniques to control the duty cycle of the transformer drive (lower diagram). Although more efficient, this results in more noise at the output than linear post-regulation.

It is important to understand that noise is generated in every stage of the switcher. The first stage AC line rectification creates current spikes, which produce line-related harmonic noise. In the inverter stage, fast pulse edges generate harmonics extending well beyond 5MHz. Furthermore, the parasitic capacitance within the primary and secondary windings of the transformer provide an additional path through which high-frequency noise can corrupt the DC output voltage. Finally, high-frequency noise is also generated by both rectifier stages.

An understanding of the EMI process is necessary to understand the effects of supply noise on analog circuits and systems. Every interference problem has a *source*, a *path*, and a *receptor* [Reference 1]. In general, there are three methods for dealing with interference. First, source emissions can be minimized by proper layout, pulse-edge rise time control/reduction, filtering, and proper grounding. Second, radiation and conduction paths should be reduced through shielding and physical separation. Third, receptor immunity to interference can be improved, via supply and signal line filtering, impedance level control, impedance balancing, and utilizing differential techniques to reject undesired common-mode signals. From this array of general noise immunity approaches, this section focuses on reducing switching power supply noise with external post filters.

THE INTERFERENCE PROCESS

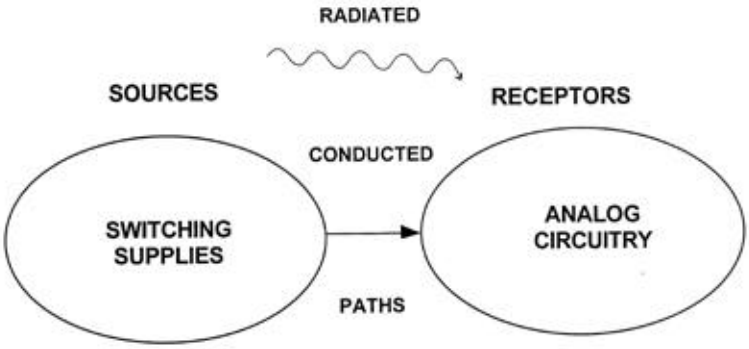

Figure 9.23

Before designing a switching supply filter, it is helpful to determine whether or not the supply noise is actually affecting the circuit performance. If critical node voltages in the circuit have transients synchronous with the switcher's operating frequency, then the supply is the likely culprit. A highly recommended method for determining if the supply is the noise source is to temporarily operate the circuit from a clean linear power supply or battery. If the interfering noise level drops dramatically, the switcher is guilty as charged. Note that lowering the power supply noise level may also help identify other noise sources which were masked by the higher switcher noise. Once the noise source is quantified and its path (radiated or conducted) identified, the process of reducing or eliminating it can begin.

Tools which can be used to combat switcher noise are highlighted by Figure 9.24. These tools differ in their electrical characteristics as well as their practicality towards noise reduction. For this reason they are listed roughly in a suggested order of priorities. Of the tools, inductance and capacitance are the most powerful filtering elements, and can also be the most cost-effective and small in size.

NOISE REDUCTION TOOLS

- **Capacitors**
- **Inductors**
- **Ferrites**
- **Resistors**
- **Linear Post Regulation**
- **PHYSICAL SEPARATION FROM SENSITIVE ANALOG CIRCUITS !!**

Figure 9.24

Capacitors are probably the single most important filter component for switchers. There are many different types of capacitors, and an understanding of their individual characteristics is absolutely mandatory to the design of practical, effective power supply filters. There are generally three classes of capacitors useful in filters in the 10kHz-100MHz frequency range suitable for switchers. These are broadly distinguished by their generic dielectric types; *electrolytic*, *film*, and *ceramic*. These dielectrics can in turn can be further sub-divided as discussed below. A thumbnail sketch of capacitor characteristics is shown in the chart of Figure 9.25. Background and tutorial information on capacitors can be found in Reference 2 and many vendor catalogs.

CAPACITOR SELECTION

	Aluminum Electrolytic (General Purpose)	Aluminum Electrolytic (Switching Type)	Tantalum Electrolytic	Polyester (Stacked Film)	Ceramic (Multilayer)
Size	100 µF (1)	120 µF (1)	100 µF (1)	1 µF	0.1 µF
Rated Voltage	25 V	25 V	20 V	400 V	50 V
ESR	0.6 Ω @ 100 kHz	0.18 Ω @ 100 kHz	0.12 Ω @ 100 kHz	0.11 Ω @ 1 MHz	0.12 Ω @ 1 MHz
Operating Frequency (2)	≅ 100 kHz	≅ 500 kHz	≅ 1 MHz	≅ 10 MHz	≅ 1 GHz

(1) Types shown in Figure 9.26 data
(2) Upper frequency limit is strongly size and package dependent

Figure 9.25

With any dielectric, a major potential filter loss element is ESR (equivalent series resistance), the net parasitic resistance of the capacitor. ESR provides an ultimate limit to filter performance, and requires more than casual consideration, because it can vary both with frequency and temperature in some types. Another capacitor loss element is ESL (equivalent series inductance). ESL determines the frequency where the net impedance of the capacitor switches from a capacitive to inductive

characteristic. This varies from as low as 10kHz in some electrolytics to as high as 100MHz or more in chip ceramic types. Both ESR and ESL are minimized when a leadless package is used, and all capacitor types discussed here are available in surface mount packages, which are preferable for high speed uses.

The *electrolytic* family provides an excellent, cost-effective low-frequency filter component, because of the wide range of values, a high capacitance-to-volume ratio, and a broad range of working voltages. It includes *general purpose aluminum electrolytic* types, available in working voltages from below 10V up to about 500V, and in size from 1 to several thousand µF (with proportional case sizes). All electrolytic capacitors are polarized, and thus cannot withstand more than a volt or so of reverse bias without damage. They have relatively high leakage currents (this can be tens of µA, but is strongly dependent upon specific family design, electrical size and voltage rating vs. applied voltage). However, this is not likely to be a major factor for basic filtering applications.

Also included in the electrolytic family are *tantalum* types, which are generally limited to voltages of 100V or less, with capacitance of 500µF or less[Reference 3]. In a given size, tantalums exhibit a higher capacitance-to-volume ratios than do the general purpose electrolytics, and have both a higher frequency range and lower ESR. They are generally more expensive than standard electrolytics, and must be carefully applied with respect to surge and ripple currents.

A subset of aluminum electrolytic capacitors is the *switching* type, which is designed and specified for handling high pulse currents at frequencies up to several hundred kHz with low losses [Reference 4]. This type of capacitor competes directly with the tantalum type in high frequency filtering applications, and has the advantage of a much broader range of available values.

More recently, high performance aluminum electrolytic capacitors using an organic semiconductor electrolyte have appeared [Reference 5]. These *OS-CON* families of capacitors feature appreciably lower ESR and higher frequency range than do the other electrolytic types, with an additional feature of low low-temperature ESR degradation.

Film capacitors are available in very broad ranges of values and an array of dielectrics, including polyester, polycarbonate, polypropylene, and polystyrene. Because of the low dielectric constant of these films, their volumetric efficiency is quite low, and a 10µF/50V polyester capacitor (for example) is actually a handful. Metalized (as opposed to foil) electrodes does help to reduce size, but even the highest dielectric constant units among film types (polyester, polycarbonate) are still larger than any electrolytic, even using the thinnest films with the lowest voltage ratings (50V). Where film types excel is in their low dielectric losses, a factor which may not necessarily be a practical advantage for filtering switchers. For example, ESR in film capacitors can be as low as 10milliohms or less, and the behavior of films generally is very high in terms of Q. In fact, this can cause problems of spurious resonance in filters, requiring damping components.

Typically using a wound layer-type construction, film capacitors can be inductive, which can limit their effectiveness for high frequency filtering. Obviously, only non-inductively made film caps are useful for switching regulator filters. One specific style which is non-inductive is the *stacked-film* type, where the capacitor plates are cut as small overlapping linear sheet sections from a much larger wound drum of dielectric/plate material. This technique offers the low inductance attractiveness of a plate sheet style capacitor with conventional leads [see type "V" of Reference 4, plus Reference 6]. Obviously, minimal lead length should be used for best high frequency effectiveness. Very high current polycarbonate film types are also available, specifically designed for switching power supplies, with a variety of low inductance terminations to minimize ESL [Reference 7].

Dependent upon their electrical and physical size, film capacitors can be useful at frequencies to well above 10MHz. At the very high frequencies, stacked film types only should be considered. Some manufacturers are also supplying film types in leadless surface mount packages, which eliminates the lead length inductance.

Ceramic is often the capacitor material of choice above a few MHz, due to its compact size, low loss, and availability in values up to several µF in the high-K dielectric formulations of X7R and Z5U, at voltage ratings up to 200V [see ceramic families of Reference 3]. NP0 (also called COG) types use a lower dielectric constant formulation, and have nominally zero TC, plus a low voltage coefficient (unlike the less stable high-K types). The NP0 types are limited in available values to 0.1µF or less, with 0.01µF representing a more practical upper limit.

Multilayer ceramic "chip caps" are increasingly popular for bypassing and filtering at 10MHz or more, because their very low inductance design allows near optimum RF bypassing. In smaller values, ceramic chip caps have an operating frequency range to 1GHz. For these and other capacitors for high frequency applications, a useful value can be ensured by selecting a value which has a self-resonant frequency *above* the highest frequency of interest.

All capacitors have some finite ESR. In some cases, the ESR may actually be helpful in reducing resonance peaks in filters, by supplying "free" damping. For example, in general purpose, tantalum and switching type electrolytics, a broad series resonance region is noted in an impedance vs. frequency plot. This occurs where |Z| falls to a minimum level, which is nominally equal to the capacitor's ESR at that frequency. In an example below, this low Q resonance is noted to encompass quite a wide frequency range, several octaves in fact. Contrasted to the very high Q sharp resonances of film and ceramic caps, this low Q behavior can be useful in controlling resonant peaks.

In most electrolytic capacitors, ESR degrades noticeably at low temperature, by as much as a factor of 4-6 times at –55°C vs. the room temperature value. For circuits where a high level of ESR is critical, this can lead to problems. Some specific electrolytic types do address this problem, for example within the HFQ switching types, the –10°C ESR at 100kHz is no more than 2× that at room temperature. The OSCON electrolytics have a ESR vs. temperature characteristic which is relatively flat.

Figure 9.26 illustrates the high frequency impedance characteristics of a number of electrolytic capacitor types, using nominal 100µF/20V samples. In these plots, the impedance, |Z|, vs. frequency over the 20Hz-200kHz range is displayed using a high resolution 4-terminal setup [Reference 8]. Shown in this display are performance samples for a 100µF/25V general purpose aluminum unit (top curve @ right), a 120µF/25V HFQ unit (next curve down @ right), a 100µF/20V tantalum bead type (next curve down @ right), and a 100µF/20V OS-CON unit (lowest curve @ right). While the HFQ and tantalum samples are close in 100kHz impedance, the general purpose unit is about 4 times worse. The OS-CON unit is nearly an order of magnitude lower in 100kHz impedance than the tantalum and switching electrolytic types.

IMPEDANCE Z (Ω) VS. FREQUENCY (Hz) FOR 100µF ELECTROLYITC CAPACITORS (AC CURRENT = 50mA RMS)

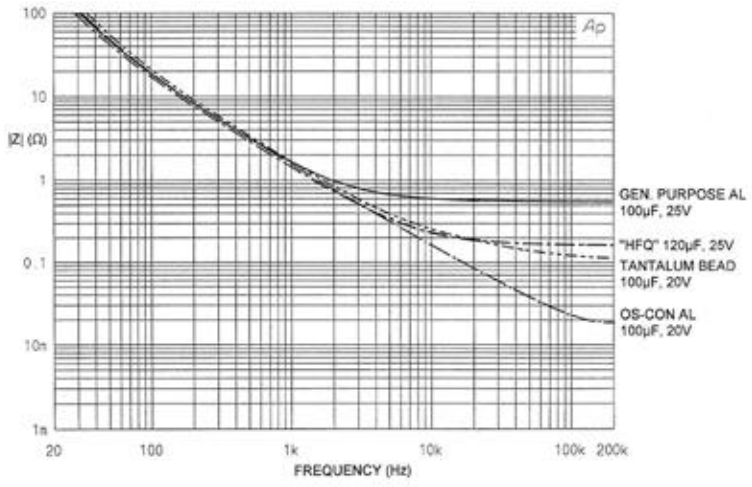

Figure 9.26

As noted above, all real capacitors have parasitic elements which limit their performance. As an insight into why the impedance curves of Figure 9.26 appear the way they do, a (simplified) model for a 100µF/20V tantalum capacitor is shown in Figure 9.27.

SIMPLIFIED SPICE MODEL FOR LEADED
100μF/20V TANTALUM ELECTROLYTIC CAPACITOR

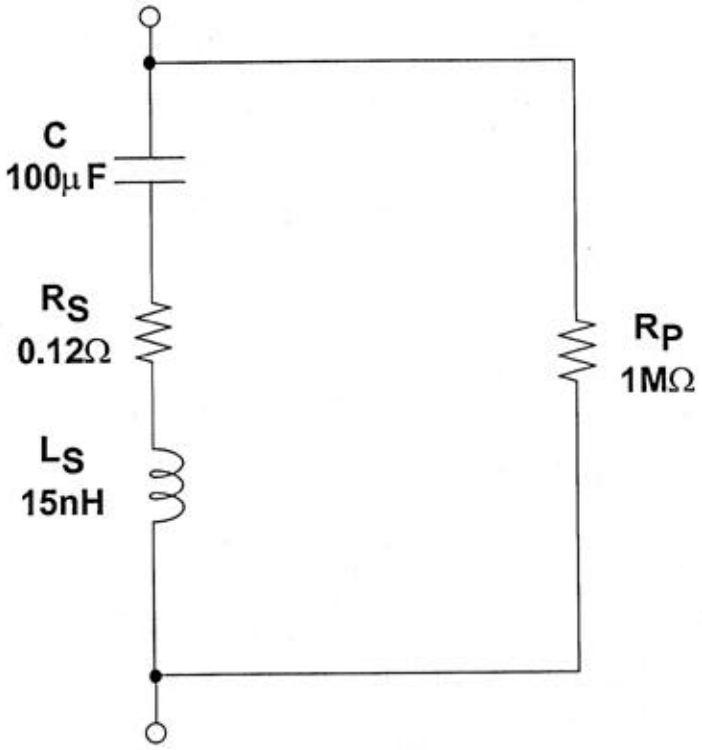

Figure 9.27

The electrical network representing this capacitor is shown, and it models the ESR and ESL components with simple R and L elements, plus a 1megohm shunt resistance. While this simple model ignores temperature and dielectric absorption effects which occur in the real capacitor, it is still sufficient for this discussion.

When driven with a constant level of AC current swept from 10Hz to 100MHz, the voltage across this capacitor model is proportional to its net impedance, which is shown in Figure 9.28.

100μF / 20V TANTALUM CAPACITOR SIMPLIFIED MODEL
IMPEDANCE (Ω) VS. FREQUENCY (Hz)

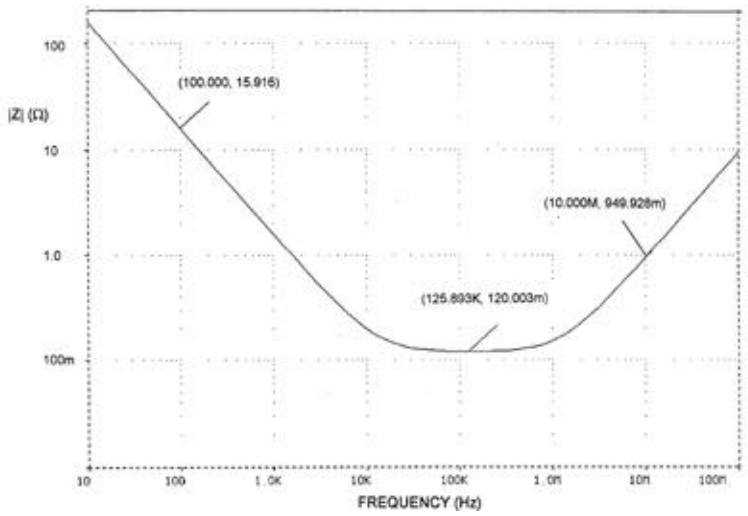

Figure 9.28

At low frequencies the net impedance is almost purely capacitive, as noted by the 100Hz impedance of 15.9ohms. At the bottom of this "bathtub" curve, the net impedance is determined by ESR, which is shown to be 0.12ohms at 125kHz. Above about 1MHz this capacitor becomes inductive, and impedance is dominated by the effect of ESL. While this particular combination of capacitor characteristics have been chosen purposely to correspond to the tantalum sample used with Figure 9.26, it is also true that all electrolytics will display impedance curves which are similar in general shape. The minimum impedance will vary with the ESR, and the inductive region will vary with ESL (which in turn is strongly effected by package style). The simulation curve of Figure 9.28 can be considered as an extension of the 100μF/20V tantalum capacitor curve from Figure 9.26.

Ferrites (non-conductive ceramics manufactured from the oxides of nickel, zinc, manganese, or other compounds) are extremely useful for decoupling in power supply filters [Reference 9]. At low frequencies (<100kHz), ferrites are inductive; thus they are useful in low-pass LC filters. Above 100kHz, ferrites becomes resistive, an important characteristic in high-frequency filter designs. Ferrite impedance is a function of material, operating frequency range, DC bias current, number of turns, size, shape, and temperature. Figure 9.29 summarize a number ferrite characteristics.

CHARACTERISTICS OF FERRITES

- **Good for frequencies above 25kHz**
- **Many sizes and shapes available including leaded "resistor style"**
- **Ferrite impedance at high frequencies is primarily resistive – Ideal for HF filtering**
- **Low DC loss: Resistance of wire passing through ferrite is very low**
- **High saturation current**
- **Low cost**

Figure 9.29

Several ferrite manufacturers offer a wide selection of ferrite materials from which to choose, as well as a variety of packaging styles for the finished network (see References 10 and 11). The most simple form is the *bead* of ferrite material, a cylinder of the ferrite which is simply slipped over the power supply lead to the stage being decoupled. Alternately, the *leaded ferrite bead* is the same bead, mounted by adhesive on a length of wire, and used simply as a component (Reference 11 typifies these two styles). More complex beads offer multiple holes through the cylinder for increased decoupling, plus other variations. Surface mount bead styles are also available.

FERRITE IMPEDANCE DEPENDS ON

- **Material**
- **Permeability**
- **Frequency**
- **Number of Turns**
- **Size**
- **Shape**
- **Temperature**
- **Field Strenght (generated by current flowing through wire)**

Figure 9.30

Recently, PSpice ferrite models for Fair-Rite materials have become available that allow ferrite impedance to be estimated [Reference 12]. The models of Fair-Rite materials #43 and #73 can be downloaded from the MicroSim bulletin board (714-830-1550). These models have been designed to match measured impedances rather than theoretical impedances.

A ferrite's impedance is dependent upon a number of inter-dependent variables, and is difficult to quantify analytically, thus selecting the proper ferrite is not straightforward. However, knowing the following system characteristics will make selection easier. First, determine the frequency range of the noise to be filtered. A spectrum analyzer is useful here. Second, the expected temperature range of the filter should be known, because ferrite impedance varies with temperature. Third, the DC bias current flowing through the ferrite must be known, to ensure that the ferrite does not saturate. Although models and other analytical tools may prove useful, the general guidelines given above, coupled with some experimentation with the actual filter connected to the supply output under system load conditions, should ultimately lead to the selection of the proper ferrite.

CHOOSING THE RIGHT FERRITE DEPENDS ON

- **Source of Interference**
- **Interference Frequency Range**
- **Impedance Required at Interference Frequency**
- **Environmental Conditions:**
  Temperature, AC and DC Field Strength,
  Size / Space Available
- **Don't fail to Test the Design -------**

EXPERIMENT! EXPERIMENT!

Figure 9.31

Maintaining high power supply efficiency requires the intelligent limiting of series resistors and linear post regulators in the switching supply's output. However, small resistors (generally less than 10ohms) can be used in applications where load currents are low and load regulation is not highly critical.

Higher performance linear post regulators can provide 60dB and more of power supply rejection up to 100kHz, for example see the designs of [Reference 8]. When used with effective input filtering, their PSRR can be extended above 1MHz or higher. Linear post regulation will generally result in a net efficiency decrease, which can be serious if the regulator requires several volts of headroom. The PSRR vs. frequency performance of a linear post regulator should also be carefully considered. For example, some low dropout linear regulators offer very little power supply rejection at frequencies above a few kHz, a performance fact of life which must be traded off against the efficiency advantages of the <100mV level dropouts they can boast.

Using the component selection choices mentioned above, low and high frequency band filters can be designed to smooth the noisy switcher's DC output so as to produce an *analog ready* 5V supply. It is most practical to do this over two (and sometimes more) stages, with each stage optimized for a range of frequencies. One basic stage can be used to carry all of the DC load current, and filter noise by 60dB or more up to about 10MHz. This larger filter is used as a *card entry filter* providing broadband filtering for all analog power entering the PC board. Thereafter, smaller

and more simple local filter stages can be used to provide very high frequency decoupling, right at the power pins of the individual ICs.

Figure 9.32 illustrates a card entry filter suitable for use with switching supplies. Because of the low rolloff point of 1.5kHz and mV level DC errors, it will be effective for a wide variety of filter applications just as it is shown. This filter is a single stage LC low-pass filter covering the 1kHz to 1MHz range, using carefully chosen parts. Because of component losses, it begins to lose effectiveness above a few MHz, but is still able to achieve an attenuation approaching 60dB at 1MHz.

The key to low DC losses is the use of input choke, L1, a ferrite-core unit selected for a low DC resistance (DCR) of <0.25ohms at the 100µH inductance. The prototype was tested with an axial lead type 5250 choke, but the radial style 6000-101K should give comparable results [Reference 13]. Both chokes have a low inductance shift due to the 300mA load current. The low DCR allows the 300mA to be passed with no more than 75mV of DC error at full load. Alternately, resistive filtering might be used in place of L1, but the basic tradeoff here is that load current capacity will be compromised for comparable DC errors. For example, a 1ohm resistor with a 75mV DC allowable error can pass only a 75mA current.

C1, a 100µF/20V tantalum type, provides the bulk of the capacitive filtering, shunted by a 1µF multilayer ceramic. The remaining part of the filter is R1, a damping resistor used to control resonant peaks.

"CARD-ENTRY" SWITCHING SUPPLY FILTER

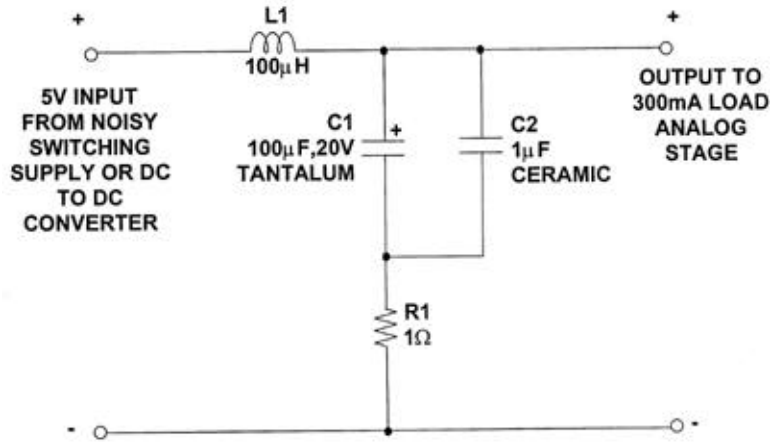

Figure 9.32

Figure 9.33 shows the frequency response of this filter, both in terms of a SPICE simulation as well as lab measurements. There is good agreement between the simulation and the measurements for the common range below 1MHz. Measurements were not made above 1MHz, since higher frequencies are attenuated by second stage localized high frequency filters.

This filter has some potential pitfalls, and one of them is the control of resonances. If the LCR circuit formed does not have sufficiently high resistance at the resonant frequency, amplitude peaking will result. This peaking can be minimized with resistance at two locations: in series with L1, or in series with C1+C2. Obviously, limited resistance is usable in series with L1, as this increases the DC errors. Thus the use of the C1+C2 series damping resistor R1, which should not be eliminated. The 1ohm value used actually provides a slightly underdamped response, with peaking on the order of 1dB. An alternate value of 1.5ohms can also be used for less peaking, if this is desired, but the tradeoff here is that the attenuation below 1MHz will then suffer.

Note that if the damping resistor were to be eliminated or an excessively low value used, it is possible that a transient at the frequency of L1-(C1+C2) resonance could cause the filter to ring, actually exacerbating whatever peak amplitude occurs at the input. Of course, keeping the basic filter corner frequency well below the lowest commonly used switcher frequency of 20kHz also helps to minimize this possibility. A side benefit of R1 is that it buffers variations in parasitic resistance in L1 and C1, by making them smaller percentage of the total resistance, and thus less likely to effect overall performance. For wide temperature applications however, temperature changes of the filter characteristics will still need consideration.

OUTPUT RESPONSE OF "CARD-ENTRY" FILTER
LAB VS. SIMULATION

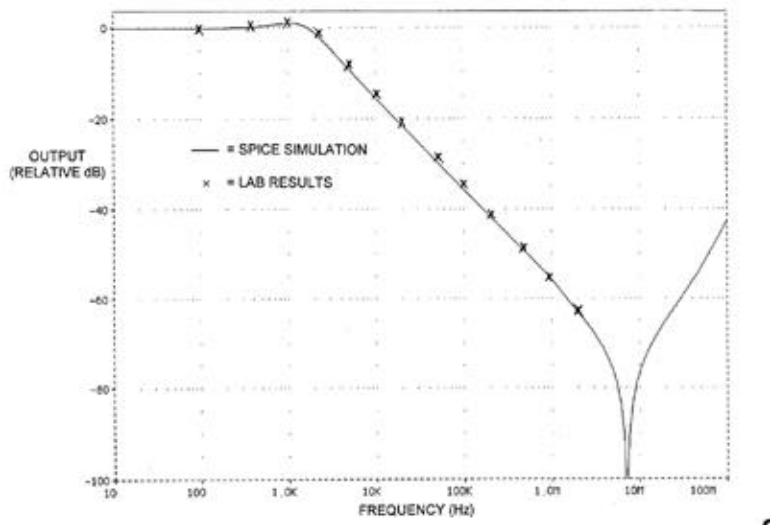

Figure 9.33

Because of the high sensitivity to source series resistance of this filter, measuring its frequency response is not a trivial task. The low output impedance high current unity gain buffer of Figure 9.34 was used for the data of Figure 9.33. Note that the filter presents a load of ~1ohms to the source at resonance, so the buffer drive level is kept less than 100mV RMS, to prevent buffer current limiting.

TEST SETUP FOR MEASURING FILTER FREQUENCY RESPONSE

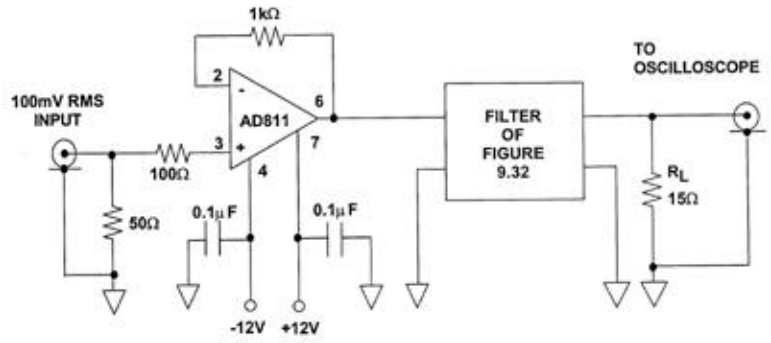

Figure 9.34

A local high frequency filter which can be used in conjunction with the card entry filter is shown in Figure 9.35. This simple filter can be considered an option, one which is exercised dependent upon the high frequency characteristics of the associated IC and the relative attenuation desired. It is composed of Z1, a leaded ferrite bead such as the Panasonic EXCELSA39, which provides a resistance of more than 80ohms at 10MHz, increasing to over 100ohms at 100MHz. The ferrite bead is best used with a local high frequency decoupling cap right at the IC power pins, such as a 0.1μF ceramic unit shown.

HIGH FREQUENCY LOCALIZED DECOUPLING

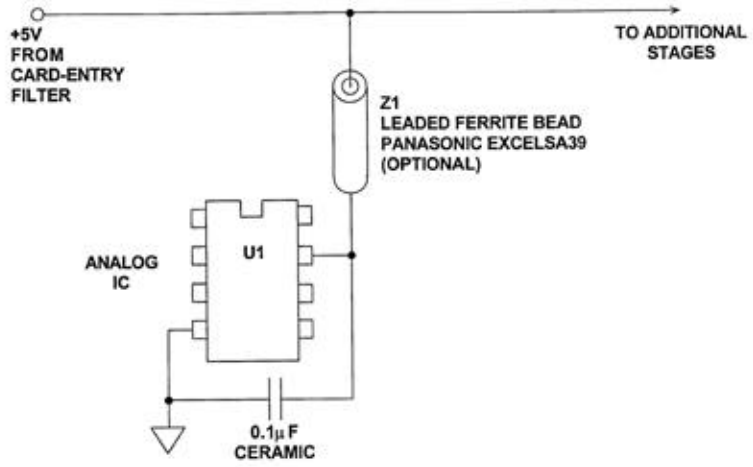

Figure 9.35

Both the card entry filter and the local high frequency decoupling filters are designed to filter differential-mode noise only. They use components commonly available off the shelf from national distributors [Reference 14].

The following is a list of switching power supply filter layout and construction guidelines which will help guarantee that the filter does the best job possible:

(1) *Pick the highest electrical value and voltage rating for filter capacitors which is consistent with budget and space limits. This minimizes ESR, and maximizes filter performance. Pick chokes for low inductance change at the rated DC current, as well as low DCR.*

(2) *Use short and wide PCB tracks to decrease voltage drops and minimize inductance. Make track widths at least 200 mils for every inch of track length for lowest DCR, and use 1 oz or 2 oz copper PCB traces to further reduce IR drops and inductance.*

(3) *Use short leads or leadless components, to minimize lead inductance. This will minimize the tendency to add excessive ESL and/or ESR. Surface mount packages are preferred.*

(4) *Use a large-area ground plane for minimum impedance.*

(5) *Know what your components do over frequency, current and temperature variations! Make use of vendor component models for the simulation of prototype designs, and make sure that lab measurements correspond reasonably with the simulation. While simulation is not* absolutely *necessary, it does instill confidence in a design when correlation is achieved* (see Reference 15).

The discussion of switching power supplies so far has focused on filtering the output of the supply. This assumes that the incoming AC power is relatively clean, an assumption not always valid. However, the AC power can also be an EMI path, both entering and exiting the equipment. To remove this path and reduce emissions caused by the switching power supply and other circuits in the instrument, a power line filter is required. *Remember that the AC line power can be lethal! Do not experiment without proper equipment and training!*

All components used in power line filters should be UL approved, and the best way to provide this for your equipment is to specify only a complete, packaged UL approved filter. It should be installed in such a manner that it is the first thing the AC line sees upon entering the equipment. Standard three wire IEC style line cords are designed to mate with three terminal male connectors, which are integral to many line filters. This is the best way to do this function, as this automatically grounds the third wire to the shell of the filter and equipment chassis via a low inductance path.

POWER LINE FILTERING IS ALSO IMPORTANT

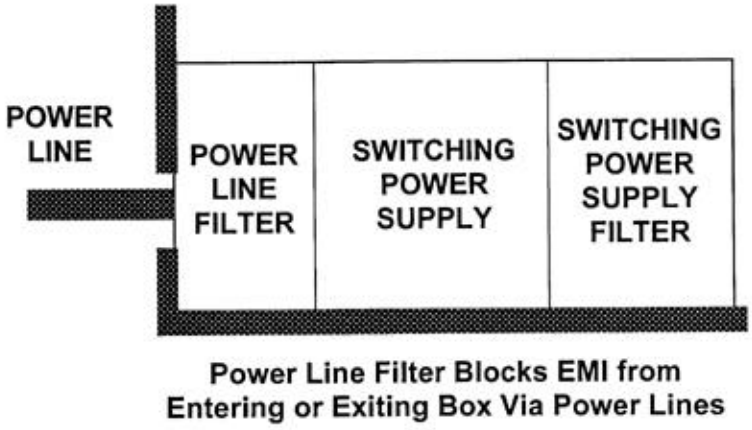

Figure 9.36

Commercial power line filters, such as the one shown schematically in Figure 9.37, can be quite effective in reducing noise. AC power-line noise is generally has both common-mode and differential-mode components. Common-mode noise is noise that is found on any two of the three power connections (black, white, or green) with the same amplitude and polarity. In contrast, differential-mode noise is noise found only between two lines.

TYPICAL COMMERCIAL POWER LINE FILTER

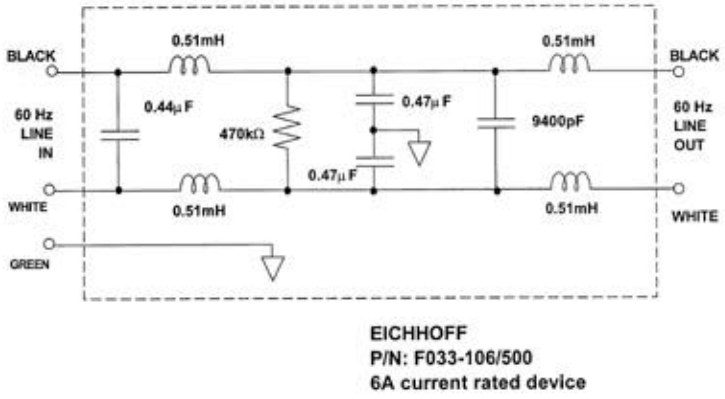

Figure 9.37

Common-mode noise is dominant at frequencies over 1MHz and is generally introduced into the AC lines through capacitive coupling. Ferrites provide effective filtering of the high frequency common-mode noise when used as common-mode chokes. For example, to create an effective common-mode choke, a few turns of the input power leads can be wound around a large ferrite. This provides a simple and effective solution for common-mode noise, but is ineffective against differential-mode noise. Differential-mode noise can be minimized by using proper LC filtering

techniques as described earlier in this section, using proper UL approved across-the-line rated components. A power-line filter must be designed to minimize both common- and differential-mode noise to keep EMI from entering and leaving the system.

POWER LINE NOISE MODES

- **Common Mode:**
  - **Dominates above 1MHz, Primarily Capacitive Coupled**
  - **2200 to 4700pF typical shunt capacitor values**
  - **0.5 to 10mH typical series ferrite values**
- **Differential Mode:**
  - **Dominates below 1MHz**
  - **0.1 to 2.2μF typical shunt capacitor values**
  - **Molyperm or powdered iron inductors, 100 to 200μH, typical series values**

Figure 9.38

Notice the common-mode choke formed by the inductors on both sides of the filter in Figure 9.37. These inductors have a dual role, because they are also part of the differential-mode LC filters. This filter, using multiple stages, is an example of a higher quality type.

As noted, the AC power line filter should be in good electrical contact with the chassis of the instrument. Furthermore, connecting the AC power line directly into the power line filter reduces the possibility of EMI entering or exiting the instrument. If this is not possible, routing the filter AC input power lines close to the chassis and twisting them will help minimize loop areas and minimize LF magnetic coupling.

The power supply filter should be located as close as possible to the switching power supply; i.e., in commercial units it is always integral to the supply. Many switching power supplies have steel enclosures which can be used for electric and LF magnetic shielding (however, the enclosure must be connected to chassis ground to act as a Faraday shield).

If digital circuitry is present, the digital power pick-off point should occur *before* the switching power supply filter. This minimizes the digital noise in the output of the switching supply filter, plus minimizes any potential DC error form the higher currents.

POWER LINE FILTER PLACEMENT IS IMPORTANT

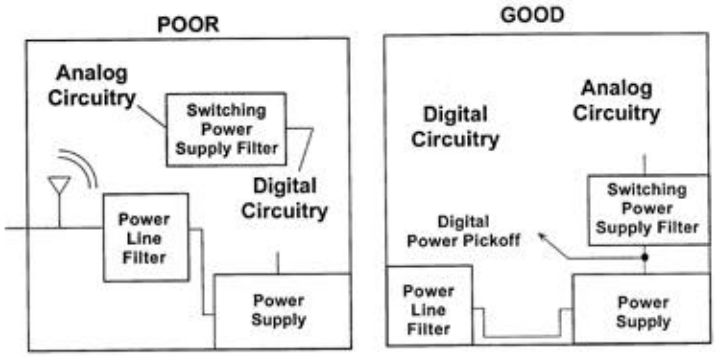

Figure 9.39

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LOW DROPOUT REFERENCES AND REGULATORS

Walt Jung

Many circuits require stable regulated voltages relatively close in potential to an unregulated source. An example would be a linear post regulator for a switching power supply, where voltage loss is critical. This low dropout type of regulator is readily implemented with a rail-rail output op amp. The wide output swing and low saturation voltage enables outputs to come within a fraction of a volt of the source for medium current (<30mA) loads, such as reference applications. For higher output currents, the rail-rail voltage swing feature allows direct drive to low saturation voltage pass devices, such as power PNPs or P-channel MOSFETs. Op amps which work from 3V up with the rail-rail features are most suitable here, providing power economy and maximum flexibility.

BASIC REFERENCES IN LOW POWER SYSTEMS

Among the many problems in making stable DC voltage references work from 5V and lower supplies are quiescent power consumption, overall efficiency, the ability to operate down to 3V, low input/output (dropout) capability, and minimum noise output. Because such low voltage supplies can't support 6V zeners, these low voltage references must necessarily be bandgap based-- a 1.2V potential.

One difficulty is simply to get a reference circuit which works well at 3V inputs, conditions which dictate a lower voltage reference diode. A workhorse circuit solution is the reference and appropriate low power scaling buffer shown in Figure 9.40. Here a low current 1.2V diode is used for D1, the 1.235V AD589. Resistor R1 sets the current, chosen for 50µA at the minimum supply of 2.7V. Obviously, loading on the unbuffered diode must be minimized at the V_{REF} node.

RAIL-RAIL OUTPUT OP AMPS ALLOW GREATEST FLEXIBILITY IN LOW DROPOUT REFERENCES

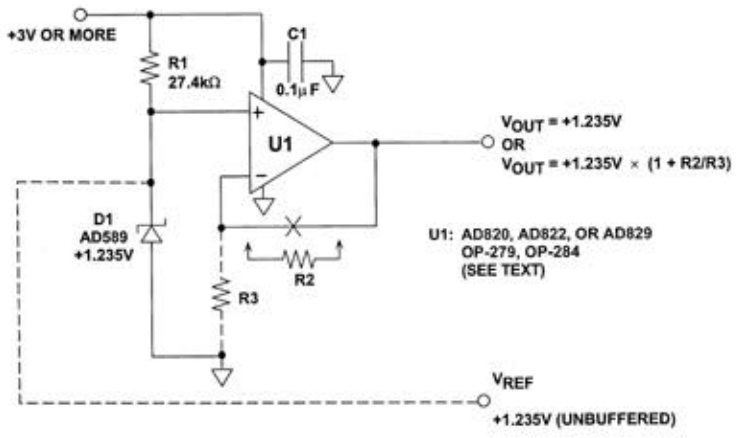


Figure 9.40

The amplifier U1 both buffers and optionally scales up the 1.2V reference, allowing higher source/sink currents. A higher op amp quiescent current is expended in doing this, and is a basic design tradeoff of this approach. This current can range from 150-300µA/channel with the OP295/495 and OP191/291/491 series for U1, 620µA/channel using an AD820/822/824 section, or in the range of 1000-2000µA/channel with the OP284 and OP279. The former two series are most useful for very light loads (<2mA), while the latter three series provide device dependent outputs up to 50mA. All devices are simply used in the circuit as shown, and their key specs are summarized in Figure 9.41.

OP AMPS USEFUL IN LOW VOLTAGE RAIL-RAIL REFERENCES AND REGULATORS

Device*	Iq/channel mA	Vsat(+), V(min @ mA)	Vsat(-), V (max @ mA)	Isc, mA (min)
OP193/293/493	0.017	4.20 @ 1	0.280 @ 1 (typ)	± 8
OP295/495	0.150 (max)	4.50 @ 1	0.110 @ 1	± 11
OP191/291/491	0.300	4.80 @ 2.5	0.075 @ 2.5	± 8.75
AD820/822	0.620	4.89 @ 2	0.055 @ 2	± 15
OP284/484	1.250 (max)	4.85 @ 2.5	0.125 @ 2.5	± 7.5
OP279	2.000	4.80 @ 10	0.075 @ 10	± 45

*Typical device specifications @ Vs = +5V, T_A = 25°C, unless otherwise noted.

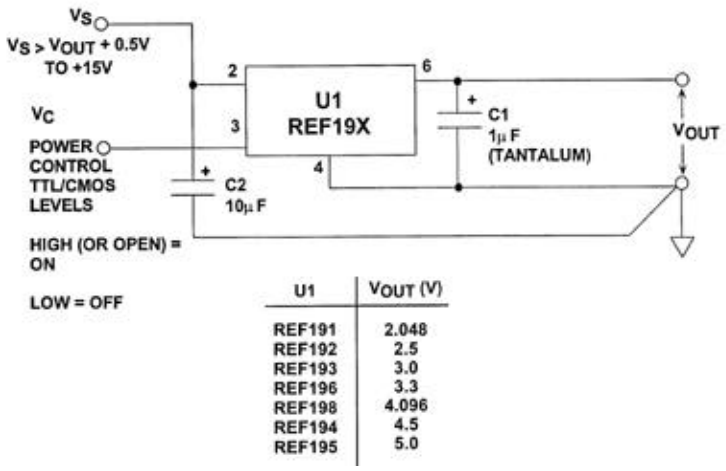
Figure 9.41

In Figure 9.40, without gain scaling resistors R2-R3, V_{OUT} is simply 1.235V. With the resistors, V_{OUT} can be anywhere between the rails, due to the rail-rail output swing of the op amps mentioned above. With rail-rail devices, this buffered reference is inherently "low dropout", allowing a +4.5V reference output on a +5V supply, for example. The general expression for V_{OUT} is shown in the figure, where "V_{REF}" is the reference voltage, in this case 1.235V.

Amplifier standby current can be optionally reduced to below 20µA if an amplifier from the OP193/293/493 series is used. This will be at the expense of current drive and positive rail saturation, but does provide the lowest possible quiescent current when necessary. All devices operate from voltages down to 3V (except the OP279, which operates at 5V).

Power conservation can be a critical issue with references, as can output DC precision. For such applications, simple one-package fixed voltage references which simply "drop in" with minimal external circuitry and deliver high accuracy are most attractive. Two unique features of the three terminal REF19X bandgap reference family are low power, and shutdown capability. The series allows fixed outputs from 2.048-5V to be controlled between ON and OFF, via a TTL/CMOS power control input. It provides precision reference quality for those popular voltages shown in Figure 9.42.

30mA REFERENCE FAMILY WITH OPTIONAL SHUTDOWN



U1	VOUT (V)
REF191	2.048
REF192	2.5
REF193	3.0
REF196	3.3
REF198	4.096
REF194	4.5
REF195	5.0

Figure 9.42

The REF19X family can be used as a simple three terminal fixed reference as per the table by tying pins 2 and 3 together, or as an ON/OFF controlled device, by programming pin 3 as noted. In addition to the shutdown capacity, the distinguishing functional features are a low dropout of 0.5V at 10mA, and a low current drain for both quiescent and shutdown states, 45 and 15µA (max.), respectively. For example, working from inputs in the range of 6.3 to 15V, a REF195 used as shown drives 5V loads at up to 30mA, with grade dependent tolerances of ±2 to ±5mV, and max TCs of 5 to 25ppm/°C. Other devices in the series provide comparable accuracy specifications, and all have low dropout features.

To maximize DC accuracy in this circuit, the output of U1 should be connected directly to the load with short heavy traces, to minimize IR drops. The common terminal (pin 4) is less critical due to lower current in this leg.

LOW DROPOUT REGULATORS

By adding a boost transistor to the basic rail-rail output low dropout reference of Figure 9.40, output currents of 100mA or more are possible, while still retaining features of low standby current and low dropout voltage. Figure 9.43 shows a low dropout regulator with 800µA standby current, suitable for a variety of outputs at current levels of 100mA.

100mA LOW NOISE, LOW DROPOUT REGULATOR

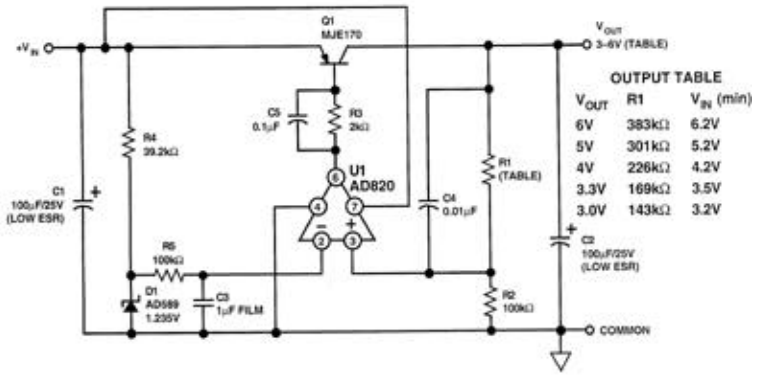


Figure 9.43

The 100mA output is achieved with a controlled gain bipolar power transistor for pass device Q1, an MJE170. Maximum output current control is provided by limiting base drive to Q1 with series resistor R3. This limits the base current to about 2mA, so the max H_{FE} of Q1 then allows no more than 500mA, thus limiting Q1's short circuit dissipation to safe levels.

Overall, the circuit operates as a follower with gain, as was true in the case of Figure 9.40, so V_{OUT} has a similar output expression. The circuit is adapted for different voltages simply by programming R1 via the table. Dropout with a 100mA load is about 200mV, thus a 5V output is maintained for inputs above 5.2V (see table), and V_{OUT} levels down to 3V are possible. Step load response of this circuit is quite good, and transient error is only a few mVp-p for a 30-100mA load change. This is achieved with low ESR switching type capacitors at C1-C2, but the circuit also works with conventional electrolytics (with higher transient errors).

If desired, lowest output noise with the AD820 is reached by including the optional reference noise filter, R5-C3. Lower current op amps can also be used for lower standby current, but with larger transient errors due to reduced bandwidth.

While the 30mA rated output current of the REF19X series is higher than most reference ICs, it can be boosted to much higher levels if desired, with the addition of a PNP transistor, as shown in Figure 9.44. This circuit uses full time current limiting for protection of pass transistor shorts.

150mA BOOSTED OUTPUT REGULATOR/REFERENCE WITH CURRENT LIMITING

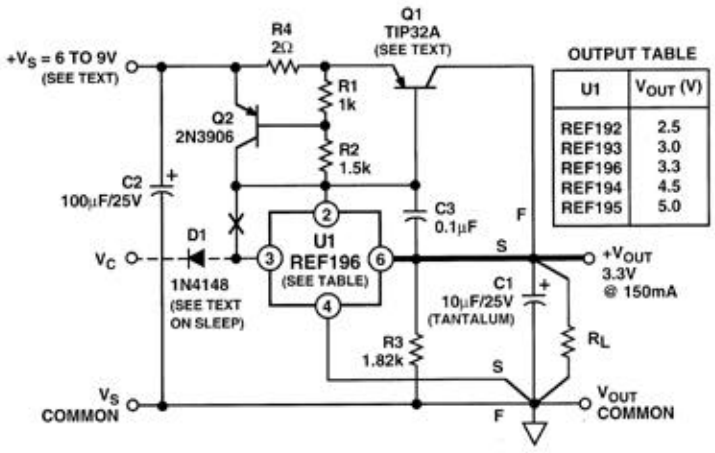


Figure 9.44

In this circuit the supply current of reference U1 flows in R1-R2, developing a base drive for pass device Q1, whose collector provides the bulk of the output current. With a typical gain of 100 in Q1 for 100-200mA loads, U1 is never required to furnish more than a few mA, and this factor minimizes temperature related drift. Short circuit protection is provided by Q2, which clamps drive to Q1 at about 300mA of load current. With separation of control/power functions, DC stability is optimum, allowing best advantage of premium grade REF19X devices for U1. Of course, load management should still be exercised. A short, heavy, low resistance conductor should be used from U1-6 to the V_{OUT} sense point "S", where the collector of Q1 connects to the load.

Because of the current limiting, dropout voltage is raised about 1.1V over that of the REF19X devices. However, overall dropout typically is still low enough to allow operation of a 5 to 3.3V regulator/reference using the 3.3V REF-196 for U1, with a Vs of 4.5V and a load current of 150mA.

The heat sink requirements of Q1 depend upon the maximum power. With Vs = 5V and a 300mA current limit, the worst case dissipation of Q1 is 1.5W, less than the TO-220 package 2W limit. If TO-39 or TO-5 packaged devices such as the 2N4033 are used, the current limit should be reduced to keep maximum dissipation below the package rating, by raising R4. A tantalum output capacitor is used at C1 for its low ESR, and the higher value is required for stability. Capacitor C2 provides input bypassing, and can be a ordinary electrolytic.

Shutdown control of the booster stage is shown as an option, and when used, some cautions are in order. To enable shutdown control, the connection to U1-2 and U1-3 is broken at "X", and diode D1 allows a CMOS control source to drive U1-3 for ON/OFF control. Startup from shutdown is not as clean under heavy load as it is with the basic REF19X series stand-alone, and can require several milliseconds

under load. Nevertheless, it is still effective, and can fully control 150mA loads. When shutdown control is used, heavy capacitive loads should be minimized.

By combining a REF19X series reference IC with a rail-rail output op amp, the best of both worlds is realized performance-wise (see Figure 9.45). The REF19X basic reference provides a stable low TC voltage source with low current drain, while the rail-rail output op amp provides high output current with both sink/source load capability.

30mA OUTPUT CURRENT REGULATOR/REFERENCE

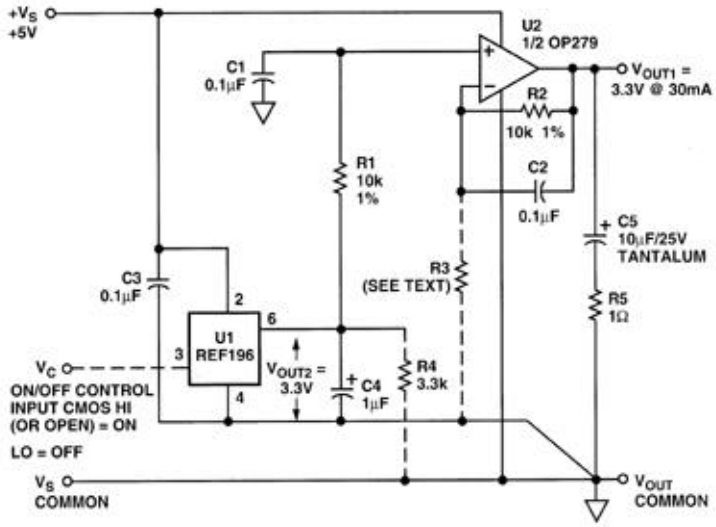


Figure 9.45

The low dropout performance of this circuit is provided by stage U2, 1/2 of an OP279 connected as a follower/buffer for the V_{OUT2} as produced by U1. The low voltage saturation characteristic of the OP279 allows up to 30 mA of load current in the illustrated use, a 5V to 3.3V converter. In this application the stable 3.3V from U1 is applied to U2 through a noise filter, R1-C1. U2 replicates the U1 voltage within a few mV, but at a higher current output at V_{OUT1}. It also has ability to both sink and source output current(s), unlike most IC references. R2 and C2 in the feedback path of U2 provide bias compensation for lowest DC error and additional noise filtering.

To scale V_{OUT2} to another (higher) output level, the optional resistor R3 (shown dotted) is added, causing the new V_{OUT1} to become:

$$V_{OUT1} = V_{OUT2}\left[1 + \frac{R2}{R3}\right]$$

As an example, for a V_{OUT1} = 4.5V, and V_{OUT2} = 2.5V from a REF192, the gain required of U2 is 1.8 times, so R3 and R2 would be chosen for a ratio of 1.25/1, or 22.5kohm/18kohm. Note that for the lowest V_{OUT1} DC error, R2||R3 should be

maintained equal to R1 (as here), and the R2-R3 resistors should be stable, close tolerance metal film types.

Performance of the circuit is good in both AC and DC senses, with the measured DC output change for a 30mA load change under 1mV, equivalent to an output impedance of <0.03ohm. The transient performance for a step change of 0-10mA of load current is determined largely by the R5-C5 output network. With the values shown, the transient is about 10mV peak, and settles to within 2mV in 8µs, for either polarity. Further reduction in transient amplitude is possible by reducing R5 and possibly increasing C3, but this should be verified by experiment to minimize excessive ringing with some capacitor types. Load current step changes smaller than 10mA will of course show less transient error.

The circuit can be used either as shown as a 5 to 3.3V reference/regulator, or it can also be used with ON/OFF control. By driving pin 3 of U1 with a logic control signal as noted, the output is switched ON/OFF. Note that when ON/OFF control is used, resistor R4 must be used with U1, to speed ON-OFF switching.

As noted, the “low dropout” style of regulator is readily implemented with a rail-rail output op amps such as those of Figure 9.41, as their wide output swing allows easy drive to a low saturation voltage pass device. Further, it is most useful when the op amp has a rail-rail input feature, as this allows high-side current sensing, for positive rail current limiting. Typical applications are voltages developed from a 3-9V range system sources, or anywhere where low dropout performance is required for power efficiency. The 4.5V case here works from 5V nominal sources, with worst-case levels down to 4.6V or less.

Figure 9.46 shows such a regulator using an OP284 plus a low $R_{ds(on)}$ P-channel MOSFET pass device. Low dropout performance is provided by Q1, with a rating of 0.11ohm with a gate drive of 2.7V. This relatively low gate drive allows operation on supplies as low as 3V without compromise to overall performance.

300mA LOW DROPOUT REGULATOR
WITH HIGH-SIDE CURRENT SENSING

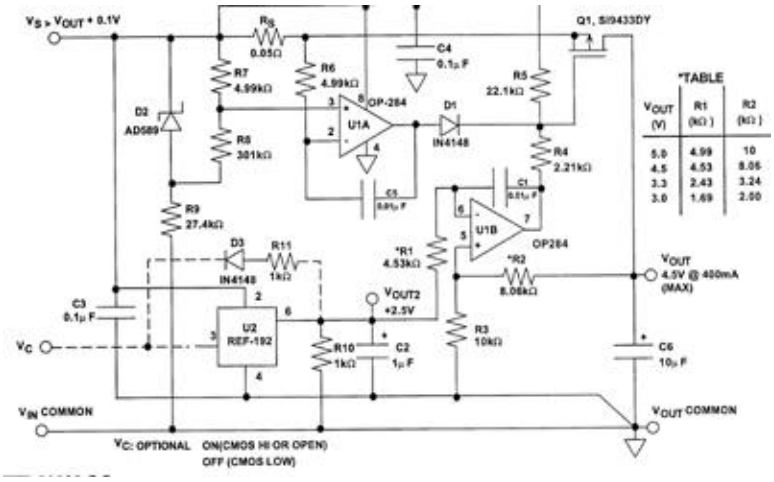


Figure 9.46

The circuit's main voltage control loop operation is provided by U1B, half of the OP284. This voltage control amplifier amplifies the 2.5V reference voltage produced by U2, a REF192. The regulated output voltage V_{OUT} is then of the same form as noted in the previous circuit.

Note that for the lowest V_{OUT} DC error, R2||R3 should be maintained equal to R1 (as here), and the R2-R3 resistors should be stable, close tolerance metal film types. The table suggests R1-R3 values for popular output voltages. In general, V_{OUT} can be anywhere between V_{OUT2} and the 12V maximum rating of Q1.

While the low voltage saturation characteristic of Q1 is part of the low dropout key, the other advantage is a low and accurate current-sense comparison. Here, this is provided by current sense amplifier U1A, which is provided a 20mV reference from the 1.235V AD589 reference diode D2 and the R7-R8 divider. When the product of the output current and Rs match this threshold, current control is activated, and U1A drives Q1's gate via D1. Overall circuit operation is then under current mode control, with a current limit I_{limit} defined as:

$$I_{limit} = \frac{V_{R(D2)}}{Rs} \left[\frac{R7}{R7 + R8} \right]$$

Obviously the comparison voltage should be small, since it becomes a significant portion of the overall dropout voltage. Here, the 20mV value used is higher than the typical offset of the OP284, but still reasonably low as a percentage of V_{OUT} (<0.5%). For other I_{limit} levels, sense resistor Rs should be set along with R7-R8, to maintain this threshold voltage between 20 and 50mV.

For a 4.5V output version, measured DC output change for a 225mA load change was on the order of a few µV, while the dropout voltage at this same current level

was about 30mV. The current limit as shown is 400mA, allowing operation at levels up to 300mA or more. While the Q1 device can support currents of several amperes, a practical current rating takes into account the SO-8 device's 2.5W 25°C dissipation. A short-circuit current of 400mA at an input level of 5V will cause a 2W dissipation in Q1, so other input conditions should be considered carefully in terms of Q1's potential overheating. If higher powered devices are used for Q1, the circuit will support outputs of tens of amperes as well as the higher V_{OUT} levels noted above.

The circuit can be used either as shown for a standard low dropout regulator, or it can also be used with ON/OFF control. Note that when the output is OFF in this circuit, it is still active (i.e., not an open circuit). This is because the OFF state simply reduces the voltage input to R1, leaving the U1A/B amplifiers and Q1 still active.

When ON/OFF control is used, resistor R10 should be used with U1, to speed ON-OFF switching, and to allow the output of the circuit to settle to a nominal zero voltage. Components D3 and R11 also aid in speeding up the ON-OFF transition, by providing a dynamic discharge path for C2. OFF-ON transition time is less than 1ms, while the ON-OFF transition is longer, but under 10ms.

REFERENCES: LOW DROPOUT REFERENCES AND REGULATORS

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EMI/RFI CONSIDERATIONS

Adolfo A. Garcia

Electromagnetic interference (EMI) has become a hot topic in the last few years among circuit designers and systems engineers. Although the subject matter and prior art have been in existence for over the last 50 years or so, the advent of portable and high-frequency industrial and consumer electronics has provided a comfortable standard of living for many EMI testing engineers, consultants, and publishers. With the help of EDN Magazine and Kimmel Gerke Associates, this section will highlight general issues of EMC (electrom agnetic compatibility) to familiarize the system/circuit designer with this subject and to illustrate proven techniques for protection against EMI.

A PRIMER ON EMI REGULATIONS

The intent of this section is to summarize the different types of electromagnetic compatibility (EMC) regulations imposed on equipment manufacturers, both voluntary and mandatory. Published EMC regulations apply at this time only to equipment and systems, and not to components. Thus, EMI *hardened* equipment does not necessarily imply that each of the components used (integrated circuits, especially) in the equipment must also be EMI *hardened*.

Commercial Equipment

The two driving forces behind commercial EMI regulations are the FCC (Federal Communications Commission) in the U. S. and the VDE (Verband Deutscher Electrotechniker) in Germany. VDE regulations are more restrictive than the FCC's with regard to emissions and radiation, but the European Community will be adding immunity to RF, electrostatic discharge, and power-line disturbances to the VDE regulations, and will require mandatory compliance in 1996. In Japan, commercial EMC regulations are covered under the VCCI (Voluntary Control Council for Interference) standards and, implied by the name, are much looser than their FCC and VDE counterparts.

All commercial EMI regulations primarily focus on *radiated* emissions, specifically to protect nearby radio and television receivers, although both FCC and VDE standards are less stringent with respect to *conducted* interference (by a factor of 10 over radiated levels). The FCC Part 15 and VDE 0871 regulations group commercial equipment into two classes: Class A, for all products intended for business environments; and Class B, for all products used in residential applications. For example, Table 9.1 illustrates the electric-field emission limits of commercial computer equipment for both FCC Part 15 and VDE 0871 compliance.

Radiated Emission Limits for Commercial Computer Equipment

Frequency (MHz)	Class A (at 3 m)	Class B (at 3 m)
30 - 88	300 µV/m	100 µV/m
88 - 216	500 µV/m	150 µV/m
216 - 1000	700 µV/m	200 µV/m

Table 9.1

In addition to the already stringent VDE emission limits, the European Community EMC standards (IEC and IEEE) will require mandatory compliance in 1996 to these additional EMI threats: Immunity to RF fields, electrostatic discharge, and power-line disturbances. All equipment/systems marketed in Europe must exhibit an immunity to RF field strengths of 1-10V/m (IEC standard 801-3), electrostatic discharge (generated by human contact or through material movement) in the range of 10-15kV (IEC standard 801-2), and power-line disturbances of 4kV EFTs (extremely fast transients, IEC standard 801-4) and 6kV lightning surges (IEEE standard C62.41).

Military Equipment

The defining EMC specification for military equipment is MIL-STD-461 which applies to radiated equipment emissions and equipment susceptibility to interference. Radiated emission limits are very typically 10 to 100 times more stringent than the levels shown in Table 9.1. Required limits on immunity to RF fields are typically 200 times more stringent (RF field strengths of 5-50mV/m) than the limits for commercial equipment.

Medical Equipment

Although not yet mandatory, EMC regulations for medical equipment are presently being defined by the FDA (Food and Drug Administration) in the USA and the European Community. The primary focus of these EMC regulations will be on immunity to RF fields, electrostatic discharge, and power-line disturbances, and may very well be more stringent than the limits spelled out in MIL-STD-461. The primary objective of the medical EMC regulations is to guarantee safety to humans.

Industrial- and Process-Control Equipment

Presently, equipment designed and marketed for industrial- and process-control applications are not required to meet pre-existing mandatory EMC regulations. In fact, manufacturers are exempt from complying to any standard in the USA. However, since industrial environments are very much electrically *hostile,* all

equipment manufacturers will be required to comply with all European Community EMC regulations by 1996.

Automotive Equipment

Perhaps the most difficult and hostile environment in which electrical circuits and systems must operate is that found in the automobile. All of the key EMI threats to electrical systems exist here. In addition, operating temperature extremes, moisture, dirt, and toxic chemicals further exacerbate the problem. To complicate matters further, standard techniques (ferrite beads, feed-through capacitors, inductors, resistors, shielded cables, wires, and connectors) used in other systems are not generally used in automotive applications because of the cost of the additional components.

Presently, automotive EMC regulations, defined by the very comprehensive SAE Standards J551 and J1113, are not yet mandatory. They are, however, very rigorous. SAE standard J551 applies to vehicle-level EMC specifications, and standard J1113 (functionally similar to MIL-STD-461) applies to all automotive electronic modules. For example, the J1113 specification requires that electronic modules cannot radiate electric fields greater than 300nV/m at a distance of 3 meters. This is roughly 1000 times more stringent than the FCC Part 15 Class A specification. In many applications, automotive manufacturers are imposing J1113 RF field immunity limits on *each of the active components* used in these modules. Thus, in the very near future, automotive manufacturers will require that IC products comply with existing EMC standards and regulations.

EMC Regulations' Impact on Design

In all these applications and many more, complying with mandatory EMC regulations will require careful design of individual circuits, modules, and systems using established techniques for cable shielding, signal and power-line filtering against both small- and large-scale disturbances, and sound multi-layer PCB layouts. The key to success is to incorporate sound EMC principles early in the design phase to avoid time-consuming and expensive redesign efforts.

PASSIVE COMPONENTS: YOUR ARSENAL AGAINST EMI

Minimizing the effects of EMI requires that the circuit/system designer be completely aware of the primary arsenal in the battle against interference: *passive components*. To successfully use these components, the designer must understand their non-ideal behavior. For example, Figure 9.47 illustrates the *real* behavior of the passive components used in circuit design. At very high frequencies, wires become transmission lines, capacitors become inductors, inductors become capacitors, and resistors behave as resonant circuits.

ALL PASSIVE COMPONENTS EXHIBIT "NON IDEAL" BEHAVIOR

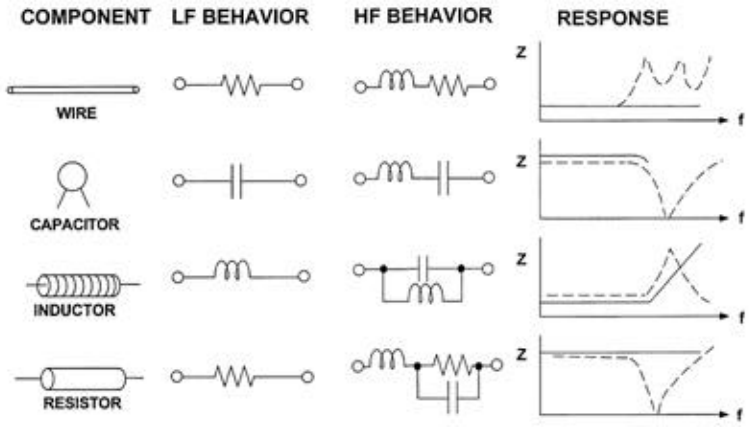

Figure 9.47

A specific case in point is the frequency response of a simple wire compared to that of a ground plane. In many circuits, wires are used as either power or signal returns, and there is no ground plane. A wire will behave as a very low resistance (less than 0.02ohm/ft for 22-gauge wire) at low frequencies, but because of its parasitic inductance of approximately 20nH/ft, it becomes inductive at frequencies above 160kHz. Furthermore, depending on size and routing of the wire and the frequencies involved, it ultimately becomes a transmission line with an uncontrolled impedance. From our knowledge of RF, unterminated transmission lines become antennas with gain, as illustrated in Figure 9.48. On the other hand, large area ground planes are much more well-behaved, and maintain a low impedance over a wide range of frequencies. With a good understanding of the behavior of *real* components, a strategy can now be developed to find solutions to most EMI problems.

IMPEDANCE COMPARISON: WIRE VS. GROUND PLANE

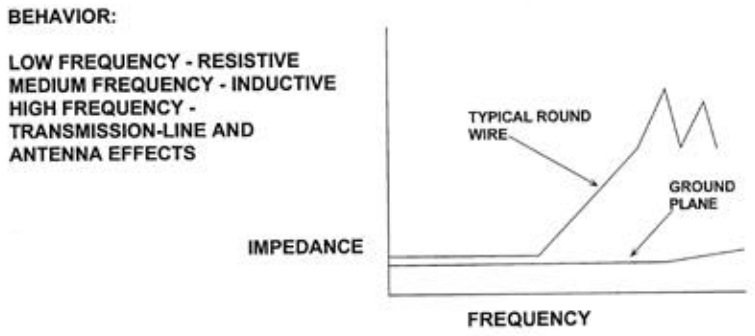

Figure 9.48

With any problem, a strategy should be developed before any effort is expended trying to solve it. This approach is similar to the scientific method: initial circuit misbehavior is noted, theories are postulated, experiments designed to test the theories are conducted, and results are again noted. This process continues until all theories have been tested and expected results achieved and recorded. With respect to EMI, a problem solving framework has been developed. As shown in Figure 9.49, the model suggested by Kimmel-Gerke in [Reference 1] illustrates that all three elements (a *source*, a *receptor* or *victim*, and a *path* between the two) must exist in order to be considered an EMI problem. The sources of electromagnetic interference can take on many forms, and the ever-increasing number of portable instrumentation and personal communications/computation equipment only adds the number of possible sources and receptors.

Interfering signals reach the receptor by *conduction* (the circuit or system interconnections) or *radiation* (parasitic mutual inductance and/or parasitic capacitance). In general, if the frequencies of the interference are less than 30MHz, the primary means by which interference is coupled is through the *interconnects*. Between 30MHz and 300MHz, the primary coupling mechanism is *cable radiation and connector leakage*. At frequencies greater than 300MHz, the primary mechanism is *slot and board radiation*. There are many cases where the interference is broadband, and the coupling mechanisms are combinations of the above.

A DIAGNOSTIC FRAMEWORK FOR EMI

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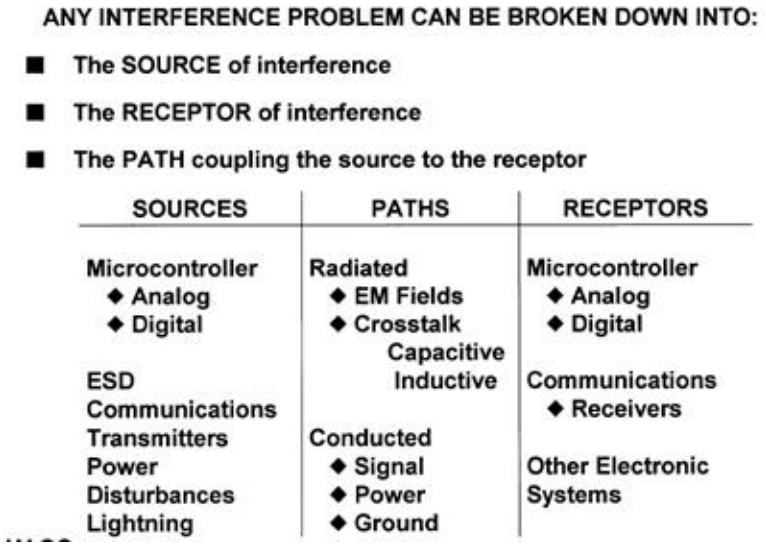


Figure 9.49

When all three elements exist together, a framework for solving any EMI problem can be drawn from Figure 9.50. There are three types of interference with which the circuit or system designer must contend. The first type of interference is that generated by and emitted from an instrument; this is known as circuit/system *emission* and can be either *conducted* or *radiated*. An example of this would be the personal computer. Portable and desktop computers must pass the stringent FCC Part 15 specifications prior to general use.

The second type of interference is circuit or system *immunity*. This describes the behavior of an instrument when it is exposed to large electromagnetic fields, primarily electric fields with an intensity in the range of 1 to 10V/m at a distance of 3 meters. Another term for immunity is *susceptibility*, and it describes circuit/system behavior against radiated or conducted interference.

The third type of interference is *internal*. Although not directly shown on the figure, internal interference can be high-speed digital circuitry within the equipment which affects sensitive analog (or other digital circuitry), or noisy power supplies which can contaminate both analog and digital circuits. Internal interference often occurs between digital and analog circuits, or between motors or relays and digital circuits. In mixed signal environments, the digital portion of the system often interferes with analog circuitry. In some systems, the internal interference reaches such high levels that even very high-speed digital circuitry can affect other low-speed digital circuitry as well as analog circuits.

THREE TYPES OF INTERFERENCE
EMISSIONS - IMMUNITY - INTERNAL

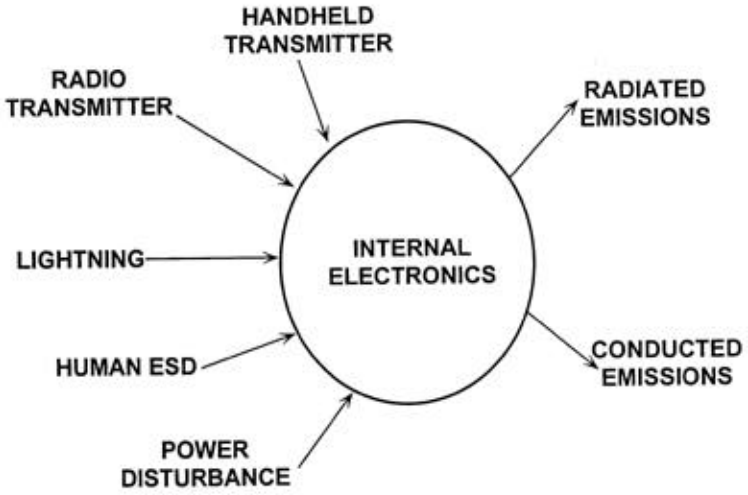


Figure 9.50

In addition to the source-path-receptor model for analyzing EMI-related problems, Kimmel Gerke Associates have also introduced the FAT-ID concept [Reference 1]. FAT-ID is an acronym that describes the five key elements inherent in any EMI problem. These five key parameters are: *frequency, amplitude, time, impedance,* and *distance.*

The *frequency* of the offending signal suggests its path. For example, the path of low-frequency interference is often the circuit conductors. As the interference frequency increases, it will take the path of least impedance, usually stray capacitance. In this case, the coupling mechanism is radiation.

Time and frequency in EMI problems are interchangeable. In fact, the physics of EMI have shows that the time response of signals contains all the necessary information to construct the spectral response of the interference. In digital systems, both the signal rise time and pulse repetition rate produce spectral components according to the following relationship:

$$f_{EMI} = \frac{1}{\pi\ t_{rise}} \qquad \text{Eq. 9.1}$$

For example, a pulse having a 1ns rise time is equivalent to an EMI frequency of over 300MHz. This time-frequency relationship can also be applied to high-speed analog circuits, where slew rates in excess of 1000V/µs and gain-bandwidth products greater than 500MHz are not uncommon.

When this concept is applied to instruments and systems, EMI emissions are again functions of signal rise time and pulse repetition rates. Spectrum analyzers and high

speed oscilloscopes used with voltage and current probes are very useful tools in quantifying the effects of EMI on circuits and systems.

Another important parameter in the analysis of EMI problems is the physical dimensions of cables, wires, and enclosures. Cables can behave as either passive antennas (receptors) or very efficient transmitters (sources) of interference. Their physical length and their shield must be carefully examined where EMI is a concern. As previously mentioned, the behavior of simple conductors is a function of length, cross-sectional area, and frequency. Openings in equipment enclosures can behave as slot antennas, thereby allowing EMI energy to affect the internal electronics.

Radio Frequency Interference

The world is rich in radio transmitters: radio and TV stations, mobile radios, computers, electric motors, garage door openers, electric jackhammers, and countless others. All this electrical activity can affect circuit/system performance and, in extreme cases, may render it inoperable. Regardless of the location and magnitude of the interference, circuits/systems must have a minimum level of immunity to radio frequency interference (RFI). The next section will cover two general means by which RFI can disrupt normal instrument operation: the direct effects of RFI sensitive analog circuits, and the effects of RFI on shielded cables.

Two terms are typically used in describing the sensitivity of an electronic system to RF fields. In communications, radio engineers define *immunity* to be an instrument's *susceptibility to the applied RFI power density at the unit*. In more general EMI analysis, the *electric-field intensity* is used to describe RFI stimulus. For comparative purposes, Equation 9.2 can be used to convert electric-field intensity to power density and vice-versa:

$$\vec{E}\left(\frac{V}{m}\right) = 61.4\sqrt{P_T\left(\frac{mW}{cm^2}\right)} \quad \text{Eq. 9.2}$$

where E = Electric Field Strength, in volts per meter, and
P_T = Transmitted power, in milliwatts per cm^2.

From the standpoint of the source-path-receptor model, the *strength of the electric field*, E, surrounding the receptor is a function of *transmitted power*, *antenna gain*, and *distance* from the source of the disturbance. An approximation for the electric-field intensity (for both near- and far-field sources) in these terms is given by Equation 9.3:

$$\vec{E}\left(\frac{V}{m}\right) = 5.5\left(\frac{\sqrt{P_T \; G_A}}{d}\right) \quad \text{Eq. 9.3}$$

where E = Electric field intensity, in V/m;
P_T = Transmitted power, in mW/cm^2;
G_A = Antenna gain (numerical); and
d = distance from source, in meters

For example, a 1W hand-held radio at a distance of 1 meter can generate an electric-field of 5.5V/m, whereas a 10kW radio transmission station located 1km away generates a field smaller than 0.6V/m.

Analog circuits are generally more sensitive to RF fields than digital circuits because analog circuits, operating at high gains, must be able to resolve signals in the microvolt/millivolt region. Digital circuits, on the other hand, are more immune to RF fields because of their larger signal swings and noise margins. As shown in Figure 9.51, RF fields can use inductive and/or capacitive coupling paths to generate noise currents and voltages which are amplified by high-impedance analog instrumentation. In many cases, out-of-band noise signals are detected and rectified by these circuits. The result of the RFI rectification is usually unexplained offset voltage shifts in the circuit or in the system.

RFI CAN CAUSE RECTIFICATION IN SENSITIVE ANALOG CIRCUITS

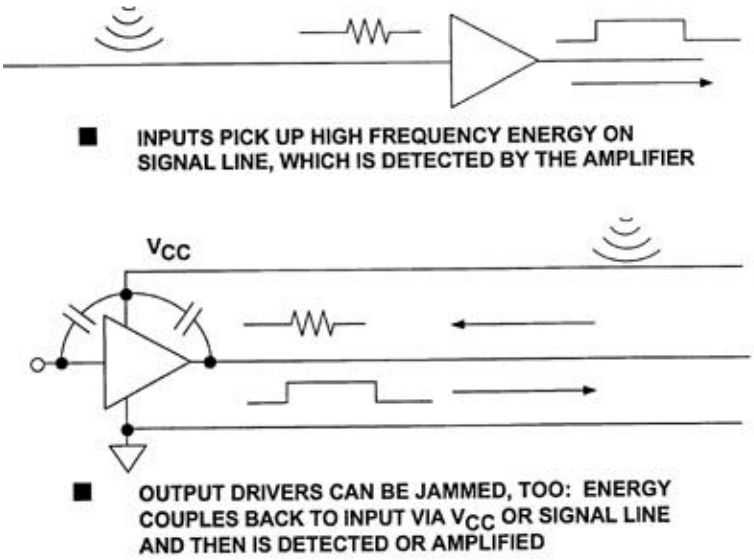


Figure 9.51

There are techniques that can be used to protect analog circuits against interference from RF fields (see Figure 9.52). The three general points of RFI coupling are *signal inputs*, *signal outputs*, and *power supplies*. At a minimum, all power supply pin connections on analog and digital ICs should be decoupled with 0.1µF ceramic capacitors. As was shown in Reference 3, low-pass filters, whose cutoff frequencies are set no higher than 10 to 100 times the signal bandwidth, can be used at the inputs and the outputs of signal conditioning circuitry to filter noise.

KEEPING RFI AWAY FROM ANALOG CIRCUITS

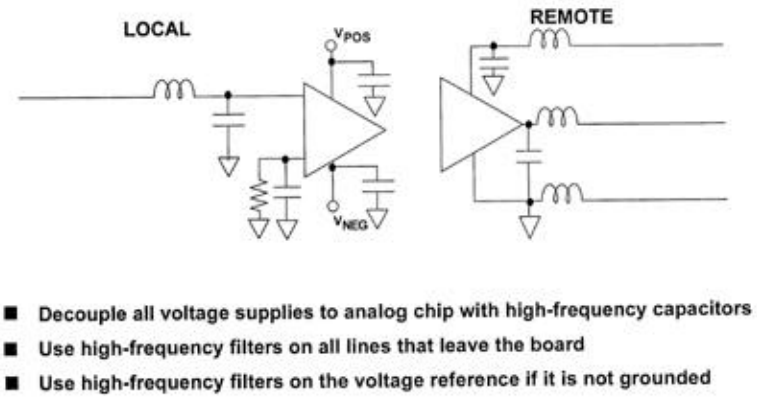


Figure 9.52

Care must be taken to ensure that the low pass filters (LPFs) are effective at the highest RF interference frequency expected. As illustrated in Figure 9.53, real low-pass filters may exhibit *leakage* at high frequencies. Their inductors can lose their effectiveness due to parasitic capacitance, and capacitors can lose their effectiveness due to parasitic inductance. A rule of thumb is that a conventional low-pass filter (made up of a single capacitor and inductor) can begin to *leak* when the applied signal frequency is 100 to 1000 higher than the filter's cutoff frequency. For example, a 10kHz LPF would not be considered very efficient at filtering frequencies above 1MHz.

A SINGLE LOW PASS FILTER LOSES EFFECTIVENESS AT 100 - 1000 f_{3dB}

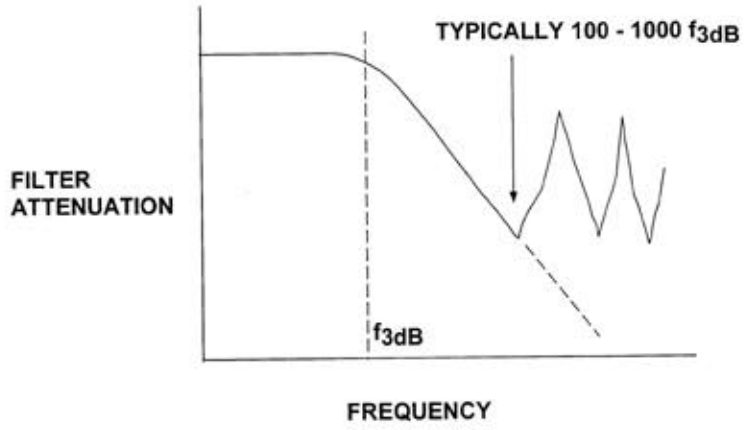


Figure 9.53

Rather than use one LPF stage, it is recommended that the interference frequency bands be separated into *low-band*, *mid-band*, and *high-band*, and then use individual filters for each band. Kimmel Gerke Associates use the stereo speaker analogy of *woofer-midrange-tweeter* for RFI low-pass filter design illustrated in Figure 9.54. In this approach, low frequencies are grouped from 10kHz to 1MHz, mid-band frequencies are grouped from 1MHz to 100MHz, and high frequencies grouped from 100MHz to 1GHz. In the case of a shielded cable input/output, the high frequency section should be located close to the shield to prevent high-frequency leakage at the shield boundary. This is commonly referred to as *feed-through* protection. For applications where shields are not required at the inputs/outputs, then the preferred method is to locate the high frequency filter section as close the analog circuit as possible. This is to prevent the possibility of pickup from other parts of the circuit.

MULTISTAGE FILTERS ARE MORE EFFECTIVE

STEREO SPEAKER ANALOGY

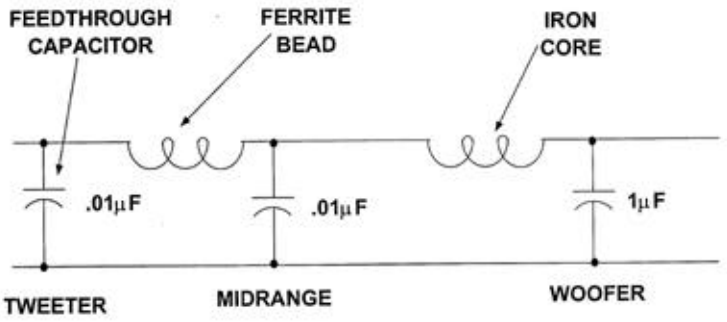


Figure 9.54

Another cause of filter failure is illustrated in Figure 9.55. If there is any impedance in the ground connection (for example, a long wire or narrow trace connected to the ground plane), then the high-frequency noise uses this impedance path to bypass the filter completely. Filter grounds must be broadband and tied to low-impedance points or planes for optimum performance. High frequency capacitor leads should be kept as short as possible, and low-inductance surface-mounted ceramic chip capacitors are preferable.

NON-ZERO (INDUCTIVE AND/OR RESISTIVE) FILTER GROUND REDUCES EFFECTIVENESS

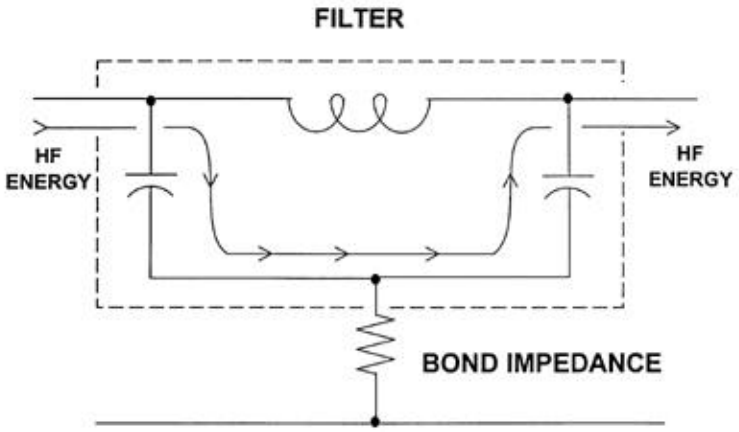
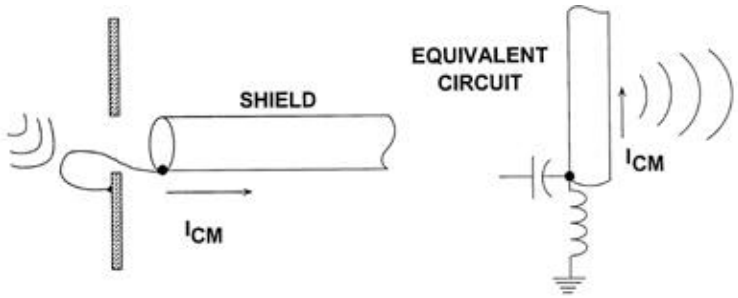


Figure 9.55

In the first part of this discussion on RF immunity, circuit level techniques were discussed. In this next section, the second strategic concept for RF immunity will be discussed: *all cables behave as antennas*. As shown in Figure 9.56, pigtail terminations on cables very often cause systems to fail radiated emissions tests because high-frequency noise has coupled into the cable shield, generally through

stray capacitance. If the length of the cable is considered *electrically long* (a concept to be explained later) at the interference frequency, then it can behave as a very efficient quarter-wave antenna. The cable pigtail forms a matching network, as shown in the figure, to radiate the noise which coupled into the shield. In general, pigtails are only recommended for applications below 10kHz, such as 50/60Hz interference protection. For applications where the interference is greater than 10kHz, shielded connectors, electrically and physically connected to the chassis, should be used. In applications where shielding is not used, filters on input/output signal and power lines work well. Small ferrites and capacitors should be used to filter high frequencies, provided that: (1) the capacitors have short leads and are tied directly to the chassis ground, and (2) the filters are physically located close to the connectors to prevent noise pickup.

"SHIELDED" CABLE CAN CARRY HIGH FREQUENCY CURRENT AND BEHAVES AS AN ANTENNA



I_{CM} = COMMON-MODECURRENT
Figure 9.56

The key issues and techniques described in this section on solving RFI related problems are summarized in Figure 9.57. Some of the issues were not discussed in detail, but are equally important. For a complete treatment of this issue, the interested reader should consult References 1 and 2. The main thrust of this section was to provide the reader with a problem-solving strategy against RFI and to illustrate solutions to commonly encountered RFI problems.

SUMMARY OF RADIO FREQUENCY INTERFERENCE AND PROTECTION TECHNIQUES

- **Radio-Frequency Interference is a Serious Threat**
  - **Equipment causes interference to nearby radio and televison**
  - **Equipment upset by nearby transmitters**
- **RF-Failure Modes**
  - **Digital circuits prime source of emissions**
  - **Analog circuits more vulnerable to RF than digital circuits**
- **Two Strategic Concepts**
  - **Treat all cables as antennas**
  - **Determine the most critical circuits**
- **RF Circuit Protection**
  - **Filters and multilayer boards**
  - **Multistage filters often needed**
- **RF Shielding**
  - **Slots and seams cause the most problems**
- **RF Cable Protection**
  - **High-quality shields and connectors needed for RF protection**

Figure 9.57

Solutions for Power-Line Disturbances

The goal of this next section is not to describe in detail all the circuit/system failure mechanisms which can result from power-line disturbances or faults. Nor is it the intent of this section to describe methods by which power-line disturbances can be prevented. Instead, this section will describe techniques that allow circuits and systems to accommodate *transient* power-line disturbances.

Figure 9.58 is an example of a hybrid power transient protection network commonly used in many applications where lightning transients or other power-line disturbances are prevalent. These networks can be designed to provide protection against transients as high as 10kV and as fast as 10ns. Gas discharge tubes (crowbars) and large geometry zener diodes (clamps) are used to provide both differential and common-mode protection. Metal-oxide varistors (MOVs) can be substituted for the zener diodes in less critical, or in more compact designs. Chokes are used to limit the surge current until the gas discharge tubes fire.

POWER LINE DISTURBANCES CAN GENERATE EMI

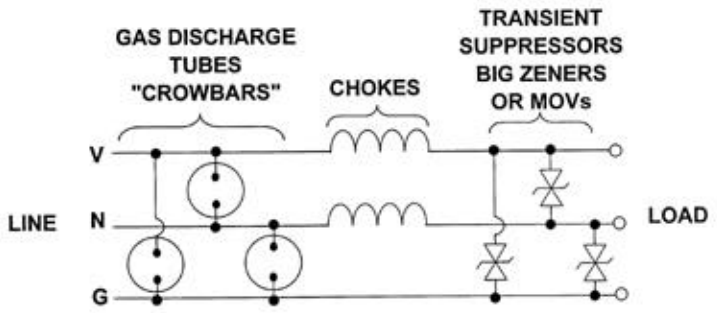


Figure 9.58

Commercial EMI filters, as illustrated in Figure 9.59, can be used to filter less catastrophic transients or high-frequency interference. These EMI filters provide both common-mode and differential mode filtering as in Figure 9.58. An optional choke in the safety ground can provide additional protection against common-mode noise. The value of this choke cannot be too large, however, because its resistance may affect power-line fault clearing.

SCHEMATIC FOR A COMMERCIAL POWER LINE FILTER

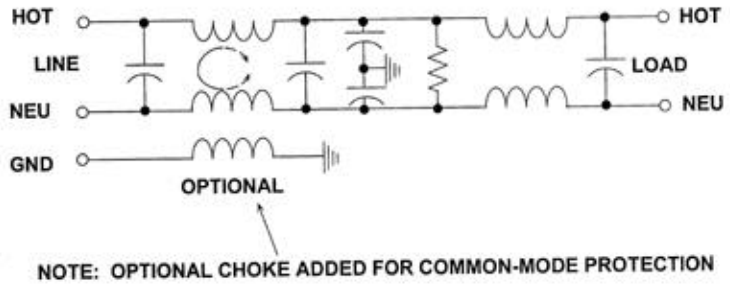


Figure 9.59

Transformers provide the best common-mode power line isolation. They provide good protection at low frequencies (<1MHz), or for transients with rise and fall times greater than 300ns. Most motor noise and lightning transients are in this range, so isolation transformers work well for these types of disturbances. Although the isolation between input and output is galvanic, isolation transformers do not provide sufficient protection against extremely fast transients (<10ns) or those caused by high-amplitude electrostatic discharge (1 to 3ns). As illustrated in Figure 9.60, isolation transformers can be designed for various levels of differential- or common-mode protection. For differential-mode noise rejection, the Faraday shield is connected to the neutral, and for common-mode noise rejection, the shield is connected to the safety ground.

FARADAY SHIELDS IN ISOLATION TRANSFORMERS PROVIDE INCREASING LEVELS OF PROTECTION

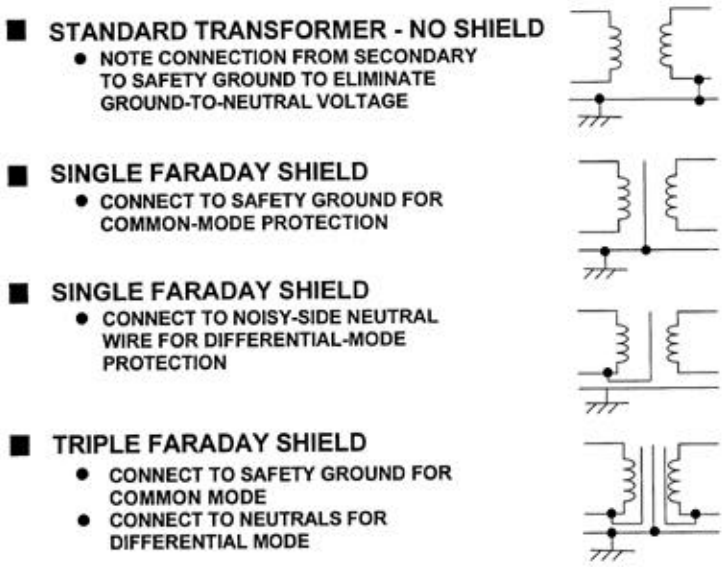


Figure 9.60

Printed Circuit Board Design for EMI Protection

This section will summarize general points regarding the most critical portion of the design phase: the printed circuit board layout. It is at this stage where the performance of the system is most often compromised. This is not only true for signal-path performance, but also for the system's susceptibility to electromagnetic interference and the amount of electromagnetic energy radiated by the system. Failure to implement sound PCB layout techniques will very likely lead to system/instrument EMC failures.

Figure 9.61 is a real-world printed circuit board layout which shows all the paths through which high-frequency noise can couple/radiate into/out of the circuit. Although the diagram shows digital circuitry, the same points are applicable to precision analog, high-speed analog, or mixed analog/digital circuits. Identifying critical circuits and paths helps in designing the PCB layout for both low emissions and susceptibility to radiated and conducted external and internal noise sources.

A key point in minimizing noise problems in a design is to *choose devices no faster than actually required by the application*. Many designers assume that faster is better: fast logic is better than slow, high bandwidth amplifiers are clearly better than low bandwidth ones, and fast DACs and ADCs are better, even if the speed is not required by the system. Unfortunately, faster is not better, but worse where EMI is concerned.

METHODS BY WHICH HIGH FREQUENCY ENERGY COUPLES AND RADIATES INTO CIRCUITRY VIA PLACEMENT

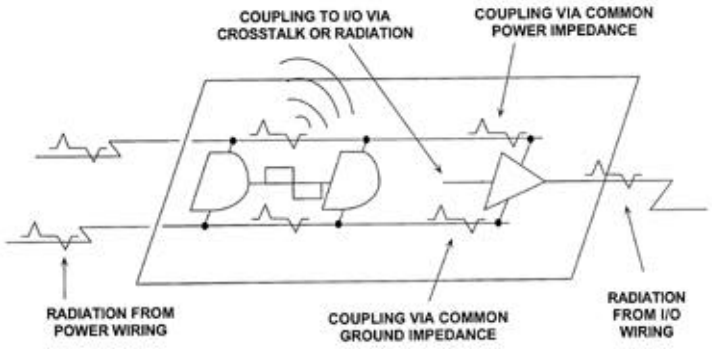


Figure 9.61

Many fast DACs and ADCs have digital inputs and outputs with rise and fall times in the nanosecond region. Because of their wide bandwidth, the sampling clock and the digital inputs and can respond to any form of high frequency noise, even glitches as narrow as 1 to 3ns. These high speed data converters and amplifiers are easy prey for the high frequency noise of microprocessors, digital signal processors, motors, switching regulators, hand-held radios, electric jackhammers, etc. With some of these high-speed devices, a small amount of input/output filtering may be required to desensitize the circuit from its EMI/RFI environment. Adding a small ferrite bead just before the decoupling capacitor as shown in Figure 9.62 is very effective in filtering high frequency noise on the supply lines. For those circuits that require bipolar supplies, this technique should be applied to both positive and negative supply lines.

To help reduce the emissions generated by extremely fast moving digital signals at DAC inputs or ADC outputs, a small resistor or ferrite bead may be required at each digital input/output.

POWER SUPPLY FILTERING AND SIGNAL LINE SNUBBING GREATLY REDUCES EMI EMISSIONS

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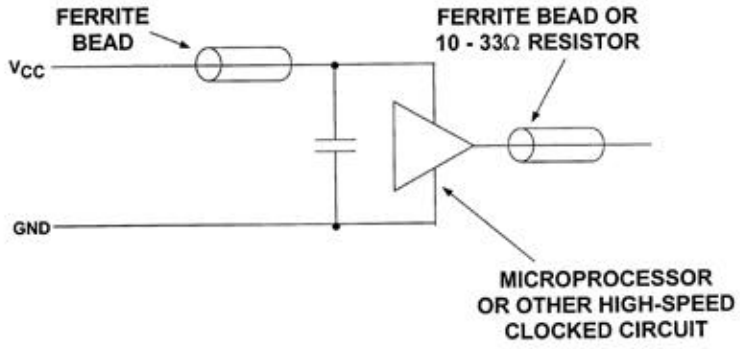

Figure 9.62

Once the system's critical paths and circuits have been identified, the next step in implementing sound PCB layout is to partition the printed circuit board according to circuit function. This involves the appropriate use of power, ground, and signal planes. Good PCB layouts also isolate critical analog paths from sources of high interference (I/O lines and connectors, for example). High frequency circuits (analog and digital) should be separated from low frequency ones. Furthermore, automatic signal routing CAD layout software should be used with extreme caution, and critical paths routed by hand.

Properly designed multilayer printed circuit boards can reduce EMI emissions and increase immunity to RF fields by a factor of 10 or more compared to double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted with signal crossovers, etc.

The preferred multi-layer board arrangement is to embed the signal traces between the power and ground planes, as shown in Figure 9.63. These low-impedance planes form very high-frequency *stripline* transmission lines with the signal traces. The return current path for a high frequency signal on a trace is located directly above and below the trace on the ground/power planes. The high frequency signal is thus contained inside the PCB, thereby minimizing emissions. The embedded signal trace approach has an obvious disadvantage: debugging circuit traces that are hidden from plain view is difficult.

“TO EMBED OR NOT TO EMBED”
THAT IS THE QUESTION

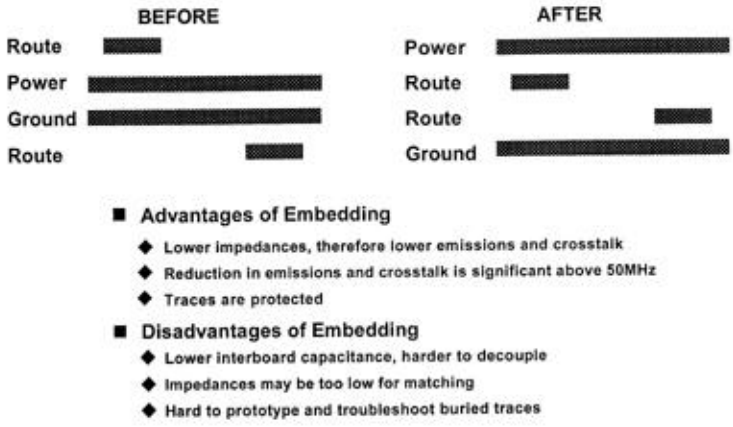

Figure 9.63

Much has been written about terminating printed circuit board traces in their characteristic impedance to avoid reflections. A good rule-of-thumb to determine when this is necessary is as follows: *Terminate the line in its characteristic impedance when the one-way propagation delay of the PCB track is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster).* A conservative approach is to use a 2 inch (PCB track length)/nanosecond (rise-, fall-time) criterion. For example, PCB tracks for high-speed logic with rise/fall time of 5ns should be terminated in their characteristic impedance and if the track length is equal to or greater than 10 inches (including any meanders). The 2 inch/nanosecond track length criterion is summarized in Figure 9.64 for a number of logic families.

LINE TERMINATION SHOULD BE USED WHEN LENGTH OF PCB TRACK EXCEEDS 2 inches / ns

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DIGITAL IC FAMILY	t_r, t_f (ns)	PCB TRACK LENGTH (inches)	PCB TRACK LENGTH (cm)
GaAs	0.1	0.2	0.5
ECL	0.75	1.5	3.8
Schottky	3	6	15
FAST	3	6	15
AS	3	6	15
AC	4	8	20
ALS	6	12	30
LS	8	16	40
TTL	10	20	50
HC	18	36	90

t_r = rise time of signal in ns
t_f = fall time of signal in ns

■ For analog signals @ f_{max}, calculate $t_r = t_f = 0.35 / f_{max}$

Figure 9.64

This same 2 inch/nanosecond rule of thumb should be used with analog circuits in determining the need for transmission line techniques. For instance, if an amplifier must output a maximum frequency of f_{max}, then the equivalent risetime, t_r, can be calculated using the equation $t_r = 0.35/f_{max}$. The maximum PCB track length is then calculated by multiplying the risetime by 2 inch/nanosecond. For example, a maximum output frequency of 100MHz corresponds to a risetime of 3.5ns, and a track carrying this signal greater than 7 inches should be treated as a transmission line.

Equation 9.4 can be used to determine the characteristic impedance of a PCB track separated from a power/ground plane by the board's dielectric (microstrip transmission line):

$$Z_O(\Omega) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98d}{0.89w + t}\right] \quad \text{Eq. 9.4}$$

where e_r = dielectric constant of printed circuit board material;
d = thickness of the board between metal layers, in mils;
w = width of metal trace, in mils; and
t = thickness of metal trace, in mils.

The one-way transit time for a single metal trace over a power/ground plane can be determined from Eq. 9.5:

$$t_{pd}(ns/ft) = 1.017\sqrt{0.475\varepsilon_r + 0.67} \quad \text{Eq. 9.5}$$

For example, a standard 4-layer PCB board might use 8-mil wide, 1 ounce (1.4 mils) copper traces separated by 0.021" FR-4 (e_r=4.7) dielectric material. The characteristic impedance and one-way transit time of such a signal trace would be

88ohms and 1.7ns/ft (7"/ns), respectively. Transmission lines can be effectively terminated in several ways depending on the application, as described in Section 2 of this book.

Figure 9.65 is a summary of techniques that should be applied to printed circuit board layouts to minimize the effects of electromagnetic interference, both emissions and immunity.

CIRCUIT BOARD DESIGN AND EMI

"ALL EMI PROBLEMS BEGIN AND END AT A CURCUIT"

- **Identify critical, sensitive circuits**
- **Where appropriate, choose ICs no faster than needed**
- **Consider and implement sound PCB design**
- **Spend time on the initial layout (by hand, if necessary)**
- **Power supply decoupling (digital and analog circuits)**
- **High-speed digital and high-accuracy analog don't mix**
- **Beware of connectors for input / output circuits**
- **Test, evaluate, and correct early and often**

Figure 9.65

A REVIEW OF SHIELDING CONCEPTS

The concepts of shielding effectiveness presented next are background material. Interested readers should consult References 1,3, and 4 cited at the end of the section for more detailed information.

Applying the concepts of shielding requires an understanding of the source of the interference, the environment surrounding the source, and the distance between the source and point of observation (the receptor or victim). If the circuit is operating close to the source (in the near-, or induction-field), then the field characteristics are determined by the source. If the circuit is remotely located (in the far-, or radiation-field), then the field characteristics are determined by the transmission medium.

A circuit operates in a near-field if its distance from the source of the interference is less than the wavelength (lambda) of the interference divided by 2pi, or lambda/2pi. If the distance between the circuit and the source of the interference is larger than this quantity, then the circuit operates in the far field. For instance, the interference caused by a 1ns pulse edge has an upper bandwidth of approximately 350MHz. The wavelength of a 350MHz signal is approximately 32 inches (the speed of light is approximately 12"/ns). Dividing the wavelength by 2pi yields a distance of

approximately 5 inches, the boundary between near- and far-field. If a circuit is within 5 inches of a 350MHz interference source, then the circuit operates in the near-field of the interference. If the distance is greater than 5 inches, the circuit operates in the far-field of the interference.

Regardless of the type of interference, there is a characteristic impedance associated with it. The characteristic, or wave impedance of a field is determined by the ratio of its electric (or E-) field to its magnetic (or H-) field. In the far field, the ratio of the electric field to the magnetic field is the characteristic (wave impedance) of free space, given by Z_O = 377ohms. In the near field, the wave-impedance is determined by the nature of the interference and its distance from the source. If the interference source is high-current and low-voltage (for example, a loop antenna or a power-line transformer), the field is predominately magnetic and exhibits a wave impedance which is less than 377ohms. If the source is low-current and high-voltage (for example, a rod antenna or a high-speed digital switching circuit), then the field is predominately electric and exhibits a wave impedance which is greater than 377ohms.

Conductive enclosures can be used to shield sensitive circuits from the effects of these external fields. These materials present an impedance mismatch to the incident interference because the impedance of the shield is lower than the wave impedance of the incident field. The effectiveness of the conductive shield depends on two things: First is the loss due to the *reflection* of the incident wave off the shielding material. Second is the loss due to the *absorption* of the transmitted wave *within* the shielding material. Both concepts are illustrated in Figure 9.66. The amount of reflection loss depends upon the type of interference and its wave impedance. The amount of absorption loss, however, is independent of the type of interference. It is the same for near- and far-field radiation, as well as for electric or magnetic fields.

REFLECTION AND ABSORPTION ARE THE TWO PRINCIPAL SHIELDING MECHANISMS

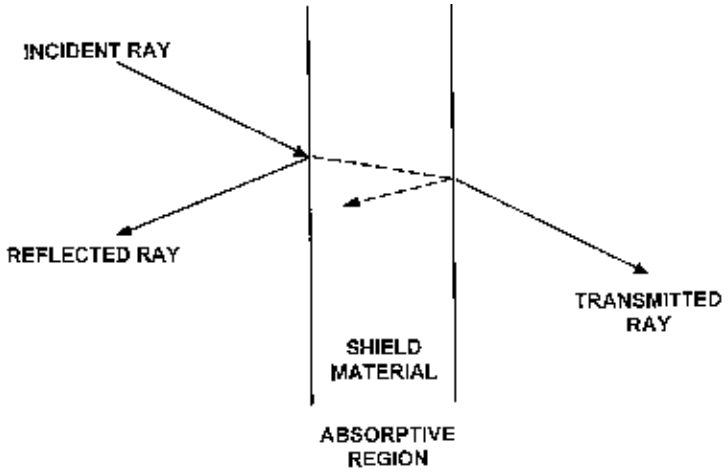


Figure 9.66

Reflection loss at the interface between two media depends on the difference in the characteristic impedances of the two media. For electric fields, reflection loss depends on the frequency of the interference and the shielding material. This loss can be expressed in dB, and is given by:

$$R_e(dB) = 322 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f^3 r^2}\right] \quad \text{Eq. 9.6}$$

where sigma r = relative conductivity of the shielding material, in Siemens per meter;
μ [sub] r = relative permeability of the shielding material, in Henries per meter;
f = frequency of the interference, and
r = distance from source of the interference, in meters

For magnetic fields, the loss depends also on the shielding material and the frequency of the interference. Reflection loss for magnetic fields is given by:

$$R_m(dB) = 14.6 + 10\log_{10}\left[\frac{f r^2 \sigma_r}{\mu_r}\right] \quad \text{Eq. 9.7}$$

and, for plane waves (r > lambda/2pi), the reflection loss is given by:

$$R_{pw}(dB) = 168 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f}\right] \quad \text{Eq. 9.8}$$

Absorption is the second loss mechanism in shielding materials. Wave attenuation due to absorption is given by:

$$A(dB) = 3.34\ t\sqrt{\sigma_r \mu_r f} \quad \text{Eq. 9.9}$$

where t = thickness of the shield material, in inches. This expression is valid for plane waves, electric and magnetic fields. Since the intensity of a transmitted field decreases exponentially relative to the thickness of the shielding material, the absorption loss in a shield one skin-depth thick is 9dB. Since absorption loss is proportional to thickness and inversely proportional to skin depth, increasing the thickness of the shielding material improves shielding effectiveness at high frequencies.

Reflection loss for plane waves in the far field decreases with increasing frequency because the shield impedance, Z_S, increases with frequency. Absorption loss, on the other hand, increases with frequency because skin depth decreases. For electric fields and plane waves, the primary shielding mechanism is reflection loss, and at high frequencies, the mechanism is absorption loss. For these types of interference, high conductivity materials, such as copper or aluminum, provide adequate

shielding. At low frequencies, both reflection and absorption loss to magnetic fields is low; thus, it is very difficult to shield circuits from low-frequency magnetic fields. In these applications, high-permeability materials that exhibit low-reluctance provide the best protection. These low-reluctance materials provide a magnetic shunt path that diverts the magnetic field away from the protected circuit. Some characteristics of metallic materials commonly used for shielded enclosures are shown in Table 9.2.

Impedance and Skin Depths for Various Shielding Materials

Material	**Conductivity** σ_r	**Permeability** μ_r	**Shield Impedance** $\lvert Z_s \rvert$	**Skin depth** δ **(inch)**
Cu	1	1	$3.68E\text{-}7\ \sqrt{f}$	$\frac{2.6}{\sqrt{f}}$
Al	1	0.61	$4.71E\text{-}7\ \sqrt{f}$	$\frac{3.3}{\sqrt{f}}$
Steel	0.1	1000	$3.68E\text{-}5\ \sqrt{f}$	$\frac{0.26}{\sqrt{f}}$
μ Metal	0.03	20,000	$3E\text{-}4\ \sqrt{f}$	$\frac{0.11}{\sqrt{f}}$

Table 9.2

where sigma 0 = 5.82 x 10^7 S/m
μo = 4pi x 10^-7 H/m
eo = 8.85 x 10^-12 F/m

A properly shielded enclosure is very effective at preventing external interference from disrupting its contents as well as confining any internally-generated interference. However, in the real world, openings in the shield are often required to accommodate adjustment knobs, switches, connectors, or to provide ventilation (see Figure 9.67). Unfortunately, these openings may compromise shielding effectiveness by providing paths for high-frequency interference to enter the instrument.

ANY OPENING IN AN ENCLOSURE CAN ACT AS AN EMI WAVEGUIDE BY COMPROMISING SHIELDING EFFECTIVENESS

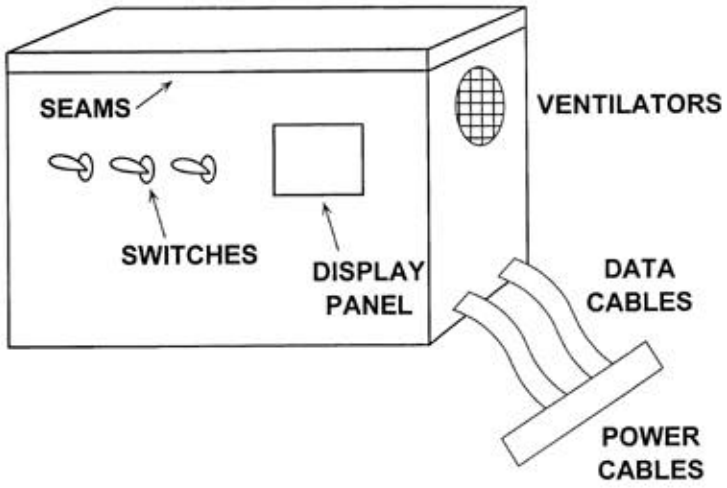


Figure 9.67

The longest dimension (not the total area) of an opening is used to evaluate the ability of external fields to enter the enclosure, because the openings behave as slot antennas. Equation 9.10 can be used to calculate the shielding effectiveness, or the susceptibility to EMI leakage or penetration, of an opening in an enclosure:

$$\text{Shielding Effectiveness}\,(\text{dB}) = 20\log_{10}\left(\frac{\lambda}{2L}\right) \qquad \text{Eq. 9.10}$$

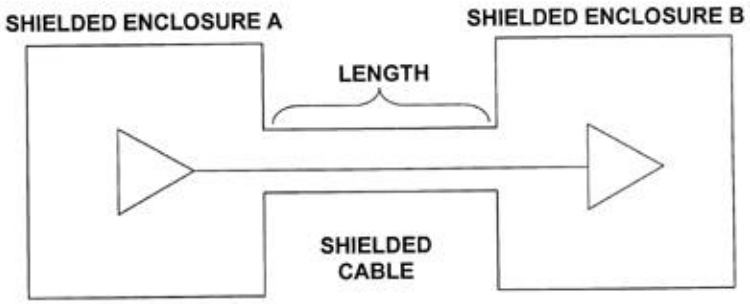
where lambda = wavelength of the interference and
L = maximum dimension of the opening

Maximum radiation of EMI through an opening occurs when the longest dimension of the opening is equal to one half-wavelength of the interference frequency (0dB shielding effectiveness). A rule-of-thumb is to keep the longest dimension less than 1/20 wavelength of the interference signal, as this provides 20dB shielding effectiveness. Furthermore, a few small openings on each side of an enclosure is preferred over many openings on one side. This is because the openings on different sides radiate energy in different directions, and as a result, shielding effectiveness is not compromised. If openings and seams cannot be avoided, then conductive gaskets, screens, and paints alone or in combination should be used judiciously to limit the longest dimension of any opening to less than 1/20 wavelength. Any cables, wires, connectors, indicators, or control shafts penetrating the enclosure should have circumferential metallic shields physically bonded to the enclosure at the point of entry. In those applications where unshielded cables/wires are used, then filters are recommended at the point of shield entry.

General Points on Cables and Shields

Although covered in more detail later, the improper use of cables and their shields is a significant contributor to both radiated and conducted interference. Rather than developing an entire treatise on these issues, the interested reader should consult References 1,2, 4, and 5. As illustrated in Figure 9.68, effective cable and enclosure shielding confines sensitive circuitry and signals within the entire shield without compromising shielding effectiveness.

LENGTH OF SHIELDED CABLES DETERMINES AN "ELECTRICALLY LONG" OR "ELECTRICALLY SHORT" APPLICATION



FULLY SHIELDED ENCLOSURES CONNECTED BY FULLY SHIELDED CABLE KEEP ALL INTERNAL CIRCUITS AND SIGNAL LINES INSIDE THE SHIELD.
● TRANSITION REGION: 1/20 WAVELENGTH

Figure 9.68

Depending on the type of interference (pickup/radiated, low/high frequency), proper cable shielding is implemented differently and is very dependent on the length of the cable. The first step is to determine whether the length of the cable is *electrically short* or *electrically long* at the frequency of concern. A cable is considered *electrically short* if the length of the cable is less than 1/20 wavelength of the highest frequency of the interference, otherwise it is *electrically long*. For example, at 50/60Hz, an *electrically short* cable is any cable length less than 150 miles, where the primary coupling mechanism for these low frequency electric fields is capacitive. As such, for any cable length less than 150 miles, the amplitude of the interference will be the same over the entire length of the cable. To protect circuits against low-frequency electric-field pickup, only one end of the shield should be returned to a low-impedance point. A generalized example of this mechanism is illustrated in Figure 9.69.

CONNECT THE SHIELD AT ONE POINT AT THE LOAD
TO PROTECT AGAINST LOW FREQUENCY (50/60Hz) THREATS

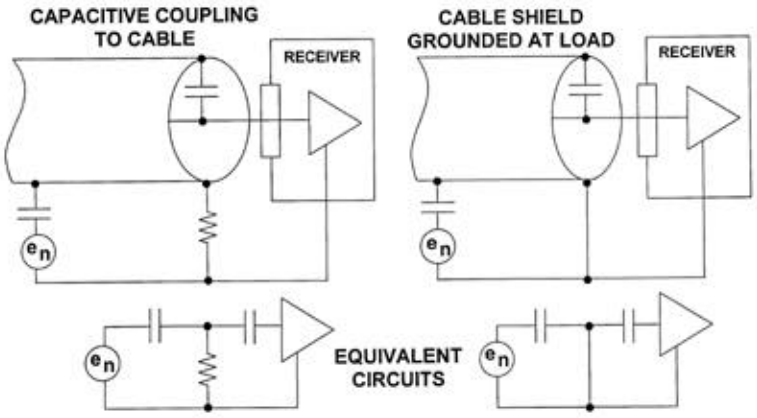


Figure 9.69

In this example, the shield is grounded at the receiver. An exception to this approach (which will be highlighted again later) is the case where line-level (>1Vrms) audio signals are transmitted over long distances using twisted pair, shielded cables. In these applications, the shield again offers protection against low-frequency interference, and an accepted approach is to ground the shield at the driver end (LF and HF ground) and ground it at the receiver with a capacitor (HF ground only).

In those applications where the length of the cable is *electrically long*, or protection against high-frequency interference is required, then the preferred method is to connect the cable shield to low-impedance points at both ends (direct connection at the driving end, and capacitive connection at the receiver). Otherwise, unterminated transmission lines effects can cause reflections and standing waves along the cable. At frequencies of 10MHz and above, circumferential (360°) shield bonds and metal connectors are required to main low-impedance connections to ground.

In summary, for protection against low-frequency (<1MHz), electric-field interference, grounding the shield at one end is acceptable. For high-frequency interference (>1MHz), the preferred method is grounding the shield at both ends, using 360° circumferential bonds between the shield and the connector, and maintaining metal-to-metal continuity between the connectors and the enclosure. Low-frequency ground loops can be eliminated by replacing one of the DC shield connections to ground with a low inductance 0.01µF capacitor. This capacitor prevents low frequency ground loops and shunts high frequency interference to ground.

EMI TROUBLE SHOOTING PHILOSOPHY

System EMI problems often occur after the equipment has been designed and is operating in the field. More often than not, the original designer of the instrument has retired and is living in Tahiti, so the responsibility of repairing it belongs to someone else who may not be familiar with the product. Figure 9.70 summarizes the EMI problem solving techniques discussed in this section and should be useful in these situations.

EMI TROUBLESHOOTING PHILOSOPHY

- **Diagnose before you fix**
- **Ask yourself:**
  - **What are the symptoms?**
  - **What are the causes?**
  - **What are the constraints?**
  - **How will you know you have fixed it?**
- **Use available models for EMI to identify source - path - victim**
- **Start at low frequency and work up to high frequency**
- **EMI doctor's bag of tricks:**
  - **Aluminum foil**
  - **Conductive tape**
  - **Bulk ferrites**
  - **Power line ferrites**
  - **Signal filters**
  - **Resistors, capacitors, inductors, ferrites**
  - **Physical separation**

Figure 9.70

REFERENCES ON EMI/RFI

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2. *Designing for EMC (Workshop Notes)*, Kimmel Gerke Associates, Ltd., 1994.

3. **Systems Application Guide**, Chapter 1, pg. 21-55, Analog Devices, Incorporated, Norwood, MA, 1994.

4. Henry Ott, **Noise Reduction Techniques In Electronic Systems**, **Second Edition**, New York, John Wiley & Sons, 1988.

5. Ralph Morrison, **Grounding And Shielding Techniques In Instrumentation, Third Edition**, New York, John Wiley & Sons, 1986.

6. **Amplifier Applications Guide**, Chapter XI, pg. 61, Analog Devices, Incorporated, Norwood, MA, 1992.

7. B.Slattery and J.Wynne, *Design and Layout of a Video Graphics System for Reduced EMI*, **Analog Devices Application Note AN-333**.

8. Paul Brokaw, *An IC Amplifier User Guide To Decoupling, Grounding, And Making Things Go Right For A Change*, **Analog Devices Application Note**, Order Number E1393-5-590.

9. A. Rich, *Understanding Interference-Type Noise*, **Analog Dialogue**, 16-3, 1982, pp. 16-19.

10. A. Rich, *Shielding and Guarding*, **Analog Dialogue**, 17-1, 1983, pp. 8-13.

11. **EMC Test & Design**, Cardiff Publishing Company, Englewood, CO. An excellent, general purpose trade journal on issues of EMI and EMC.

SENSORS AND CABLE SHIELDING
John McDonald

The environments in which analog systems operate are often rich in sources of EMI. Common EMI noise sources include power lines, logic signals, switching power supplies, radio stations, electric lighting, and motors. Noise from these sources can easily couple into long analog signal paths, such as cables, which act as efficient antennas. Shielded cables protect signal conductors from electric field (E-field) interference by providing low impedance paths to ground at the offending frequencies. Aluminum foil, copper, and braided stainless steel are materials very commonly used for cable shields due to their low impedance properties.

Simply increasing the separation between the noise source and the cable will yield significant additional attenuation due to reduced coupling, but shielding is still required in most applications involving remote sensors.

PRECISION SENSORS AND CABLE SHIELDING

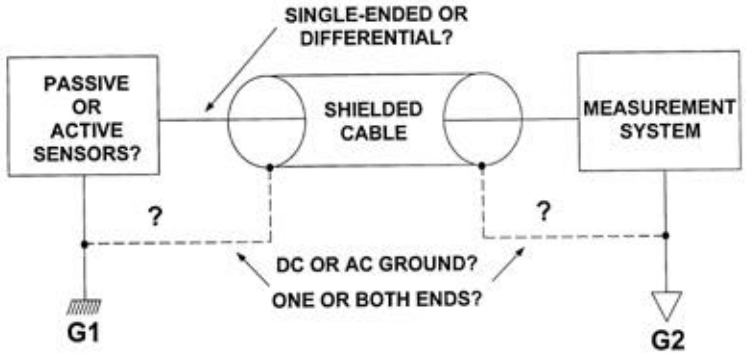

Figure 9.71

WHY SHIELD CABLES?

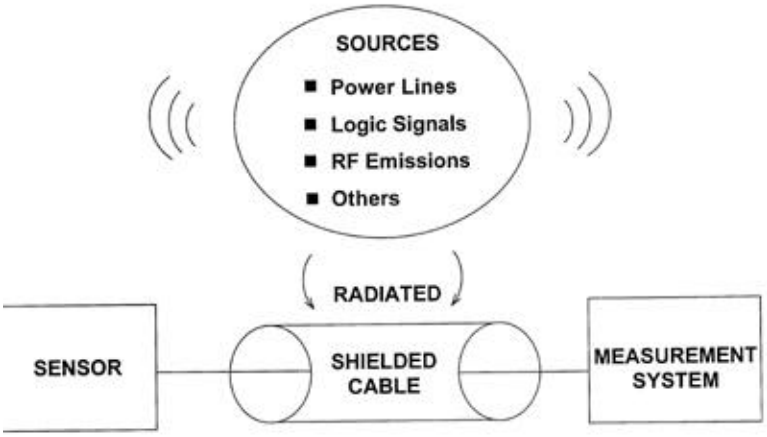

Figure 9.72

There are two paths from an EMI source to a susceptible cable: capacitive (or E-field) and magnetic (or H-field) coupling (see Figure 9.73). Capacitive coupling occurs when parasitic capacitance exists between a noise source and the cable. The amount of parasitic capacitance is determined by the separation, shape, orientation, and the medium between the source and the cable.

Magnetic coupling occurs through parasitic mutual inductance when a magnetic field is coupled from one conductor to another as shown in Figure 9.73. Parasitic mutual inductance depends on the shape and relative orientation of the circuits in question, the magnetic properties of the medium, and is directly proportional to conductor loop area. Minimizing conductor loop area reduces magnetic coupling proportionally.

Shielded *twisted pair* cables offer further noise immunity to magnetic fields. Twisting the conductors together reduces the net loop area, which has the effect of canceling any magnetic field pickup, because the sum of positive and negative incremental loop areas is ideally equal to zero.

HOW DOES INTERFERENCE ENTER THE SYSTEM?

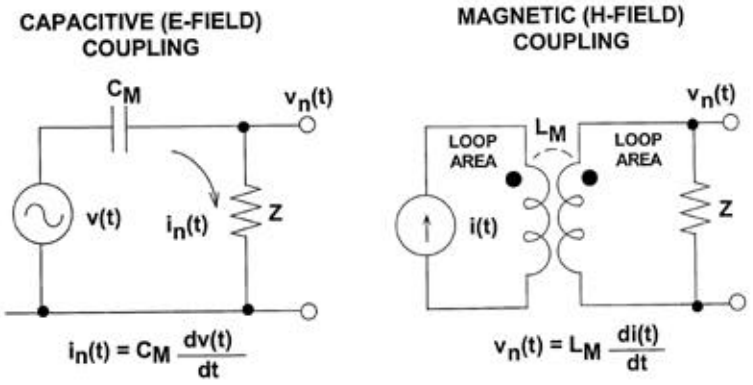

Figure 9.73

To study the shielding problem, a precision *RTD (Resistance Temperature Detector)* amplifier circuit was used as the basis for a series of experiments. A remote 100ohm RTD was connected to the bridge, bridge driver, and the bridge amplifier circuit (Figure 9.74) using 10 feet of a shielded twisted pair cable. The RTD is one element of a 4-element bridge (the three other resistor elements are located in the bridge and bridge driver circuit). The gain of the instrumentation amplifier was adjusted so that the sensitivity at the output was 10mV/°C, with a 5V full scale. Measurements were made at the output of the instrumentation amplifier with the shield grounded in various ways. The experiments were conducted in lab standard environment where a considerable amount of electronic equipment was in operation.

The first experiment was conducted with the shield ungrounded. As shown in Figure 9.74, shields left floating are not useful and offer no attenuation to EMI-induced noise, in fact, they act as antennas. Capacitive coupling is unaffected, because the floating shield provides a coupling path to the signal conductors. Most cables exhibit parasitic capacitances between 10-30pF/ft. Likewise, HF magnetically coupled noise is not attenuated because the floating cable shield does not alter either the geometry or the magnetic properties of the cable conductors. LF magnetic noise is not attenuated significantly, because most shield materials absorb very little magnetic energy.

UNGROUNDED SHIELDED CABLES ACT AS ANTENNAS

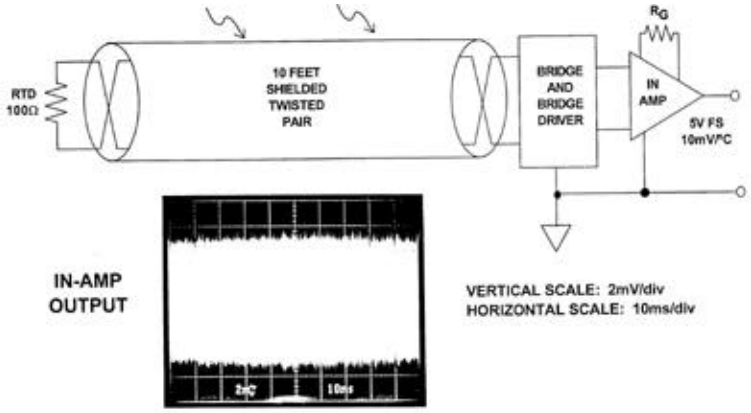

Figure 9.74

To implement effective EMI/RFI shielding, the shield must be grounded. A grounded shield reduces the value of the impedance of the shield to ground (Z in Figure 9.73) to small values. Implementing this change will reduce the amplitude of the E-Field noise substantially.

Designers often ground both ends of a shield in an attempt to reduce shield impedance and gain further E-Field attenuation. Unfortunately, this approach can create a new set of potential problems. The AC and DC ground potentials are generally different at each end of the shield. Figure 9.75 illustrates how low-frequency ground loop current is created when both ends of a shield are grounded. This low frequency current flows through the large loop area of the shield and couples into the center conductors through the parasitic mutual inductance. If the twisted pairs are precisely balanced, the induced voltage will appear as a common-mode rather than a differential voltage. Unfortunately, the conductors may not be perfectly balanced, the sensor and excitation circuit may not be fully balanced, and the common mode rejection at the receiver may not be sufficient. There will therefore be some differential noise voltage developed between the conductors at the output end, which is amplified and appears at the final output of the instrumentation amplifier. With the shields of the experimental circuit grounded at both ends, the results are shown in Figure 9.76.

SIGNAL GROUND AND EARTH GROUND HAVE DIFFERENT POTENTIALS WHICH MAY INDUCE GROUND LOOP CURRENT

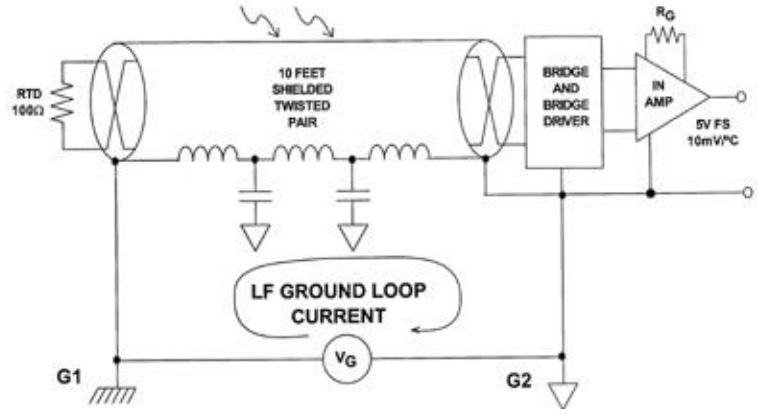

Figure 9.75

GROUNDING BOTH ENDS OF A SHIELD PRODUCES LOW FREQUENCY GROUND LOOPS

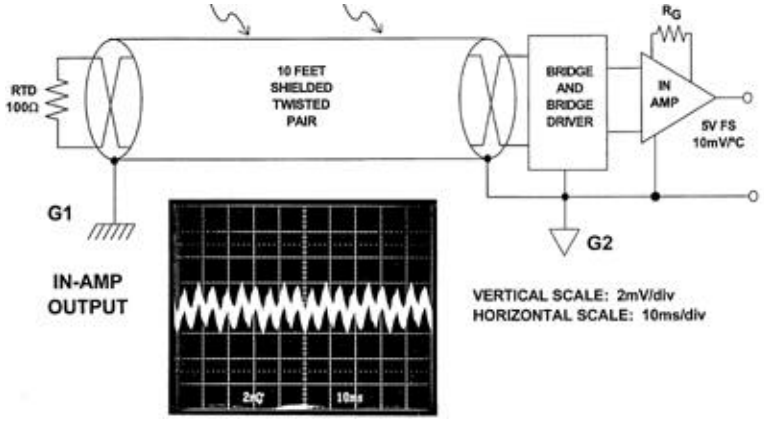

Figure 9.76

Figure 9.77 illustrates a properly grounded system with good electric field shielding. Notice that the ground loop has been eliminated. The shield has a single point ground, located at the signal conditioning circuitry, and noise coupled into the shield is effectively shunted into the receiver ground and does not appear at the output of the instrumentation amplifier.

GROUNDING SHIELD AT RECEIVER END SHUNTS LOW- AND HIGH-FREQUENCY NOISE INTO RECEIVER GROUND

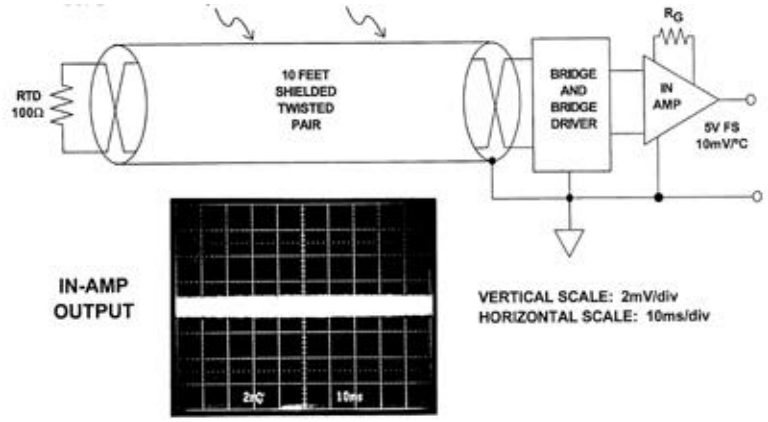

Figure 9.77

Figure 9.78 shows an example of a remotely located, ungrounded, passive sensor (EEG electrodes) which is connected to a high-gain, low power AD620 instrumentation amplifier through a shielded twisted pair cable. Note that the shield is properly grounded at the signal conditioning circuitry. The AD620 gain is 1000×, and the amplifier is operated on ±3V supplies. Notice the absence of 60Hz interference in the amplifier output.

**FOR UNGROUNDED PASSIVE SENSORS,
GROUND SHIELD AT THE RECEIVING END**

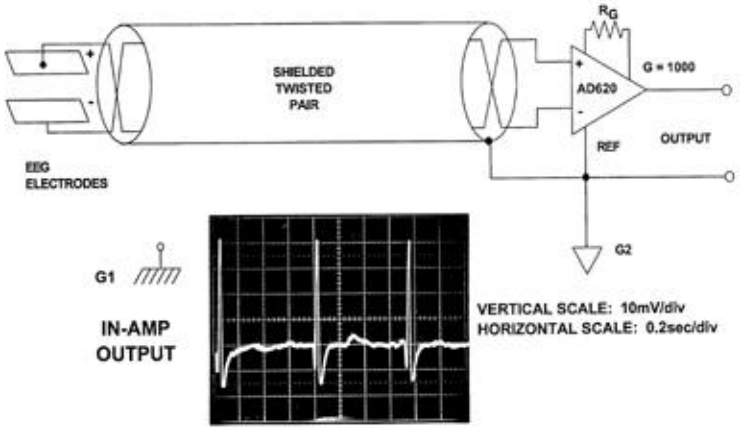

Figure 9.78

Most high impedance sensors generate low-level current or voltage outputs, such as a photodiode responding to incident light. These low-level signals are especially susceptible to EMI, and often are of the same order of magnitude as the parasitic parameters of the cable and input amplifier.

Even properly shielded cables can degrade the signals by introducing parasitic capacitance that limits bandwidth, and leakage currents that limit sensitivity. An example is shown in Figure 9.79, where a high-impedance photodiode is connected to a preamp through a long shielded twisted pair cable. Not only will the cable capacitance limit bandwidth, but cable leakage current limits sensitivity. A pre-amplifier, located close to the high-impedance sensor, is recommended to amplify the signal and to minimize the effect of cable parasitics.

**SHIELDS ARE NOT EFFECTIVE WITH
HIGH IMPEDANCE REMOTE SENSORS**

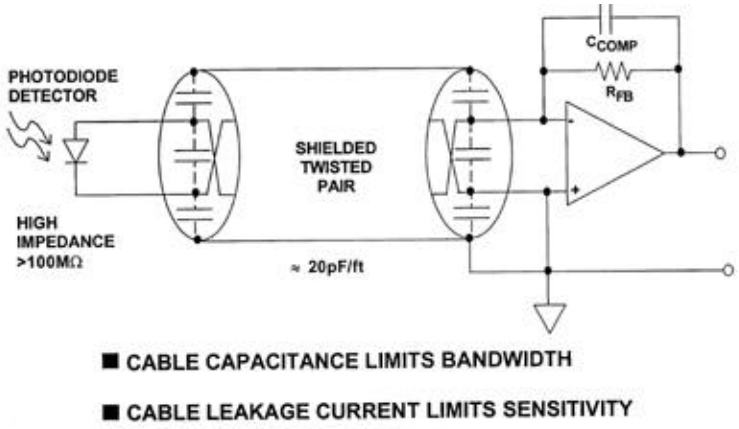

Figure 9.79

Figure 9.80 is an example of a high-impedance photodiode detector and pre-amplifier, driving a shielded twisted pair cable. Both the amplifier and the shield are grounded at a remote location. The shield is connected to the cable driver common, G1, ensuring that the signal and the shield at the driving end are both referenced to the same point. The capacitor on the receiving side of the cable shunts high frequency noise on the shield into ground G2 without introducing a low-frequency ground loop. This popular grounding scheme is known as *hybrid* grounding.

REMOTELY LOCATED HIGH IMPEDANCE SENSOR WITH PREAMP

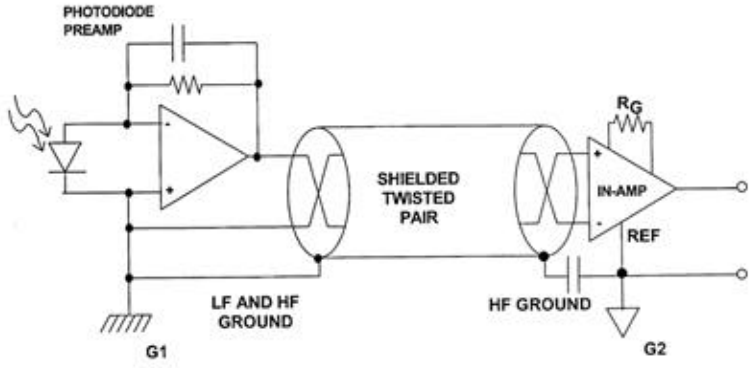

Figure 9.80

Figure 9.81 illustrates a balanced active line driver with a hybrid shield ground implementation. When a system's operation calls for a wide frequency range, the hybrid grounding technique often provides the best choice (Reference 8). The capacitor at the receiving end shunts high-frequency noise on the shield into G2 without introducing a low-frequency ground loop. At the receiver, a common-mode choke can be used to help prevent RF pickup entering the receiver, and subsequent RFI rectification (see References 9 and 10). Care should be taken that the shields are grounded to the chassis entry points to prevent contamination of the signal ground (Reference 11).

HYBRID (LF AND HF) GROUNDING WITH ACTIVE DRIVER

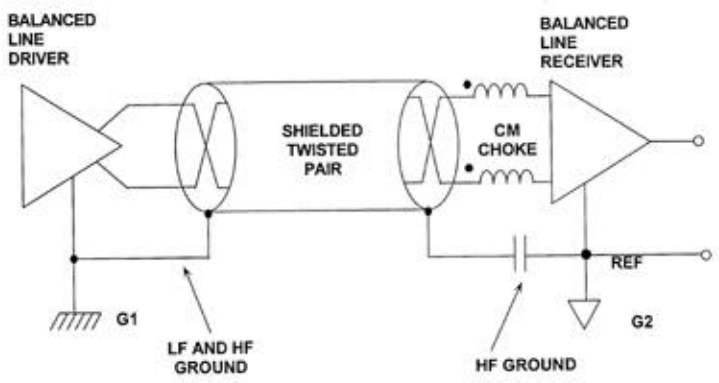

Figure 9.81

To summarize this discussion, shield grounding techniques must take into account the type and the configuration of the sensor as well as the nature of the interference. When a low-impedance passive sensor is used, grounding the shield to the receiving end is the best choice. Active sensor shields should generally be grounded at the source (direct connection to source ground) and at the receiver (connect to receiver ground using a capacitor). This hybrid approach minimizes high-frequency interference and prevents low-frequency ground loops. Shielded twisted conductors offer additional protection against shield noise because the coupled noise occurs as a common-mode, and not a differential signal.

The best shield can be compromised by poor connection techniques. Shields often use “pig-tail” connections to make the connection to ground. A “pig-tail” connection is a single wire connection from shield to either chassis or circuit ground. This type of connection is inexpensive, but at high frequency, it does not provide low impedance. Quality shields do not leave large gaps in the cable/instrument shielding system. Shield gaps provide paths for high frequency EMI to enter the system. The cable shielding system should include the cable end connectors. Ideally, cable shield connectors should make 360° contact with the chassis ground.

This section has highlighted the more common techniques used in cable shielding. There are other techniques which involve the use of driven shields, twin-shields, common-mode chokes, etc. References 1, 2, 5, 6, 7, and 8 provide an exhaustive study of the entire topic of noise reduction techniques including cable shielding.

SUMMARY OF CABLE SHIELDING TECHNIQUES

- **Do not let the shield "float"**
- **Do not connect both ends of directly to ground**
- **No LF current should flow in the shield**
- **Use the *hybrid* approach for LF and HF electric field interference**
- **The shield includes the connector, therefore avoid using *pigtails* to connect shields to ground. Use *chassis ground* to prevent *signal ground* contamination**
- **Use Common-Mode chokes at receiver to enhance RF rejection**
- **Other techniques exist:**
  Driven Shields
  Twin-Shields

Figure 9.82

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