Features

- **400 MHz to 950 MHz with Digital Channel Selection**
- **Data Rate up to 50 kbps with Data Clock Recovery**
- **FSK Modulation, Fully Integrated Demodulator**
- **Synthesized Local Oscillator for Both RX and TX**
- **Fine, Digital Tuning of the Carrier Frequency (200 Hz steps)**
- **Integrated RX/TX Switch**
- **Fast RX to TX Toggle Time: < 200 µs**
- **Fast Frequency Shifts < 50 µs for a 100 kHz Shift**
- **+10 dBm @ V_{CC} = 2.4V Output Power with 8 Digital Levels for Range Selection**
- **Power Saving Features: “Sleep” Mode and a Stand-alone “Wake-up” Procedure**
- **Easy Configuration and Dedicated Control Registers**
- **Digital RSSI and Battery Voltage Readout**
- **Available in a 48-lead TQFP Package**

Description

The AT86RF211, formerly the TRX01, is a single-chip transceiver dedicated to low power wireless applications, optimized for licence free ISM band operations from 400 MHz to 950 MHz.

Its flexibility and unique level of integration makes it a natural choice for any system related to telemetry, remote controls, alarms, radio modems, etc. It is now affordable to enhance most of these systems with bi-directional communications, and thus to secure the transmissions with hand-shake procedures! More sophisticated applications, such as “automatic meter reading” or “hand held terminals”, become both technically and economically more attractive.

The AT86RF211 can easily be reconfigured and, in particular, enables efficient FHSS operations. The selection of a channel, with a fast lock time, is indeed fully digital

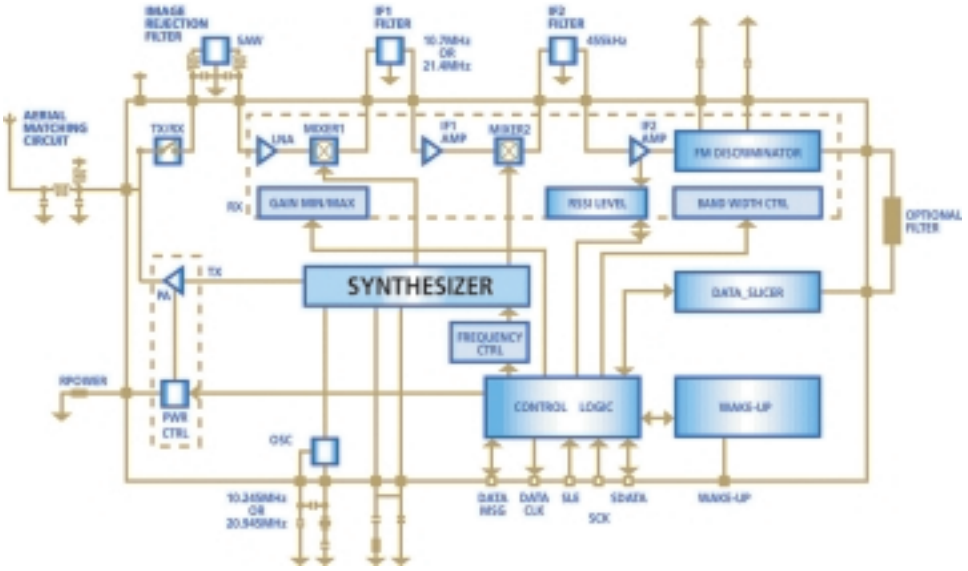
The AT86RF211 is also well adapted to battery operating systems as it can be powered with only 2.4V. It also offers a “wake up” receiver feature to save power by alerting the associated microcontroller only when a valid inquiry is detected. The output power can be controlled from -10 dBm to +14 dBm, i.e. 25 mW in 868 MHz frequency band.

FSK Transceiver for ISM Radio Applications

AT86RF211 (TRX01)

Rev. 1942B–11/00

Figure 1. AT86RF211 Block Diagram



General Characteristics

Unless otherwise specified, the parameters are given at T = 25°C, V_{CC} = 3V, R_{POWER} = 18 kΩ.

	Min	Typ	Max	Unit	Comments
Supply Voltage	2.4		5.5	volt	
Temperature	-40		85	°C	
Frequency	400		950	MHz	(1)
Current Consumption		1		µA	Power down mode after 1 ms
Current Consumption		3	5	µA	Sleep mode
Current Consumption		39		mA	TX (2)
Current Consumption		27		mA	RX

Notes:
1. Any channel can be programmed digitally by means of 3 wires interface. The following subranges are actually programmable:
   400 to 480 MHz
   800 to 950 MHz
   Atmel will provide a piece of software to translate the selected frequency into the “frequency code” to be programmed in the “frequency registers”.
2. Current consumption given for P_{OUT} = +10 dBm at 434 MHz (see PA description part for details).

Pinouts

Pin	Name	Comments
1	RPOWER	Full scale output power resistor
2	TXGND1	GND
3	RF	RF input / output
4	TXGND2	GND
5	TXGND3	GND
6	TXGND4	GND
7	TXVCC	VCC
8	TXGND5	GND
9	DIGND	GND
10	DIVCC	VCC
11	DATAMSG	Input/output digital message
12	SLE	Serial interface (enable)
13	SCK	Serial interface (clock)
14	SDATA	Serial interface (data)
15	WAKEUP	Wake-up output
16	DATACLK	Data clock recovery
17	-	Test pin: do not connect
18	EVCC1	VCC
19	EGND1	GND
20	-	Test pin: do not connect
21	CGND1	GND
22	CVCC1	VCC
23	XTAL1	Crystal input
24	XTAL2	Crystal output

Pin	Name	Comments
25	SKFILT	Threshold for data slicer
26	DSIN	Data slicer input
27	DISCOUT	Discriminator output
28	IF2VCC	VCC
29	IF2GND	GND
30	IF2IN	IF2 amplifier input
31	IF2DEC	2.2 nF to ground
32	DISCFILT	Discriminator bypass
33	IF2OUT	IF2 mixer output
34	IF1DEC	4.7 nF to ground
35	IF1IN	IF1 amplifier input
36	IF1OUT	IF1 mixer output
37	AGND	GND
38	AVCC	VCC
39	CVCC2	VCC
40	CGND2	GND
41	FILT1	Synthesizer output
42	VCOIN	Synthesizer input (VCO)
43	EVCC2	VCC
44	EGND2	GND
45	RXIN	LNA input from SAW filter
46	RXVCC	VCC
47	RXGND	GND
48	SWOUT	Switch output

Synthesizer Specifications

	Min	Typ	Max	Unit	Comments
Frequency Range	400		950	MHz	Digital programming
Crystal Frequency		10.245		MHz	IF 1 = 10.7 MHz
Crystal Frequency		20.945		MHz	IF 1 = 21.4 MHz
Oscillator Settling Time		8		ms	Depending on quartz specifications
Lock Time			500	µs	From oscillator settling
Lock Time			200	µs	10.7 MHz shift (RX to TX toggle)
Lock Time			50	µs	100 kHz shift
Phase Noise		-80		dBc/Hz	At 10 kHz from the carrier
Phase Noise		-86		dBc/Hz	At 100 kHz from the carrier

Transmitter Specifications

Unless otherwise specified, the parameters are given at T = 25°C, V_{CC} = 3V, R_{POWER} = 18 kΩ.

	Min	Typ	Max	Unit	Comments
Output Power	-10		+12	dBm	(1)
Output Power Dynamic Range		12		dB	Digital programming (2)
Automatic Level Control Accuracy		1		dB	
Spurious Level			-46	dBc	P_{OUT} = +10 dBm
2nd Harmonic			-25	dBc	P_{OUT} = +10 dBm (3)
3rd Harmonic			-12	dBc	P_{OUT} = +10 dBm (3)
Power Amplifier Load Impedance		300		Ω	Best efficiency (3)
FSK Data Rate			50	kbps	
RX to TX Toggle Time			200	µs	

Notes:
1. The output power is regulated against process, temperature and power supply variations by an internal ALC loop.
2. The maximum power is set by an external resistor, connected to pin R_{POWER}. The actual output power can be digitally programmed / re-programmed, up to -12 dB below this limit, by means of a 3-bit word: TXLVL of CTRL1 register.
3. As the optimum load impedance for the Power Amplifier (PA) is 300Ω, a matching network is usually inserted between the PA output and the antenna. This matching network, which is basically a band pass filter, must be designed to reduce the spurious and harmonic levels in compliance with the relevant regulation (see application schematics).
4. The PA can be supplied by a different voltage source than the general power supply of the component. Maximum output powers are given below for popular frequency bands with R_{POWER} = R_{NOM} =18 kΩ at V_{CC} = 3.5V.

Frequency	Output Power for TXLVL (CTRL1) = '111'
433 MHz	+16 dBm
868 MHz	+12 dBm
915 MHz	+10 dBm

P_{OUT} can be increased with lower values for R_{POWER}, for example 10 kΩ (see PA description part for details).

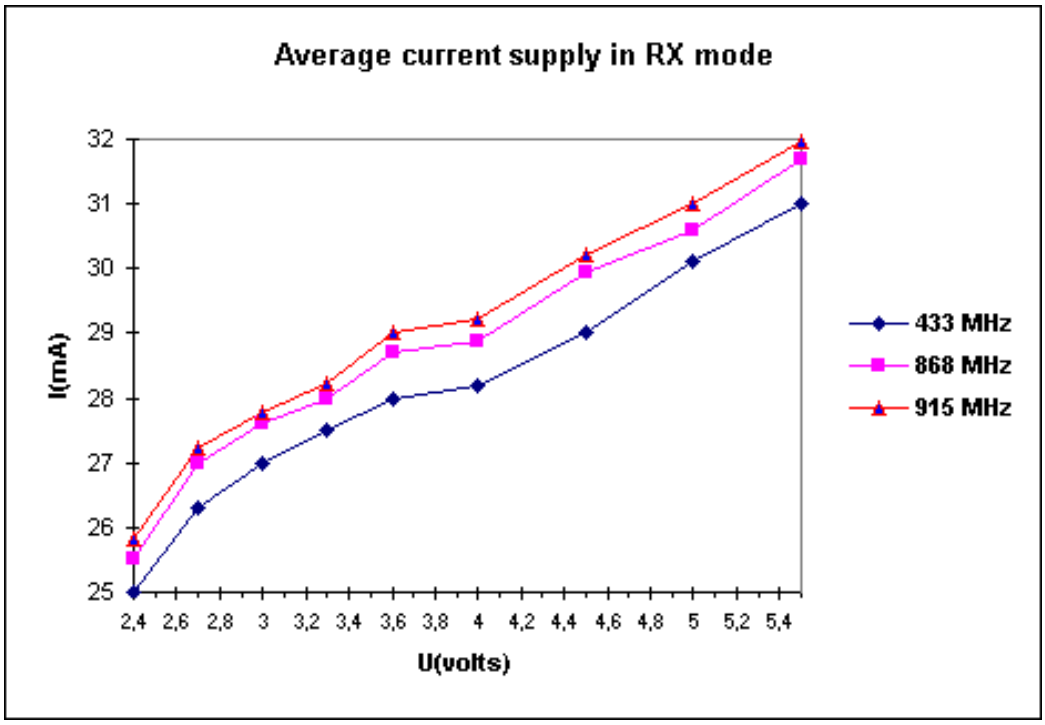
Receiver Specifications

	Min	Typ	Max	Unit	Comments
IF1	10.7		21.4	MHz	
IF1 Filter Impedance		330		Ω	
IF2		455		kHz	
IF2 Filter Impedance		1700		Ω	
FSK Sensitivity	-105			dBm	4800 bps & BER = 1%; BW = 20 kHz; input matched
Noise Figure			15	dB	Input matched, complete RX chain
Input IP3	-10			dBm	
Max Input Power			0	dBm	BER = 0.1
RF Switch Input Capacitance		1		pF	
RF Switch Output Capacitance		1		pF	
RXIN Pin Impedance		1000 // 1		Ω // pF	LNA input
R_{OPT} for Minimum Noise	450		500	Ω	(1)

Notes: 1. At 434 MHz, the optimized impedance viewed from the input of the LNA should be 500Ω. For 868 MHz / 915 MHz frequency bands, this impedance falls to 450Ω.

The current consumption of RX mode for various levels of voltage supply is given in the following table.

Figure 2.



IF1 choice

For selectivity purpose, a classical 2 IF superheterodyne architecture has been selected for the AT86RF211. In order to minimize the external components cost, the most popular IF values have been chosen. The impedances of the input/output of the mixing stages have been internally matched to the most usual ceramic filter impedances.

Two typical IF values are proposed:

- 10.7 MHz. The most popular option.
- 21.4 MHz. The image frequency is far enough from the carrier frequency to enable the use of a front-end ceramic filter instead of a SAW filter. It is also noticeable that 21.4 MHz quartz filters usually have more abrupt slopes than 10.7 MHz ceramic filters.

Filters choice

To further reduce the filtering cost, the IF filters may be replaced by just a coupling capacitor, with the following consequences:

IF1 filter removal

The replacement coupling capacitor value should be >100 pF.

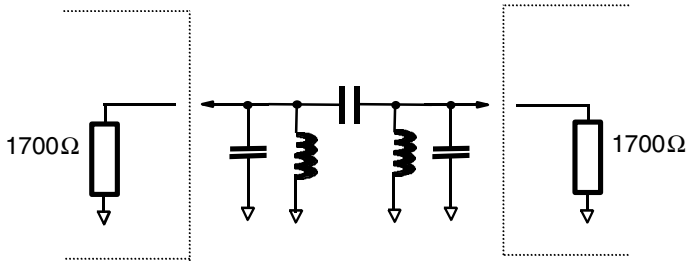
As a usual front-end SAW filter is not able to reject the image frequency (2 x 455 kHz from the carrier frequency), the selectivity is then lessen and a 3dB sensitivity degradation is expected, not mentioning the jamming effects of a high power device transmitting at the image frequency.

IF2 filter removal

The replacement coupling capacitor value should be >1 nF. The selectivity is then set by the IF1 filter.

Currently available commercial filters have a maximum bandwidth of ±35 kHz enabling a data rate up to 20 kbps. For applications with higher data rates, the ceramic filter can be replaced by a LC band-pass filter as described hereafter:

Figure 3.



Detailed Description

The AT86RF211 is a fully integrated radio transceiver, optimized to operate in the ISM bands up to 930 MHz.

Only the input SAW filter and the aerial impedance matching network are to be changed when a new ISM band is selected.

The AT86RF211 has been designed for high-performance applications, based on the natural benefits of a 2 IF superheterodyne architecture.

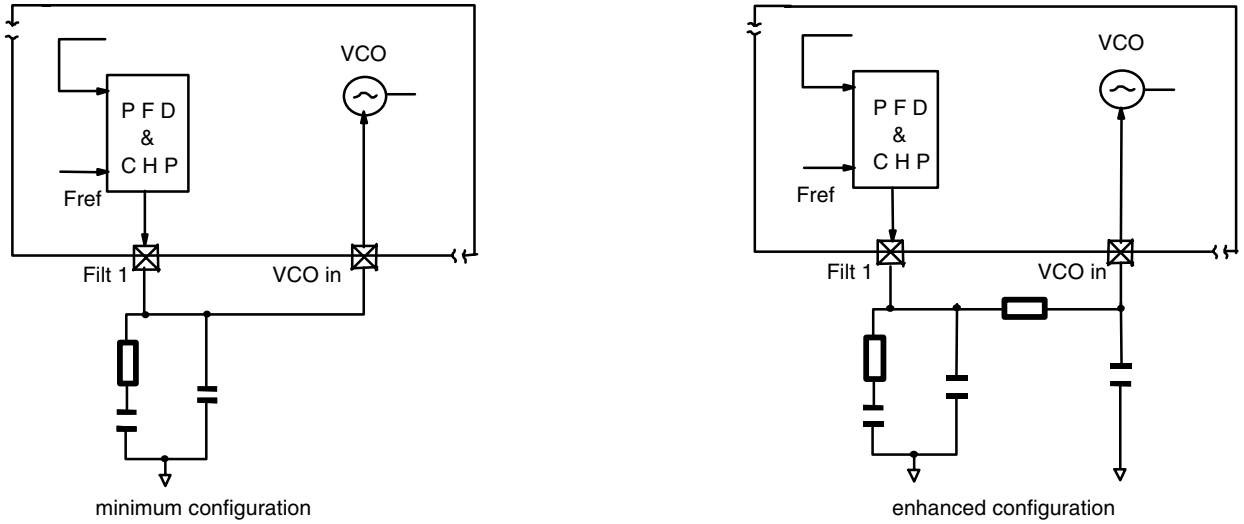
It includes all the logic control part to conveniently monitor the transmission (frequencies selection, gain, output power optimization, etc.), and the digital processing to deliver demodulated, reshaped bits for CMOS level interfaces. This includes the choice for the 1st stage input gain, the IF1 frequency, the bandwidth of the baseband data stream bits and the voltage reference for the data slicer.

In order to save energy, a “wake-up” functionality is implemented that keeps the component in a low current consumption mode and turns it ON in RX mode periodically. This mode is able to analyze the received bit stream and detect the occurrence of the predefined message format that will wake up the external microcontroller.

Synthesizer

A high speed, high resolution multi-loops synthesizer is integrated. It can be tuned to two frequency bands: 400 MHz to 480 MHz or 800 MHz to 950 MHz. All the channels in these two bands can be selected through software programming. All the circuitry is on chip, with the exception of the PLL loop filter. The phase comparison is made thanks to a charge pump topology.

Figure 4.



The full frequency ranges of usual ISM bands (434,868 and 915 MHz) are covered with power supply voltage from 2.4V to 5.5V.

The VCO slope is 150 MHz/V for the 400-480 MHz and 800-950 MHz ranges. Obviously, such high slopes require a careful board design, in order to avoid any noise picking.

The equivalent reference frequency of the loop depends on the LO frequency, and is in the range of 500 to 1000 kHz. The loop filter is designed in a classical way, because parasitic phenomena such as fractional spurii do not have to be taken into account. The loop bandwidth is, as usual, close to 10% of the reference frequency. Typically, with a reference frequency of 800 kHz, the loop bandwidth will be in the 60-80 kHz range, enabling the great frequency agility required by full digital FSK modulation and frequency hopping. With an optimized loop, and for frequency shifts less than 100 kHz, the synthesizer lock time is less than 50 µs.

Full digital FSK modulation is possible up to 50 kbps. The user pre-loads the two used frequencies and the AT86RF211 automatically switches from one value to the other, according to the DATAMSG pin state. It should be noted for the design of the loop filter that the capacitance at VCOIN pin is around 20 pF.

Frequency selection has a resolution typically around 200 Hz. For some frequencies, the resolution can be reduced to 2.6 kHz (worst case). But, this phenomenon only arises every multiple of 10.245 MHz or 20.945/2 MHz depending on crystal frequency. In practice, only the wide 902-928 MHz US ISM band can be affected and for only two frequencies as its width is 26 MHz: 922.05 MHz and 911.805 MHz with 10.245 MHz crystal, or 911.1075 MHz and 921.58 MHz with 20.945 MHz crystal.

Figure 5. Schematic output of the charge pump

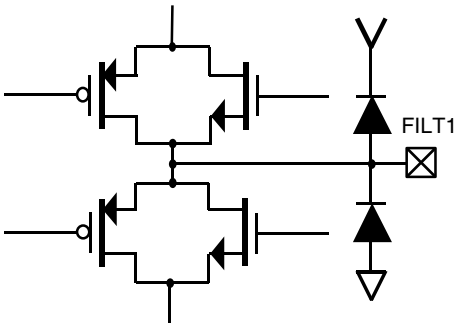
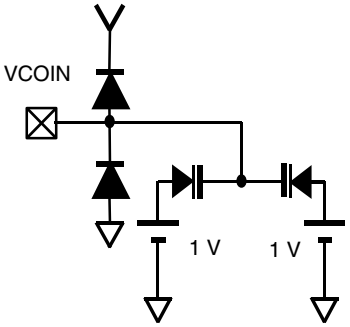


Figure 6. Schematic input of the VCO



Power Amplifier

The Power Amplifier (PA) is able to deliver +10 dBm, i.e. 10 mW, in the 3 popular frequency bands 434 MHz, 868 MHz and 915 MHz. This can be obtained with the optimum specified R_{POWER} = 18 kΩ. The +10 dBm specification is intended to be on the aerial.

But this is not the maximum output power. P_{OUT} max. available is higher depending on maximum consumption affordable on V_{DD} and on the frequency band. For instance, the power available for F_{RF} = 915 MHz under V_{DD} = 4V with I_{CONS} = 55 mA for the whole component is +11.5 dBm with R_{POWER} = 12 kΩ and ad hoc output matching network. The curves next page show the expected current consumed compared to the power available on the aerial. These values are a trade-off between maximum power and current consumption considering that I_{SUPPLY} has to be as low as possible for +10 dBm output power.

With R_{POWER} = 12 kΩ, P_{OUT} can be up to +19 dBm in the 400 MHz. Considering the regulations, this can be useful in some frequency bands where such high level of power is authorized.

In the 868 MHz ISM band, European committees have regulated the maximum output power to +14 dBm, i.e. 25 mW, and the AT86RF211 was made in order to reach this maximum authorized level of power.

Output is an open-collector type.

Figure 7. Output of the power amplifier

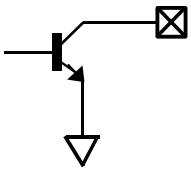
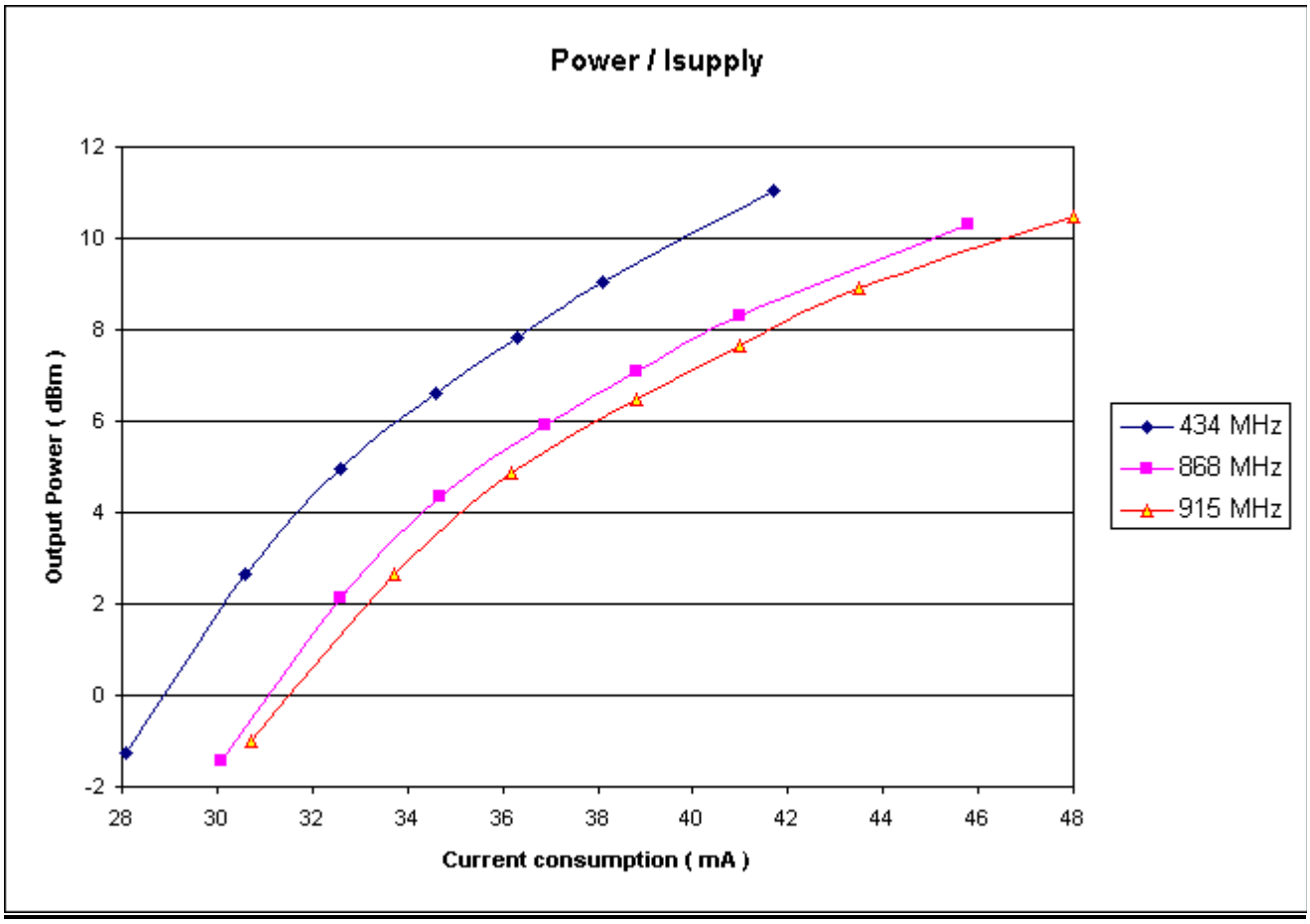


Figure 8. Output power



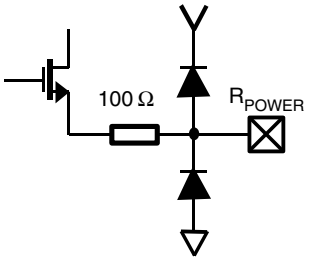
All the output powers specified above are supposed to be measured with impedance matching at the output of the power amplifier. Output impedance of the P.A. is around 300Ω. The current consumption for a +10 dBm output power is thus 39 mA at 434 MHz, 45 mA at 868 MHz and 46 mA at 915 MHz.

Output Power User Control

The actual output power can be set in two steps, first on the board, second with programming:

- an external resistor, connected at pin R_{POWER}, set the maximum output power (for instance, the regulation upper limit in a particular ISM band)
- the power can then be adjusted, from this value set by R_{POWER} down to a maximum of -12 dB below, by programming the bits 6 to 8 of the CTRL1 register. So, 8 levels are selectable, with a linear variation of the output power. The minimum regulated output power is set to -10 dBm.

Figure 9. Schematic of the input of R_{POWER}

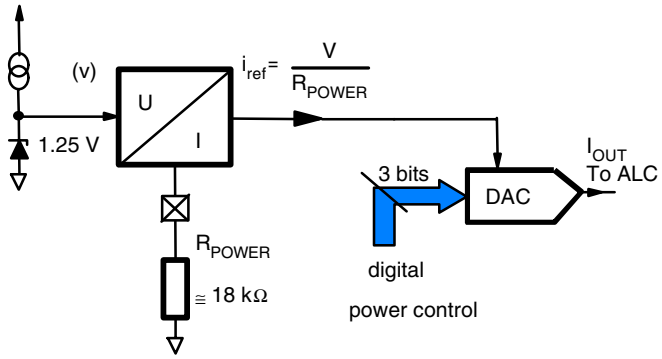


This option can naturally be very useful to save power, in particular in the case of roaming systems: the two transmission points can exchange their RSSI values (bits 24 to 29 of the STATUS register) and then adapt their output power level accordingly.

Output Power Automatic Control

An automatic level control loop (ALC) is integrated, in order to minimize the sensitivity of the PA to the temperature, process and power supply variations. The ALC is controlled by a current which is generated in the following way:

Figure 10. ALC of the power amplifier



The output current I_{OUT} is inversely proportional to the R_{POWER} resistor. Lower values of R_{POWER} lead to high output power.

To get a +10dBm output power, I_{OUT} should be about 70 µA and R_{POWER} sets to about 18 kΩ.

Impedance Matching

Naturally, the greater the PA output voltage swing, the better the power efficiency. As the PA output is supplied through an inductor, a swing of 2 x V_{DD} is possible. In practice, due to saturation effects, the voltage swing is limited to approximately (2 x V_{DD}) - 1V.

With a power supply voltage of 3V, the PA output voltage is 5V peak-to-peak, or 1.77 V_{EFF}. If 10 mW have to be delivered, i.e. +10 dBm, the optimum load resistor is given by the classical formula:

$$P_{out} = 0.01W = V^2_{RMS} / R_{LOAD} \Longrightarrow R_{LOAD} = 314\Omega$$

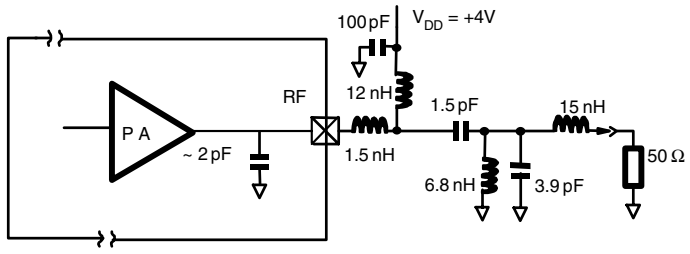
As the usual impedance of an aerial is 50Ω, a matching network (either a low-pass or a band-pass filter) must be inserted between the PA output and the aerial.

An indirect benefit of this network is to filter out the output signal harmonic levels; it can hence be designed to meet a particular regulation.

It is noticeable that the implementation of this network on a board requires some cautious choices (small surface mount components, compact layout, good grounding topology) in order to limit the radiating of the harmonic levels.

The design of this network should also take into account the PA output capacitance of about 2 pF.

Figure 11. Example of 300Ω to 50Ω matching network at 868 MHz from our demo board



Maximum Output Power

To get this power out of the AT86RF211, it is mandatory to implement efficient grounding techniques. Excessive inductor values to ground will not only limit the PA output voltage swing, but may also trigger RF instability. Careful board design is vital to avoid parasitic loss when high output power is needed.

Receiver

The AT86RF211 includes a complete receiver, from a SPST switch to the FSK discriminator. All the cells are designed to operate from 400 to 1000 MHz, and at 10.7 MHz / 21.4 MHz or at 455 kHz for intermediate frequencies. The gain of the 1st stage is selectable (2 values in CTRL1, bit 25). However, other IFs can be chosen, with only minor performance degradation.

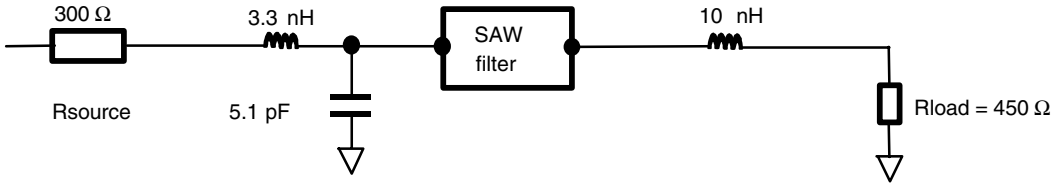
RX/TX Switch

A SPST switch is integrated.

In the transmission mode, it protects the LNA input from the large voltage swings of the PA output (up to 10V peak-to-peak with a power supply voltage of 5.5V), which is switched to a high impedance state.

It is automatically turned ON or OFF by the RX/TX control bit.

Figure 12.

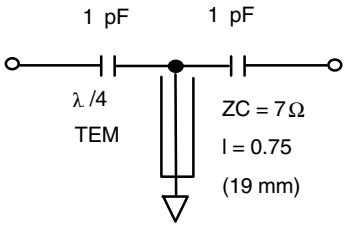


Each SAW filter manufacturer will give the ad hoc impedance for matching.

If a moderate image rejection can be tolerated by the application, the SAW filter can be replaced by lower loss TEM ceramic or helicoïdal filters.

Alternatively, a ceramic coax λ/4 resonator can be designed as a narrow band-pass filter. For instance, with an IF selected at 10.7 MHz, a -3 dB bandwidth of 5 MHz, with an insertion loss of 1 dB and an image rejection of 12 dB, can be achieved in the following:

Figure 13.



Such a filter also provides an out-of-band interference rejection greater than 20dB, at 40MHz away from 433MHz.

The insertion loss is about 2 dB, and the reverse isolation about 30 dB in a 300Ω environment.

Image Rejection Filter

The AT86RF211 can be used with an external image rejection band-pass filter. If IF1 = 10.7 MHz, the image frequency is 21.4 MHz away from the desired frequency, and must be eliminated by a narrow, sharp band-pass filter like a usual SAW filter.

Naturally, the SAW filter impedance has to be matched with the 500Ω LNA optimum impedance. Even with a 50Ω environment, a matching network is anyway needed in most applications, as the usual SAW filter internal impedance is in the range of 50Ω to 1000Ω. Manufacturers of such filters give networks for optimum adaptation.

For instance, the matching network to 450Ω for the SAW filter in our demo board is given by the following scheme at 868 MHz.

LNA and First Mixer

The high integration of the receiving input part of the AT86RF211 makes it possible to have a high gain and a low NF with an optimized power consumption. Its main characteristics are:

- voltage gain:
  17 dB typ. for the LNA / Mixer; 11 dB if gain min. is selected
- bandwidth:
  1.2 GHz
- noise figure of LNA alone:
  3 dB typ. @ 900 MHz, best matching
- noise figure of LNA + mixer:
  8 dB typ. @ 900 MHz, with maximum gain and best matching
  12 dB typ. @ 900 MHz, with minimum gain and best matching
- input impedance:
  1000Ω // 1 pF
- 1 dB compression point:
  -20 dBm at the input of LNA
- input IP3:
  -10 dBm

Gain is programmable through bit 25 of CTRL1 register (6 dB attenuation when gain min is selected). The choice for a matching impedance of 500Ω at 434 MHz and 450Ω at 868 MHz / 915 MHz is made for noise figure optimization. However, as input impedance is about 1000Ω, a loss of gain appears due to the mismatch. But, the benefit obtained in NF justifies this loss.

The LNA is directly coupled to the first mixer for consumption and performance optimization. Input and output of the LNA / Mixer must be connected through capacitor because of their internal DC coupling.

Figure 14. Schematic input of the LNA

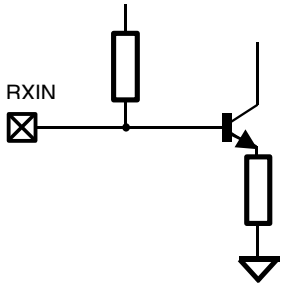
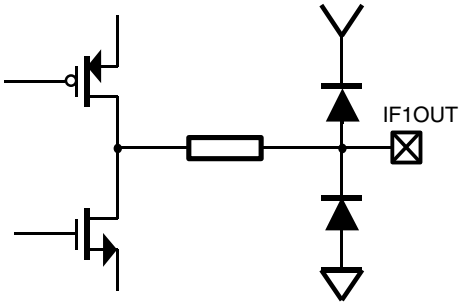


Figure 15. Schematic output of the mixer



The first mixer translates the input RF signal down to 21.4 MHz or 10.7 MHz as chosen by the user. The local oscillator is provided by the same synthesizer which is then programmed to generate a local frequency 21.4 MHz or 10.7 MHz away from the TX carrier frequency.

The output impedance of the mixer is 330Ω with a 20% accuracy, so that low cost, standard 10.7 MHz ceramic filters can be directly driven.

Other IF may be chosen thanks to the high bandwidth (50 MHz) of the mixer.

IF1 Amplifier Chain and Second Mixer

The input impedance of the IF1 amplifier is naturally 330Ω to match the input filter. The voltage gain, i.e. gain at 10.7 MHz or 21.4 MHz added to the conversion gain at 455 kHz is 14 dB when loaded by 1700Ω.

The second mixer operates at a fixed LO frequency of 20.945 MHz or 10.245 MHz. Its output impedance is 1700Ω in parallel with 20 pF.

Figure 16. Schematic input of IF1 amplifier

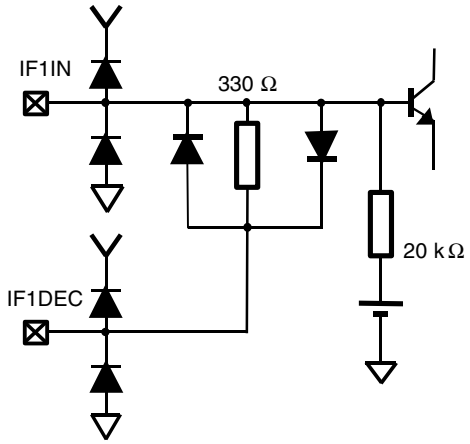
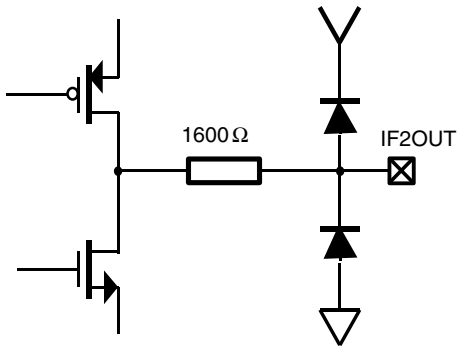


Figure 17. Schematic output of the 2nd mixer



It operates as a limiting IF chain.

IF2 Amplifier Chain

The input impedance of the IF2 amplifier is 1700Ω. This value enable the use of popular filters with impedance between 1500Ω and 2000Ω.

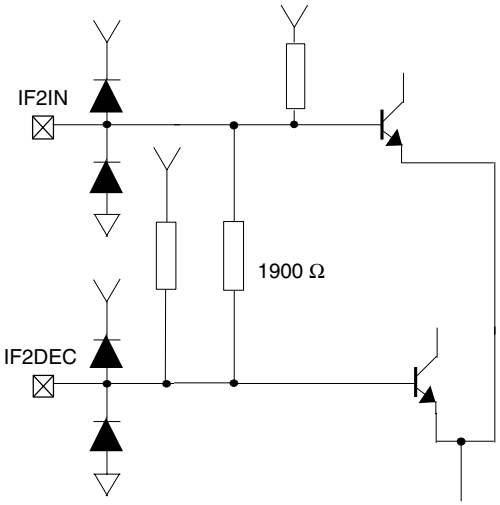
It is directly connected to the FSK demodulator.

The bandwidth is internally limited to 1 MHz to minimize the noise before the discriminator. It acts like a bandpass filter centered at 455 kHz with capacitive coupling between stages of amplifier and mixer. Total voltage gain is typically 86 dB.

Thanks to the capacitive coupling, no slow DC feedback loop is needed enabling a fast turn on.

IF2DEC has to be decoupled with at least 2.2 nF.

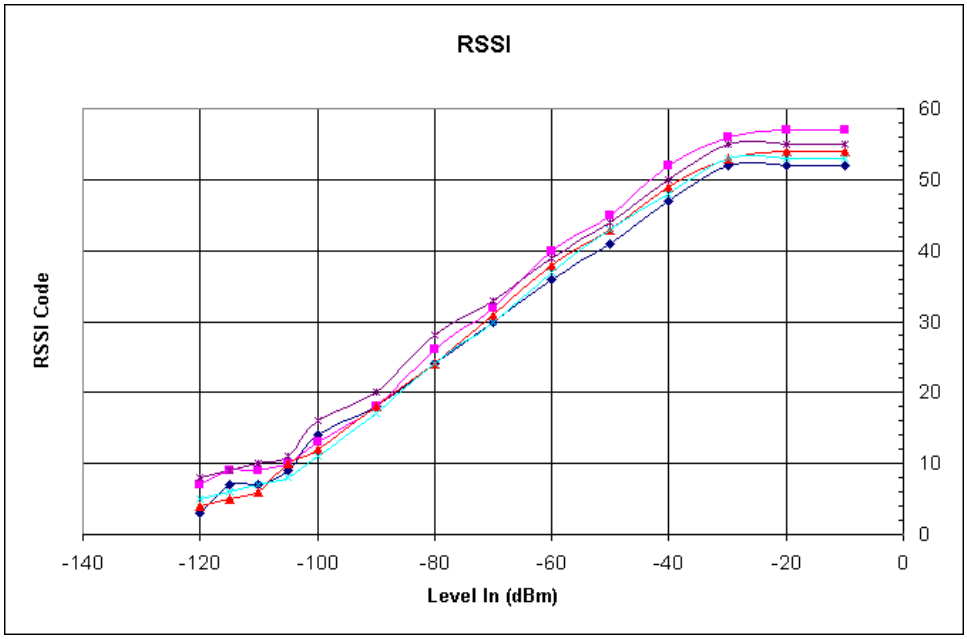
Figure 18. Schematic of the input of IF2 amplifier



RSSI Output

The RSSI value can be read as a 6 bits word in the STATUS register. Its value is linear in dB as plotted below (5 samples curves):

Figure 19. RSSI coding



The RSSI dynamic range is 65 dB from -105 dBm to -40 dBm RF input signal power, over temperature and power supply ranges. The RSSI LSB's value weights about 1.6 dB in the linear area.

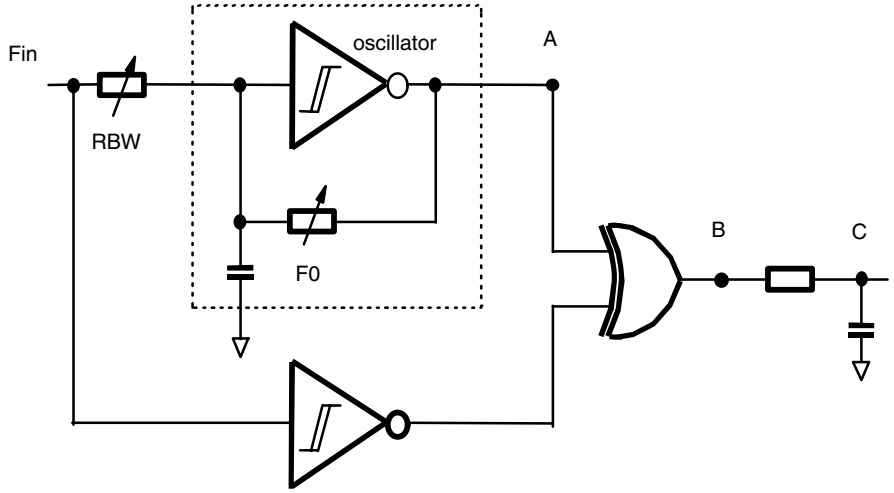
The RSSI value is measured from the IF2 chain.

The RSSI is periodically measured, every 12 ms. Its value is compared with a user predefined value, so that the demodulated data is enabled only if the RSSI value is above this threshold. Some hysteresis effect may be added (see Control Register's content).

FSK Demodulator

The structure of the FSK demodulator is based on an oscillator:

Figure 20. Schematic of the FSK demodulator



The oscillator, which natural frequency is F_0, actually oscillates at the F_{in} frequency. The signal phase at the output of the oscillator (A) is proportional to the frequency delta between F_{in} and F_0. The XOR function translates the phase difference into a pulse duty cycle (B), and then the low-pass filter transforms this duty cycle into a mean voltage (C).

When $F_{in} = F_0$, the duty cycle is 50%; thereby, the output voltage in C is naturally $V_{DD}/2$.

The input RBW resistor controls the discriminator bandwidth. Two ranges can be selected (see Control Register's content):

- ±50 kHz: this range suits the high data rate applications, with a frequency shift of several tens of kHz.
- ±25 kHz: this range better suits lower data rate applications with smaller frequency shifts.

The oscillator feedback resistor controls the centre frequency. It is adjusted according to the output of a dummy FSK demodulator driven by a 455 kHz reference frequency divided from the crystal frequency.

For integration purpose, the resistors are actually current sources.

The low-pass filter is designed with constant group delay for minimum distortion of the bit stream.

It is also noticeable that the linearity range of this structure is fairly wide. Because of the known output voltage value, a true DC coupling can be used between the demodulator and the data slicer (no need to compare with the mean value of the data stream). Thanks to this feature, the first received bit can be sliced perfectly and there is no need for classical 010101… starting pattern.

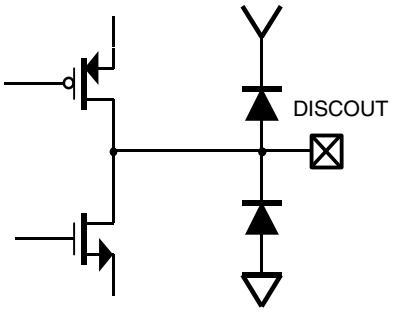
The nominal demodulated voltage is 100 mV peak-to-peak for the discriminator full range (±50 kHz or ±25 kHz).

To avoid any signal distortion, the output current should be limited to ±50 µA peak-to-peak.

The slope of the discriminator is +14 mV/kHz for V_{DD} = 2.4V. Add 5 mV/kHz/V for other voltage supplies.

The output of the discriminator is a rail-to-rail amplifier.

Figure 21. Schematic of the output of demodulated data



Data Slicer

The externally low-pass filtered analog signals out of the demodulator are converted into CMOS level data by a high resolution comparator (voltage gain ~ 100 kV/V).

The SKFILT pin is used to extract the mean value of the analog demodulated signal and to adjust the comparison threshold.

If the data stream is made of the same number of '0' and '1', as for Manchester code for instance, such a scheme is both very simple and efficient. It is noticeable that the SKFILT pin is in a high-impedance state when the AT86RF211 is in "sleep" mode, so that its value is kept constant till the next receive cycle.

An alternate implementation is to set the SKFILT voltage at $V_{DD}/2$ with an external resistive voltage divider. In this case, NRZ coding is possible.

To permit accurate detection of signal level, a programmable DAC allows the designer to modify the comparison voltage around $V_{DD}/2$. The programming is made through 4 bits of DTR's register. The value of the LSB is 5.7 mV for 1V of voltage supply which means 17 mV for V_{DD} = 3V. This can be useful to compensate crystal deviation of few ppms, between -8 kHz to +7 kHz. The right value of this register can be obtained when the lowest BER is measured or when the DATAMSG's bits widths are equal to one another. The input of the data slicer is a CMOS rail-to-rail amplifier.

Figure 22. Schematic of the data slicer input

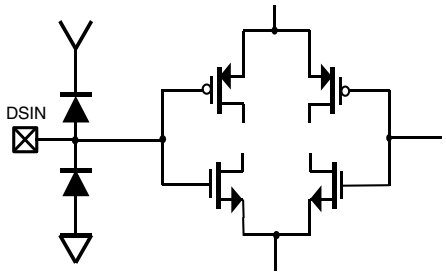
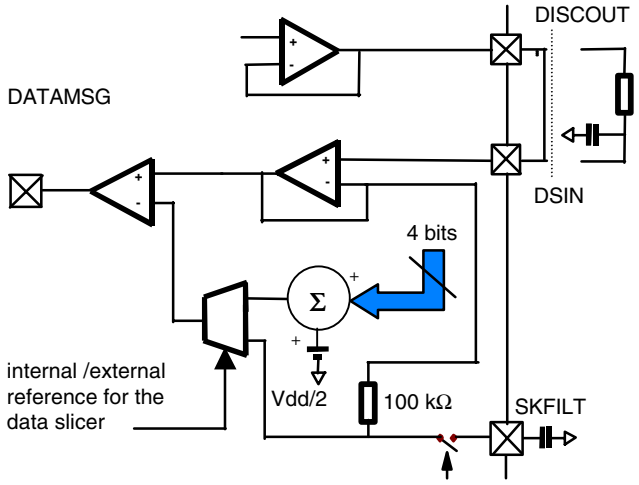


Figure 23. Schematic of the data slice



Crystal Reference Oscillator

It is based on a classical COLPITTS architecture with two external capacitors.

A XTAL with load capacitor in the range of 10-20 pF is recommended. The bias circuitry of the oscillator is optimized to produce a low drive level for the XTAL. This reduces XTAL ageing. Any standard, parallel, 20.945 MHz or 10.245 MHz crystal can be used.

Figure 24. Schematic of the crystal oscillator input

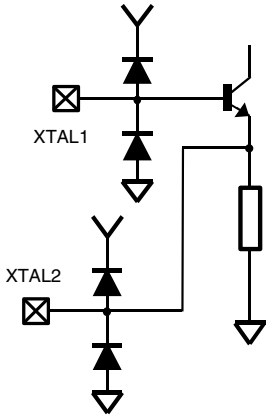
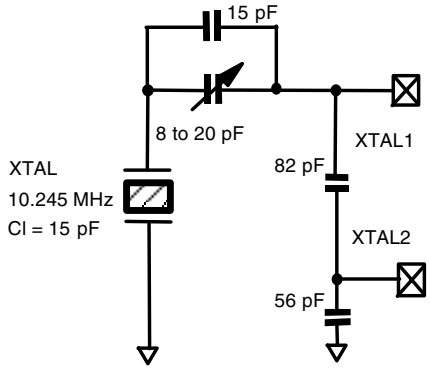


Figure 25. Input crystal network



Serial Data Interface

The application microcontroller can control and monitor the AT86RF211 through a synchronous, bi-directional, serial interface made of 3 wires:

- SLE: enable input
- SCK: clock input
- SDATA: data in/out

When SLE='1', the interface is inhibited, i.e. the SCK and SDATA (in) values are not propagated into the IC - reducing the power consumption and preventing any risk of parasitic write or read cycle.

A "read" or "write" cycle starts when SLE is set to '0', and stops when SLE is set to '1'. Only one operation can be performed in one access cycle: only one register can be either read or written.

Register Interface Format

A message is made of 3 fields:

- address A[3:0]: 4 bits (MSB first)
- R/W: read/write selection
- data D[31:0]: up to 32 bits (MSB first)

ADDRESS				R/W	DATA up to 32 bits (variable length)		
A[3]	A[2]	A[1]	A[0]	R/W	MSB	D[nbit-1:0]	LSB

Variable register length and partial read or write cycles are supported.

In case of partial read or write cycles, the first data (in or out) is always the MSB of the register.

WRITE Mode (R/W = 1)

The address, R/W, and data bits are clocked on the rising edge of SCK.

If the number of data bits is lower than the register capacity, the LSB bits keep their former value. If the number of data bits is greater than the register capacity, the extra bits are ignored.

The data is actually written into the register on the rising edge of SLE, when the data length is less or equal to the register length.

When trying to write more data than the register length, data is written on the first extra rising clock edge, regarding register length.

Figure 26. Write Chronogram: Complete write cycle in a 10 bit register

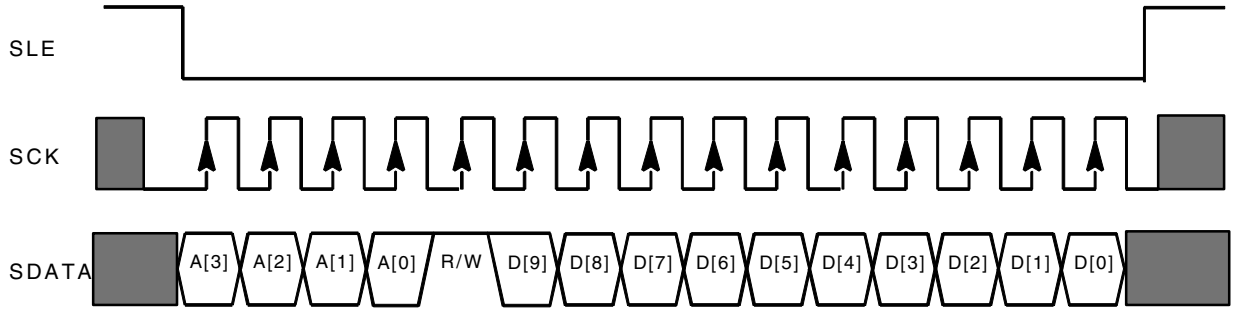
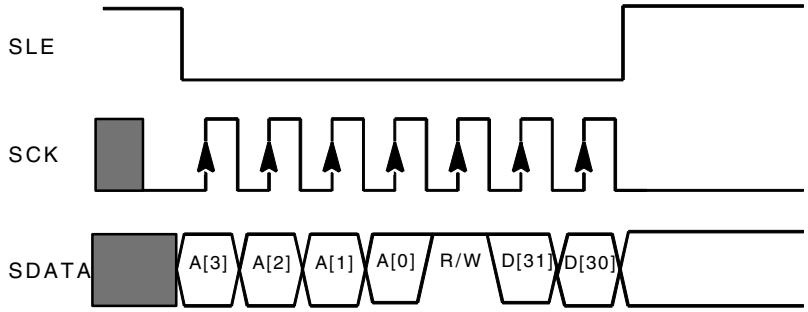


Figure 27. Write Chronogram: partial write cycle, writing 2 bits



READ Mode (R/W = 0)

The address and R/W bits are clocked on the rising edge of SCK.

The data bits are changed on the falling edge of SCK. The MSB of the register is the first bit read.

It is possible to stop reading a register (SLE back to “1”) at any time.

If an attempt to read more bits than the register capacity is detected, SDATA is clamped to “0”.

If the address of a register is not valid, SDATA is set to “1” during the first 32 SCK periods, then to “0” during all the extra periods.

SDATA is switched back to the input state when SLE is back to “1”.

Figure 28. Read Chronogram: complete read cycle from a 10 bit register

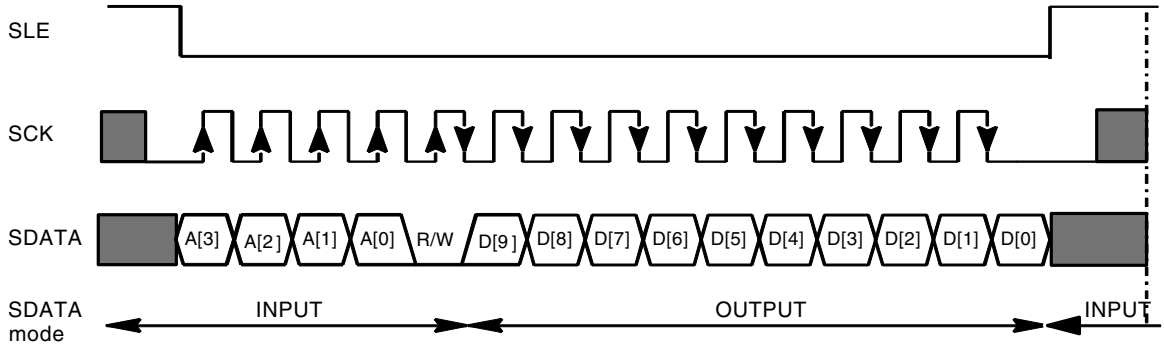
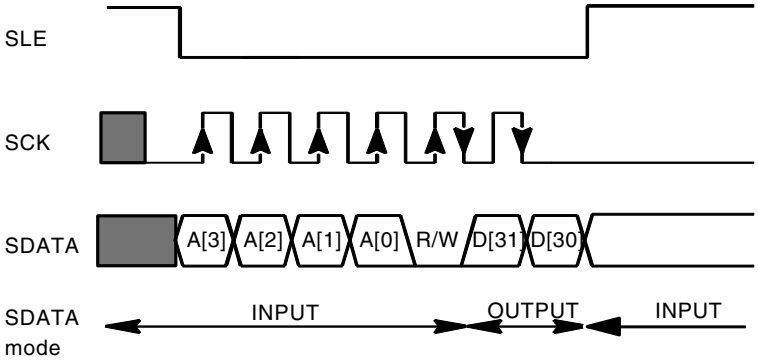


Figure 29. Read Chronogram: partial read cycle, reading 2 bits

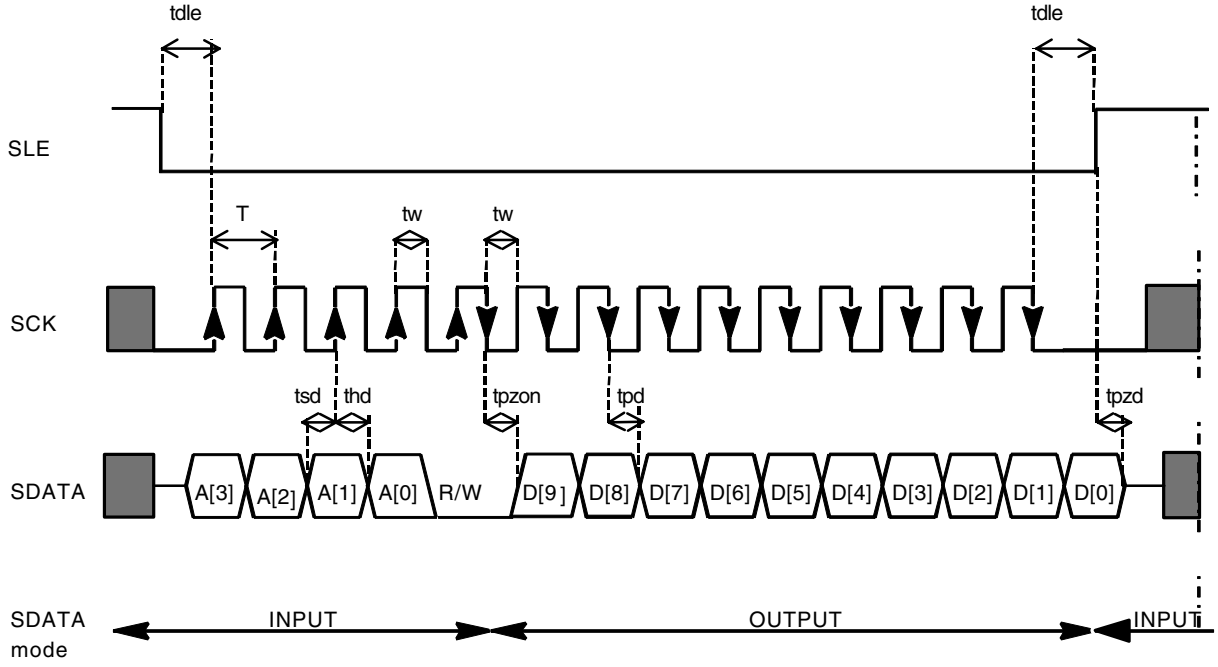


Timings

Table 1. Timing table

Name	Description	Min	Max	Unit
F	SCK frequency	0	5	MHz
T	SCK period	200		ns
tw	SCK low or high time	60		ns
tsd	SDATA setup before SCK rising	40		ns
thd	SDATA hold after SCK rising	20		ns
tpd	SDATA output propagation delay after SCK falling (read mode) (CL= 30 pF)	2	50	ns
tpzon	Delay to switch SDATA to output after SCK falling (read mode)	3	50	ns
tdle	Minimum delay between an edge of SLE and an edge of SCK	40		ns
tpzd	Delay to switch SDATA to input (tri-state) after SLE rising (read mode)		40	ns

Figure 30. Chronogram with Timing



Registers

Table 1. Register Table

Name	Address A[3:0]	Nbits	Read-Write	Comments
F0	0000b	32	R-W	F0 Frequency Code
F1	0001b	32	R-W	F1 Frequency Code
F2	0010b	32	R-W	F2 Frequency Code
F3	0011b	32	R-W	F3 Frequency Code
CTRL1	0100b	32	R-W	Main Control Register
STAT	0101b	31	R	Status Register
DTR	0110b	6	R-W	Data Slicer Input Offset Discriminator Adjusting
WUC	0111b	32	R-W	Wake-up Control Register
WUR	1000b	18	R-W	Wake-up Data Rate Register
WUA	1001b	25	R-W	Wake-up Address Register
WUD	1010b	32	R	Wake-up Data Register
RESET	1011b	1	W	Reset
-	1100b			Reserved
-	1101b			Reserved
-	1110b			Reserved
CTRL2	1111b	32	R-W	Control Register (Lock Detect - Clock Recovery)

Reset Register (RESET)

Name	RESET
nbit	0

Writing in this register (0 or 1) triggers an asynchronous reset. This register can only be written.

All registers return to reset state. The chip returns in power-down. So all the following blocks are reset:

- All registers.
- Wake-up function.
- Clock recovery function.

And with the power-down state, reset is applied to the following blocks:

- Synthesizer divider.
- Clock recovery function.
- PLL lock detect.
- “Refstart”: block for detection of ckrefc (clock 10MHz) start: refstart signal after 64 clock period.
- RSSI detection block.
- Discriminator clock (455 kHz).

Control Register (CTRL1)

Name	PDN	RXTX	DATACLK	TXLOCK	PAPDN	WUEN	LNAGSEL	MVCC	TRSSI	HRSSI
nbit	31	30	29	28	27	26	25	24	23-18	17-15
init	0	0	0	1	0	0	0	0	000000	000

Name	TXLVL	TXFS	RXFS	XTALFQ	FSKBW	FSKPOL	DSREF	-	-	-	-
nbit	14-12	11-10	9-8	7	6	5	4	3	2	1	0
init	000	00	00	0	1	1	1	0	0	0	0

Register reset value = 0x 10000270

Name	# of bits	Comments
PDN	1	General power down 0: power down mode; only the serial interface is active 1: AT86RF211 activated reset value: 0
RXTX	1	Reception or transmission selection 0: RX mode 1: TX mode reset value: 0
DATACLK	1	DATA clock recovery selection 0: no signal on DATACLK output pin 1: Clock recovery active: DATACLK activated reset value: 0
TXLOCK	1	Transmission on PLL lock 0: transmission enabled, regardless of the PLL lock status 1: transmission only when the PLL is locked reset value: 1 note: the PLL status is stored in the PLLL bit of the STATUS register
PAPDN	1	Power amplifier power down 0: TX Power Amplifier power down mode 1: TX Power Amplifier activated (only if PDN=1) reset value: 0
WUEN	1	Wake-up function enable 0: wake-up function disabled, whatever the content of the wake-up control registers 1: wake-up function activated, depending on the content of wake-up control registers reset value: 0
LNAGSEL	1	LNA gain selection 0: maximum gain 1: minimum gain reset value: 0
MVCC	1	RSSI or VCC power supply measure selection 0: RSSI voltage measure, value is stored in STAT register: bits MRSSI 1: VCC voltage measure, value is stored in STAT register: bits MVCC reset value: 0
TRSSI	6	RSSI value threshold DATAMSG validated if RSSI ≥ TRSSI + HRSSI (high RSSI level) DATAMSG inhibited if RSSI < TRSSI - HRSSI (low RSSI level) reset value: 000000b
HRSSI	3	RSSI value hysteresis reset value: 000b
TXLVL	3	TX PA output power selection 000b: minimum transmission level 111b: maximum transmission level reset value: 000b
TXFS	1	TX frequency selection 0: F0 & F1 1: F2 & F3 reset value: 0

Name	# of bits	Comments
-	1	reserved
RXFS	2	RX frequency selection 00b: F0 10b: F2 01b: F1 11b: F3 reset value: 10b
XTALFQ	1	crystal frequency 0: 10.245 MHz (when IF1 = 10.7 MHz) 1: 20.945 MHz (when IF1 = 21.4 MHz) reset value: 0
FSKBW	1	Discriminator range 0: ±25 kHz FSK discriminator range 1: ±50 kHz FSK discriminator range reset value: 1
FSKPOL	1	Polarity of demodulated signal choice 0: inverted signal 1: direct signal reset value: 1
DSREF	1	data slicer reference voltage 0: external voltage (SKFILT pin voltage) 1: internal voltage (VDD/2) reset value: 1
-	1	reserved, must be kept to reset value: 0
-	1	reserved, must be kept to reset value: 0
-	1	reserved, must be kept to reset value: 0
-	1	reserved, must be kept to reset value: 0

RSSI and VCC Measurement

Notes:
1. The same ADC is used to measure RSSI or VCC voltage. When the VCC voltage is measured, the RSSI measurement is stopped (previously measured RSSI is kept). This can disturb the reception process (output data validation). So, it is not recommended to measure VCC in reception mode.
2. VCC measurement can not be done when the AT86RF211 is in power-down mode.
3. Description of RSSI measurement with hysteresis mechanism: If the RSSI measure is higher than the high RSSI level, DATAMSG is validated (high RSSI level = TRSSI + HRSSI). If the RSSI measure is lower than the low RSSI level, DATAMSG is inhibited (low RSSI level = TRSSI - HRSSI). Between these two levels, DATAMSG validation depends on the previous measurement.

Example

TRSSI = 32 High RSSI level = 36

HRSSI = 4 Low RSSI level = 28

MRSSI	27	32	35	36	35	32	29	28	27	25
RSSI level	NOK	NOK	NOK	OK	OK	OK	OK	OK	NOK	NOK
DATAMSG				valid	valid	valid	valid	valid		

Control Register (CTRL2)

Name	DATARATE	DATATOL	LDCK	N0LD1	N1LD2
nbit	31-18	17-10	9	8-5	4-0
init	0x0000 (14bits)	0x00 (8 bits)	0	0010b	10111b

Register reset value = 0x 00000057

Name	# of bits	Comments
DATARATE	14	Received DATAMSG rate This value must be programmed to have the DATACLK activated. (selected with DATACLK bit in CTRL1 register). Value from 1 kbps to 50 kbps reset value: 0x0000
DATATOL	8	Tolerance for DATACLK, clock recovery Advisable value = 2% of the rate. reset value: 0x00
LDCK	1	Clock frequency doubled to increase precision of PLL lock detection 0: 10 MHz clock frequency 1: doubled clock frequency reset value: 0
N0LD2	4	PLL unlock condition trigger Advisable values are reset values reset value: 0010b
N1LD2	5	PLL lock condition trigger Advisable values are reset values reset value: 10111b

Clock Recovery Function

The clock recovery function is activated by setting to ‘1’ the DATACLK bit of the CTRL1 register.

The clock recovery function provides on DATACLK pin the data clock, synchronized on the received data flow. The targeted position for the rising edge of the clock is the middle of the data bit. It is then easy for microcontroller to read without synchro troubles.

Clock recovery mechanism is based on the generation of a basic data clock with a period given by DATARATE of CTRL2, with a step of about 100 ns. This basic clock is synchronized on the received data flow with a phase correction step fixed by DATATOL of CTRL2 register (step of about 100 ns too)

So, DATATOL can

- compensate difference between the read data rates from transmitter and receiver (fixed by DATARATE).
- allow fast initial synchronization of data clock, avoiding bit transition times and converge toward the middle of the bit.
- keep the right data rate (no additional and no removed bit) when a noisy data with bad bit transition position arrives.

Best value of DATATOL is a trade-off between these considerations. A typical recommended value of RATETOL is 2% of DATARATE.

If the tolerance is too high, rate value is reached earlier, and the rate value could be unstable (too big step).

If the tolerance is too low, it could be difficult to catch up the DATA and the function could get lost.

Notice that maximum acceptable distance between two data transitions is depending on the precision of DATARATE versus transmitter actual data rate.

Synchronization mechanism is explained with the chronogram below. The synchronization is done for the first bit. In worst case conditions, when data and clock arrive at the same time, it begins at the second bit.

The programmed data rate allows the creation of a basic clock at the programmed DATARATE frequency at the beginning of the reception. Then, the clock is shifted if necessary from the tolerance value, depending on the previous DATA transition: the clock is moved later or sooner, depending on the gap between CLOCK and DATA.

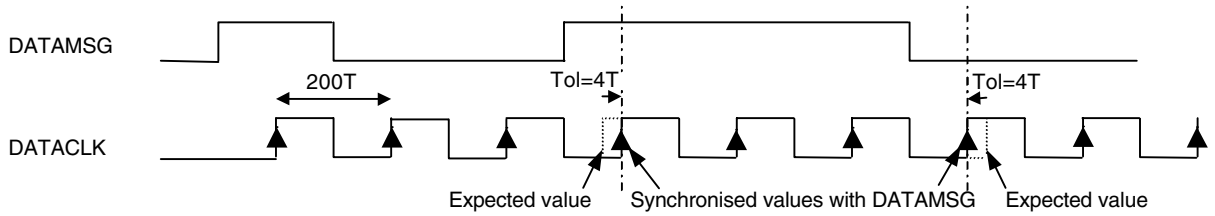
For example:

if DATARATE = 50 kbit/s, which is equivalent to a duration of 200 x T for 1 bit,

with T = 100ns = base clock period.

if DATATOL = 2% x DATARATE = 4 x T.

Figure 31.



DATARATE Programming

This value must be programmed only when the DATA clock is needed on DATACLK output pin of the chip.

The DATA rate can be programmed from 1 kbit/s to 50 kbit/s with 14 bits of CTRL2 register.

DATARATE is the period of the data rate and can be programmed with a resolution given by the crystal oscillator period:

- 10.245 MHz oscillator, period = T = 97.6 ns
- 20.945 MHz oscillator, period = T = 95.5 ns

Some rate value with the 10.245 MHz oscillator given for example:

DATARATE[13:0]	Rate	Period
0d205	50 kbps	1 bit ~ 205 x T
0dvv	……	1 bit ~ vv x T
0d534	19.2 kbps	1 bit ~ 534 x T
0d1024	10 kbps	1 bit ~ 1024 x T
0d1067	9.6 kbps	1 bit ~ 1067 x T
0d2135	4.8 kbps	1 bit ~ 2135 x T
0d4269	2.4 kbps	1 bit ~ 4269 x T
0d10246	1 kbps	1 bit ~ 10246 x T

DATATOL Programming

The tolerance for the extraction of DATA rate must be nearly 2% of the RATE. The tolerance represents the step for the calculation of the rate.

If the tolerance is too high, rate value is reached earlier but the rate value could be unstable (step too big).

If the tolerance is too low, it could be difficult to catch up the DATA and the clock recovery could get lost.

Some tolerance values given for example, with tolerance = 2% x DATARATE:

DATATOL[7:0]	Rate	Period
0d4	50 kbps	1 bit ~ 4 x T
0dvv	……	1 bit ~ vv x T
0d20	10 kbps	1 bit ~ 20 x T
0d21	9.6 kbps	1 bit ~ 21 x T
0d43	4.8 kbps	1 bit ~ 43 x T
0d85	2.4 kbps	1 bit ~ 85 x T
0d205	1 kbit/s	1 bit ~ 205 x T

PLL Lock Detect

The PLL lock function uses UP and DOWN signal from internal phase detector. This signal are analyzed synchronously with a clock frequency, depending of LDCK bit programming (0 MHz or 20 MHz sampling).

LDCK is set to ‘1’ to double the clock frequency of the function PLL lock detect, to increase the precision of the function.

N0LD2 triggers the unlock condition of the PLL.

N0LD2 = number of consecutive edges of the sampling clock with UP and DOWN active before considering PLL unlocked.

This value must not be set to 0 or 1. The recommended value is default value, i.e. 2.

N1LD2 triggers the lock condition of the PLL.

N1LD2 = number of cycle at the PLL reference frequency, without any unlock condition before considering PLL locked.

This value must not be set to 0.

It is recommended to use default values indicated in the table.

Frequency Registers

Name	F0, F1, F2, F3
nbit	31-0

Name	# of bits	Comments
F0	32	Frequency code value F0 default register in TX mode (ZERO code in FSK modulation). reset value: 433.3 MHz.
F1	32	Frequency code value F1 default register in TX mode (ONE code frequency in FSK modulation). reset value: 433.4 MHz
F2	32	Frequency code value F2 default register in RX mode. reset value: 444 MHz
F3	32	Frequency code value F3 reset value: 422 MHz

Frequency Registers Selection

The frequency register selection depends on the control register programming and on the DATAMSG pin:

RXTX	RXFS	TXFS	DATAMSG	Mode
0	00	X	X	Receive - F0
0	01	X	X	Receive - F1
0	10	X	X	Receive - F2
0	11	X	X	Receive - F3
1	XX	0	0	Transmit - F0-F1
1	XX	0	1	Transmit - F0-F1
1	XX	1	0	Transmit - F2-F3
1	XX	1	1	Transmit - F2-F3

In reception mode, only one frequency needs to be programmed. In transmission mode, two different registers (F0 & F1, or F2 & F3) must be programmed for “0” code and “1” code transmission. The DATAMSG pin value actually selects the used register. The four registers can also be set to define two channels, so that the AT86RF211 may switch quickly from a channel to the other.

Mode	Programmed Frequency
RX	FCHANNEL ± IF1
TX	FCHANNEL ± deviation

Example:

FCHANNEL = 868.3 MHz
IF1 = 10.7 MHz
deviation = 4 kHz

Mode	FSK
RX	868.3 ± 10.7 = 879 MHz or 857.6 MHz
TX	868.3 ± 0.004 = 868.304 MHz when DATAMSG = “1” and 868.296 MHz when DATAMSG = “0”

Notes:
1. In reception mode, one of the two frequencies (879 MHz or 857.6 MHz) can be chosen, taking into account external parameters (for example, the noise in one of the two channels).
2. Two frequencies are used to transmit data: 868.304 MHz for ‘1’ transmission and 868.296 MHz for ‘0’ transmission. The polarity of DATAMSG can be swapped using bit 5 of CTRL1.

Status register (STATUS)

The STATUS register is used to read the status of internal functions (including the wake-up function) or the output value of the internal ADC. This register can only be read.

Name	PLLL	MRSSI	MVCC	WAKEUP	-	MSGERR
nbit	30	29-24	23-18	17	16	15

Name	MSGDATL	MSGMRATE
nbit	14-10	9-0

Name	# of bits	Comments
PLLL	1	PLL Lock flag 0: PLL unlocked 1: PLL locked reset value: 0
MRSSI	6	Measured RSSI level reset value: 0x00
MVCC	6	Measured VCC power supply voltage reset value: 0x00
WAKEUP	1	WAKEUP flag Copy of the WAKEUP pin, but not affected by polarity selection. 0: no wake-up message received 1: wake-up message received reset value: 0
-	1	reserved reset value: 0
MSGERR	1	Wake-up message error in test message mode 0: no error detected in the received message 1: message received with error reset value: 0
MSGDATL	5	Wake-up message data length length of the data stored in WUD (received message). reset value: 0
MSGMRATE	10	Wake-up message measured data rate bit period extracted from message header of the wake-up message. measured as a multiple of 1.56 ms (like RATE in WUR register). 0: 1 x 1.56 µs vvx: vv x 1.56 µs 3ffx: 1024 x 1.56 µs reset value: 0x000

DTR Register

The DTR register allows the user to precisely adjust the offset of the data slicer input.

Name	DSOFFSET[3:0]	-	-
nbit	5-2	1	0
init	1000	0	0

Register reset value = 0 x 20

Name	# of bits	Comments
DSOFFSET	4	Input data slicer offset tuning 0000 to 1111 reset value: 1000b
-	1	reserved
-	1	reserved

This offset leads to a difference between the width of ‘1’ and ‘0’ at DATAMSG. So, this parameter needs to be optimized in order to obtain maximum performance in reception.

Note: this adjustment is to be done only once for each AT86RF211. A good criteria to reach the right value is to increase from 0000 to 1111, and find the best performance for BER or find a equal width for a ‘1’ and for a ‘0’.

Wake-up Control Register (WUC)

Name	WUE	DATA	STOP	DATL	ADD	-	WPER	WL1
nbit	31	30	29	28-24	23	22	21-13	12-6
init	0	1	1	11111b	1	0	001011111b	0000100b

Name	WL2	ISTU	-	-
nbit	5-3	2	1	0
init	010b	0	0	0

Register reset value = 0x 7F8BE110

Name	# of bits	Comments
WUE	1	Wake-up function enable Returns to “0” when a valid message is received. 0: wake-up disable 1: wake-up enable reset value: 0
DATA	1	Data content 0: message without data field 1: message with data field reset value: 1
STOP	1	STOP field usage 0: fixed data length: data length set from 1 to 32 by DATL 1: variable data length: data length given by the STOP field location; DATL must be set to 11111b. reset value: 1
DATL	5	Data length Valid in fixed data length mode (STOP = 0). 00000b: 1 bit (min data length value) ---------- 11110b: 31 bits 11111b: 32 bits (max data length value) reset value: 11111b
ADD	1	Address content 0: message without address field 1: message with address field reset value: 1
MSGTST	1	Message error test 0: no error detection mode 1: error detection enabling for debugging reset value: 0
WPER	9	Wake-up period Variable from 10 ms to 328 s with an accuracy of ±20%.(on-chip RC oscillator) reset value: 960 ms reset value: 0x5F
WL1	7	Minimum delay before TEST1 (check of RSSI level) Variable from 1ms to 1.024 s. Delay calculation starts when the reference oscillator starts. reset value: 5ms reset value: 0x04

Name	# of bits	Comments
WL2	3	Minimum delay between TEST 1 and TEST 2 (check of header detection) Variable as multiple of WL1 from 0 to 31 x WL1. reset value: 2 x WL1 reset value: 0x2
ISTU	1	Inhibit stuff mechanism 0: stuff is used for wake-up message. 1: no stuff used in the wake-up message. reset value: 0
-	2	reserved, must be kept to reset value reset value: 00

WPER Programming

WPER can be set from 10 ms to 328 s with an accuracy of ±20%.

A 10 ms period clock is used for this period generation.

Bit 8 and 7 give a period multiplication factor of 1, 16 or 256 (with two serial by 16 clock prescalers).

Bit 6 to 0 give the number of cycles of the divided clock from 1 to 128 (counter).

WPER[8:0]	WPER[8:7]	WPER[6:0]	Period	Prescaler	Comments
0x000	00b	0x00	10 ms	1	1 x 10 ms
0x001	00b	0x01	20 ms	1	2 x 10 ms
–	00b	0xvv	–	–	(vv +1) x 10 ms
0x07e	00b	0x7e	1270 ms	1	1 x 1270 ms
0x07f	00b	0x7f	1280 ms	1	1 x 1280 ms
0x100 or 0x080	10b or 01b	0x01	170 ms	16	((16 x 1)+1) x 10 ms
0x101 or 0x081	10b or 01b	0x02	330 ms	16	((16 x 2)+1) x 10 ms
–	10b or 01b	0xvv	–	–	((16 x vv)+1) x 10 ms
0x17e or 0x0fe	10b or 01b	0x7e	20.2 s	16	((16 x 126)+1) x 10 ms
0x17f or 0x0ff	10b or 01b	0x7f	20.3 s	16	((16 x 127)+1) x 10 ms
0x180	11b	0x01	2.57 s	256	((256 x 1)+1) x 10 ms
0x181	11b	0x02	5.13 s	256	((256 x 2)+1) x10 ms
–	11b	0xvv	–	–	((256 x vv) +1) x 10 ms
0x1fe	11b	0x7e	323 s	256	((256 x 126)+1) x 10 ms
0x1ff	11b	0x7f	325 s	256	((256 x 127)+1) x 10 ms

WL1 Programming

WL1 can be set from 1 ms to 1.024 s.

A 1 ms period clock is used for this delay generation.

Bit 6 give a period multiplication factor of 1 or 16 (by 16 clock prescaler).

Bit 5 to 0 give the number of cycles of the divided clock from 1 to 64 (counter).

WL1[6:0]	WL1[6]	WL1[5:0]	Period	Prescaler	Comments
0x00	0	0x00	1 ms	1	1 x 1 ms
0x01	0	0x01	2 ms	1	1 x 2 ms
0xvv	0	0xvv	0xvv + 1 ms	1	1x (vv +1) ms
0x3e	0	0x3e	63 ms	1	1 x 63 ms
0x3f	0	0x3f	64 ms	1	1 x 64 ms
0x40	1	0x00	16 ms	16	16 x 1 ms
0x41	1	0x01	32 ms	16	16 x 2 ms
–	1	0xvv	–	16	16 x (vv +1) ms
0x7e	1	0x3e	1.008 s	16	16 x 63 ms
0x7f	1	0x3f	1.024 s	16	16 x 64 ms

WL2 programming

WL2 can be set as a multiple of WL1 from 0 to 31 WL1.

WL2[2:0]	Period	Comments
000	0	Simultaneous TEST 1 and TEST2
001	1 x WL1	
010	2 x WL1	
011	3 x WL1	
100	4 x WL1	
101	8 x WL1	
110	16 x WL1	
111	31 x WL1	

Wake-up Data Rate Register (WUR)

Name	WUOP	RATECHK	RATE	RATETOL
nbit	17-16	15	14-5	4-0
init	01	0	0000010000b	01000b

Name	# of bits	Comments
WUOP	2	WAKEUP output polarity 00b: WAKEUP pin active low 01b: WAKEUP pin active high 1Xb: WAKEUP pin open drain (active low, inactive tristate) reset value: 01b
RATECHK	1	Data rate check the data rate is automatically extracted from the HEADER field. the data rate can be compared to RATE with a tolerance of plus or minus RATETOL. Data rate is computed from a unit of 1.56 ms (Reference clock divided by 16). 0: data rate not checked. 1: data rate check done (header ignored if check fails). reset value: 0
RATE	10	Data rate value 0d: min value = 1 x 1.56 µs 1023d: max value = 1024 x 1.56 µs reset value: 64x1.56 ms reset value: 64d
RATETOL	5	Data rate tolerance 0d: min value = 0 x 1.56 µs 31d: max value = 31 x 1.56 µs reset value: 8x1.56 ms reset value: 8d

The data rate (in bps) and the decimal value to be coded in the register are related by the equation:

$$RATE = \frac{640000}{\text{rate (bps)}}$$

The following table gives the programming values of commonly used rates:

Rate	WUR RATE
1200 bits/s	533d
2400 bits/s	267d
4800 bits/s	133d
9600 bits/s	67d

Wake-up Address Register (WUA)

Name	ADDL	ADD
nbit	24-20	19-0
init	01001	0x0F0F0

Name	nb of bits	Comments
ADDL	5	Wake-up address length 0d: wake-up address length = 1 bit 1d: wake-up address length = 2 bits ..... 19d: wake-up address length = 20bits >19d: forbidden reset value: 10 bits
ADD	20	Wake-up address If wake-up address length is less than 20 bits, MSB bits are ignored reset value: 0x0f0f0

Concerning this register, attention should be paid on the fact that the last bit of the address field is not taken into account and that an extra unused bit must be added in order that the whole address is used.

Wake-up Data Register (WUD)

Name	WUD
nbit	(data length -1) - 0

Name	# of bits	Comments
WUD	length	Wake-up message data Warning: The length of this register is variable: * case fixed data length (STOP=0 of WUC) data length is given by DATL of WUC. * case variable data length (STOP=1 of WUC) data length is given by MSGDATL of STAT register. Warning: The first bit of received data is the LSB: WUD[0].

Functional Modes

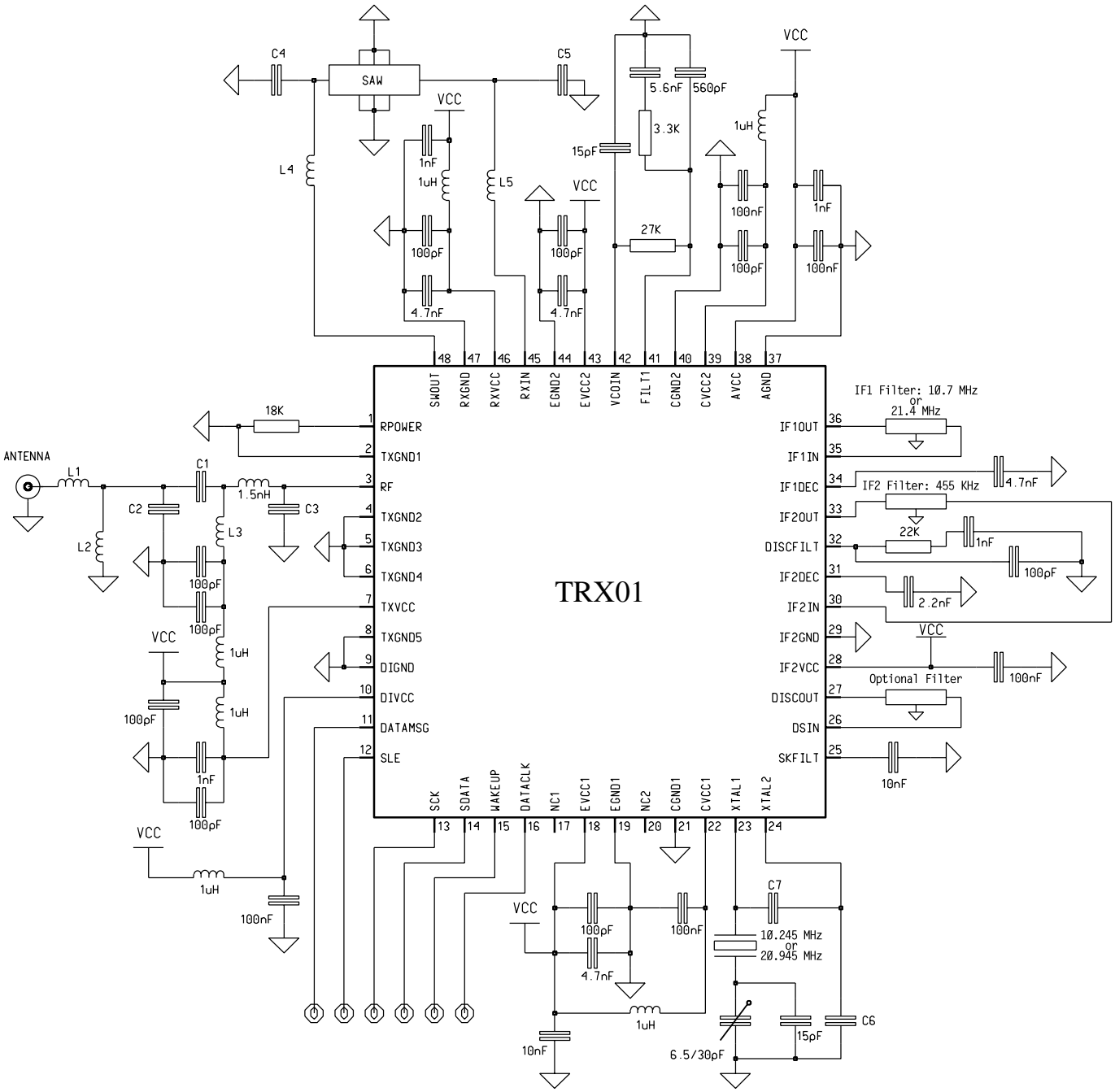
The following table describes the main functional modes of the AT86RF211, and the corresponding values of the main control register bits.

PDN	PAPDN	RXTX	WUEN	WUE	Mode	Sub-mode
0	X	X	0	X	Power Down	No Activity
0	X	X	1	0		Wake Up Can Be Activated
0	0	0	0	0	Initial State	After Reset
1	0 1	1	X	X	Transmit	PA off PA on
1	X	0	0	X	Receive	
1	X	0	1	0	Receive	
0	X	0	1	1	Wake-up	

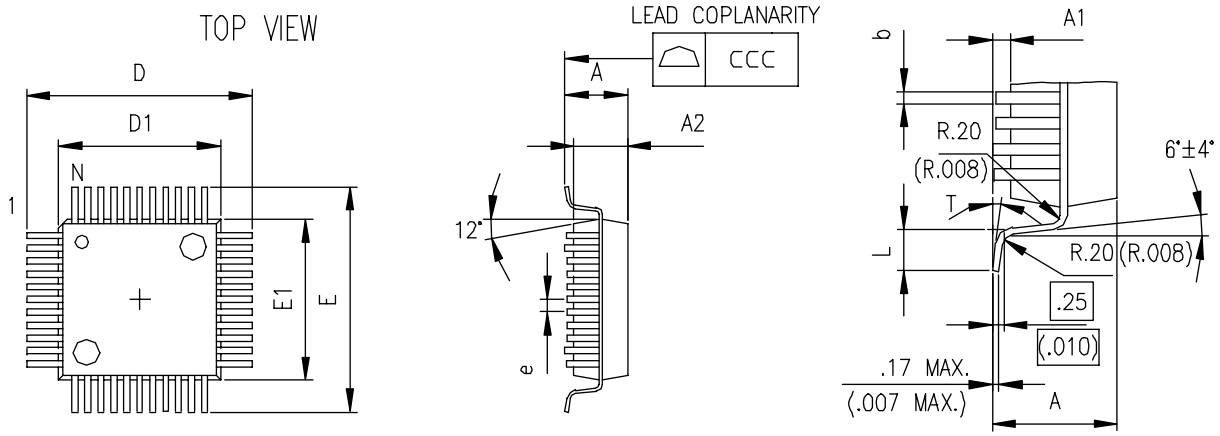
Functional Mode Description

- Power down mode: in the power-down mode, all the functions of the chip are disabled (including the power amplifier: the priority of PDN is greater than the priority of PDNPA). In this mode, the power consumption is minimum. Only the serial interface is active and the registers can be monitored.
  The initial state is the state of the chip after a general reset (write in the RESET register). It is the default value of the control register's bits when no programming has been done.
- Transmission mode: in this configuration, the AT86RF211 is a transmitter. The Power Amplifier (PA) can be on or off, controlled by PDNPA.
- Reception mode: in this configuration, the AT86RF211 is a receiver. With WUEN=1, WUE=0, the chip stays in reception mode.
- Wake-up mode: in power-down mode, the AT86RF211 can be placed in a "sleep" mode. In this mode, the AT86RF211 periodically scans the RF signal, waiting for a particular message. The wake-up function is activated, depending on the programmed wake-up parameters in the wake-up registers.

Typical Application Implementation



Package Information: 48-lead TQFP



Dimension	Nominal Value (mm)	Tolerance
A	1.60	max
A1	0.05 min / 0.15 max	
A2	1.40	±0.05
D	9.00	±0.20
D1	7.00	±0.10
E	9.00	±0.20
E1	7.00	±0.10
L	0.60	+0.15 / -0.10
e	0.50	basic
b	0.22	±0.05
ccc	0.08	max

Dimension	Nominal Value (inch)	Tolerance
A	0.063	max
A1	0.002 min / 0.06 max	
A2	0.055	±0.002
D	0.354	±0.008
D1	0.275	±0.004
E	0.354	±0.008
E1	0.275	±0.004
L	0.024	+0.006 / -0.004
e	0.020	basic
b	0.009	±0.002
ccc	0.003	max

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