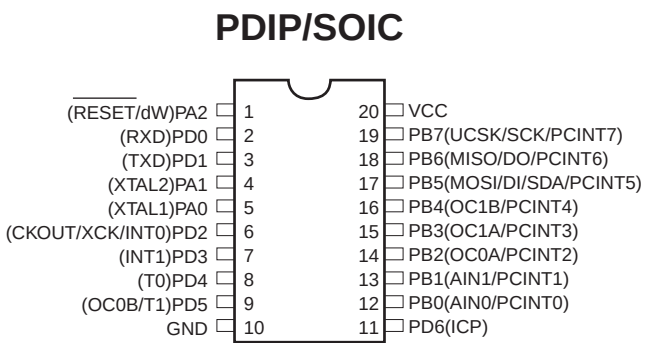
- AVR® RISC
- AVR – RISC
  - 120 –
  - 32 8
  -
  - 20 MHz 20 MIPS
-
  - 2K Flash
    : 10,000
  - 128 EEPROM
    : 100,000
  - 128 SRAM
  - EEPROM
-
  - 8 /
  - 16 /
  - PWM
  -
  -
  - USI –
  - USART
-
  - debugWIRE
  - SPI
  - /
  - Standby
  -
  -
  -
- I/O
  - 18 I/O
  - 20 PDIP, 20 SOIC 32 MLF
-
  - 1.8 - 5.5V (ATtiny2313V)
  - 2.7 - 5.5V (ATtiny2313)
-
  - ATtiny2313V: 0 - 4 MHz @ 1.8 - 5.5V, 0 - 10 MHz @ 2.7 - 5.5V
  - ATtiny2313: 0 - 10 MHz @ 2.7 - 5.5V, 0 - 20 MHz @ 4.5 - 5.5V
-
  - :
    1 MHz, 1.8V: 300 µA
    32 kHz, 1.8V: 20 µA ( )
  - :
    < 0.2 µA at 1.8V

2KB Flash 8 AVR®

ATtiny2313/V

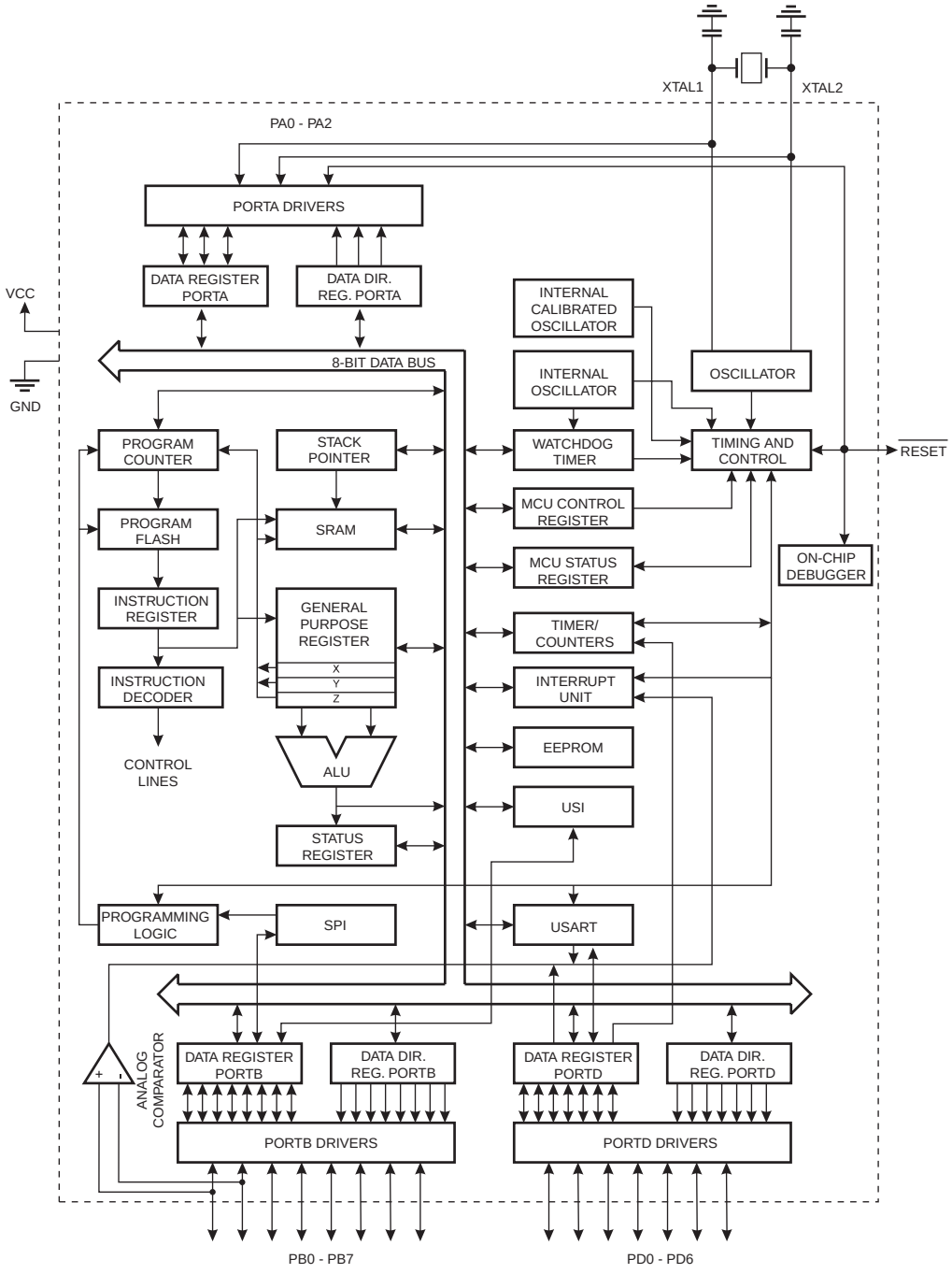
Rev. 2543F–AVR–07/04

Figure 1. ATtiny2313



ATtiny2313 AVR RISC 8 CMOS
ATtiny2313 1 MIPS/MHz

Figure 2.


XTAL1
XTAL2
PA0 - PA2
PORTA DRIVERS
DATA REGISTER PORTA
DATA DIR. REG. PORTA
VCC
GND
8-BIT DATA BUS
INTERNAL CALIBRATED OSCILLATOR
INTERNAL OSCILLATOR
OSCILLATOR
PROGRAM COUNTER
STACK POINTER
WATCHDOG TIMER
TIMING AND CONTROL
RESET
PROGRAM FLASH
SRAM
MCU CONTROL REGISTER
MCU STATUS REGISTER
ON-CHIP DEBUGGER
INSTRUCTION REGISTER
GENERAL PURPOSE REGISTER
X
Y
Z
TIMER/ COUNTERS
INSTRUCTION DECODER
INTERRUPT UNIT
CONTROL LINES
ALU
EEPROM
USI
STATUS REGISTER
PROGRAMMING LOGIC
SPI
USART
ANALOG COMPARATOR
DATA REGISTER PORTB
DATA DIR. REG. PORTB
DATA REGISTER PORTD
DATA DIR. REG. PORTD
PORTB DRIVERS
PORTD DRIVERS
PB0 - PB7
PD0 - PD6

AVR 32
(ALU)
CISC 10

ATtiny2313 2K Flash 128 EEPROM 128 SRAM 18
I/O 32 2
/ / USART

CPU SRAM T/C
Standby

Atmel SPI
8 RISC CPU
Flash ATtiny2313

ATtiny2313 AVR C
/

VCC

GND

A(PA2..PA0)	A	3	I/O

A

A P51

B(PB7..PB0)	B	8	I/O

B

B P51

D(PD6..PD0)	D	7	I/O

D

D P54

RESET

P32Table 15 PA2 dW

XTAL1 XTAL1 PA0

XTAL2 XTAL2 PA1

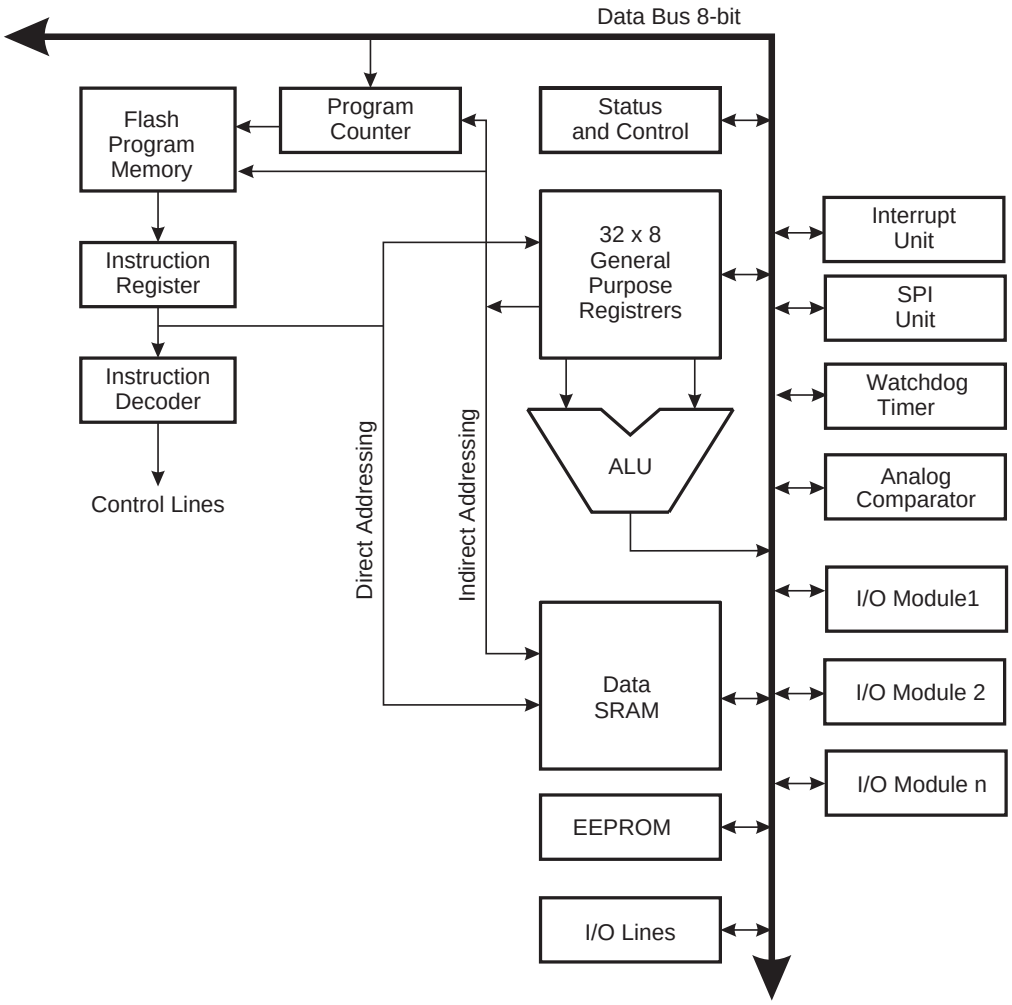
C

C

AVR

AVR CPU

Figure 3. AVR



AVR Harvard
CPU

( )
Flash

32 8
ALU ALU

6 3 16

16 X Y Z

ALU ALU

/
16 16 32

(PC)
SRAM SRAM
SP I/O SRAM 5

AVR

AVR I/O

I/O 64 CPU I/O
0x20 - 0x5F

ALU

AVR ALU 32
ALU ALU 3
/

ALU

AVR SREG

Bit	7	6	5	4	3	2	1	0	
	I	T	H	S	V	N	Z	C	SREG
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

- **Bit 7 – I:**

I I

I RETI

I I SEI CLI

- **Bit 6 – T:**

BLD BST T BST T

BLD T

- **Bit 5 – H:**

H BCD

- **Bit 4 – S: , S = N ⊕ V**

S N 2 V

- **Bit 3 – V: 2**

2

- **Bit 2 – N:**

- **Bit 1 – Z:**

- **Bit 0 – C:**

AVR RISC

/

- 8 8
- 8 8
- 8 16
- 16 16

Figure 4 CPU 32

Figure 4. AVR CPU

7 0	Addr.
R0	0x00
R1	0x01
R2	0x02
…	
R13	0x0D
R14	0x0E
R15	0x0F
R16	0x10

R17	0x11	
…		
R26	0x1A	X
R27	0x1B	X
R28	0x1C	Y
R29	0x1D	Y
R30	0x1E	Z
R31	0x1F	Z

Figure 4
32 SRAM
X Y Z

X Y Z R26..R31
Figure 5

Figure 5. X Y Z

/

AVR

SRAM

0x60 PUSH

POP RET RETI

AVR I/O 8

AVR SPL SPH

Bit	15	14	13	12	11	10	9	8	
	–	–	–	–	–	–	–	–	SPH
	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SPL
	7	6	5	4	3	2	1	0	
/	R	R	R	R	R	R	R	R	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

AVR CPU clk_{CPU}

Figure 6 Harvard

1 MIPS/MHz

/ /

Figure 6.

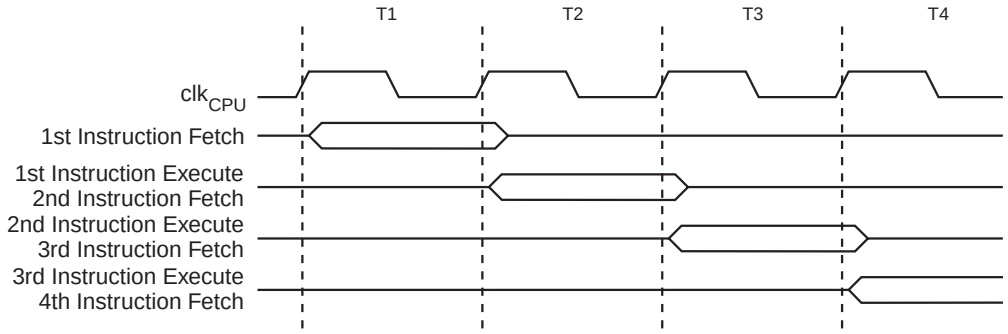
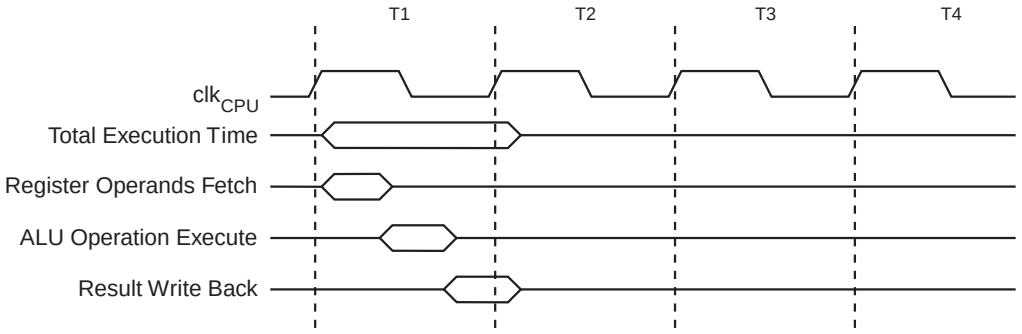


Figure 7 ALU

Figure 7. ALU



AVR

I

P42“ ”
RESET
INT0 – 0 P42“ ”

I

I

RETI I

”1”

"0"

I

AVR

CLI CLI

CLI CLI
EEPROM

EEPROM

```
in  r16, SREG     ;     SREG
cli    ;
sbi EECR, EEMWE   ;     EEPROM
sbi EECR, EEWE
out SREG, r16     ;     SREG (I   )
```

C

```
char cSREG;
cSREG = SREG; /*     SREG    */
/*         */
__disable_interrupt();
EECR |= (1<<EEMWE); /*     EEPROM      */
EECR |= (1<<EEWE);
SREG = cSREG; /*     SREG (I   )*/
```

SEI

```
sei   ;
sleep ;
;     :                       MCU
```

C

```
_SEI(); /*                  */
_SLEEP(); /*                      */
/*     :                       MCU                */
```

AVR 4 4
4 PC
3
MCU MCU
4

4 PC( )
SREG I

AVR ATtiny2313

ATtiny2313 AVR
ATtiny2313 EEPROM

Flash

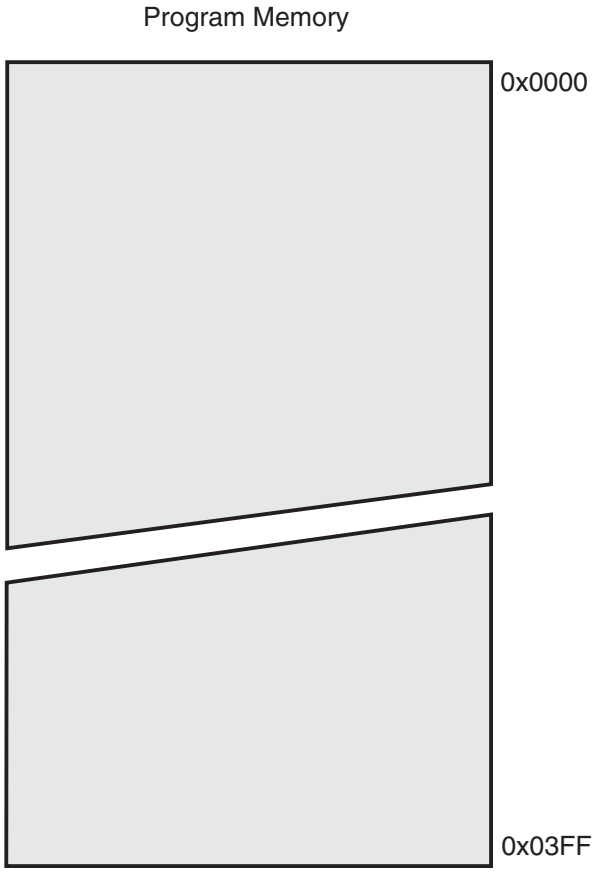
ATtiny2313 2K Flash
AVR 16 32 Flash 1K x 16

Flash 10,000 ATtiny2313 (PC) 10
1K P150“ ” SPI Flash

(LPM)

P10“ ”

Figure 8.



SRAM

Figure 9 ATtiny2313 SRAM

224 I/O I/O SRAM
32 64 I/O 128 SRAM

5

R26 R31

Y Z 63

X Y Z

ATtiny2313 32 64 I/O 128 SRAM
P8“ ”

Figure 9.

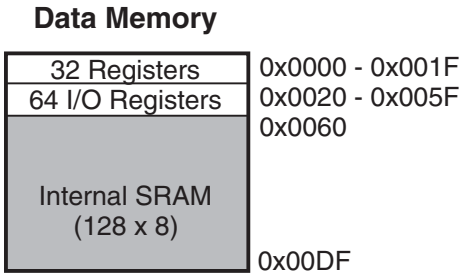
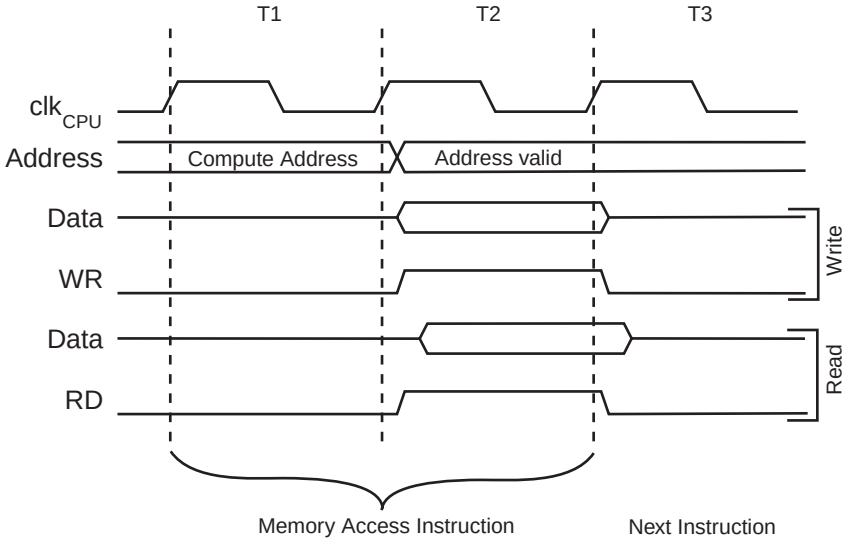


Figure 10 SRAM

clk_{CPU}

Figure 10. SRAM



EEPROM

ATtiny2313 128 EEPROM
EEPROM 100,000 EEPROM
EEPROM

EEPROM /

EEPROM I/O

EEPROM Table 1
EEPROM
/ V_{CC} / CPU
P19 “ EEPROM ” EEPROM

EEPROM EEPROM

EEPROM CPU 4
EEPROM CPU 2

EEPROM

Bit	7	6	5	4	3	2	1	0	
	–	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	EEAR
/	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	X	X	X	X	X	X	X	

- **Bit 7 – Res:**

- **Bits 6..0 – EEAR6..0: EEPROM**

EEPROM EEARL 128 EEPROM EEPROM
0 127 EEAR EEPROM

EEPROM EEDR

Bit	7	6	5	4	3	2	1	0	
	MSB							LSB	EEDR
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

- **Bits 7..0 – EEDR7..0: EEPROM**

EEPROM EEDR EEAR EEDR
EEARL

EEPROM EECR

Bit	7	6	5	4	3	2	1	0	
	–	–	EEPM1	EEPM0	EERIE	EEMPE	EEPE	EERE	EECR
/	R	R	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	X	X	0	0	X	0	

- **Bits 7..6 – Res:**

- **Bits 5, 4 – EEPM1 EEPM0: EEPROM**

EEPE
( ) Table 1
EEPE EEPMn EEPROM
EEPMn 0b00

Table 1. EEPROM

EEPM1	EEPM0		
0	0	3.4 ms	
0	1	1.8 ms	
1	0	1.8 ms	
1	1	–	

- **Bit 3 – EERIE: EEPROM**

SREG I "1" EERIE EEPROM EERIE
EEPROM

- **Bit 2 – EEMPE: EEPROM**

EEMPE EEPE "1”

EEMPE "1" EEPE EEPROM
EEMPE "0“ EEPE EEMPE "1”

- **Bit 1 – EEPE: EEPROM**

EEPE EEPROM EEPE "1" EEPMn
EEPROM EEPE "1" EEMPE "1" EEPROM
EEPE EEPE CPU

- **Bit 0 – EERE: EEPROM**

EERE EEPROM EEPROM EERE
EEARL EEPROM EEPROM
CPU 4 EEPROM
EEPE EEPROM EEAR

EEPROM
EEARL EEDR EEPMn EEPE (
EEMPE) /
Table 1 EEPE
EEPROM

(
)
( )

EEARL EEPMn 0b01 EEPE (EEMPE
) (Table 1) EEPE
EEPROM

EEARL EEDR EEPMn 0b10 EEPE
(EEMPE) (Table 1)
EEPE
EEPROM

EEPROM P25“ OSCCAL”

C EEPROM

```
EEPROM_write:
  ;
  sbic EECR,EEPE
  rjmp EEPROM_write
  ;
  ldi  r16, (0<<EEPM1)|(0<<EEPM0)
  out  EECR, r16
  ;            r17
  out EEARL, r17
  ;                (r16)
  out EEDR,r16
  ;    EEMWE
  sbi EECR,EEMWE
  ;    EEWE
  sbi EECR,EEWE
  ret
```

C

```
void EEPROM_write(unsigned char ucAddress, unsigned char ucData)
{
  /*                */
  while(EECR & (1<<EEPE))
    ;
  /*          */
  EECR = (0<<EEPM1)|(0>>EEPM0)
  /*                */
  EEARL = ucAddress;
  EEDR = ucData;
  /*    EEMWE */
  EECR |= (1<<EEMWE);
  /*    EEWE          */
  EECR |= (1<<EEWE);
}
```

C EEPROM

```
EEPROM_read:
  ;
  sbic EECR,EEPE
  rjmp EEPROM_read
  ;            r17
  out  EEARL, r17
  ;     EERE
  sbi  EECR,EERE
  ;
  in   r16,EEDR
  ret
```

C

```
unsigned char EEPROM_read(unsigned char ucAddress)
{
  /*                */
  while(EECR & (1<<EEPE))
    ;
  /*             */
  EEARL = ucAddress;
  /*     EERE          */
  EECR |= (1<<EERE);
  /*                */
  return EEDR;
}
```

EEPROM

CPU EEPROM EEPROM ( ) EEPROM

EEPROM EEPROM CPU

EEPROM

AVR RESET BOD BOD

I/O

ATtiny2313 I/O P202“ ”

ATtiny2313 I/O I/O I/O LD/LDS/LDD ST/STS/STD 32 I/O 0x00 - 0x1F I/O SBI CBI SBIS SBIC IN OUT 0x00 - 0x3F SRAM LD ST I/O 0x20

"0" I/O

"1" AVR

CBI SBI

CBI SBI 0x00 0x1F

I/O

I/O ATtiny2313 3 I/O

0x00 - 0x1F I/O SBI CBI

SBIS SBIC

I/O 2

GPIOR2

Bit	7	6	5	4	3	2	1	0	
	MSB							LSB	GPIOR2
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

I/O 1

GPIOR1

Bit	7	6	5	4	3	2	1	0	
	MSB							LSB	GPIOR1
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

I/O 0

GPIOR0

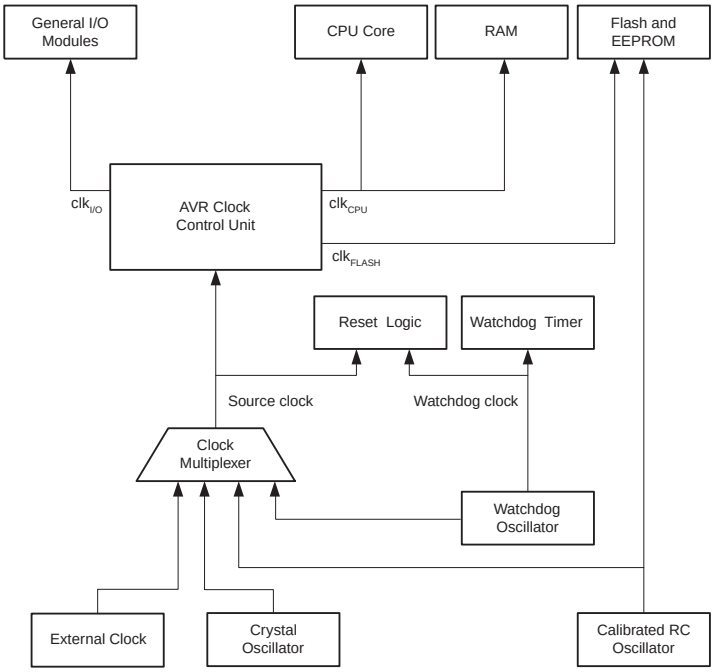
Bit	7	6	5	4	3	2	1	0	
	MSB							LSB	GPIOR0
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

Figure 11 AVR

P29“

” Figure 11

Figure 11.



CPU **clk_{CPU}** CPU AVR
CPU

I/O **$clk_{I/O}$** I/O I/O / USART I/O
I/O
$clk_{I/O}$ USI
USI

Flash **clk_{FLASH}** Flash Flash CPU

ATtiny2313 Flash AVR

Table 2. (1)

	CKSEL3..0
	0000
4MHz RC	0010
8MHz RC	0100

Table 2. (1)

	CKSEL3..0
	0000
128kHz	0110
	1000 - 1111
	0001/0011/0101/0111

Note: 1. “1” “0”

CPU

CPU

MCU

WDT

Table 3 P171“ATtiny2313 ”

Table 3.

(V_{CC} = 5.0V)	(V_{CC} = 3.0V)	
4.1 ms	4.3 ms	4K (4,096)
65 ms	69 ms	64K (65,536)

CKSEL = “0010” SUT = “10” CKDIV8

RC 8

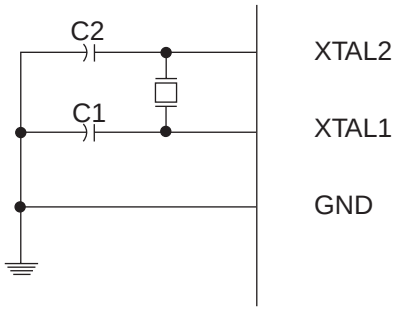
ISP

XTAL1 XTAL2 P22Figure 12

C1 C2

P23Table 4

Figure 12.



CKSEL3..1 Table 4

Table 4.

CKSEL3..1	(1) (MHz)	C1 C2 (pF)
100(2)	0.4 - 0.9	–
101	0.9 - 3.0	12 - 22
110	3.0 - 8.0	12 - 22
111	8.0 -	12 - 22

Notes: 1.
2.

Table 5 CKSEL0 SUT1..0

Table 5.

CKSEL0	SUT1..0		(V_{CC} = 5.0V)	
0	00	258 CK(1)	14CK + 4.1 ms	
0	01	258 CK(1)	14CK + 65 ms	
0	10	1K CK(2)	14CK	BOD
0	11	1K CK(2)	14CK + 4.1 ms	
1	00	1K CK(2)	14CK + 65 ms	
1	01	16K CK	14CK	BOD
1	10	16K CK	14CK + 4.1 ms	
1	11	16K CK	14CK + 65 ms	

Notes: 1.

2.

RC

RC 8.0 MHz 3V 25°C
CKDIV8
8 CKDIV8
Table 6 CKSEL
OSCCAL RC 3V 25°C
± 10% www.atmel.com/avr
± 2%

P152“ ”

Table 6. RC

CKSEL3..0	
0010 - 0011	4.0 MHz(1)
0100 - 0101	8.0 MHz

Note: 1.

SUT Table 7

Table 7. RC

SUT1..0		(V_{CC} = 5.0V)	
00	6 CK	14CK	BOD

Table 7. RC

SUT1..0		(V_{CC} = 5.0V)	
01	6 CK	14CK + 4.1 ms	
10(1)	6 CK	14CK + 65 ms	
11			

Note: 1.

OSCCAL

Bit	7	6	5	4	3	2	1	0	
	–	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	OSCCAL
/	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- **Bits 6..0 – CAL6..0:**

OSCCAL
0x7F
EEPROM Flash EEPROM Flash
10% 8.0/4.0 MHz
Table 8
MCU RC
2% OSCCAL 0x20

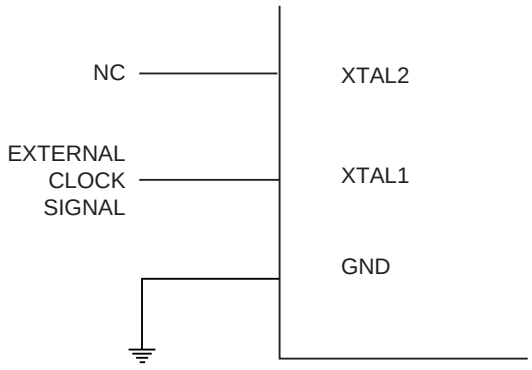
Table 8. RC

OSCCAL		
0x00	50%	100%
0x3F	75%	150%
0x7F	100%	200%

XTAL1 Figure 13

CKSEL “0000”

Figure 13.



SUT Table 10

Table 9.

CKSEL3..0	
0000 - 0001	0 - 16 MHz

Table 10.

SUT1..0		**(V_{CC} = 5.0V)**	
00	6 CK	14CK	BOD
01	6 CK	14CK + 4.1 ms	
10	6 CK	14CK + 65 ms	
11			

MCU

2% MCU

128 kHz

The 128 kHz Internal Oscillator is a low power Oscillator providing a clock of 128 kHz. The frequency is nominal at 3 V and 25°C. This clock may be selected as the system clock by programming the CKSEL Fuses to “0110 - 0111”.128 kHz
128 kHz 3V 25°C CKSEL
“0110 - 0111”

Table 11 SUT

Table 11. 128 kHz

SUT1..0			
00	6 CK	14CK	BOD
01	6 CK	14CK + 4 ms	
10	6 CK	14CK + 64 ms	
11			

CLKPR

Bit	7	6	5	4	3	2	1	0	
	CLKPCE	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	CLKPR
/	R/W	R	R	R	R/W	R/W	R/W	R/W	
	0	0	0	0					

- **Bit 7 – CLKPCE:**

CLKPCE "1” CLKPS CLKPR "0” CLK-PCE CLKPCE CLKPS
CLKPCE CLKPCE

- **Bits 3..0 – CLKPS3..0:** **3 - 0**

MCU
Table 12

CLKPS

1. CLKPCE "1” CLKPR "0”
2. CLKPS CLKPCE "0”

CKDIV8 CLKPS CKDIV8 CLKPS “0000”
CKDIV8 CLKPS “0011” 8
CLKPS
CKDIV8
CKDIV8

Table 12.

CLKPS3	CLKPS2	CLKPS1	CLKPS0	
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	8
0	1	0	0	16

Table 12.

CLKPS3	CLKPS2	CLKPS1	CLKPS0	
0	1	0	1	32
0	1	1	0	64
0	1	1	1	128
1	0	0	0	256
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

MCU AVR

MCUCR SE SLEEP
(Standby) MCUCR SM1 SM0 Table
13 MCU 4
MCU SLEEP
SRAM MCU

P21Figure 11 ATtiny2313

MCU MCUCR

Bit	7	6	5	4	3	2	1	0	
	PUD	SM1	SE	SM0	ISC11	ISC10	ISC01	ISC00	MCUCR
/	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

- **Bits 6, 4 – SM1..0: 1 0**

  Table 13

Table 13.

SM1	SM0	
0	0	
0	1	
1	1	
1	0	Standby

Note: 1. Standby

- **Bit 5 – SE:**

  MCU SLEEP SE
  SLEEP SE MCU
  SE

  SM1..0 00 SLEEP MCU CPU
  ADC /
  clk_{CPU} clk_{FLASH}

  MCU MCU
  ACSR
  ACD ADC

  SM1..0 01 11 SLEEP MCU
  USI
  BOD USI INT0
  MCU

  MCU
  P57“ ”

CKSEL P21“ ”

Standby SM1..0 10 SLEEP MCU Standby
6

Table 14.

	clk_{CPU}	clk_{FLASH}	clk_{IO}		INT0, INT1	USI	SPM/EEPROM	I/O
			X	X	X	X	X	X
					X(2)	X		
Standby(1)				X	X(2)	X		

Notes: 1.
2. INT0

AVR

P141“ ”

BOD BOD BODLEVEL
BOD
P33“ ” BOD

BOD

P36“ ”

P42“ ”

I/O $clk_{I/O}$

P48“ ”
$V_{CC}/2$

$V_{CC}/2$ DIDR
P142“ DIDR”

AVR I/O
JMP
Figure 14 Table
15
I/O

MCU
SUT CKSEL P21“ ”

The ATtiny2313 4

- V_{POT} MCU
- $\overline{\text{RESET}}$ MCU
-
- V_{BOT}
  MCU

Figure 14.

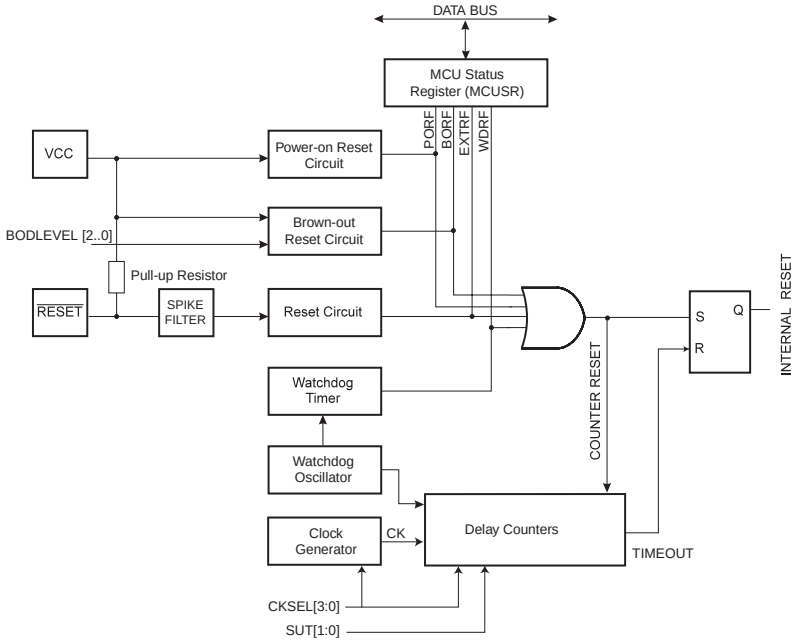


Table 15.

			(1)	(1)	(1)	
V_{POT}	( )	T_A = -40 - 85°C		1.2		V
	( )(2)	T_A = -40 - 85°C		1.1		V
V_{RST}	$\overline{\text{RESET}}$	V_{CC} = 1.8 - 5.5V	0.1 V_{CC}		0.9 V_{CC}	V
t_{RST}	$\overline{\text{RESET}}$	V_{CC} = 1.8 - 5.5V			2.5	µs

Notes: 1.
2. V_{POT}

(POR) Table 15 V_{CC}
POR POR

POR V_{CC}
V_{CC} RESET

Figure 15. MCU $\overline{\text{RESET}}$ V_{CC}

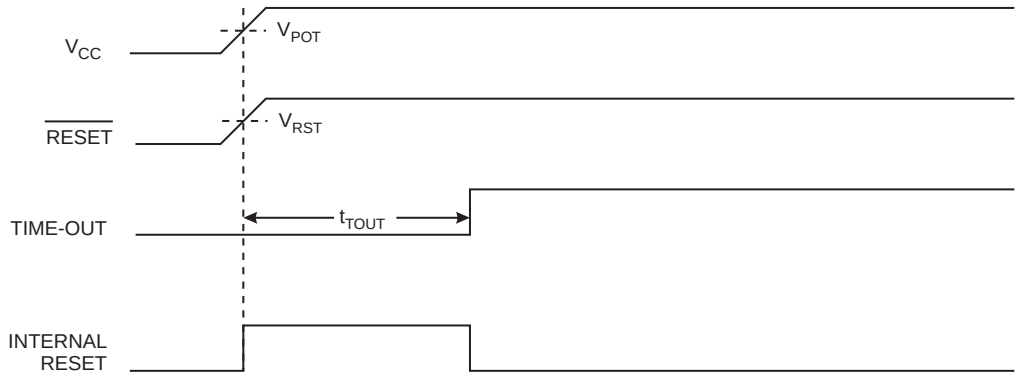
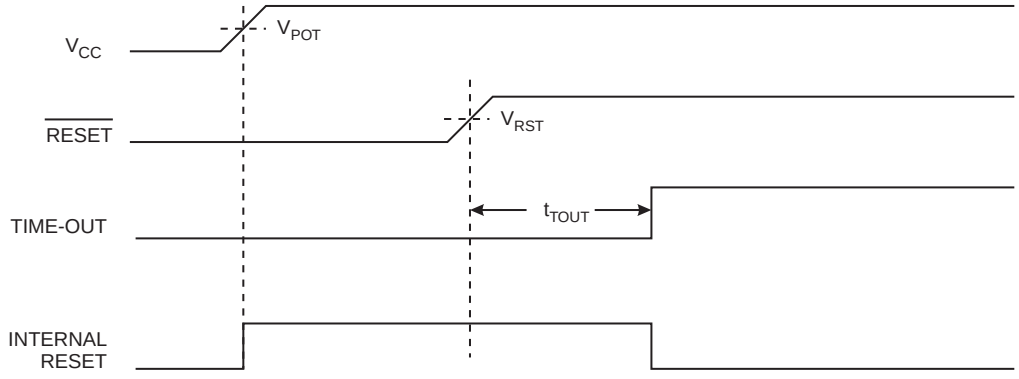
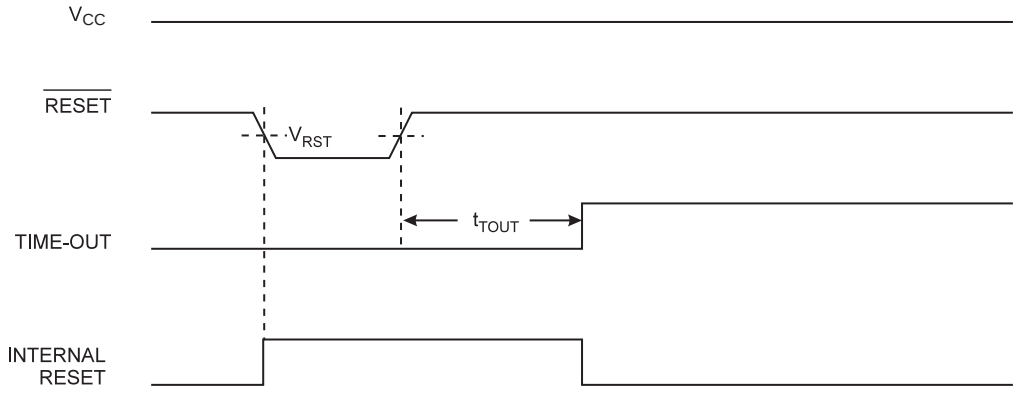


Figure 16. MCU $\overline{\text{RESET}}$



$\overline{\text{RESET}}$
(Table 15)
V_{RST}( ) t_{TOUT} MCU

Figure 17.



ATtiny2313 BOD(Brown-out Detection)
V_{CC} BODLEVEL BOD
$V_{BOT+} = V_{BOT} +$
$V_{HYST}/2$ $V_{BOT-} = V_{BOT} - V_{HYST}/2$

Table 16. BODLEVEL (1)

BODLEVEL [1..0]	V_{BOT}	V_{BOT}	V_{BOT}	
111	BOD			
110		1.8		V
101		2.7		
100		4.3		
011				
010				
001				
000				

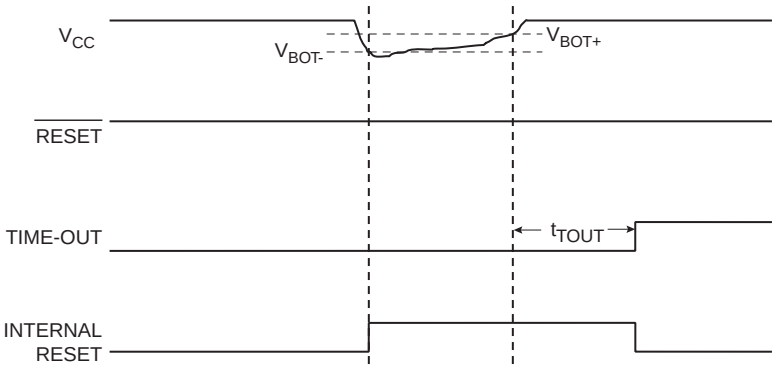
Note: 1. V_{BOT} V_{CC}
$= V_{BOT}$ V_{CC} ATtiny2313V
BODLEVEL = 110 ATtiny2313L BODLEVEL = 101

Table 17.

V_{HYST}	BOD		50		mV
t_{BOD}			2		µs

BOD V_{CC} (V_{BOT-} Figure 18) BOD
V_{CC} (V_{BOT+} Figure 18)
t_{TOUT} MCU
V_{CC} Table 15 t_{BOD} BOD

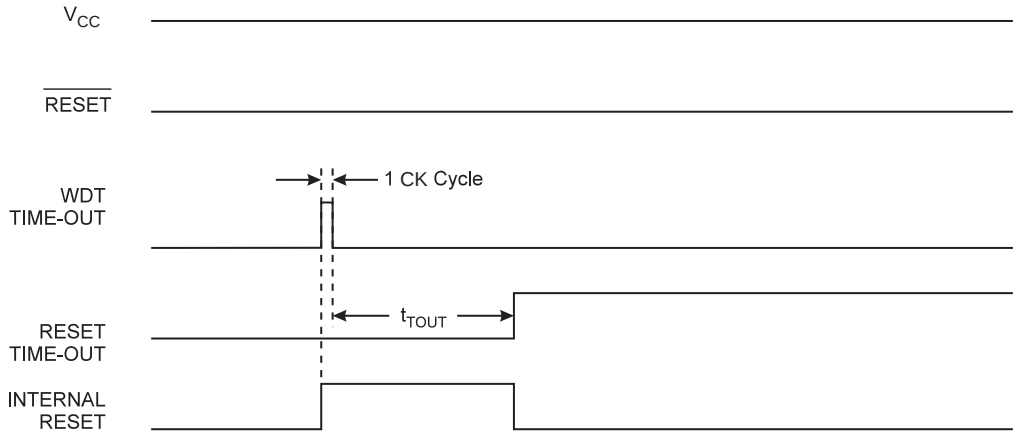
Figure 18.



1 CK

t_{TOUT}

Figure 19.



MCU MCUSR MCU MCU

Bit	7	6	5	4	3	2	1	0	
	–	–	–	–	WDRF	BORF	EXTRF	PORF	MCUSR
/	R	R	R	R	R/W	R/W	R/W	R/W	
	0	0	0						

- **Bit 3 – WDRF:**

”0”

- **Bit 2 – BORF:**

”0”

- **Bit 1 – EXTRF:**

”0”

- **Bit 0 – PORF:**

”0”

Table 18.

1. BOD (BODLEVEL [2..0])
2. (ACSR ACBG)

BOD ACBG

Table 18. (1)

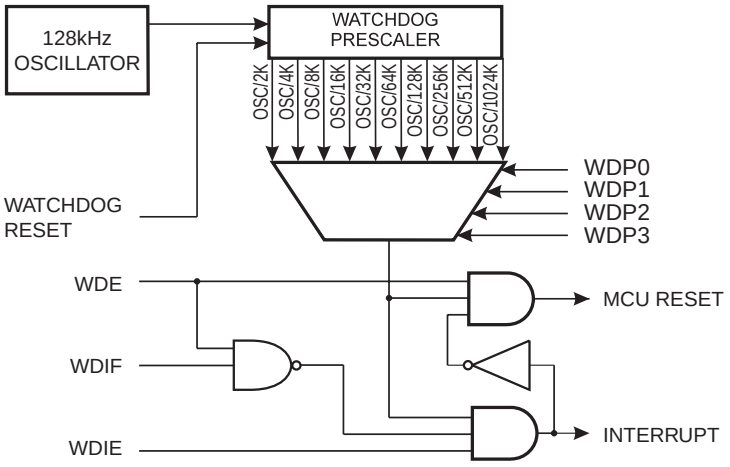
V_{BG}		V_{CC} = 2.7V, T_A = 25°C	1.0	1.1	1.2	V
t_{BG}		V_{CC} = 2.7V, T_A = 25°C		40	70	µs
I_{BG}		V_{CC} = 2.7V, T_A = 25°C		15		µA

Note: 1.

ATtiny2313 (WDT)

-
- **3**
  - –
  - –
  - –
- **16ms 8s**
-

Figure 20.



128 kHz WDT

WDT

WDT

WDTON
(WDE) (WDTIE) 1 0

1. WDCE WDE "1" WDE
   ”1”
2. WDE WDP WDCE

C WDT

( )

(1)

```
WDT_off:
  ;
  cli
  ; WDT
  wdr
  ;     MCUSR        WDRF
  in    r16, MCUSR
  andi  r16, (0xff & (0<<WDRF))
  out   MCUSR, r16
  ;   WDCE   WDE        1
  ;
  in    r16, WDTCR
  ori   r16, (1<<WDCE) | (1<<WDE)
  out   WDTCR, r16
  ;     WDT
  ldi   r16, (0<<WDE)
  out   WDTCR, r16
  ;
  sei
  ret
```

C (1)

```
void WDT_off(void)
{
  __disable_interrupt();
  __watchdog_reset();
  /*     MCUSR        WDRF*/
  MCUSR &= ~(1<<WDRF);
  /*   WDCE   WDE        1*/
  /*                              */
  WDTCR |= (1<<WDCE) | (1<<WDE);
  /*     WDT */
  WDTCR = 0x00;
  __enable_interrupt();
}
```

Note: 1.

WDRF WDE

C

(1)

```
WDT_Prescaler_Change:
  ;
  cli
  ;
  wdr
  ;
  in    r16, WDTCR
  ori   r16, (1<<WDCE) | (1<<WDE)
  out   WDTCR, r16
  ; --                          -
  ;               = 64K    (~0.5 s)
  ldi   r16, (1<<WDE) | (1<<WDP2) | (1<<WDP0)
  out   WDTCR, r16
  ; --                  2     -
  ;
  sei
  ret
```

C (1)

```
void WDT_Prescaler_Change(void)
{
  __disable_interrupt();
  __watchdog_reset();
  /*         */
  WDTCR |= (1<<WDCE) | (1<<WDE);
  /*               = 64K    (~0.5 s) */
  WDTCR = (1<<WDE) | (1<<WDP2) | (1<<WDP0);
  __enable_interrupt();
}
```

Note: 1.

WDP WDP

WDTCSR

Bit	7	6	5	4	3	2	1	0	
	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	WDTCSR
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	X	0	0	0	

- **Bit 7 - WDIF:**

WDTIF "1” SREG I
WDTIE

- **Bit 6 - WDIE:**

SREG I WDE

WDE
WDIF WDIE WDIF(
)
WDIE

Table 19.

WDTON	WDE	WDIE		
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	x	x		

- **Bit 4 - WDCE:**

WDE WDCE WDE /

"1” WDCE

- **Bit 3 - WDE:**

WDE MCUSR WDRF WDRF WDE
WDE WDRF

- **Bit 5, 2..0 - WDP3..0: 3, 2, 1 0**

WDP3..0 P40Table 20

Table 20.

WDP3	WDP2	WDP1	WDP0		V_{CC} = 5.0V
0	0	0	0	2K (2048)	16 ms
0	0	0	1	4K (4096)	32 ms
0	0	1	0	8K (8192)	64 ms

Table 20.

WDP3	WDP2	WDP1	WDP0		V_{CC} = 5.0V
0	0	1	1	16K (16384)	0.125 s
0	1	0	0	32K (32768)	0.25 s
0	1	0	1	64K (65536)	0.5 s
0	1	1	0	128K (131072)	1.0 s
0	1	1	1	256K (262144)	2.0 s
1	0	0	0	512K (524288)	4.0 s
1	0	0	1	1024K (1048576)	8.0 s
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

ATtiny2313 AVR P11“ ”

ATtiny2313

Table 21.

1	0x0000	RESET	
2	0x0001	INT0	0
3	0x0002	INT1	1
4	0x0003	TIMER1 CAPT	/ 1
5	0x0004	TIMER1 COMPA	/ 1 A
6	0x0005	TIMER1 OVF	/ 1
7	0x0006	TIMER0 OVF	/ 0
8	0x0007	USART0, RX	USART0
9	0x0008	USART0, UDRE	USART0
10	0x0009	USART0, TX	USART0
11	0x000A	ANALOG COMP	
12	0x000B	PCINT	
13	0x000C	TIMER1 COMPB	/ 1 B
14	0x000D	TIMER0 COMPA	/ 0 A
15	0x000E	TIMER0 COMPB	/ 0 B
16	0x000F	USI START	USI
17	0x0010	USI OVERFLOW	USI
18	0x0011	EE READY	EEPROM
19	0x0012	WDT OVERFLOW	

ATtiny2313

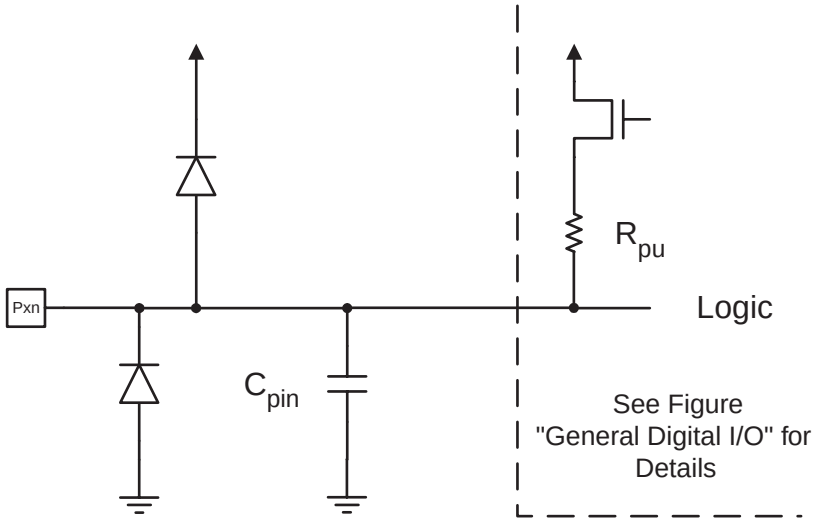
```
0x0000         rjmp   RESET          ;
0x0001         rjmp   INT0           ;        0
0x0002         rjmp   INT1           ;        1
0x0003         rjmp   TIM1_CAPT      ;      1
0x0004         rjmp   TIM1_COMPA     ;      1    A
0x0005         rjmp   TIM1_OVF       ;      1
0x0006         rjmp   TIM0_OVF       ;      0
0x0007         rjmp   USART0_RXC     ; USART0
0x0008         rjmp   USART0_DRE     ; USART0,UDR
0x0009         rjmp   USART0_TXC     ; USART0
0x000A         rjmp   ANA_COMP       ;
0x000B         rjmp   PCINT          ;
0x000C         rjmp   TIMER1_COMPB   ;      1    B
0x000D         rjmp   TIMER0_COMPA   ;      0    A
0x000E         rjmp   TIMER0_COMPB   ;      0    B
0x000F         rjmp   USI_START      ; USI
0x0010         rjmp   USI_OVERFLOW   ; USI
0x0011         rjmp   EE_READY       ; EEPROM
0x0012         rjmp   WDT_OVERFLOW   ;

;
0x0013  RESET: ldi    r16, low(RAMEND);
0x0014         out    SPL,r16                    RAM
0x0015         sei                   ;
0x0016         <instr>  xxx
  ...     ...     ...  ...
```

I/O

I/O AVR I/O - -
SBI CBI

LED
V_{CC} Figure 21 P168“
”

Figure 21. I/O



“x” “n”
PORTB3 B 3
PORTxn I/O P56“I/O ”
I/O – PORTx – DDRx
– PINx /
PINx "1“
"0“ “1“ MCUCR PUD

I/O P44“ I/O ”
P48“ ”

I/O

I/O I/O Figure 22 I/O

Table 22

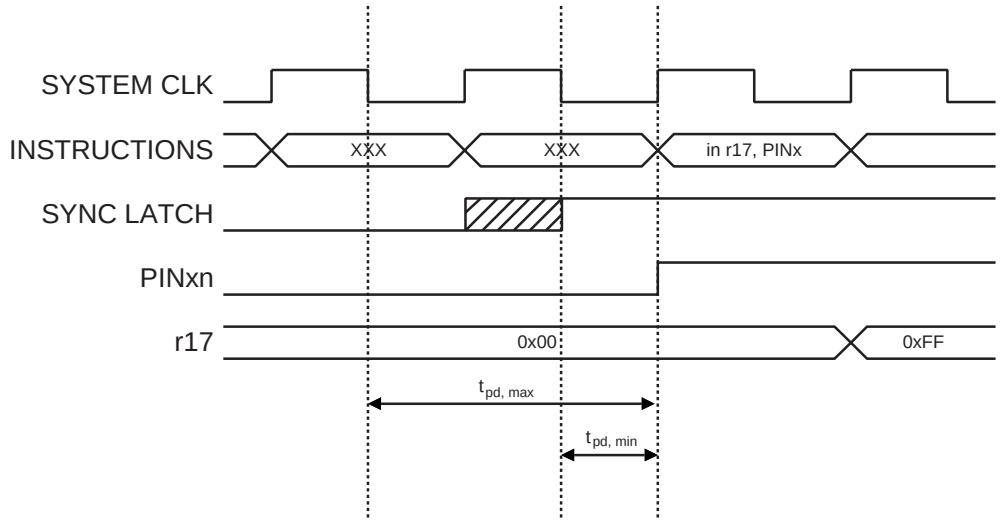
Table 22.

DDxn	PORTxn	PUD (MCUCR2)	I/O		
0	0	X		No	(Hi-Z)
0	1	0		Yes	
0	1	1		No	(Hi-Z)
1	0	X		No	( )
1	1	X		No	( )

DDxn PINxn Figure 22
PINxn

Figure 23 $t_{pd,max}$
$t_{pd,min}$

Figure 23.



SYNC LATCH

PINxn

$t_{pd,max}$

$t_{pd,min}$

½ ~ 1½

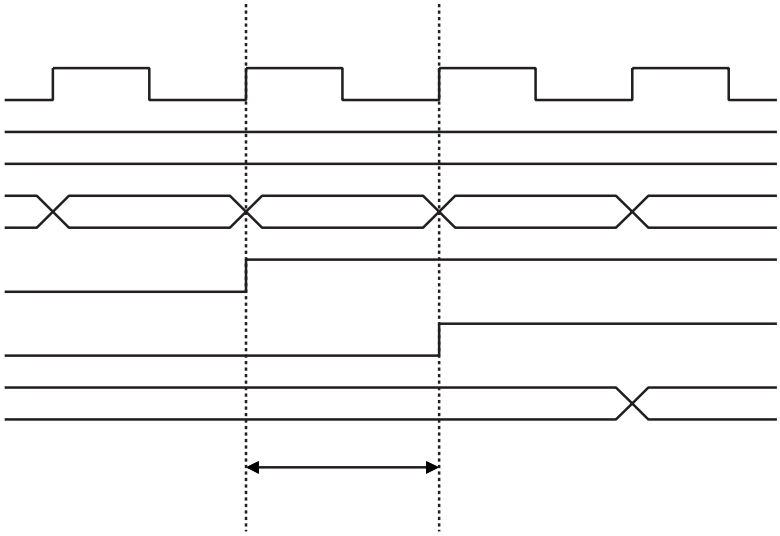
Figure 24

out *in*

nop *out* SYNC LATCH

t_{pd}

Figure 24.



B 0 1 2 3 4 7
6 7

nop

(1)

```
...
;
;
ldi  r16,(1<<PB7)|(1<<PB6)|(1<<PB1)|(1<<PB0)
ldi  r17,(1<<DDB3)|(1<<DDB2)|(1<<DDB1)|(1<<DDB0)
out  PORTB,r16
out  DDRB,r17
;          nop
nop
;
in   r16,PINB
...
```

C

```
unsigned char i;
...
/*                        */
/*               */
PORTB = (1<<PB7)|(1<<PB6)|(1<<PB1)|(1<<PB0);
DDRB = (1<<DDB3)|(1<<DDB2)|(1<<DDB1)|(1<<DDB0);
/*           nop    */
__no_operation();
/*           */
i = PINB;
...
```

Note: 1.
0 1 6 7 2 3 0 1

Figure 22 ( ) SLEEP
MCU Standby
$V_{CC}/2$
SLEEP SLEEP
SLEEP P48“ ”

(“1”) "
"
"1” "0”
"0” ”1”

I/O Figure 25 Figure
22
AVR

Table 23.

PUOE		PUOV {DDxn, PORTxn, PUD} = 0b010
PUOV		PUOE PUOV / / DDxn PORTxn PUD
DDOE		DDOV DDxn
DDOV		DDOE DDOV / / DDxn
PVOE		PVOV PVOE PORTxn
PVOV		PVOE PVOV PORTxn
PTOE		PTOE
DIEOE		DIEOV DIEOE MCU ( )
DIEOV		DIEOE DIEOV / / MCU ( )
DI		
AIO	 /	/

MCU MCUCR

Bit	7	6	5	4	3	2	1	0	
	PUD	SM1	SE	SM0	ISC11	ISC10	ISC01	ISC00	MCUCR
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

- **Bit 7 – PUD:**

1 DDxn PORTxn ({DDxn, PORTxn} = 0b01) I/O P45“ ”

A A Table 5

Table 24. A

PA2	RESET, dW
PA1	XTAL2
PA0	XTAL1

B B Table 25

Table 25. B

PB7	USCK/SCL/PCINT7
PB6	DO/PCINT6
PB5	DI/SDA/PCINT5
PB4	OC1B/PCINT4
PB3	OC1A/PCINT3
PB2	OC0A/PCINT2
PB1	AIN1/PCINT1
PB0	AIN0/PCINT0

- **USCK/SCL/PCINT7 - B, Bit 7**

USCK

SCL USI

PCINT7 7 PB7

- **DO/PCINT6 - B, Bit 6**

DO PORTB6
DDB6 1 PORTB6 1 PORTB6

PCINT6 6 PB6

- **DI/SDA/PCINT5 - B, Bit 5**

DI

SDA

PCINT5 5 PB5

- **OC1B/PCINT4 – B, Bit 4**

OC1B B PB4 T/C1 B
(DDB6 1) OC1B PWM

PCINT4 4 PB4

- **OC1A/PCINT3 – B, Bit 3**

OC1A A PB3 T/C1 A
(DDB3 1) OC1A PWM

PCINT3 3 PB3

- **OC0A/PCINT2 – B, Bit 2**

OC0A A PB2 T/C0 A
(DDB2 1) OC0A PWM

PCINT2 2 PB2

- **AIN1/PCINT1 – B, Bit 1**

AIN1

PCINT1 1 PB1

- **AIN0/PCINT0 – B, Bit 0**

AIN0

PCINT0 0 PB0

Table 26 Table 27 B P49Figure 25 SPI MSTR INPUT SPI SLAVE OUTPUT MISO MOSI SPI MSTR OUTPUT SPI SLAVE INPUT

Table 26. PB7..PB4

	PB7/USCK/ SCL/PCINT7	PB6/DO/PCINT6	PB5/SDA/ DI/PCINT5	PB4/OC1B/ PCINT4
PUOE	0	0	0	0
PUOV	0	0	0	0
DDOE	USI_TWO_WIRE	0	USI_TWO_WIRE	0
DDOV	(USI_SCL_HOLD + $\overline{\text{PORTB7}}$)•DDB7	0	($\overline{\text{SDA}}$ + $\overline{\text{PORTB5}}$)• DDRB5	0
PVOE	USI_TWO_WIRE • DDRB7	USI_THREE_WIRE	USI_TWO_WIRE • DDRB5	OC1B_PVOE
PVOV	0	DO	0	0OC1B_PVOV
PTOE	USI_PTOE	0	0	0
DIEOE	(PCINT7•PCIE) +USISIE	(PCINT6•PCIE)	(PCINT5•PCIE) + USISIE	(PCINT4•PCIE)
DIEOV	1	1	1	1
DI	PCINT7 USCK SCL	PCINT6	PCINT5 SDA DI	PCINT4
AIO	–	–	–	–

Table 27. PB3..PB0

	PB3/OC1A/ PCINT3	PB2/OC0A/ PCINT2	PB1/AIN1/ PCINT1	PB0/AIN0/ PCINT0
PUOE	0	0	0	0
PUOV	0	0	0	0
DDOE	0	0	0	0
DDOV	0	0	0	0
PVOE	OC1A_PVOE	OC0A_PVOE	0	0
PVOV	OC1A_PVOV	OC0A_PVOV	0	0
PTOE	0	0	0	0
DIEOE	(PCINT3 • PCIE)	(PCINT2 • PCIE)	(PCINT1 • PCIE)	(PCINT0 • PCIE)
DIEOV	1	1	1	1
DI	PCINT7	PCINT6	PCINT5	PCINT4
AIO	–	–	AIN1	AIN0

D D Table 28

Table 28. D

PD6	ICP
PD5	OC0B/T1
PD4	T0
PD3	INT1
PD2	INT0/XCK/CKOUT
PD1	TXD
PD0	RXD

- **ICP – D, Bit 6**

ICP T/C1 PD6 T/C1

- **OC1B/T1 – D, Bit 5**

OC0B B PD5 T/C0 B
(DDB5 1) OC0B PWM

T1 T/C1 TCCR1 CS02 CS01 T/C1

- **T0 – D, Bit 4**

T0 T/C0 TCCR0 CS02 CS01 T/C0

- **INT1 – D, Bit 3**

INT0 0 PD3 MCU

- **INT0/XCK/CKOUT – D, Bit 2**

INT1 1 PD2 MCU

XCK USART

CKOUT

- **TXD – D, Bit 1**

TXD UART

- **RXD – D, Bit 0**

RXD UART

Table 29 Table 30 D P49Figure 25

Table 29. PD7..PD4

	PD6/ICP	PD5/OC1B/T1	PD4/T0
PUOE	0	0	0
PUOV	0	0	0
DDOE	0	0	0
DDOV	0	0	0
PVOE	0	OC1B_PVOE	0
PVOV	0	OC1B_PVOV	0
PTOE	0	0	0
DIEOE	ICP	T1	T0
DIEOV	1	1	1
DI	ICP	T1	T0
AIO	–	–	AIN1

Table 30. PD3..PD0

	PD3/INT1	PD2/INT0/XCK/ CKOUT	PD1/TXD	PD0/RXD
PUOE	0	0	TXD_OE	RXD_OE
PUOV	0	0	0	PORTD0 • $\overline{PUD}$
DDOE	0	0	TXD_OE	RXD_EN
DDOV	0	0	1	0
PVOE	0	XCKO_PVOE	TXD_OE	0
PVOV	0	XCKO_PVOV	TXD_PVOV	0
PTOE	0	0	0	0
DIEOE	INT1	INT0 / XCK	0	0
DIEOV	1	1	0	0
DI	INT1	INT0 / XCK	–	RXD
AIO	–	–	–	–

I/O

A PORTA

Bit	7	6	5	4	3	2	1	0	
	–	–	–	–	–	PORTA2	PORTA1	PORTA0	PORTA
/	R	R	R	R	R	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

A DDRA

Bit	7	6	5	4	3	2	1	0	
	–	–	–	–	–	DDA2	DDA1	DDA0	DDRA
/	R	R	R	R	R	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

A PINA

Bit	7	6	5	4	3	2	1	0	
	–	–	–	–	–	PINA2	PINA1	PINA0	PINA
/	R	R	R	R	R	R/W	R/W	R/W	
	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

B PORTB

Bit	7	6	5	4	3	2	1	0	
	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	PORTB
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

B DDRB

Bit	7	6	5	4	3	2	1	0	
	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

B PINB

Bit	7	6	5	4	3	2	1	0	
	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	PINB
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

D PORTD

Bit	7	6	5	4	3	2	1	0	
	–	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	PORTD
/	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

D DDRD

Bit	7	6	5	4	3	2	1	0	
	–	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
/	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

D PIND

Bit	7	6	5	4	3	2	1	0	
	–	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	PIND
/	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

INT0 INT1 PCINT7..0 INT0
INT1 PCINT7..0
PCINT7..0 PCI0
PCMSK1 PCMSK0 PCINT7..0

A – EICRA

INT0 INT1 I/O P21“ ”
INT0 INT1
( ) I/O

MCU
MCU P21“
” SUT CKSEL

MCU MCUCR A

Bit	7	6	5	4	3	2	1	0	
	PUD	SM1	SE	SMD	ISC11	ISC10	ISC01	ISC00	MCUCR
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

- **Bit 3, 2 – ISC11, ISC10: 1 Bit 1 Bit 0**

SREG I 1 INT1
Table 32 MCU INT1

Table 31. 1

ISC11	ISC10	
0	0	INT1
0	1	INT1
1	0	INT1
1	1	INT1

- **Bit 1, 0 – ISC01, ISC00: 0 Bit1 Bit 0**

SREG I 0 INT0
Table 32 MCU INT0

Table 32. 0

ISC01	ISC00	
0	0	INT0
0	1	INT0
1	0	INT0
1	1	INT0

GIMSK

Bit	7	6	5	4	3	2	1	0	
	INT1	INT0	PCIE	–	–	–	–	–	GIMSK
/	R/W	R/W	R/W	R	R	R	R	R	
	0	0	0	0	0	0	0	0	

- **Bit 7 – INT1:** **1**

  INT1 '1' SREG I
  1 1/0 (ISC11 ISC10) INT1
  INT1

- **Bit 6 – INT0:** **0**

  INT0 '1' SREG I
  0 1/0 (ISC01 ISC00) INT0
  INT0

- **Bit 5 – PCIE:**

  PCIE '1' SREG I
  PCINT7..0 PCI PCINT7..0
  PCMSK

EIFR

Bit	7	6	5	4	3	2	1	0	
	INTF1	INTF0	PCIF	–	–	–	–	–	EIFR
/	R/W	R/W	R/W	R	R	R	R	R	
	0	0	0	0	0	0	0	0	

- **Bit 7 – INTF1:** **1**

INT1 INTF1 SREG
I GIMSK INT1 ”1” MCU
”1” INT1

- **Bit 6 – INTF0:** **0**

INT0 INTF0 SREG
I GIMSK INT0 ”1” MCU
”1” INT0

- **Bit 5 – PCIF:**

PCINT7..0 PCIF "1” SREG I GIMSK
PCIE "1” MCU
”1”

PCMSK

Bit	7	6	5	4	3	2	1	0	
	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	PCMSK
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

- **Bit 7..0 – PCINT7..0:** **15..8**

PCINT7..0 I/O PCINT7..0 PCIE
PCINT7..0

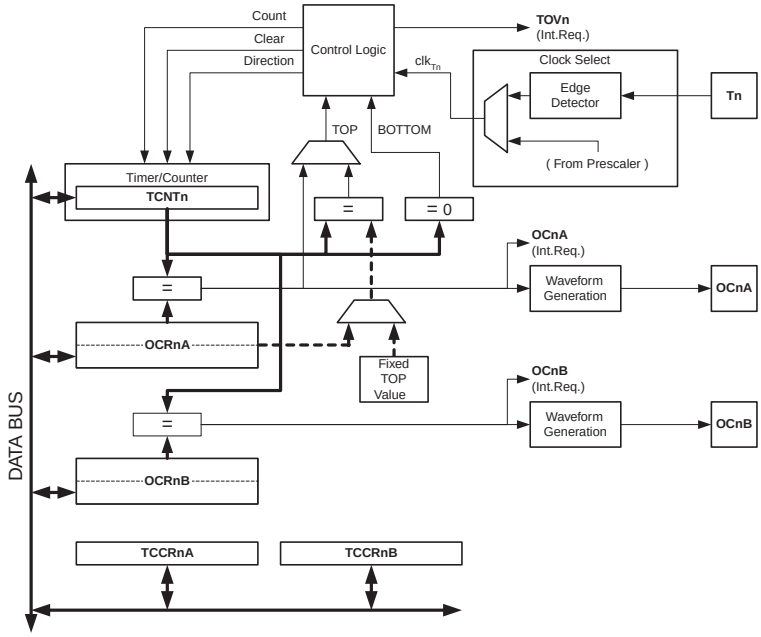
PWM 8 / 0

T/C0 8 / PWM

-
-
- ( )
- **PWM**
- **PWM**
-
- **(TOV0, OCF0A OCF0B)**

Figure 26 8 / P2“ATtiny2313 ” CPU I/O I/O P69“8 / ”

Figure 26. 8 T/C



T/C(TCNT0) (OCR0A OCR0B) 8 (Int.Req.) TIFR0 TIMSK TIFR TIMSK

T/C T0 ( )T/C T/C clk_{T0} (OCR0A OCR0B) T/C PWM OC0 P62 “ ” (OCF0A OCF0B)

“n” T/C 0 “x” A B TCNT0 T/C0

Table 33

Table 33.

BOTTOM		0x00	BOTTOM				
MAX		0xFF (	255)	MAX			
TOP				TOP	TOP		0xFF
	(MAX)		OCR0A				

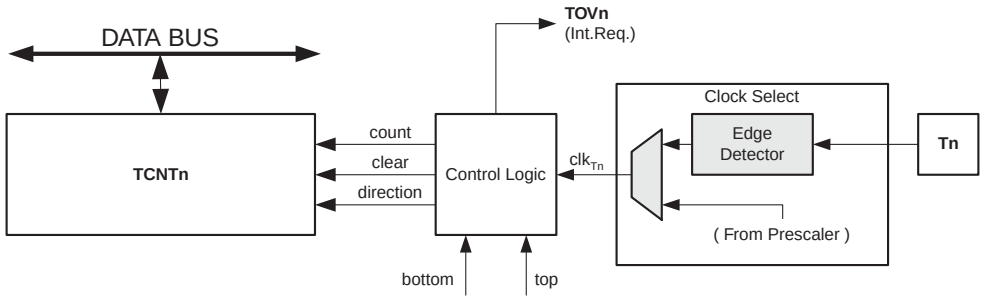
T/C

T/C

T/C TCCR0B CS02:0 P75“T/C0 T/C1
”

8 T/C Figure 27

Figure 27.



( )

count TCNT0 1 1

direction

clear TCNT0 ( )

clk$_{Tn}$ T/C clk$_{T0}$

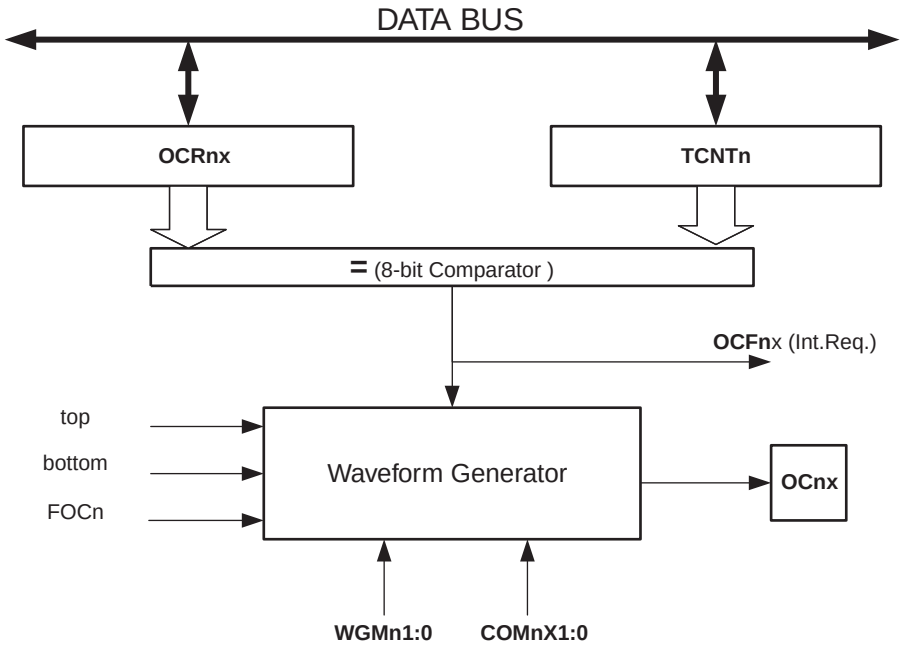
top TCNT0

bottom TCNT0 (0)

clk_{T0} clk_{T0}
CS02:0
(CS02:0 = 0) clk_{T0} CPU TCNT0 CPU
( )
T/C (TCCR0A) WGM01 WGM00 (TCCR0B) WGM02
OC0A
P87“ ”
T/C TOV0 WGM01:0 TOV0 CPU

8 TCNT0 OCR0A(OCR0B) TCNT0
OCR0A OCR0B
OCF0A(OCF0B) CPU
OCF0A(OCF0B) ”1”
WGM2:0 COM0x1:0
max bottom
(P87“ ”)
Figure 28

Figure 28.



PWM OCR0x
OCR0x top bottom
PWM
OCR0x CPU OCR0x
CPU OCR0x

PWM FOC0x ”1”
OCF0x / OC0x
(COM01:0 OC0x "0“-”1”
)

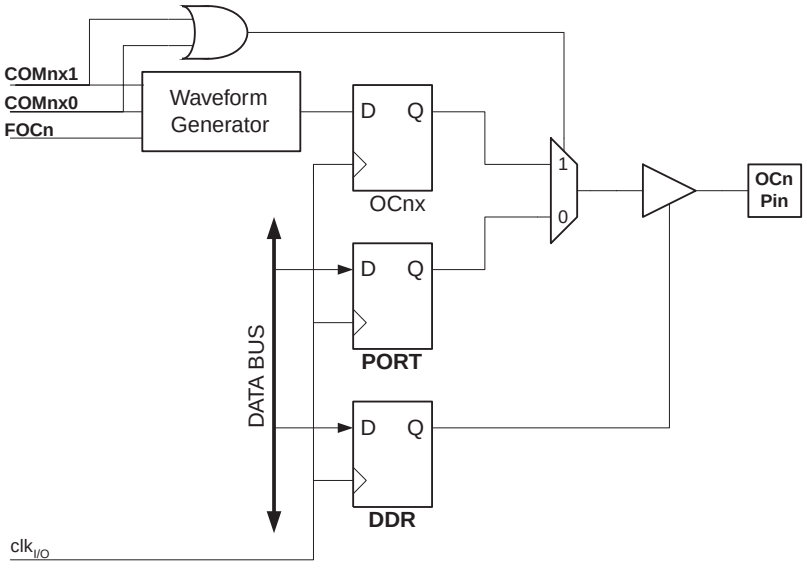
TCNT0 CPU TCNT0
OCR0x TCNT0

TCNT0
TCNT0 T/C TCNT0
OCR0x
TCNT0 BOTTOM
OC0x OC0x
FOC0x OC0x

COM0x1:0 COM0x1:0

COM0x1:0 COM0x1:0
(OC0x) COM0x1:0 OC0x
Figure 29 COM0x1:0 I/O I/O I/O
COM0x1:0 I/O (DDR
PORT) OC0x OC0x OC0x OC0x

Figure 29.



COM0x1:0 I/O OC0x
DDR OC0x
DDR_OC0x

OC0x COM0x1:0
P69 “8 / ”

COM0x1:0 CTC PWM
COM0x1:0 = 0 OC0x
PWM P62Figure 28 PWM P53Table 26 PWM P53Table 27

COM0x1:0 PWM
FOC0x

- T/C - (WGM02:0)
(COM0x1:0)
COM0x1:0 PWM PWM COM0x1:0
(P63 “
”)

P67“T/C ” Figure 33 Figure 34 Figure 35 Figure 36

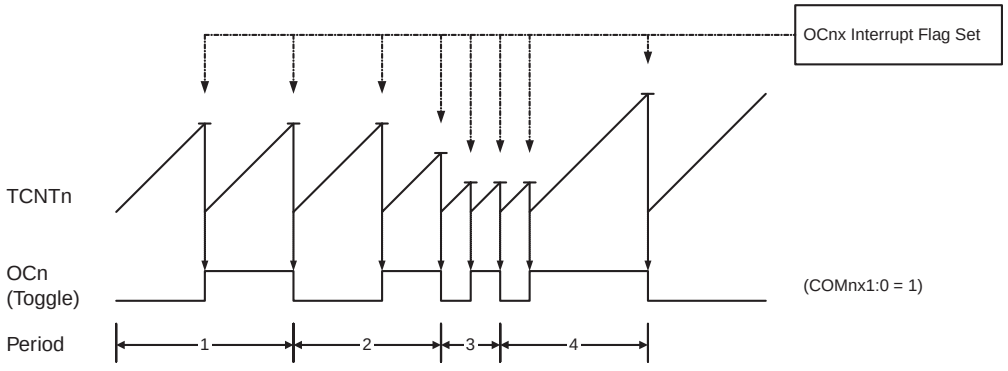
(WGM02:0 = 0) 8
(TOP = 0xFF) 0x00
TCNT0 T/C TOV0 TOV0
9 TOV0

CPU

CTC( ) CTC (WGM02:0 = 2) OCR0A
TCNT0 OCR0A OCR0A TOP

CTC Figure 30 TCNT0 TCNT0 OCR0A
TCNT0

Figure 30. CTC



OCF0A TOP
TOP CTC
TOP BOTTOM OCR0A
TCNT0
0xFF 0x00 OCF0A
CTC OC0A
COM0A1:0 = 1 OC0A
$f_{OC0} = f_{clk\_I/O}/2$ (OCR0 A= 0x00)

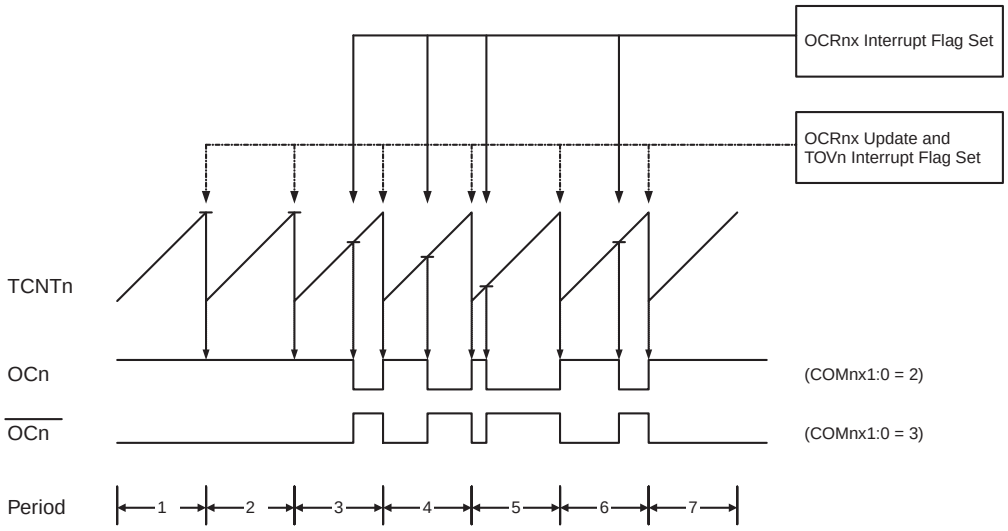
$$f_{OCnx} = \frac{f_{clk\_I/O}}{2 \cdot N \cdot (1 + OCRnx)}$$

N (1 8 64 256 1024)
TOV0 MAX 0x00

PWM PWM (WGM02:0 = 3 7) PWM PWM
PWM BOTTOM TOP
BOTTOM WGM2:0 = 3 TOP 0xFF WGM2:0 = 7
TOP OCR0A OC0x TCNT0 OCR0x
BOTTOM OC0x
PWM PWM
PWM DAC
( )

PWM TOP
Figure 29 TCNT0
PWM PWM TCNT0 OCR0x
TCNT0

Figure 31. PWM



TOP T/C TOV0

PWM OC0x PWM COM0x1:0
2 PWM 3 PWM WGM02

COM0A1:0 "1" AC0A OC0B (P53Table 26) OC0x PWM OC0x OCR0x TCNT0 ( ) (TOP BOTTOM) ( )

PWM

$$f_{OCnxPWM} = \frac{f_{clk\_I/O}}{N \cdot 256}$$

N (1 8 64 256 1024)

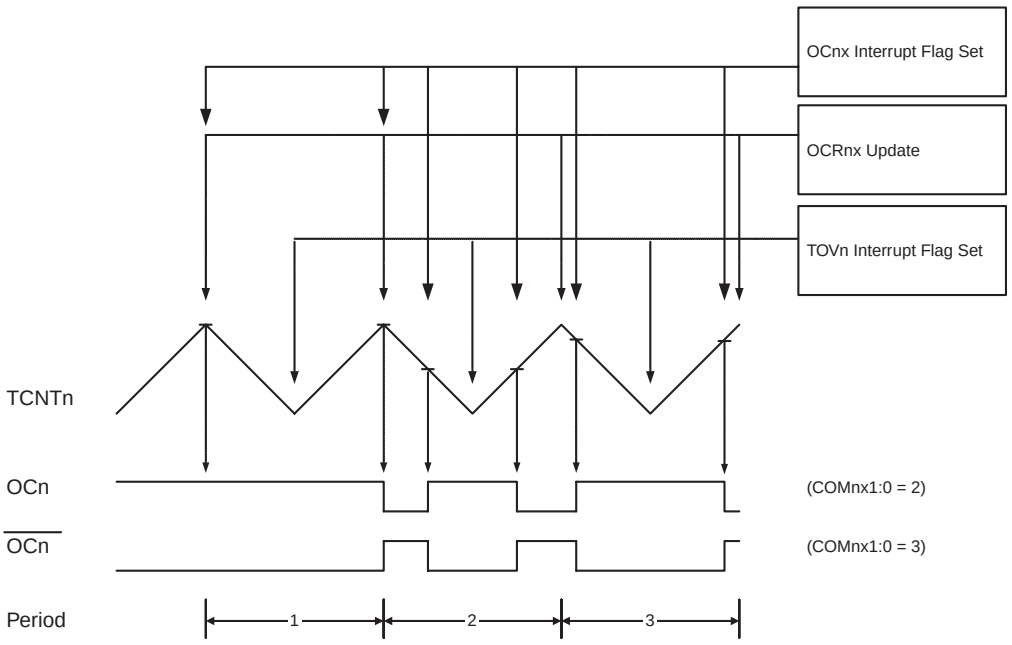
OCR0A PWM OCR0A BOTTOM MAX+1 OCR0A MAX COM0A1:0

OC0x (COM0x1:0 = 1) 50% OCR0A 0 $f_{oc0} = f_{clk\_I/O}/2$ CTC OC0A PWM

PWM PWM (WGM02:0 = 1 5) PWM BOTTOM TOP TOP BOTTOM WGM2:0 = 1 TOP 0xFF WGM2:0 = 5 TOP OCR0A TOP TCNT0 OCR0x OC0x BOTTOM TCNT0 OCR0x OC0x

TOP TCNT0 TOP Figure 32 TCNT0 PWM PWM TCNT0 OCR0x TCNT0

Figure 32. PWM



BOTTOM T/C TOV0

PWM OC0x PWM COM0x1:0
2 PWM COM0x1:0 3 PWM WGM02
COM0A0 "1” OC0A OC0B
(P53Table 27) OC0x
OCR0x TCNT0 OC0x
PWM PWM

$$f_{OCnxPCPWM} = \frac{f_{clk\_I/O}}{N \cdot 510}$$

N (1 8 64 256 1024)

OCR0A PWM PWM
OCR0A BOTTOM OCR0A MAX
PWM

Figure 32 2 OCn
BOTTOM

- Figure 32 OCR0A MAX OCR0A MAX
  OCn
  BOTTOM T/C MAX OCn

- OCR0A
  OCn

T/C

T/C clk_{T0}
Figure 33 T/C PWM
MAX

Figure 33. T/C

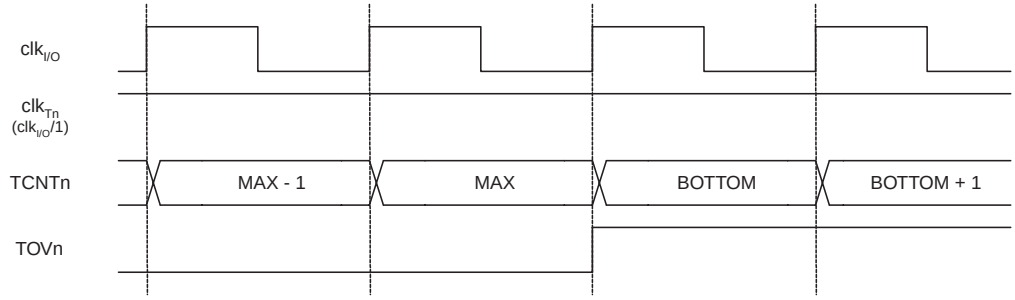


Figure 33

Figure 34. T/C $f_{clk\_I/O}/8$

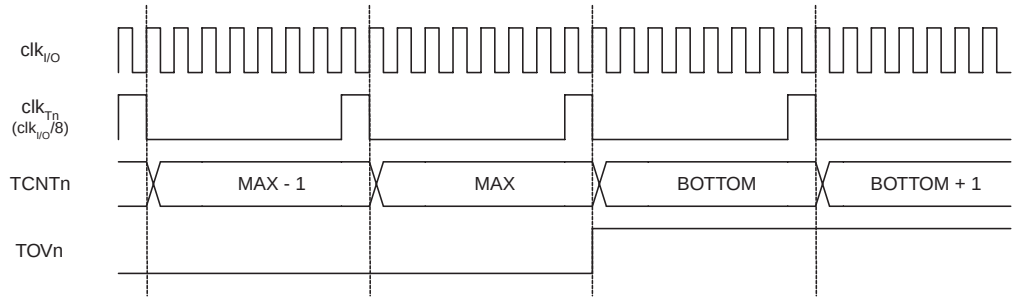


Figure 35 OCF0B (CTC)OCF0A OCR0A TOP

Figure 35. T/C OCF0x $f_{clk\_I/O}/8$

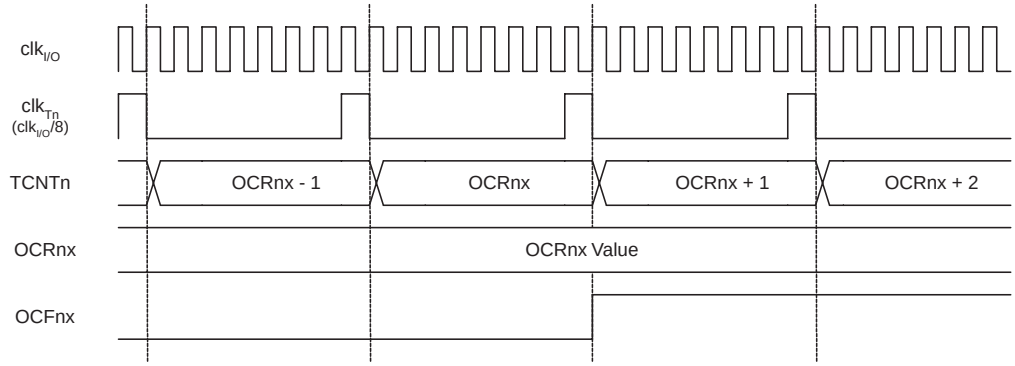
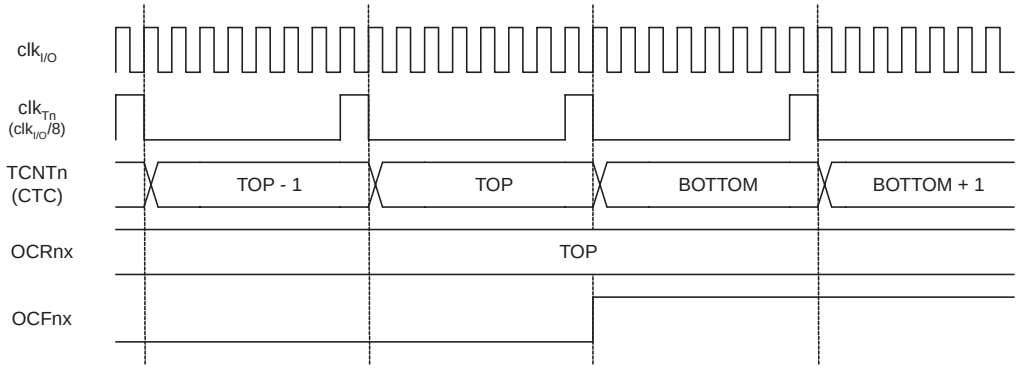


Figure 36 CTC PWM OCF0A TCNT0 OCR0A TOP

Figure 36. T/C CTC $f_{clk\_I/O}/8$



8 /

T/C A TCCR0A

Bit	7	6	5	4	3	2	1	0	
	COM0A1	COM0A0	COM0B1	COM0B0	–	–	WGM01	WGM00	TCCR0A
/	R/W	R/W	R/W	R/W	R	R	R/W	R/W	
	0	0	0	0	0	0	0	0	

- **Bits 7:6 – COM0A1:0: A**

(OC0A) COM0A1:0 OC0A
I/O OC0A DDR

OC0A COM0A1:0 WGM02:0 Table 34
WGM02:0 CTC (PWM) COM0A1:0

Table 34. PWM

COM0A1	COM0A0	
0	0	OC0A
0	1	OC0A
1	0	OC0A
1	1	OC0A

Table 35 WGM01:0 PWM COM01:0

Table 35. PWM (1)

COM0A1	COM0A0	
0	0	OC0A
0	1	WGM02 = 0: OC0A WGM02 = 1: OC0A
1	0	OC0A TOP OC0A
1	1	OC0A TOP OC0A

Note: 1. OCR0A TOP COM01
TOP OC0 P65“ PWM ”

Table 36 WGM02:0 PWM COM0A1:0

Table 36. PWM (1)

COM0A1	COM0A0	
0	0	OC0A
0	1	WGM02 = 0: OC0A WGM02 = 1: OC0A
1	0	OC0A OC0A
1	1	OC0A OC0A

Note: 1. OCR0A TOP COM0A1
TOP OC0A P66“ PWM ”

- **Bits 5:4 – COM0B1:0:** **B**

OC0B COM0B1:0
OC0B 1

OC0B COM0B1:0 WGM01:0 Table 37
WGM02:0 CTC COM0B1:0

Table 37. PWM

COM0B1	COM0B0	
0	0	OC0B
0	1	OC0B
1	0	OC0B
1	1	OC0B

Table 38 WGM02:0 PWM COM0B1:0

Table 38. PWM (1)

COM0B1	COM0B0	
0	0	OC0B
0	1	
1	0	OC0B TOP OC0B
1	1	OC0B TOP OC0B

Note: 1. OCR0B TOP COM0B1
TOP OC0B P65“ PWM ”

Table 39 WGM02:0 PWM COM0B1:0

Table 39. PWM (1)

COM0B1	COM0B0	
0	0	OC0B
0	1	
1	0	OC0B OC0B
1	1	OC0B OC0B

Note: 1. OCR0B TOP COM0B1
TOP OC0B P66“ PWM ”

- **Bits 3, 2 – Res:**

- **Bits 1:0 – WGM01:0:**

TCCR0B WGM02 TOP
Table 40 T/C ( ) CTC
PWM (P87“ ”)

Table 40.

Mode	WGM2	WGM1	WGM0	T/C	TOP	OCRx	TOV (1)(2)
0	0	0	0		0xFF		MAX
1	0	0	1	PWM	0xFF	TOP	BOTTOM
2	0	1	0	CTC	OCRA		MAX
3	0	1	1	PWM	0xFF	TOP	MAX
4	1	0	0		–	–	–
5	1	0	1	PWM	OCRA	TOP	BOTTOM
6	1	1	0		–	–	–
7	1	1	1	PWM	OCRA	TOP	TOP

Notes: 1. MAX = 0xFF
2. BOTTOM = 0x00

T/C B TCCR0B

Bit	7	6	5	4	3	2	1	0	
	FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00	TCCR0B
/	W	W	R	R	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

- **Bit 7 – FOC0A: A**

FOC0A WGM PWM

PWM TCCR0B

1 OC0A COM0A1:0

FOC0A

COM0A1:0

FOC0A OCR0A TOP CTC

FOC0A 0

- **Bit 6 – FOC0B: B**

FOC0B WGM PWM

PWM TCCR0B

1 OC0B COM0B1:0

FOC0B

COM0B1:0

FOC0B OCR0B TOP CTC

FOC0B 0

- **Bits 5:4 – Res:**

- **Bit 3 – WGM02:**

P69“T/C A TCCR0A”

- **Bits 2:0 – CS02:0:**

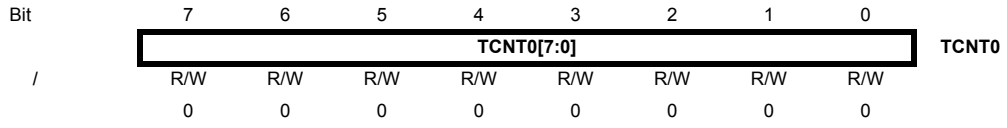
T/C P73Table 41

Table 41.

CS02	CS01	CS00	
0	0	0	T/C
0	0	1	$clk_{I/O}$/1 ( )
0	1	0	$clk_{I/O}$/8 ( )
0	1	1	$clk_{I/O}$/64 ( )
1	0	0	$clk_{I/O}$/256 ( )
1	0	1	$clk_{I/O}$/1024 ( )
1	1	0	T0
1	1	1	T0

T/C0 T0

T/C TCNT0

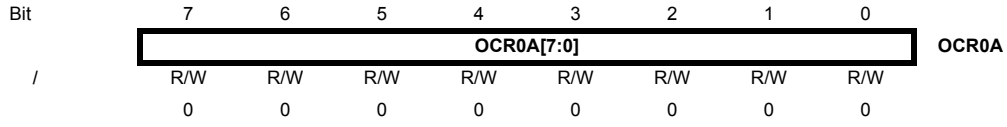


T/C 8 TCNT0

TCNT0

TCNT0 OCR0x

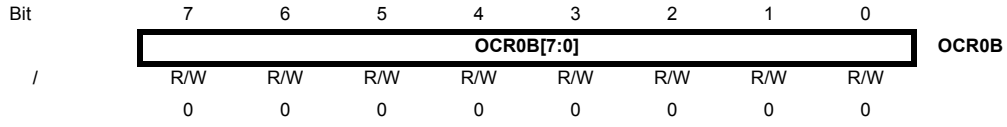
A OCR0A



8 TCNT0

OC0A

B OCR0B



8 TCNT0

OC0B

T/C TIMSK

Bit	7	6	5	4	3	2	1	0	
	TOIE1	OCIE1A	OCIE1B	–	ICIE1	OCIE0B	TOIE0	OCIE0A	TIMSK
/	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

- **Bit 4 – Res:**

- **Bit 2 – OCIE0B: T/C0 B**

  OCIE0B I ”1” T/C B T/C TIFR OCF0B

- **Bit 1 – TOIE0: T/C0**

  TOIE0 I ”1” T/C0 T/C0 TIFR TOV0

- **Bit 0 – OCIE0A: T/C0 A**

  OCIE0A I ”1” T/C0 A T/C0 TIFR OCF0A

T/C TIFR

Bit	7	6	5	4	3	2	1	0	
	TOV1	OCF1A	OCF1B	–	ICF1	OCF0B	TOV0	OCF0A	TIFR
/	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

- **Bit 4 – Res:**

- **Bit 2 – OCF0B: 0 B**

  T/C OCR0B(0B) OCF0B 1 SREG I OCIE0B(T/C0 B) OCF0B

- **Bit 1 – TOV0: T/C0**

  T/C0 TOV0 TOV0 1 SREG I TOIE0(T/C0) TOV0

  WGM02:0 Table 40 P71“ ”

- **Bit 0 – OCF0A: 0 A**

  T/C0 OCR0A(0) OCF0A 1 SREG I OCIE0A(T/C0) OCF0A

T/C0 T/C1

T/C1 T/C0 T/C1
T/C0

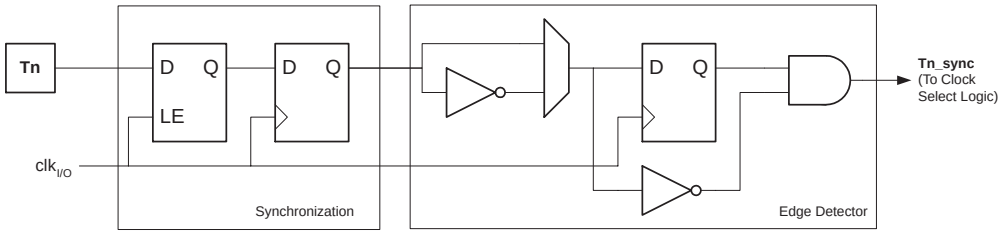
CSn2:0 = 1 T/C T/C
$f_{CLK\_I/O}$ 4 $f_{CLK\_I/O}/8$
$f_{CLK\_I/O}/64$ $f_{CLK\_I/O}/256$ $f_{CLK\_I/O}/1024$

T/C T/C1
T/C0 T/C
(6 >
CSn2:0 > 1) 1 N+1
N (8 64 256 1024)
T/C
T/C T/C

T1/T0 T/C clk_{T1}/clk_{T0}
T1/T0 ( ) Figure 37
T1/T0 $clk_{I/O}$

CSn2:0 = 7 clk_{T1} CSn2:0 = 6
clk_{T1}/clk_{T0}

Figure 37. T1/T0

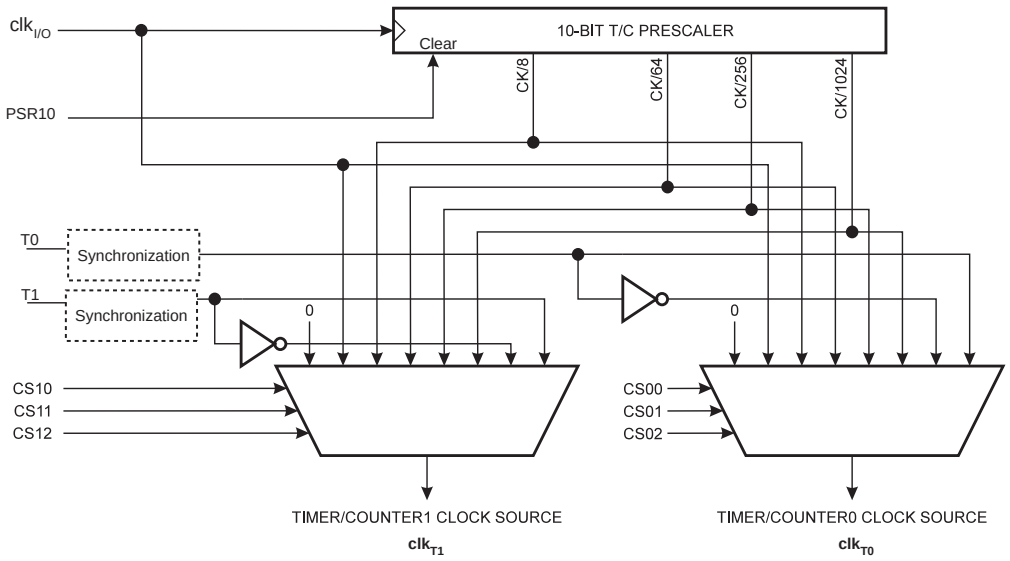


T1/T0 2.5 3.5

T1/T0
T/C

50%
($f_{ExtClk} < f_{clk\_I/O}/2$)
(Nyquist)
( )
$f_{clk\_I/O}/2.5$

Figure 38. T/C0 T/C1 (1)



Note: 1. (T1/T0) Figure 37.

T/C GTCCR

Bit	7	6	5	4	3	2	1	0	
	—	–	–	–	–	–	—	PSR10	GTCCR
/	R	R	R	R	R	R	R	R/W	
	0	0	0	0	0	0	0	0	

- **Bits 7..1 – Res:**

- **Bit 0 – PSR10: T/C1 T/C0**

T/C1 T/C0
T/C1 T/C0

16 / 1

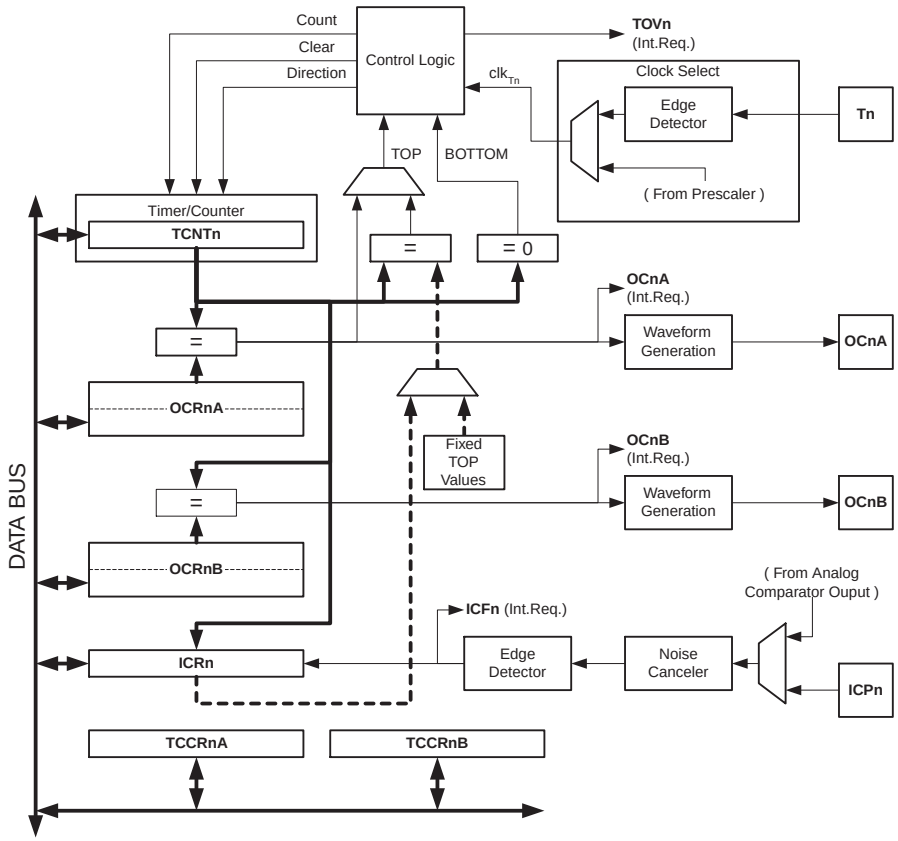
16 T/C ( )

- **16 (16 PWM)**
- **2**
- **(TOV1 OCF1A OCF1B ICF1)**

“n” T/C “x”
TCNT1 T/C1

16 T/C Figure 39 I/O P2“ATtiny2313
” CPU I/O I/O I/O I/O
P97“16 / ”

Figure 39. 16 T/C (1)



Note: 1. P2Figure 1 P56Table 25 P61Table 31 T/C1

/ TCNT1 OCR1A/B ICR1 16
16 P78“ 16 ” T/C
TCCR1A/B 8 CPU (

Int.Req.) TIFR1
TIMSK TIFR TIMSK

T/C T1 T/C (
) T/C
clk_{T1}

OCR1A/B T/C
PWM OC1A/B P84 “ ”
OCF1A/B

ICP1 (P141 “ ”)
( ) T/C
( )

TOP T/C OCR1A ICR1
PWM OCR1A TOP OCR1A
PWM OCR1A TOP
TOP ICR1 OCR1A PWM

Table 42.

BOTTOM	0x0000 BOTTOM
MAX	0xFFFF (65535) MAX
TOP	TOP TOP 0x00FF 0x01FF 0x03FF OCR1A ICR1

16 T/C 16 AVRT/C

- 16 T/C I/O
- 16 T/C
-

- PWM10 WGM10
- PWM11 WGM11
- CTC1 WGM12

16 T/C
- TCCR1C FOC1A FOC1B
- TCCR1B WGM13

16 T/C

16

TCNT1 OCR1A/B ICR1 AVR CPU 8 16
16 16 8 8
16 16 16
CPU 16 8
8 16 16 CPU
16

16 OCR1A/B

16 16

16

OCR1A/B ICR1 “C”

16

(1)

```
...
;     TCNT1   0x01FF
ldi r17,0x01
ldi r16,0xFF
out TCNT1H,r17
out TCNT1L,r16
;    TCNT1    r17:r16
in  r16,TCNT1L
in  r17,TCNT1H
...
```

C (1)

```
unsigned int i;
...
/*     TCNT1   0x01FF */
TCNT1 = 0x1FF;
/*   TCNT1    i */
i = TCNT1;
...
```

Note: 1. I/O I/O “LDS” “STS” “SBRS” “SBRC” “SBR” “CBR” I/O “IN” “OUT” “SBIS” “SBIC” “CBI” “SBI”

r17:r16 TCNT1

16 16

16

16

16

TCNT1 OCR1A/B ICR1

(1)

```
TIM16_ReadTCNT1:
  ;
  in  r18,SREG
  ;
  cli
  ;   TCNT1    r17:r16
  in  r16,TCNT1L
  in  r17,TCNT1H
  ;
  out SREG,r18
  ret
```

C (1)

```
unsigned int TIM16_ReadTCNT1( void )
{
  unsigned char sreg;
  unsigned int i;
  /*               */
  sreg = SREG;
  /*        */
  _CLI();
  /*   TCNT1    i */
  i = TCNT1;
  /*               */
  SREG = sreg;
  return i;
}
```

Note: 1. I/O I/O
r17:r16
“LDS” “STS” “SBRS” “SBRC” “SBR” “CBR” I/O
“IN” “OUT” “SBIS” “SBIC” “CBI” “SBI”

TCNT1

TCNT1 OCR1A/B ICR1

(1)
TIM16_WriteTCNT1: ; **in** r18,SREG ; **cli** ; *TCNT1* r17:r16 **out** TCNT1H,r17 **out** TCNT1L,r16 ; **out** SREG,r18 **ret**
C (1)

void TIM16_WriteTCNT1 (**unsigned int i**)
{
unsigned char sreg;
unsigned int i;
/* */
sreg = SREG;
/* */
_CLI();
/* *TCNT1* *i* */
TCNT1 = i;
/* */
SREG = sreg;
}

Note: 1.
I/O I/O
“LDS” “STS” “SBRS” “SBRC” “SBR” “CBR” I/O
“IN” “OUT” “SBIS” “SBIC” “CBI” “SBI”

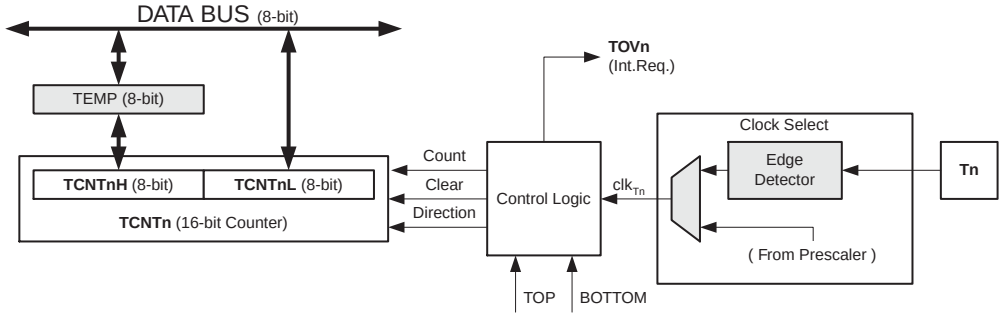
r17:r16 TCNT1

16

/ T/C T/C B(TCCR1B) (CS12:0) P75“T/C0 T/C1 ”

16 T/C 16 Figure 40

Figure 40.



( )

Count TCNT1 1 1

Direction

Clear TCNT1

clk$_{T1}$ /

TOP TCNT1

BOTTOM TCNT1 (0)

16 8 I/O TCNT1H 8 TCNT1L 8 CPU TCNT1H CPU TCNT1H (TEMP) TCNT1L TCNT1H TCNT1L TCNT1H CPU 8 16 TCNT1

clk$_{T1}$ 1 1 clk$_{T1}$ CS12:0 CS12:0= 0 CPU TCNT1 clk$_{T1}$ CPU

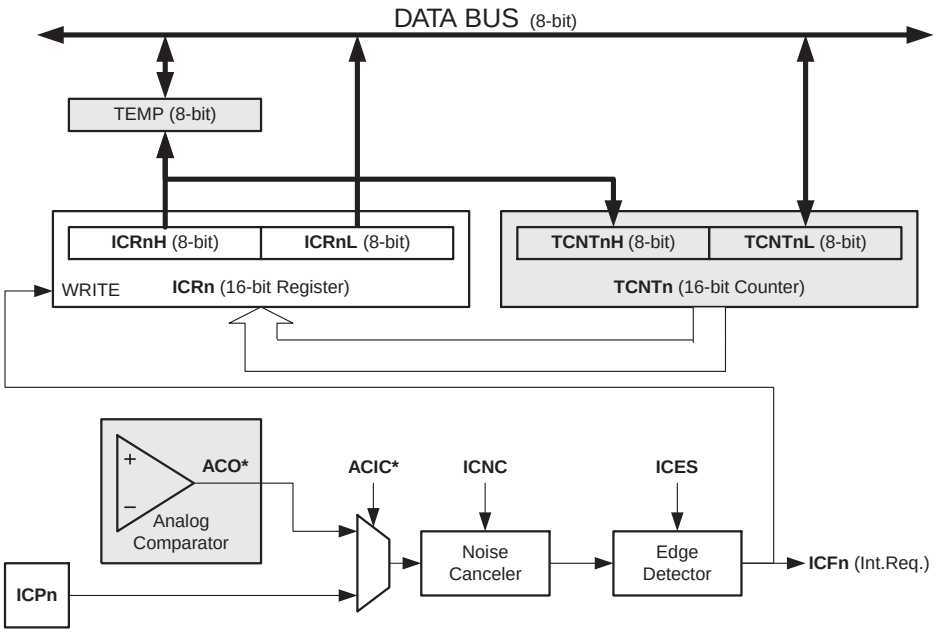
TCCR1A TCCR1B WGM13:0 ( ) OC1x P87“ ”

WGM13:0 TOV1 TOV1 CPU

T/C ICP1

Figure 41 “n” /

Figure 41.



ICP1 ( ) ACO
16 TCNT1
ICR1 ICF1 ICIE1 = 1
ICF1
I/O "1”

ICR1 ICR1L ICR1H
TEMP CPU ICR1H TEMP

ICR1 ICR1 TOP
ICR1 WGM13:0 ICR1
ICR1H I/O ICR1L

P78“ 16 ” 16

ICP1 T/C1
ACSR ACIC

ICP1 ACO T1 (P75Figure 37),
4
ICR1 TOP T/C

ICP1

4
4

TCCR1B ICNC1 ICR1
4

ICR1 ICR1

ICR1

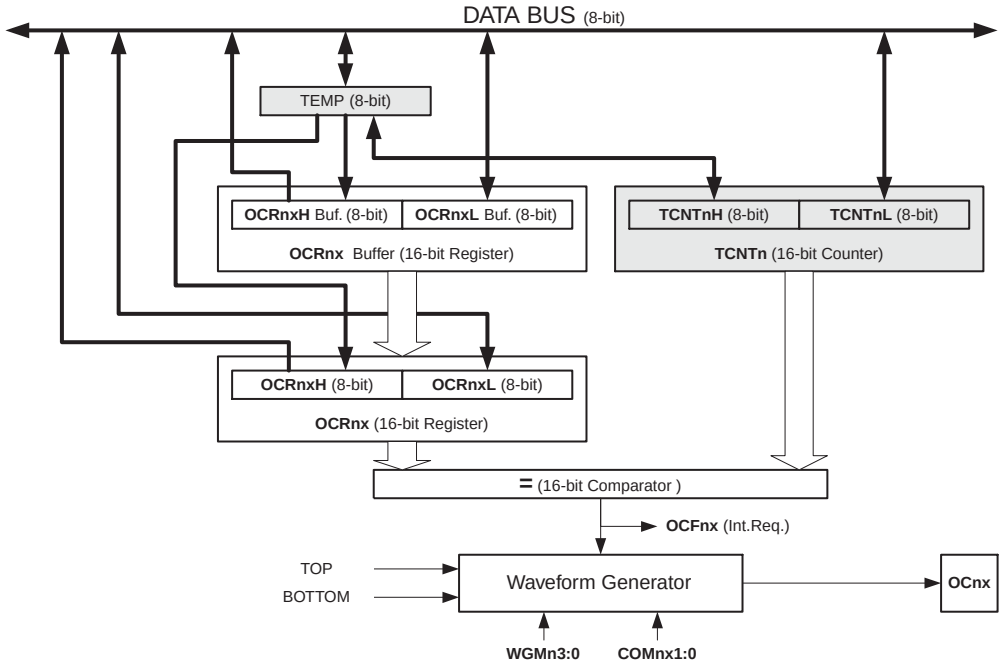
TOP

ICR1
ICF1 (I/O "1”)
ICF1

16 TCNT1 OCR1x
OCF1x OCIE1x = 1 OCF1x
OCF1x I/O
"1” WGM13:0 COM1x1:0
TOP BOTTOM
(P87 “ ”)
A T/C TOP ( ) TOP

Figure 42 “n” (n = 1
T/C1) “x” (A/B)

Figure 42.



T/C 12 PWM OCR1x
(CTC) OCR1x
TOP BOTTOM PWM
OCR1x CPU OCR1x
CPU OCR1x OCR1x( )
(T/C TCNT1 ICR1

) OCR1x TEMP 16
OCR1x TEMP
OCR1xH CPU I/O
TEMP OCR1xL TEMP
OCR1x OCR1x

P78“ 16 ” 16

PWM FOC1x ”1”
OCF1x / OC1x
(COMx1:0 OC1x
)

TCNT1 CPU TCNT1 OCR1x
TCNT1

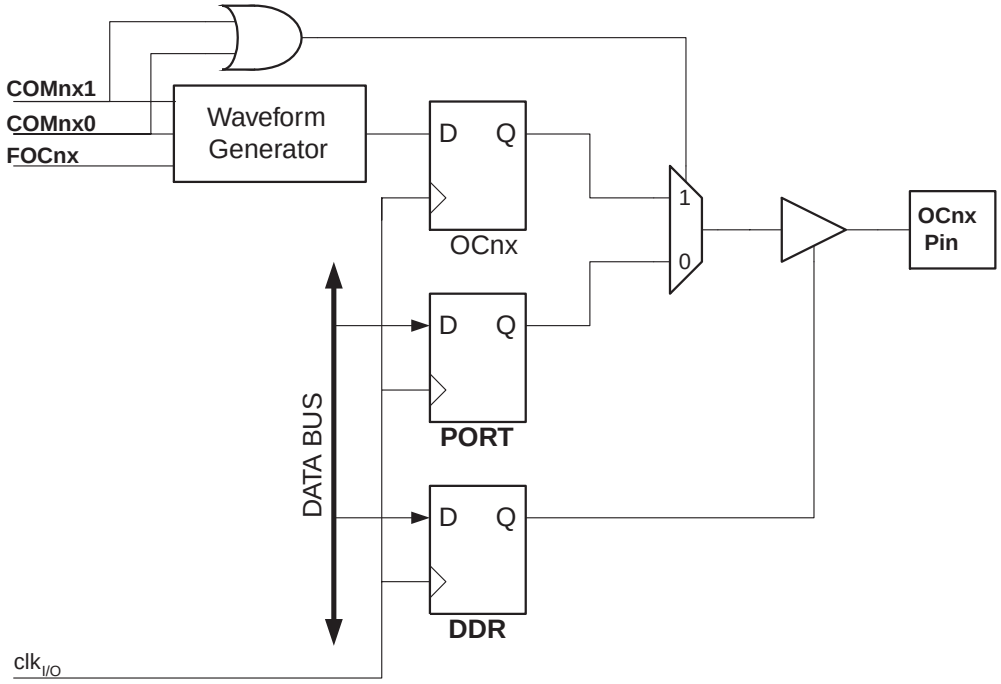
TCNT1
TCNT1 T/C TCNT1 OCR1x
PWM TOP
TCNT1 TOP
0xFFFF TCNT1 BOTTOM

OC1x OC1x
FOC1x OC1x

COM1x1:0 COM1x1:0

COM1x1:0 COM1x1:0
OC1x COM1x1:0 OC1x
Figure 43 COM1x1:0 I/O I/O I/O
COM1x1:0 I/O (DDR PORT)
OC1x OC1x OC1x
COM1x "0”

Figure 43.



COM1x1:0 OC1x I/O
OC1x (DDR) OC1x
DDR_OC1x
Table 43 Table 44 Table
45
OC1x COM1x1:0
P97 “16 / ”
COM1x1:0

COM1x1:0 CTC PWM
COM1x1:0 = 0 OC1x
PWM P97Table 43 PWM P97Table 44 PWM P98Table 45

COM1x1:0 PWM
FOC1x

- T/C - (WGM13:0) (COM1x1:0)
COM1x1:0 PWM PWM COM1x1:0
(P86 “ ”)

P95“ / ”

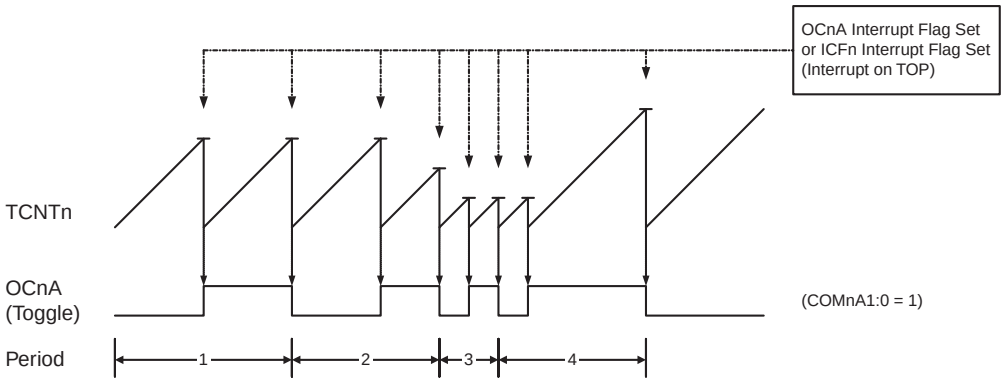
(WGM13:0 = 0)
(MAX = 0xFFFF) 0x0000
TCNT1 T/C TOV1 TOV1 17
TOV1

CPU

CTC( ) CTC (WGM13:0 = 4 12) OCR1A ICR1
TCNT1 OCR1A(WGM13:0 = 4) ICR1 (WGM13:0 = 12)
OCR1A ICR1 TOP

CTC P87Figure 44 TCNT1 TCNT1 OCR1A
ICR1 TCNT1

Figure 44. CTC



OCF1A ICF1 TOP
TOP CTC
TOP BOTTOM OCR1A
ICR1 TCNT1

0xFFFF 0x0000 OCR1A
ICR1 PWM
OCR1A TOP (WGM13:0 = 15) OCR1A
CTC OC1A
COM1A1:0 = 1 OC1A
(DDR_OC1A = 1) $f_{OC2} = f_{clk\_I/O}/2$ (OCR1A = 0x0000)

$$f_{OCnA} = \frac{f_{clk\_I/O}}{2 \cdot N \cdot (1 + OCRnA)}$$

N (1 8 64 256 1024)
TOV1 MAX 0x0000

PWM

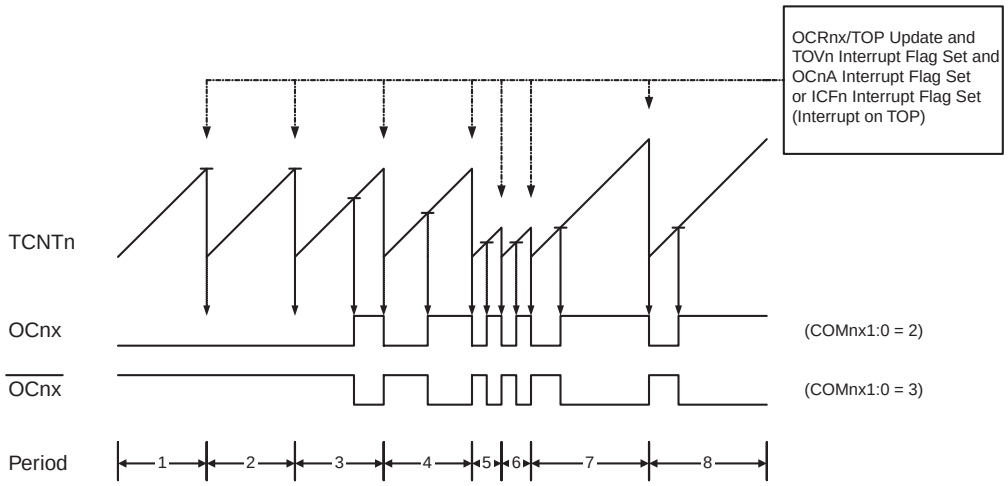
PWM (WGM13:0 = 5 6 7 14 15) PWM
PWM PWM BOTTOM
TOP BOTTOM OC1x
TCNT1 OCR1x TOP OCR1x
PWM
PWM PWM
DAC ( )

PWM PWM 8 9 10 ICR1 OCR1A
2 (ICR1 OCR1A 0x0003) 16 (ICR1
OCR1A MAX) PWM

$$R_{FPWM} = \frac{\log(TOP + 1)}{\log(2)}$$

PWM 0x00FF 0x01FF 0x03FF
(WGM13:0 = 5 6 7) ICR1 (WGM13:0 = 14) OCR1A (WGM13:0 = 15)
Figure 45 OCR1A ICR1
TOP PWM TCNT1
PWM PWM TCNT1
OCR1x TCNT1 OC1x

Figure 45. PWM



TOP T/C TOV1 TOP OCR1A ICR1
OC1A ICF1 TOV1
TOP

TOP TOP TCNT1 OCR1x
TOP OCR1x
"0”

TOP ICR1 OCR1A ICR1
ICR1
ICR1 TCNT1
0xFFFF
0x0000 OCR1A
OCR1A OCR1A TCNT1 TOP
OCR1A
TCNT1 TOV1

TOP ICR1 TOP OCR1A OC1A
PWM PWM (TOP) OCR1A

PWM OC1x PWM COM1x1:0
2 PWM 3 PWM (P97Table 43)
OC1x DDR_OC1x
PWM OC1x OCR1x TCNT1 ( )
(TOP BOTTOM) ( )

PWM

$$f_{OCnxPWM} = \frac{f_{clk\_I/O}}{N \cdot (1 + TOP)}$$

N (1 8 64 256 1024)

OCR1x PWM OCR1x
BOTTOM(0x0000) TOP+1 OCR1x TOP
COM1x1:0

OC1A (COM1A1:0 = 1)
50% OCR1A TOP (WGM13:0 = 15) OCR1A
0(0x0000) $f_{oc2} = f_{clk\_I/O}/2$ CTC OC1A
PWM

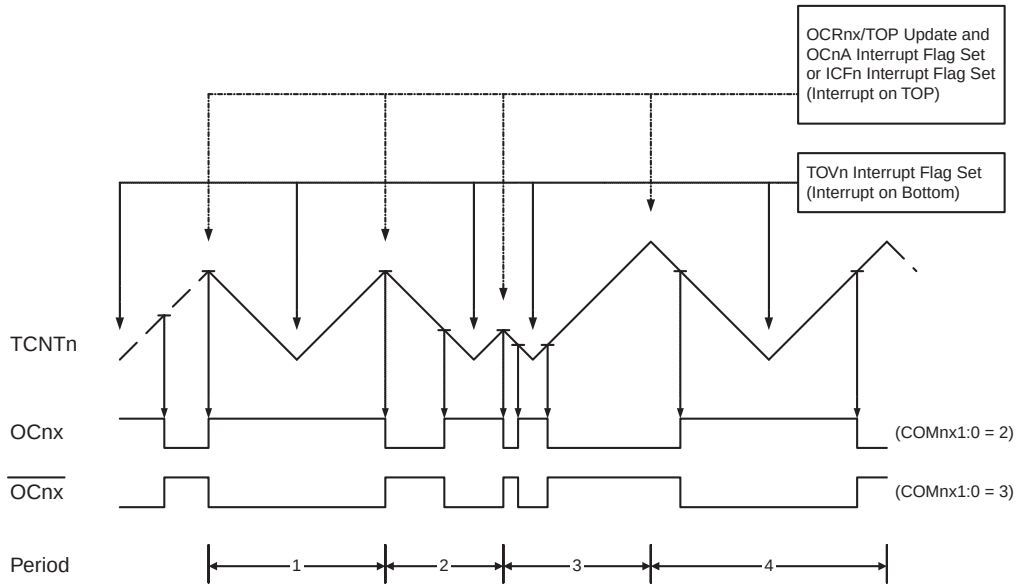
PWM PWM (WGM13:0 = 1 2 3 10 11)
PWM
BOTTOM TOP TOP BOTTOM
TOP TCNT1 OCR1x OC1x
BOTTOM TCNT1 OCR1x OC1x

PWM PWM 8 9 10 ICR1 OCR1A
2 (ICR1 OCR1A 0x0003) 16 (ICR1 OCR1A
MAX) PWM

$$R_{PCPWM} = \frac{\log(TOP + 1)}{\log(2)}$$

PWM 0x00FF 0x01FF
0x03FF (WGM13:0 = 1 2 3) ICR1 (WGM13:0 = 10) OCR1A (WGM13:0 = 11)
TCNT1 TOP Figure
46 OCR1A ICR1 TOP PWM
TCNT1 PWM PWM
TCNT1 OCR1x TCNT1 OC1x

Figure 46. PWM



BOTTOM T/C TOV1 TOP OCR1A ICR1
OCR1x OC1A ICF1

TOP TOP TCNT1 OCR1x
TOP OCR1x
"0” Figure 46 T/C
TOP OCR1x OCR1x
/ TOP PWM
TOP TOP

T/C TOP TOP

PWM OC1x PWM
COM1x1:0 2 PWM COM1x1:0 3 PWM (
P97Table 44) OC1x DDR_OC1x
OCR1x TCNT1 OC1x
PWM PWM

$$f_{OCnxPCPWM} = \frac{f_{clk\_I/O}}{2 \cdot N \cdot TOP}$$

N (1 8 64 256 1024)

OCR1x PWM PWM
OCR1x BOTTOM OCR1x TOP
PWM

PWM PWM (WGM13:0 = 8 9) - PWM -
PWM PWM
BOTTOM TOP TOP
BOTTOM TOP TCNT1 OCR1x
OC1x BOTTOM TCNT1 OCR1x OC1x

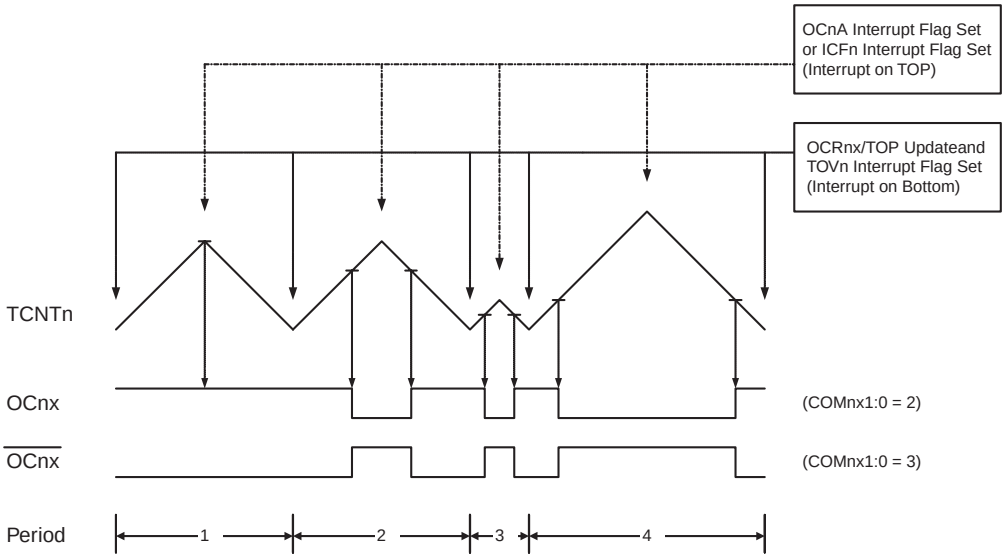
PWM PWM OCR1x
Figure 46 Figure 47

PWM PWM ICR1 OCR1A 2
(ICR1 OCR1A 0x0003) 16 (ICR1 OCR1A MAX)
PWM

$$R_{PFCPWM} = \frac{\log(TOP + 1)}{\log(2)}$$

PWM ICR1 (WGM13:0 = 8) OCR1A
(WGM13:0 = 9) TCNT1 TOP
Figure 47 OCR1A ICR1 TOP
PWM TCNT1 PWM
PWM TCNT1 OCR1x TCNT1
OC1x

Figure 47. PWM



OCR1x T/C TOV1
TOP OCR1A ICR1 TCNT1 TOP OC1A ICF1
TOP BOTTOM

TOP TOP TCNT1 OCR1x

Figure 47 PWM
OCR1x BOTTOM

TOP ICR1 TOP OCR1A OC1A
PWM PWM (TOP) OCR1A

PWM OC1x PWM
COM1x1:0 2 PWM 3 PWM (
P98Table 45) OC1x PWM
OC1x OCR1x TCNT1 ( )
TCNT1 ( ) PWM

$$f_{OCnxPFCPWM} = \frac{f_{clk\_I/O}}{2 \cdot N \cdot TOP}$$

N (1 8 64 256 1024)

OCR1x PWM PWM
OCR1x BOTTOM OCR1x TOP
PWM

/ / clk_{T1}
OCR1x OCR1x (
) Figure 48 OCF1x

Figure 48. T/C OCF1x

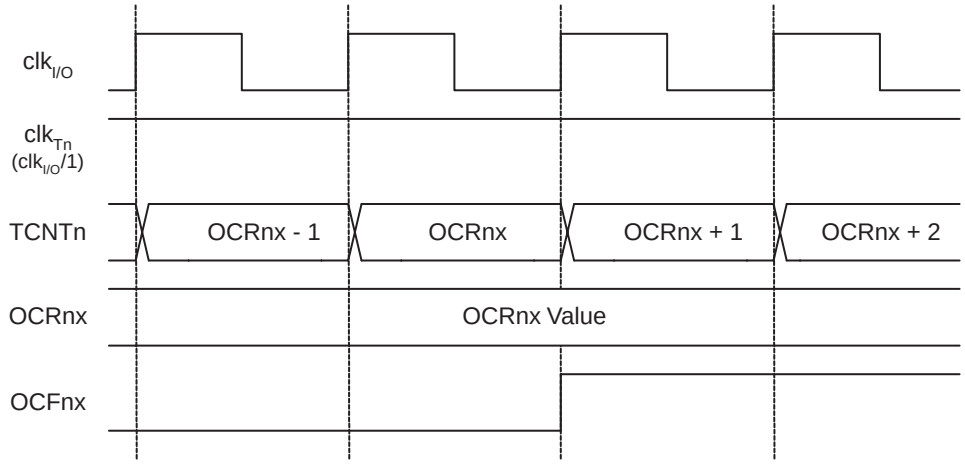


Figure 49

Figure 49. T/C OCF1x $f_{clk\_I/O}$/8

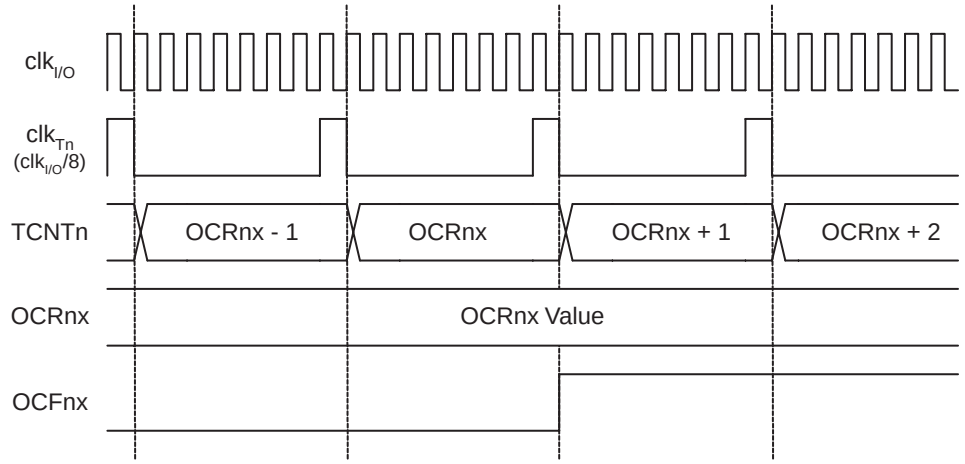


Figure 50 TOP PWM
OCR1x BOTTOM TOP BOTTOM
BOTTOM+1 TOP-1 BOTTOM TOV1

Figure 50. T/C

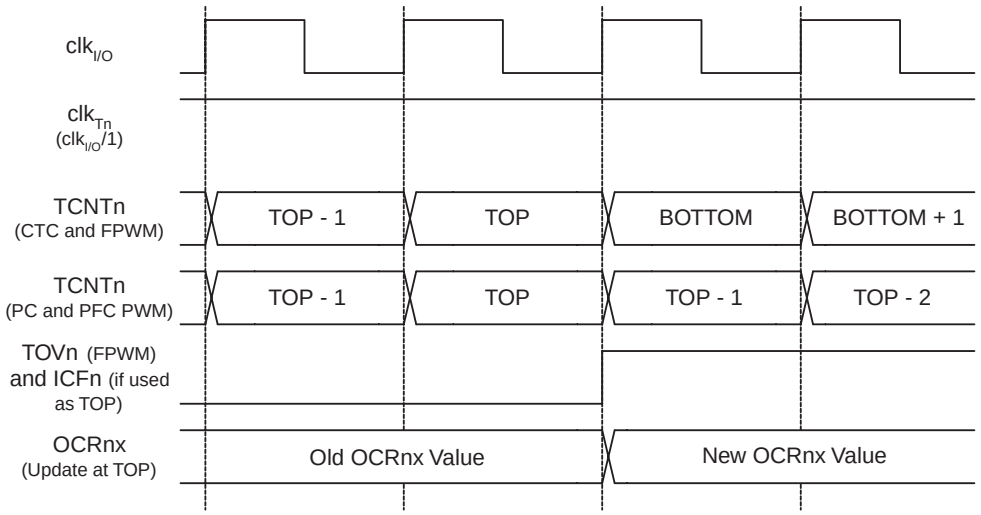
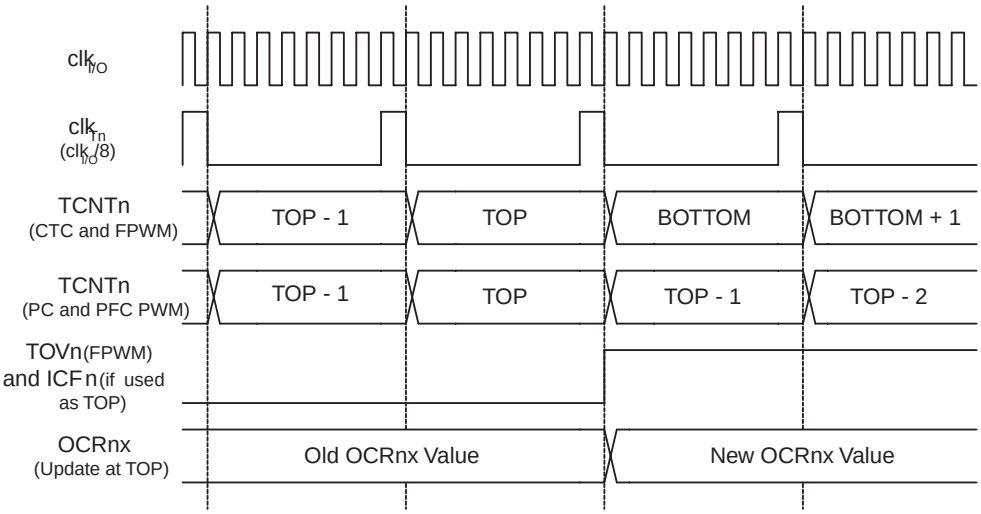


Figure 51

Figure 51. T/C $f_{clk\_I/O}/8$



16 /

T/C1 A TCCR1A

Bit	7	6	5	4	3	2	1	0	
	COM1A1	COM1A0	COM1B1	COM1B0	–	–	WGM11	WGM10	TCCR1A
/	R/W	R/W	R/W	R/W	R	R	R/W	R/W	
	0	0	0	0	0	0	0	0	

- **Bit 7:6 – COM1A1:0: A**
- **Bit 5:4 – COM1B1:0: B**

COM1A1:0 COM1B1:0 OC1A OC1B COM1A1:0
"1" OC1A I/O COM1B1:0
"1" OC1B I/O OC1A OC1B

OC1A(OC1B) COM1x1:0 WGM13:0 Table 43 WGM13:0 CTC (PWM) COM1x1:0

Table 43. PWM

COM1A1/COM1B1	COM1A0/COM1B0	
0	0	OC1A/OC1B
0	1	OC1A/OC1B
1	0	OC1A/OC1B( )
1	1	OC1A/OC1B( )

Table 44 WGM13:0 PWM COM1x1:0

Table 44. PWM(1)

COM1A1/COM1B1	COM1A0/COM1B0	
0	0	OC1A/OC1B
0	1	WGM13=0: OC1A/OC1B WGM13=1: OC1A OC1B
1	0	OC1A/OC1B TOP OC1A/OC1B
1	1	OC1A/OC1B TOP OC1A/OC1B

Note: 1. OCR1A/OCR1B TOP COM1A1/COM1B1
OC1A/OC1B / P89 “ PWM ”

Table 45 WGM13:0 PWM PWM COM1x1:0

Table 45. PWM [1]

COM1A1/COM1B1	COM1A0/COM1B0	
0	0	OC1A/OC1B
0	1	WGM13=0: OC1A/OC1B WGM13=1: OC1A OC1B/OCnC
1	0	OC1A/OC1B OC1A/OC1B
1	1	OC1A/OC1B OC1A/OC1B

Note: 1. OCR1A/OCR1B TOP COM1A1/COM1B1 P91 “ PWM ”

- **Bit 1:0 – WGM11:0:**

TCCR1B WGM13:2 —— Table 46 T/C ( ) (CTC) (PWM) (P87 “ ”)

Table 46. (1)

Mode	WGM13	WGM12 (CTC1)	WGM11 (PWM11)	WGM10 (PWM10)	/	TOP	OCR1x	TOV1
0	0	0	0	0		0xFFFF		MAX
1	0	0	0	1	8 PWM	0x00FF	TOP	BOTTOM
2	0	0	1	0	9 PWM	0x01FF	TOP	BOTTOM
3	0	0	1	1	10 PWM	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCR1A		MAX
5	0	1	0	1	8 PWM	0x00FF	TOP	TOP
6	0	1	1	0	9 PWM	0x01FF	TOP	TOP
7	0	1	1	1	10 PWM	0x03FF	TOP	TOP
8	1	0	0	0	PWM	ICR1	BOTTOM	BOTTOM
9	1	0	0	1	PWM	OCR1A	BOTTOM	BOTTOM
10	1	0	1	0	PWM	ICR1	TOP	BOTTOM
11	1	0	1	1	PWM	OCR1A	TOP	BOTTOM
12	1	1	0	0	CTC	ICR1		MAX
13	1	1	0	1		–	–	–
14	1	1	1	0	PWM	ICR1	TOP	TOP
15	1	1	1	1	PWM	OCR1A	TOP	TOP

Note: 1. CTC1 PWM11:0 WGM12:0

T/C1 B TCCR1B

Bit	7	6	5	4	3	2	1	0	
	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	TCCR1B
/	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

- **Bit 7 – ICNC1:**

  ICNC1 ICP1
  ICP1 4 4
  4

- **Bit 6 – ICES1:**

  ICP1 ICES1 "0”
  ICES1 "1”

  ICES1
  ICF1

  ICR1 TOP (TCCR1A TCCR1B WGM

- **Bit 5 –**

  TCCR1B

- **Bit 4:3 – WGM13:2:**

  TCCR1A

- **Bit 2:0 – CS12:0:**

  3 T/C Figure 48 Figure 49

Table 47.

CS12	CS11	CS10	
0	0	0	(T/C)
0	0	1	$clk_{I/O}$/1 ( )
0	1	0	$clk_{I/O}$/8 ( )
0	1	1	$clk_{I/O}$/64 ( )
1	0	0	$clk_{I/O}$/256 ( )
1	0	1	$clk_{I/O}$/1024 ( )
1	1	0	T1
1	1	1	T1

T1 1
T/C1

T/C1 C TCCR1C

Bit	7	6	5	4	3	2	1	0	
	FOC1A	FOC1B	–	–	–	–	–	–	TCCR1C
/	W	W	R	R	R	R	R	R	
	0	0	0	0	0	0	0	0	

- **Bit 7 – FOC1A: A**
- **Bit 6 – FOC1B: B**

FOC1A/FOC1B WGM13:0 PWM
PWM TCCR1A 1 FOC1A/FOC1B "1”
COM1x1:0
OC1A/OC1B FOC1A/FOC1B COM1x1:0

FOC1A/FOC1B OCR1A
TOP CTC

FOC1A/FOC1B

T/C1 TCNT1H TCNT1L

Bit	7	6	5	4	3	2	1	0	
	TCNT1[15:8]								TCNT1H
	TCNT1[7:0]								TCNT1L
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

TCNT1H TCNT1L T/C1 TCNT1 /
16 CPU
8 TEMP TEMP 16 P78
“ 16 ”

TCNT1 TCNT1 OCR1x

TCNT1

1A OCR1AH OCR1AL

Bit	7	6	5	4	3	2	1	0	
	OCR1A[15:8]								OCR1AH
	OCR1A[7:0]								OCR1AL
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

1B OCR1BH
OCR1BL

Bit	7	6	5	4	3	2	1	0	
	OCR1B[15:8]								OCR1BH
	OCR1B[7:0]								OCR1BL
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

16 TCNT1
OC1x

16 CPU
8 TEMP TEMP 16 P78 “
16 ”

1 ICR1H
ICR1L

Bit	7	6	5	4	3	2	1	0	
	ICR1[15:8]								ICR1H
	ICR1[7:0]								ICR1L
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

ICP1(T/C1) TCNT1
ICR1 ICR1 TOP

16 CPU
8 TEMP TEMP 16 P78 “
16 ”

/
TIMSK

Bit	7	6	5	4	3	2	1	0	
	TOIE1	OCIE1A	OCIE1B	–	ICIE1	OCIE0B	TOIE0	OCIE0A	TIMSK
/	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

- **Bit 7 – TOIE1:T/C1**

"1” I ”1” T/C1
TIFR TOV1 CPU T/C1 (P42 “ ”)

- **Bit 6 – OCIE1A: T/C1 A**

"1” I "1” T/C1 A
TIFR1 OCF1A CPU T/C1 A
(P42 “ ”)

- **Bit 5 – OCIE1B: T/C1 B**

"1” I "1” T/C1 B
TIFR1 OCF1B CPU T/C1 B
(P42 “ ”)

- **Bit 3 – ICIE1: T/C1**

"1” I "1” T/C1
TIFR1 ICF1 CPU T/C1 (P42 “ ”)

T/C TIFR

Bit	7	6	5	4	3	2	1	0	
	TOV1	OCF1A	OCF1B	–	ICF1	OCF0B	TOV0	OCF0A	TIFR
/	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

- **Bit 7 – TOV1: T/C1**

  T/C1 CTC T/C1 TOV1
  TOV1 P99Table 46

  TOV1 "1”

- **Bit 6 – OCF1A: T/C1 A**

  TCNT1 OCR1A "1”

  (FOC1A) OCF1A

  A OCF1A "1”

- **Bit 5 – OCF1B: T/C1 B**

  TCNT1 OCR1B "1”

  (FOC1B) OCF1B

  B OCF1B "1”

- **Bit 3 – ICF1: T/C1**

  ICP1 ICF1 ICR1 TOP
  TOP ICF1

  ICF1 "1”

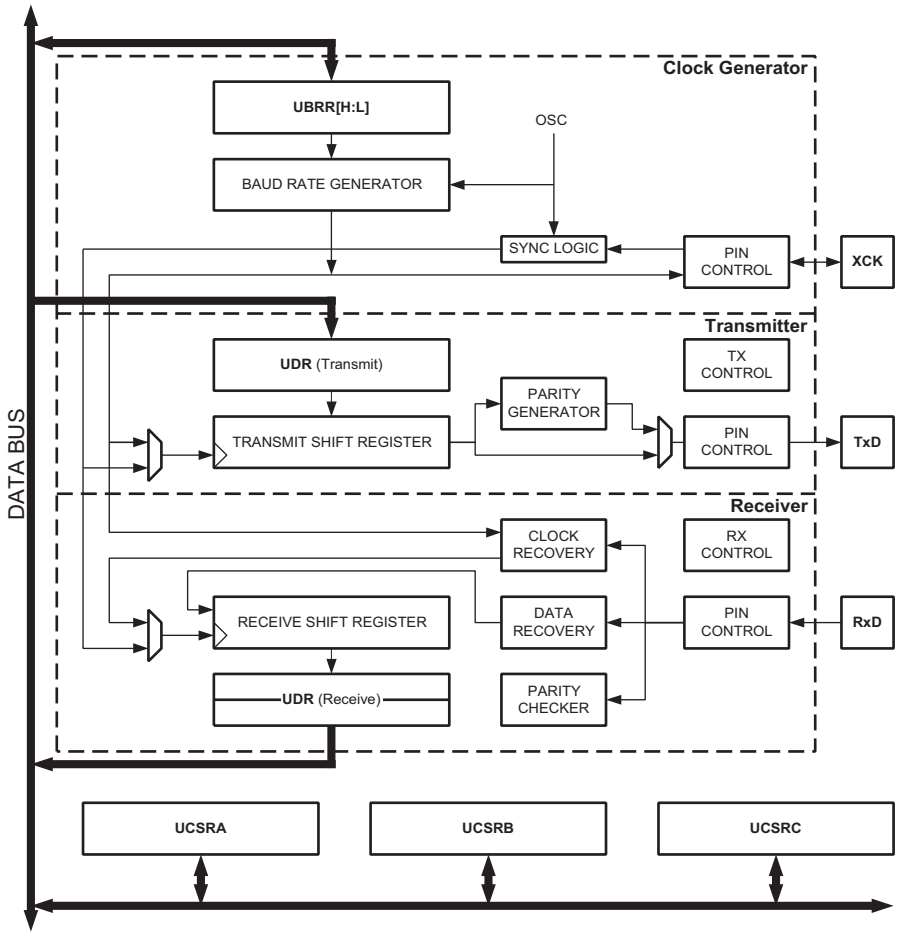
USART

(USART)

- ( )
-
-
-
- **5, 6, 7, 8, 9 1 2**
-
-
-
-
-
- ,
-
-

Figure 52 USART CPU I/O I/O

Figure 52. USART (1)



Note: 1. P2Figure 1 P55Table 29 P53Table 26 USART

USART

XCK ( )

USART

UDR

AVR USART AVR UART USART AVR UART

- USART
-
-
-
-

- FIFO
FE DOR 9 RXB8
UDR

-
(Figure 52)
USART (DOR)

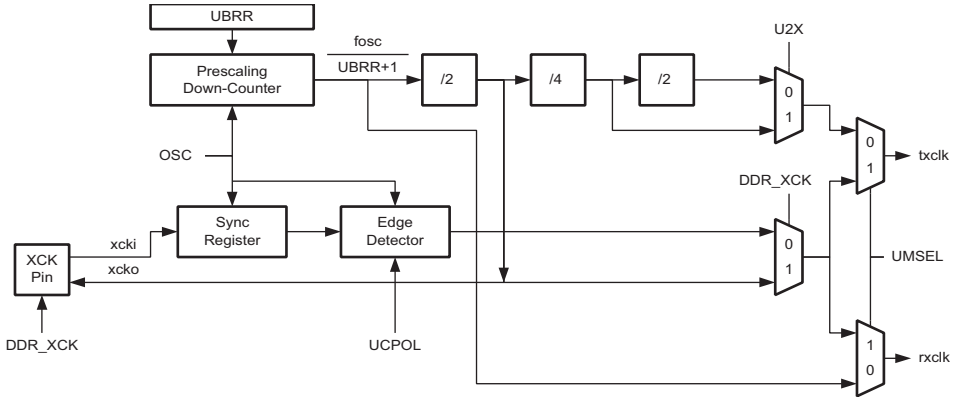
:

- CHR9 UCSZ2
- OR DOR

USART 4 :
USART
C (UCSRC) ( )
UCSRA U2X (UMSEL = 1) XCK
(DDR_XCK) ( ) ( )
XCK

Figure 53

Figure 53.



txclk ( )

rxclk ( )

xcki XCK ( )

xcko XCK ( ).

fosc XTAL ( )

Figure 53

USART UBRR

UBRRL

UBRR

f_{osc}/(UBRR+1) 2 8

16

2 8 16 UMSEL

U2X DDR_XCK

Table 48 (/) UBRR

Table 48.

	(1)	UBRR
(U2X = 0)	$BAUD = \frac{f_{OSC}}{16(\mathbf{UBRR}+1)}$	$\mathbf{UBRR} = \frac{f_{OSC}}{16BAUD} - 1$
(U2X = 1)	$BAUD = \frac{f_{OSC}}{8(\mathbf{UBRR}+1)}$	$\mathbf{UBRR} = \frac{f_{OSC}}{8BAUD} - 1$
	$BAUD = \frac{f_{OSC}}{2(\mathbf{UBRR}+1)}$	$\mathbf{UBRR} = \frac{f_{OSC}}{2BAUD} - 1$

Note: 1. (bps)

BAUD (bps)

f_{OSC}

UBRR UBRRH UBRRL (0-4095)

Table 56 UBRR

(U2X) UCSRA U2X
"0”

16 8

Figure 53

XCK

CPU

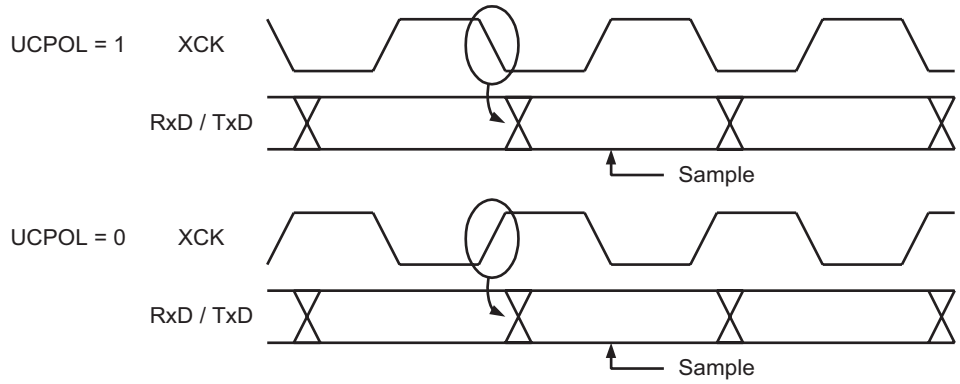
XCK

$$f_{XCK} < \frac{f_{OSC}}{4}$$

f_{osc}

(UMSEL = 1)XCK ( ) (
)
TxD XCK RxD

Figure 54. XCK .



UCRSC UCPOL XCK
Figure 54 UCPOL=0 XCK XCK
UCPOL=1 XCK XCK

( )

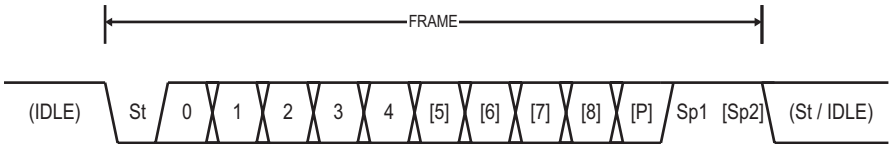
USART 30

- 1
- 5 6 7 8 9
-
- 1 2

9

Figure
55

Figure 55.



St

(n) (0 8)

P

Sp

IDLE (RxD TxD)

UCSRB UCSRC UCSZ2:0 UPM1:0 USBS

USART UCSZ2:0 UPM1:0
USBS
(FE) "0”

:

$$P_{even} = d_{n-1} \oplus \ldots \oplus d_3 \oplus d_2 \oplus d_1 \oplus d_0 \oplus 0$$
$$P_{odd} = d_{n-1} \oplus \ldots \oplus d_3 \oplus d_2 \oplus d_1 \oplus d_0 \oplus 1$$

P_{even}

P_{odd}

d_n n

USART

USART

USART

( )

USART TXC

RXC

(UDR)TXC

USART ( )

r17:r16

(1)

```
USART_Init:
  ;
  out   UBRRH, r17
  out   UBRRL, r16
  ;
  ldi   r16, (1<<RXEN)|(1<<TXEN)
  out   UCSRB,r16
  ;         : 8       , 2
  ldi   r16, (1<<USBS)|(3<<UCSZ0)
  out   UCSRC,r16
  ret
```

C (1)

```
void USART_Init( unsigned int baud )
{
  /*          */
  UBRRH = (unsigned char)(baud>>8);
  UBRRL = (unsigned char)baud;
  /*                */
  UCSRB = (1<<RXEN)|(1<<TXEN);
  /*          : 8       , 2        */
  UCSRC = (1<<USBS)|(3<<UCSZ0);
}
```

Note: 1. I/O I/O “LDS” “STS” “SBRS” “SBRC” “SBR” “CBR” I/O “IN” “OUT” “SBIS” “SBIC” “CBI” “SBI”

I/O

USART UCSRB TXEN USART TxD
I/O USART
XCK

5 8 CPU UDR

( )

UDRE 8
UDR
USART R16

(1)

```
USART_Transmit:
  ;
  sbis  UCSRA,UDRE
  rjmp  USART_Transmit
  ;
  out   UDR,r16
  ret
```

C (1)

```
void USART_Transmit( unsigned char data )
{
  /*                 */
  while ( !( UCSRA & (1<<UDRE)) )
        ;
  /*                       */
  UDR = data;
}
```

Note: 1. I/O I/O "LDS" "STS" "SBRS" "SBRC" "SBR" "CBR" I/O "IN" "OUT" "SBIS" "SBIC" "CBI" "SBI"

UDRE

9 9 (UCSZ = 7) 9 UCSRB TXB8 8 UDR 9 R17:R16

(1)(2)

```
USART_Transmit:
  ;
  sbis  UCSRA,UDRE
  rjmp  USART_Transmit
  ;    9    r17        TXB8
  cbi   UCSRB,TXB8
  sbrc  r17,0
  sbi   UCSRB,TXB8
  ;    8
  out   UDR,r16
  ret
```

C (1)(2)

```
void USART_Transmit( unsigned int data )
{
  /*                 */
  while ( !( UCSRA & (1<<UDRE))) )
       ;
  /*     9       TXB8 */
  UCSRB &= ~(1<<TXB8);
  if ( data & 0x0100 )
    UCSRB |= (1<<TXB8);
  /*                        */
  UDR = data;
}
```

Notes: 1. UCSRB UCSRB TXB8

2. I/O I/O “LDS” “STS” “SBRS” “SBRC” “SBR” “CBR” I/O “IN” “OUT” “SBIS” “SBIC” “CBI” “SBI”

9

USART USART UDRE TXC

UDRE
"1”
UCSRA "0”
UCSRB UDRIE "1” UDRE (
) USART UDR
UDRE
UDR UDRE

TXC TXC "1” TXC
RS-485

UCSRB TXCIE "1” TXC
USART TXC
TXC

(UPM1 = 1)

TXEN
TxD I/O

USART UCSRB (RXEN) USART RxD
USART
XCK

5 8
XCK

UDR
RXC 8
UDR 0 USART

(1)

```
USART_Receive:
  ;
  sbis  UCSRA, RXC
  rjmp  USART_Receive
  ;
  in    r16, UDR
  ret
```

C (1)

```
unsigned char USART_Receive( void )
{
  /*            */
  while ( !(UCSRA & (1<<RXC)) )
        ;
  /*                      */
  return UDR;
}
```

Note: 1.
I/O I/O "LDS" "STS" "SBRS" "SBRC" "SBR" "CBR" I/O "IN" "OUT" "SBIS" "SBIC" "CBI" "SBI"

RXC

9

9 (UCSZ=7) UDR 8
UCSRB RXB8 9 FE DOR
UPE UCSRA UDR UDR
FIFO FIFO TXB8 FE DOR UPE

USART 9

(1)

```
USART_Receive:
  ;
  sbis  UCSRA, RXC
  rjmp  USART_Receive
  ;                   9
  in    r18, UCSRA
  in    r17, UCSRB
  in    r16, UDR
  ;             -1
  andi  r18,(1<<FE)|(1<<DOR)|(1<<UPE)
  breq  USART_ReceiveNoError
  ldi   r17, HIGH(-1)
  ldi   r16, LOW(-1)
USART_ReceiveNoError:
  ;      9
  lsr   r17
  andi  r17, 0x01
  ret
```

C (1)

```
unsigned int USART_Receive( void )
{
  unsigned char status, resh, resl;
  /*            */
  while ( !(UCSRA & (1<<RXC)) )
       ;
  /*                    9        */
  status = UCSRA;
  resh = UCSRB;
  resl = UDR;
  /*              -1 */
  if ( status & (1<<FE)|(1<<DOR)|(1<<UPE) )
    return -1;
  /*      9              */
  resh = (resh >> 1) & 0x01;
  return ((resh << 8) | resl);
}
```

Note: 1.
I/O I/O “LDS” “STS” “SBRS” “SBRC” “SBR” “CBR” I/O “IN” “OUT” “SBIS” “SBIC” “CBI” “SBI”

I/O

USART

(RXC)

1 0( )

(RXEN = 0) RXC

UCSRB (RXCIE) RXC (

) USART

UDR RXC

USART (FE) (DOR) (UPE)

UCSRA UDR

UCSRA (UDR)

"0“

(FE)

(1) FE 0 FE 1

UCSRC USBS FE

UCSRA

0

(DOR) (

)

DOR UDR UDR

UCSRA 0

DOR

(UPE)

UPE UCSRA

0 P109“ ” P117“ ”

UPM1 ( ) UPM0

(UPE)

(UPM1 = 1)

UPE (UDR)

(RXEN

) RxD FIFO

FIFO

UDR RXC

(1)
USART_Flush: **sbis** UCSRA, RXC **ret** **in** r16, UDR **rjmp** USART_Flush
C (1)

void USART_Flush(**void**)
{
unsigned char dummy;
while (UCSRA & (1<<RXC)) dummy = UDR;
}

Note: 1. I/O I/O “LDS” “STS” “SBRS” “SBRC” “SBR” “CBR” I/O “IN” “OUT” “SBIS” “SBIC” “CBI” “SBI”

USART

RxD

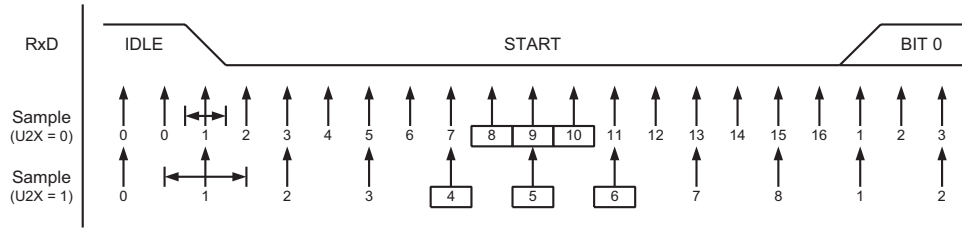
Figure 56

16

8 (U2X = 1)

RxD ( ) 0

Figure 56.



RxD ( ) ( )

1 0

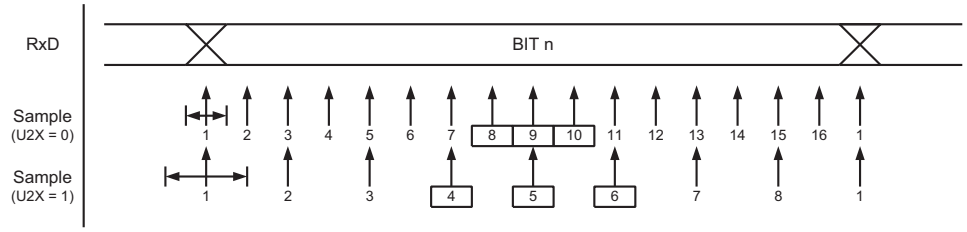
8 9 10( ) 4 5 6( )

( )

16 8

Figure 57

Figure 57.

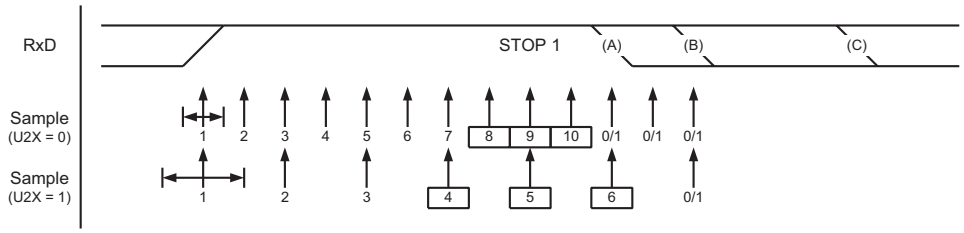


2 3 1 2

3 0 RxD

Figure 58

Figure 58.



0 FE

Figure 58 A

B C

(

Table 49)

$$R_{slow} = \frac{(D+1)S}{S-1+D\cdot S+S_F} \qquad R_{fast} = \frac{(D+2)S}{(D+1)S+S_M}$$

D (D = 5 10)

S S = 16 S = 8

S_F S_F = 8 S_F = 4

S_M S_M = 9 S_M = 5

R_{slow} R_{fast}

Table 49 Table 50

Table 49. (U2X = 0)

# (D +)	R_{slow} (%)	R_{fast} (%)	(%)	(%)
5	93.20	106.67	+6.67/-6.8	± 3.0
6	94.12	105.79	+5.79/-5.88	± 2.5
7	94.81	105.11	+5.11/-5.19	± 2.0
8	95.36	104.58	+4.58/-4.54	± 2.0
9	95.81	104.14	+4.14/-4.19	± 1.5
10	96.17	103.78	+3.78/-3.83	± 1.5

Table 50. (U2X = 1)

# (D +)	R_{slow} (%)	R_{fast} (%)	(%)	(%)
5	94.12	105.66	+5.66/-5.88	± 2.5
6	94.92	104.92	+4.92/-5.08	± 2.0
7	95.52	104,35	+4.35/-4.48	± 1.5
8	96.00	103.90	+3.90/-4.00	± 1.5
9	96.39	103.53	+3.53/-3.61	± 1.5
10	96.70	103.23	+3.23/-3.30	± 1.0

(XTAL)

2%

UBRR

UCSRA (MPCM) USART

CPU

MPCM

5 8

9 9 (RXB8)

(9) 1

MPCM 9 (UCSZ = 7)

(TXB8 = 1) 9 (TXB8) 1 (TXB = 0)

9

1. (UCSRA MPCM)
2. UCSRA

   RXC
3. UDR

   UCSRA MPCM

   MPCM 1
4. MPCM 1
5. MPCM

   2

5 8 n n+1

5 8 (USBS = 1)

- - (SBI CBI) MPCM MPCM TXC

I/O SBI CBI

USART

USART I/O UDR

Bit	7	6	5	4	3	2	1	0	
	RXB[7:0]								UDR ( )
	TXB[7:0]								UDR ( )
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

USART USART I/O

USART UDR UDR

(TXB) UDR (RXB)

5 6 7 0

UCSRA UDRE UDRE

UDR USART

TxD

FIFO FIFO
- - (SBI CBI) (SBIC SBIS)
FIFO

USART A
UCSRA

Bit	7	6	5	4	3	2	1	0	
	RXC	TXC	UDRE	FE	DOR	UPE	U2X	MPCM	UCSRA
/	R	R/W	R	R	R	R	R/W	R/W	
	0	0	1	0	0	0	0	0	

- **Bit 7 – RXC: USART**

RXC
RXC RXC (RXCIE)

- **Bit 6 – TXC: USART**

(UDR) TXC
TXC 1 TXC
(TXCIE)

- **Bit 5 – UDRE: USART**

UDRE (UDR) UDRE 1
UDRE (UDRIE)

UDRE

- **Bit 4 – FE:**

0 FE (UDR)
1 FE 0 UCSRA 0

- **Bit 3 – DOR:**

DOR ( )

(UDR) UCSRA 0

- **Bit 2 – UPE: USART**

(UPM1 = 1)
UPE (UDR) UCSRA
0

- **Bit 1 – U2X:**

1 16 8

- **Bit 0 – MPCM:**

MPCM USART
MPCM P121“
”

USART B
UCSRB

Bit	7	6	5	4	3	2	1	0	
	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8	UCSRB
/	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	
	0	0	0	0	0	0	0	0	

- **Bit 7 – RXCIE:**

RXC RXCIE 1 SREG UCSRA
RXC 1 USART

- **Bit 6 – TXCIE:**

TXC TXCIE 1 SREG UCSRA
TXC 1 USART

- **Bit 5 – UDRIE: USART**

UDRE UDRIE 1 SREG UCSRA
UDRE 1 USART

- **Bit 4 – RXEN:**

USART RxD USART
FE DOR UPE

- **Bit 3 – TXEN:**

USART TxD USART
TXEN
TxD I/O

- **Bit 2 – UCSZ2:**

UCSZ2 UCSRC UCSZ1:0 (
)

- **Bit 1 – RXB8: 8**

9 RXB8 9 UDR
RXB8

- **Bit 0 – TXB8: 8**

9 TXB8 9 UDR

USART C
UCSRC

Bit	7	6	5	4	3	2	1	0	
	–	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	UCSRC
/	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	1	1	0	

- **Bit 6 – UMSEL: USART**

Table 51. UMSEL

UMSEL	
0	
1	

- **Bit 5:4 – UPM1:0:**

UPM0 UCSRA UPE

Table 52. UPM

UPM1	UPM0	
0	0	
0	1	
1	0	
1	1	

- **Bit 3 – USBS:**

Table 53. USBS

USBS	
0	1
1	2

- **Bit 2:1 – UCSZ1:0:**

UCSZ1:0 UCSRB UCSZ2 (
) P126Table 54

Table 54. UCSZ

UCSZ2	UCSZ1	UCSZ0	
0	0	0	5
0	0	1	6
0	1	0	7
0	1	1	8
1	0	0	
1	0	1	
1	1	0	
1	1	1	9

- **Bit 0 – UCPOL:**

UCPOL

XCK

Table 55. UCPOL

UCPOL	(TxD)	(RxD)
0	XCK	XCK
1	XCK	XCK

USART UBRRL
UBRRH

Bit	15	14	13	12	11	10	9	8	
	–	–	–	–	UBRR[11:8]				UBRRH
	UBRR[7:0]								UBRRL
	7	6	5	4	3	2	1	0	
/	R	R	R	R	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

- **Bit 15:12 –**

UBRRH

- **Bit 11:0 – UBRR11:0: USART**

12 USART UBRRH USART
4 UBRRL 8
UBRRL

Table 56 UBRR
0.5%
(
P119“ ”)

$$\text{Error}[\%] = \left(\frac{\text{BaudRate}_{\text{Closest Match}}}{\text{BaudRate}} - 1\right) \bullet 100\%$$

Table 56. UBRR

	f_{osc} = 1.0000 MHz				f_{osc} = 1.8432 MHz				f_{osc} = 2.0000 MHz			
	U2X = 0		U2X = 1		U2X = 0		U2X = 1		U2X = 0		U2X = 1	
(bps)	UBRR		UBRR		UBRR		UBRR		UBRR		UBRR	
2400	25	0.2%	51	0.2%	47	0.0%	95	0.0%	51	0.2%	103	0.2%
4800	12	0.2%	25	0.2%	23	0.0%	47	0.0%	25	0.2%	51	0.2%
9600	6	-7.0%	12	0.2%	11	0.0%	23	0.0%	12	0.2%	25	0.2%
14.4k	3	8.5%	8	-3.5%	7	0.0%	15	0.0%	8	-3.5%	16	2.1%
19.2k	2	8.5%	6	-7.0%	5	0.0%	11	0.0%	6	-7.0%	12	0.2%
28.8k	1	8.5%	3	8.5%	3	0.0%	7	0.0%	3	8.5%	8	-3.5%
38.4k	1	-18.6%	2	8.5%	2	0.0%	5	0.0%	2	8.5%	6	-7.0%
57.6k	0	8.5%	1	8.5%	1	0.0%	3	0.0%	1	8.5%	3	8.5%
76.8k	–	–	1	-18.6%	1	-25.0%	2	0.0%	1	-18.6%	2	8.5%
115.2k	–	–	0	8.5%	0	0.0%	1	0.0%	0	8.5%	1	8.5%
230.4k	–	–	–	–	–	–	0	0.0%	–	–	–	–
250k	–	–	–	–	–	–	–	–	–	–	0	0.0%
(1)	62.5 kbps		125 kbps		115.2 kbps		230.4 kbps		125 kbps		250 kbps	

1. UBRR = 0, = 0.0%

Table 57. UBRR

	f_{osc} = 3.6864 MHz				f_{osc} = 4.0000 MHz				f_{osc} = 7.3728 MHz			
	U2X = 0		U2X = 1		U2X = 0		U2X = 1		U2X = 0		U2X = 1	
(bps)	UBRR		UBRR		UBRR		UBRR		UBRR		UBRR	
2400	95	0.0%	191	0.0%	103	0.2%	207	0.2%	191	0.0%	383	0.0%
4800	47	0.0%	95	0.0%	51	0.2%	103	0.2%	95	0.0%	191	0.0%
9600	23	0.0%	47	0.0%	25	0.2%	51	0.2%	47	0.0%	95	0.0%
14.4k	15	0.0%	31	0.0%	16	2.1%	34	-0.8%	31	0.0%	63	0.0%
19.2k	11	0.0%	23	0.0%	12	0.2%	25	0.2%	23	0.0%	47	0.0%
28.8k	7	0.0%	15	0.0%	8	-3.5%	16	2.1%	15	0.0%	31	0.0%
38.4k	5	0.0%	11	0.0%	6	-7.0%	12	0.2%	11	0.0%	23	0.0%
57.6k	3	0.0%	7	0.0%	3	8.5%	8	-3.5%	7	0.0%	15	0.0%
76.8k	2	0.0%	5	0.0%	2	8.5%	6	-7.0%	5	0.0%	11	0.0%
115.2k	1	0.0%	3	0.0%	1	8.5%	3	8.5%	3	0.0%	7	0.0%
230.4k	0	0.0%	1	0.0%	0	8.5%	1	8.5%	1	0.0%	3	0.0%
250k	0	-7.8%	1	-7.8%	0	0.0%	1	0.0%	1	-7.8%	3	-7.8%
0.5M	–	–	0	-7.8%	–	–	0	0.0%	0	-7.8%	1	-7.8%
1M	–	–	–	–	–	–	–	–	–	–	0	-7.8%
(1)	230.4 kbps		460.8 kbps		250 kbps		0.5 Mbps		460.8 kbps		921.6 kbps	

1. UBRR = 0, = 0.0%

Table 58. UBRR

	f_{osc} = 8.0000 MHz				f_{osc} = 11.0592 MHz				f_{osc} = 14.7456 MHz			
	U2X = 0		U2X = 1		U2X = 0		U2X = 1		U2X = 0		U2X = 1	
(bps)	UBRR		UBRR		UBRR		UBRR		UBRR		UBRR	
2400	207	0.2%	416	-0.1%	287	0.0%	575	0.0%	383	0.0%	767	0.0%
4800	103	0.2%	207	0.2%	143	0.0%	287	0.0%	191	0.0%	383	0.0%
9600	51	0.2%	103	0.2%	71	0.0%	143	0.0%	95	0.0%	191	0.0%
14.4k	34	-0.8%	68	0.6%	47	0.0%	95	0.0%	63	0.0%	127	0.0%
19.2k	25	0.2%	51	0.2%	35	0.0%	71	0.0%	47	0.0%	95	0.0%
28.8k	16	2.1%	34	-0.8%	23	0.0%	47	0.0%	31	0.0%	63	0.0%
38.4k	12	0.2%	25	0.2%	17	0.0%	35	0.0%	23	0.0%	47	0.0%
57.6k	8	-3.5%	16	2.1%	11	0.0%	23	0.0%	15	0.0%	31	0.0%
76.8k	6	-7.0%	12	0.2%	8	0.0%	17	0.0%	11	0.0%	23	0.0%
115.2k	3	8.5%	8	-3.5%	5	0.0%	11	0.0%	7	0.0%	15	0.0%
230.4k	1	8.5%	3	8.5%	2	0.0%	5	0.0%	3	0.0%	7	0.0%
250k	1	0.0%	3	0.0%	2	-7.8%	5	-7.8%	3	-7.8%	6	5.3%
0.5M	0	0.0%	1	0.0%	–	–	2	-7.8%	1	-7.8%	3	-7.8%
1M	–	–	0	0.0%	–	–	–	–	0	-7.8%	1	-7.8%
(1)	0.5 Mbps		1 Mbps		691.2 kbps		1.3824 Mbps		921.6 kbps		1.8432 Mbps	

1. UBRR = 0, = 0.0%

Table 59.

UBRR

	f_{osc} = 16.0000 MHz			
	U2X = 0		U2X = 1	
(bps)	UBRR		UBRR	
2400	416	-0.1%	832	0.0%
4800	207	0.2%	416	-0.1%
9600	103	0.2%	207	0.2%
14.4k	68	0.6%	138	-0.1%
19.2k	51	0.2%	103	0.2%
28.8k	34	-0.8%	68	0.6%
38.4k	25	0.2%	51	0.2%
57.6k	16	2.1%	34	-0.8%
76.8k	12	0.2%	25	0.2%
115.2k	8	-3.5%	16	2.1%
230.4k	3	8.5%	8	-3.5%
250k	3	0.0%	7	0.0%
0.5M	1	0.0%	3	0.0%
1M	0	0.0%	1	0.0%
(1)	1 Mbps		2 Mbps	

1. UBRR = 0, = 0.0%

USI

USI

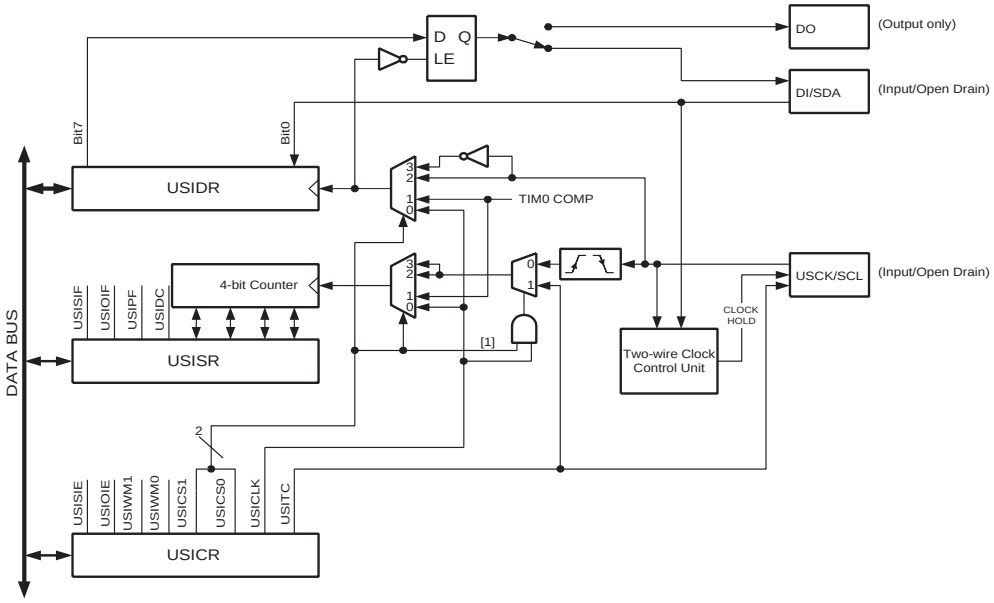
USI

USI

- (, $f_{SCLmax} = f_{CK}/16$)
- ($f_{SCKmax} = f_{CK}/4$)
-
-
-
-

Figure 59. USI I/O P2“ATtiny2313 ”
CPU I/O I/O
P137“USI ”

Figure 59.



8

(DI)

4

USCK 0

USI (SPI) 0 1 (SS)
DI DO USCK

Figure 60.

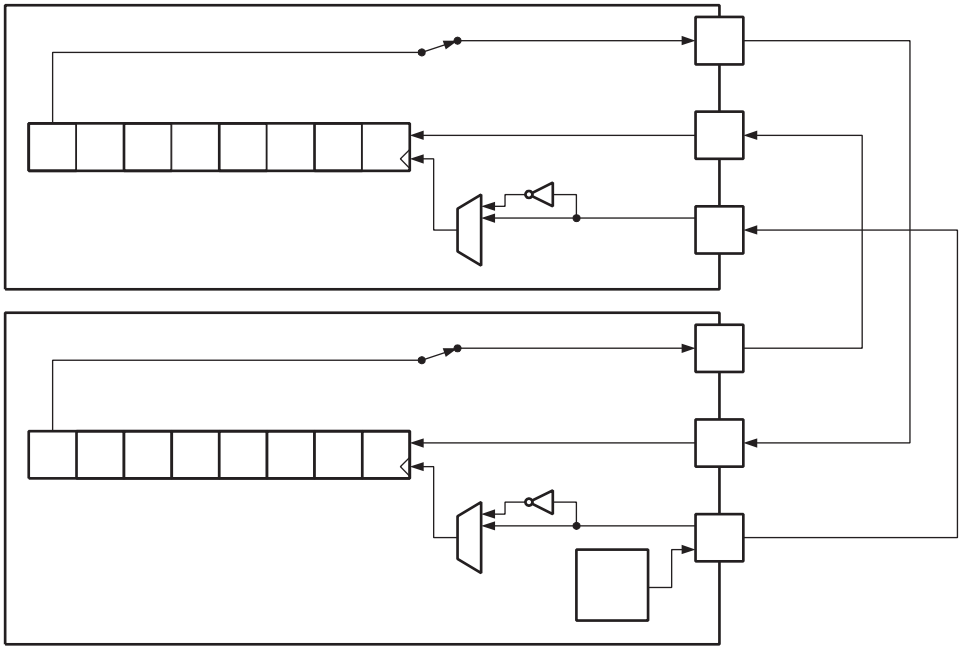


Figure 60 USI
8 USCK
USI 4 ( ) USIOI
USCK
USICR USITC

Figure 61.

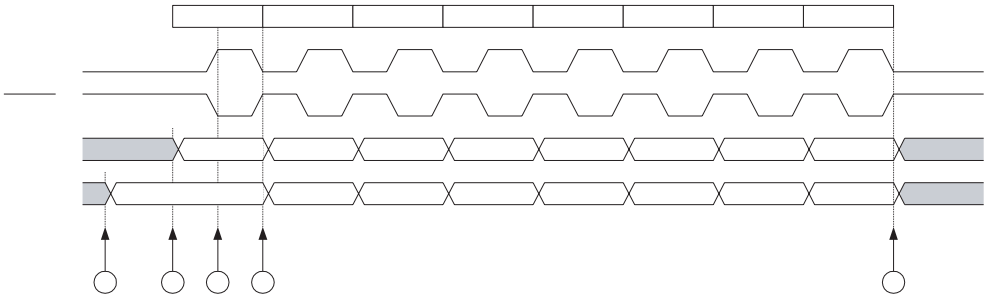


Figure 61. USCK
USI (USIDR) USCK
0(USICS0 = 0) DI DO
( ) 1(USICS0 = 1) 0
USI SPI
0 1

Figure 61.
1.
A B

C USCK
4 0

2. USCK (C D)
(DI) USI (C) (D) 4

3. ( ) 2 8
4. 8 (16)

SPI USI SPI

```
SPITransfer:
    out    USIDR,r16
    ldi    r16,(1<<USIOIF)
    out    USISR,r16
    ldi    r16,(1<<USIWM0)|(1<<USICS1)|(1<<USICLK)|(1<<USITC)
SPITransfer_loop:
    out    USICR,r16
    sbis   USISR,USIOIF
    rjmp   SPITransfer_loop
    in     r16,USIDR
    ret
```

8 (+ ret) DO USCK
DDRE r16
r16

USI USI
USITC USCK
16

(fsck = fck/2) USI SPI

```
SPITransfer_Fast:

   out    USIDR,r16
   ldi    r16,(1<<USIWM0)|(0<<USICS0)|(1<<USITC)
   ldi    r17,(1<<USIWM0)|(0<<USICS0)|(1<<USITC)|(1<<USICLK)

   out    USICR,r16 ; MSB
   out    USICR,r17
   out    USICR,r16
   out    USICR,r17
   out    USICR,r16
   out    USICR,r17
   out    USICR,r16
   out    USICR,r17
   out    USICR,r16
   out    USICR,r17
   out    USICR,r16
   out    USICR,r17
   out    USICR,r16
   out    USICR,r17
   out    USICR,r16 ; LSB
   out    USICR,r17

   in     r16,USIDR
ret
```

SPI USI SPI

```
init:
   ldi    r16,(1<<USIWM0)|(1<<USICS1)
   out    USICR,r16
...
SlaveSPITransfer:
   out    USIDR,r16
   ldi    r16,(1<<USIOIF)
   out    USISR,r16
SlaveSPITransfer_loop:
   sbis   USISR,USIOIF
   rjmp   SlaveSPITransfer_loop
   in     r16,USIDR
   ret
```

8 (+ ret) DO USCK
DDR r16
r16

USI

USI IC (TWI)
SCL SDA

Figure 62.

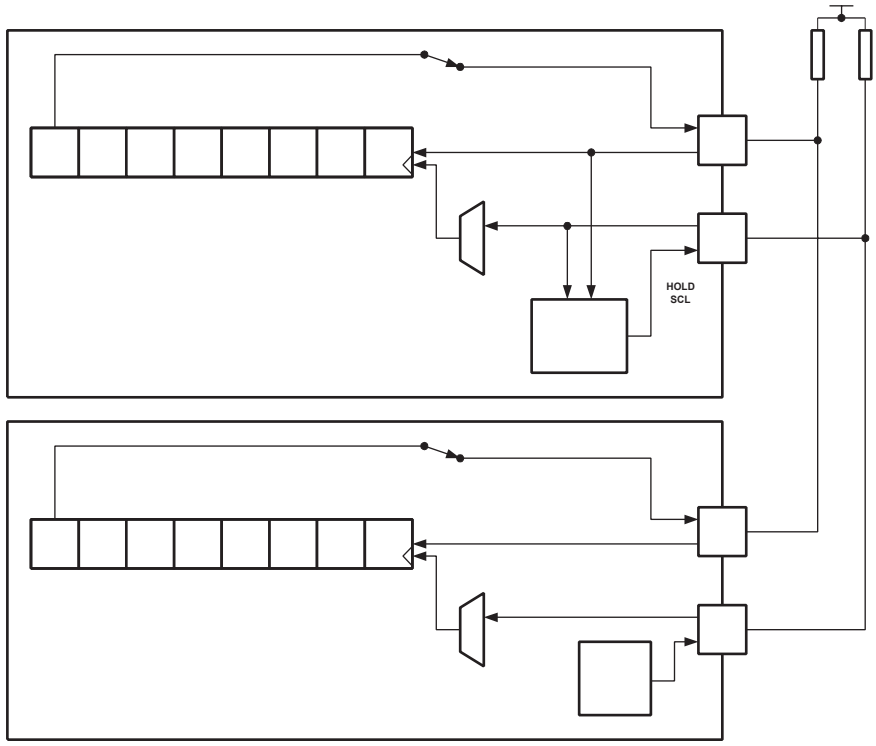
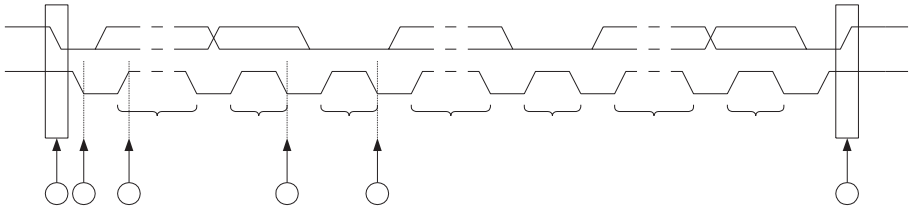


Figure 62 USI

SCL
SCL
PORT
USCK
TWI

Figure 63.



(Figure 63.)

1. SCL (A) SDA
SDA 7 0 PORT
0

(Figure 64.) USISIF

2. SCL (B) SCL

3. SCL (C) SCL

4. ( ) 8
SCL (D)
SCL

5. SCL (SCL(D)
14) SDA R/W
R/W 1 (SDA) (E)
SCL

6. (F)

Figure 64.

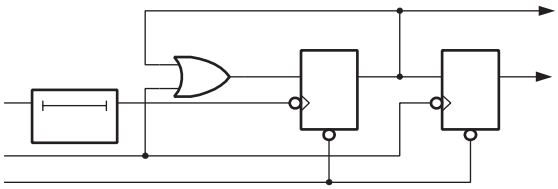


Figure 64. SDA (50 300 ns) SCL

SCL CKSEL
P21“ ”

USI

USI

UART

4 4

12 / USI 4 / 0 12

(F)
USICS1

USI

USI USIDR

Bit	7	6	5	4	3	2	1	0	
	MSB							LSB	USIDR
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

USI USIDR

USICS1..0 / 0
USICLK (USIWM1..0 = 0)
(DI/SDA) (USCK/SCL)

(DO SDA) (7)
(USICS1 = 1) (
) (USICS1 = 0)
MSB

USI USISR

Bit	7	6	5	4	3	2	1	0	
	USISIF	USIOIF	USIPF	USIDC	USICNT3	USICNT2	USICNT1	USICNT0	USISR
/	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

- **Bit 7 – USISIF:**

USISIF
(USICSx = 0b11 & USICLK = 0) (USICS = 0b10 & USICLK = 0) SCK

USISIF USICR USISIE
USISIF 1
USCL

- **Bit 6 – USIOIF:**

4 (15 0) USICR USIOIE
USIOIF 1
SCL

- **Bit 5 – USIPF:**

USIPF USIOIF
1

- **Bit 4 – USIDC:**

7 USIDC

- **Bits 3..0 – USICNT3..0:**

4 CPU

/ 0
USICLK USITC USICS1..0
USITC (USICS1 = 1)
USICLK 1

(USIWM1..0 = 0)
(USCK/SCL)

USI USICR

Bit	7	6	5	4	3	2	1	0	
	USISIE	USIOIE	USIWM1	USIWM0	USICS1	USICS0	USICLK	USITC	USICR
/	R/W	R/W	R/W	R/W	R/W	R/W	W	W	
	0	0	0	0	0	0	0	0	

- **Bit 7 – USISIE:**

1 USISIE

- **Bit 6 – USIOIE:**

1 USIOIE

- **Bit 5..4 – USIWM1..0:**

USIWM1..0 USI
P139Table 60

Table 60. USIWM1..0 USI

USIWM1	USIWM0	
0	0	
0	1	DO DI USCK (DO) IO DDR PORT (DI) (USCK) PORT USICR USITC
1	0	SDA (DI) SCL (USCK) (1) (SDA) (SCL) DDR SDA PORT 0 SDA SDA ( ) SCL PORT 0 SCL SCL SCL (USISIF) SDA SCL SDA SCL
1	1	SDA SCL SCL (USIOIF)

Note: 1. DI USCK (SDA) (SCL)

- **Bit 3..2 – USICS1..0:**

(USCK/SCL) (DI/SDA)
/ 0
USICS1..0 0 USICLK 1
(USICS1 = 1) USICLK
USITC

Table 61 USICS1..0 USICLK 4

Table 61. USICS1..0 USICLK

USICS1	USICS0	USICLK		4
0	0	0		
0	0	1	(USICLK)	(USICLK)
0	1	X	/ 0	/ 0
1	0	0		
1	1	0		
1	0	1		(USITC)
1	1	1		(USITC)

- **Bit 1 – USICLK:**

USICS1..0 0 USICLK

0

(USICS1 = 1) USICLK
USICLK USITC 4 (Table 61)

- **Bit 0 – USITC:**

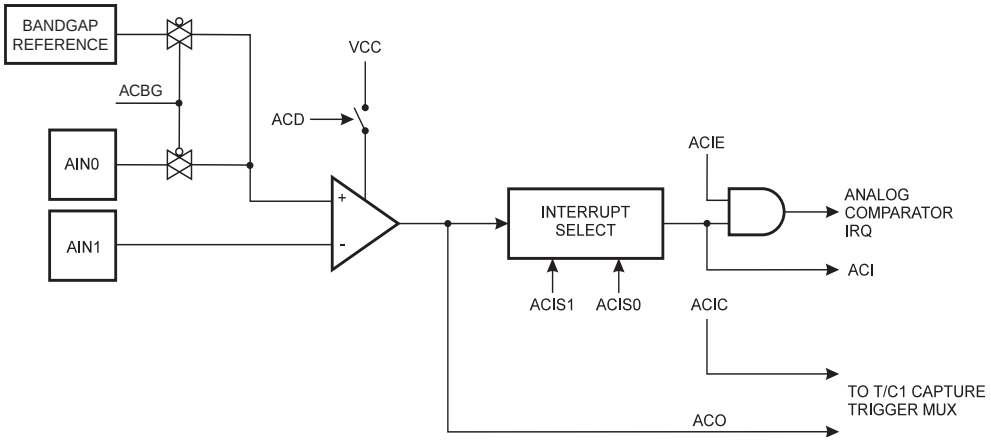
USITC USCK/SCL 0 1
DDRE4
0

(USICS1 = 1) USICLK 1 USITC 4

AIN0 AIN1 AIN0 AIN1
ACO /
1

Figure 65

Figure 65.



ACSR

Bit	7	6	5	4	3	2	1	0	
	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	ACSR
/	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
	0	0	N/A	0	0	0	0	0	

- **Bit 7 – ACD:**

ACD
ACD ACSR
ACIE ACD

- **Bit 6 – ACBG:**

ACBG "1" ACBG AIN0
P36 " "

- **Bit 5 – ACO:**

ACO 1 - 2

- **Bit 4 – ACI:**

ACIS1 ACIS0 ACI
ACIE SREG I
ACI ACI 1

- **Bit 3 – ACIE:**

ACIE 1 I

- **Bit 2 – ACIC:**

T/C1
T/C1
T/C1
(TIMSK) ICIE1

- **Bits 1, 0 – ACIS1, ACIS0:**

Table 62

Table 62. ACIS1/ACIS0

ACIS1	ACIS0	
0	0	
0	1	
1	0	
1	1	

ACIS1/ACIS0 ACSR

DIDR

Bit	7	6	5	4	3	2	1	0	
	–	–	–	–	–	–	AIN1D	AIN0D	DIDR
/	R	R	R	R	R	R	R/W	R/W	
	0	0	0	0	0	0	0	0	

- **Bit 1, 0 – AIN1D, AIN0D: AIN1, AIN0**

"1” AIN1/0 AIN1/0

"1”

debugWIRE

-
- **RESET**
-
- **(C HLL)**
- **( )**
-
-
-
-
-

debugWIRE CPU AVR

debugWIRE DWEN debugWIRE
RESET ( ) I/O

Figure 66. debugWIRE

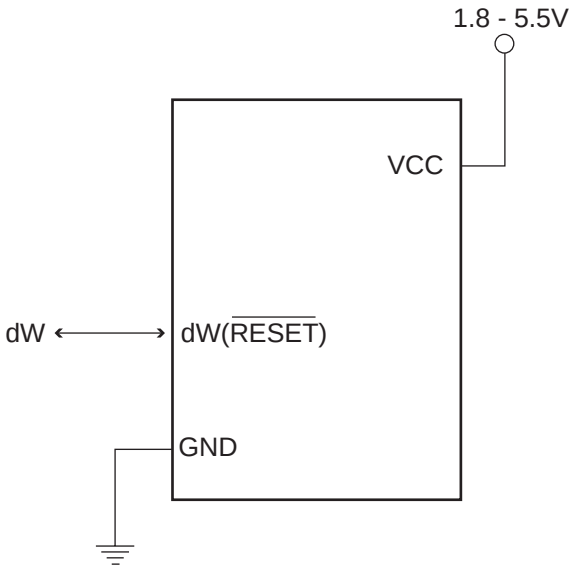


Figure 66 debugWIRE MCU
debugWIRE CKSEL

debugWIRE

- dW/(RESET) 10kΩ debugWIRE
- RESET V_{CC}
- debugWIRE RESET
-

debugWIRE AVR AVR Studio®
BREAK BREAK

BREAK

Flash AVR Studio® debugWIRE
Flash

debugWIRE

debugWIRE (dW) (RESET) debugWIRE

CPU debugWIRE I/O CPU
I/O debugWIRE

DWEN
debugWire DWEN

I/O debugWIRE

debugWire

debugWire DWDR

Bit	7	6	5	4	3	2	1	0	
	DWDR[7:0]								DWDR
/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

DWDR MCU debug-
WIRE

Flash

MCU

( )

SPM

1

-
-
-

2

-
-
-

(

) 1 Boot Loader - -

2

SPM Z “00000011” SPMCSR

SPM R1 R0 Z

PCPAGE Z

- CPU

( ) Z R1:R0

“00000001” SPMCSR SPM Z

PCWORD SPMCSR CTPB

SPM EEPROM

Z “00000101” SPMCSR

SPM R1 R0 Z

PCPAGE Z

- CPU

Flash Z SPM

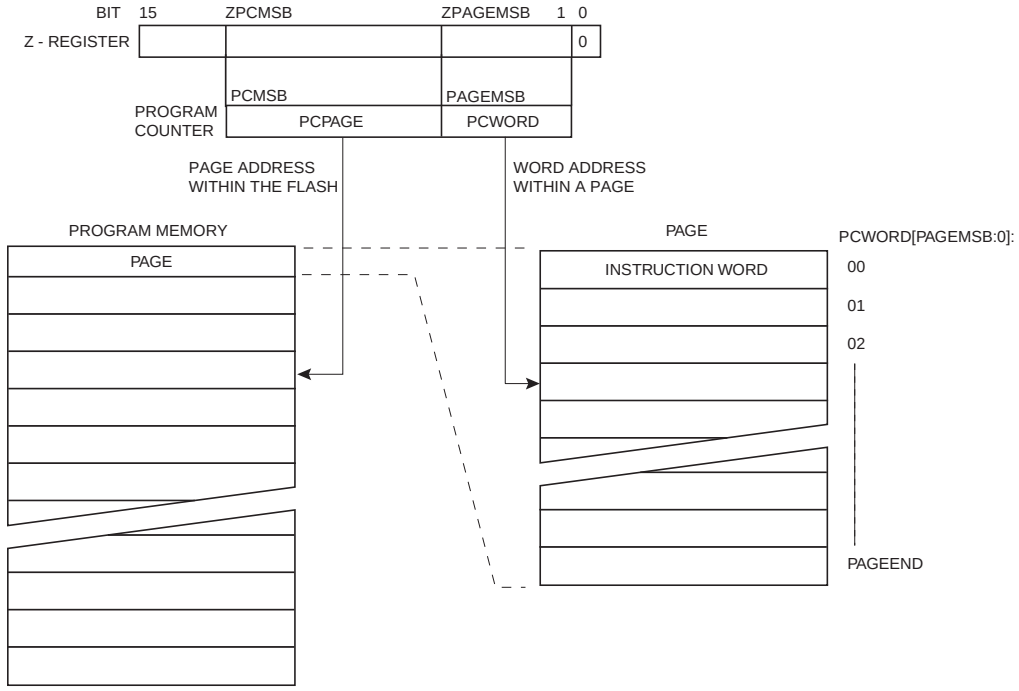
Bit	15	14	13	12	11	10	9	8
ZH (R31)	Z15	Z14	Z13	Z12	Z11	Z10	Z9	Z8
ZL (R30)	Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0
	7	6	5	4	3	2	1	0

Flash (P152Table 69)

Figure 67 Boot Loader

LPM Z Z LSB (Z0)

Figure 67. SPM (1)



Note: 1. Figure 67 P152Table 69

(SPM) SPMCSR

SPMCSR Boot Loader

Bit	7	6	5	4	3	2	1	0	
	–	–	–	CTPB	RFLB	PGWRT	PGERS	SELFPRGEN	SPMCSR
/	R	R	R	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

- **Bits 7..5 – Res:**

  ATtiny2313 "0”

- **Bit 4 – CTPB:**

  CTPB

- **Bit 3 – RFLB:**

  SPMCSR RFLB SELFPRGEN LPM (Z Z0) P148“EEPROM SPMCSR ”

- **Bit 2 – PGWRT:**

  SELFPRGEN SPM Flash Z R1 R0 SPM PGWRT CPU

- **Bit 1 – PGERS:**

  SELFPRGEN SPM Z R1 R0 SPM PGERS CPU

- **Bit 0 – SELFPRGEN:**

  SPM CTPB RFLB PGWRT PGERS SPM SELFPRGEN SPM R1:R0 Z Z LSB SPM SPM SPMEN SELFPRGEN

  “10001” “01001” “00101” “00011” “00001”

EEPROM EEPROM Flash

SPMCSR SPMCSR EECR EEWE

0x0001 Z

SPMCSR RFLB SELFPRGEN RFLB SELFPRGEN CPU LPM

CPU LPM CPU SPM RFLB

Flash V_{CC} CPU Flash Flash
Flash

Flash Flash
CPU

Flash ( )

1. AVR RESET
BOD

2. AVR CPU
SPMCSR Flash

SPM **Flash** RC Flash Table 63 CPU Flash

Table 63. SPM

Flash (

ATtiny2313 2 (“0”) (“1”)
Table 65 “1”

Table 64. (1)

	7	–	1 ( )
	6	–	1 ( )
	5	–	1 ( )
	4	–	1 ( )
	3	–	1 ( )
	2	–	1 ( )
LB2	1		1 ( )
LB1	0		1 ( )

Note: 1. “1” “0”

Table 65. (1)(2)

LB	**LB2**	**LB1**	
1	1	1	
2	1	0	Flash EEPROM (1)
3	0	0	Flash EEPROM (1)

Notes: 1. LB1 LB2 Boot
2. “1” , “0”

ATtiny2313 Table 67 Table 68
“0”

Table 66.

	7	–	1 ( )
	6	–	1 ( )
	5	–	1 ( )
	4	–	1 ( )
	3	–	1 ( )
	2	–	1 ( )
	1	–	1 ( )
SELFPRGEN	0		1 ( )

Table 67.

DWEN(3)	7	debugWIRE	1 ( )
EESAVE	6	EEPROM	1 (EEPROM)
SPIEN(1)	5		0 (SPI)
WDTON(2)	4		1 ( )
BODLEVEL2(4)	3	BOD	1 ( )
BODLEVEL1(4)	2	BOD	1 ( )
BODLEVEL0(4)	1	BOD	1 ( )
RSTDISBL(5)	0		1 ( )

Note: 1. SPIEN
2. P40“ WDTCSR”
3. DWEN DWEN
4. P33Table 16 BODLEVEL
5. RSTDISBL P51“ A ”

Table 68.

CKDIV8	7	8	0 ( )
CKOUT	6		1 ( )
SUT1	5		1 ( )[1]
SUT0	4		0 ( )[1]
CKSEL3	3		0 ( )[2]
CKSEL2	2		0 ( )[2]
CKSEL1	1		1 ( )[2]
CKSEL0	0		0 ( )[2]

Note: 1. SUT1..0 P32Table 15
2. CKSEL3..0 RC 8 MHz

1(LB1)

EESAVE

Atmel

ATtiny2313

1. 0x000: 0x1E (Atmel l)
2. 0x001: 0x91 (2KB Flash)
3. 0x002: 0x0A (0x001 0x91 ATmega48)

ATtiny2313 RC 0x000
0x0001 4 8 MHz 4 MHz
OSCCAL RC

Table 69. Flash

Flash		PCWORD		PCPAGE	PCMSB
1K (2K)	16	PC[3:0]	64	PC[9:4]	9

Table 70. EEPROM

EEPROM		PCWORD		PCPAGE	EEAMSB
128	4	EEA[1:0]	32	EEA[6:2]	6

ATtiny2313 Flash EEPROM
250 ns

ATtiny2313 Figure 68 Table 71

XA1/XA0 XTAL1 Table 73

$\overline{WR}$ $\overline{OE}$ Table 74

Figure 68.

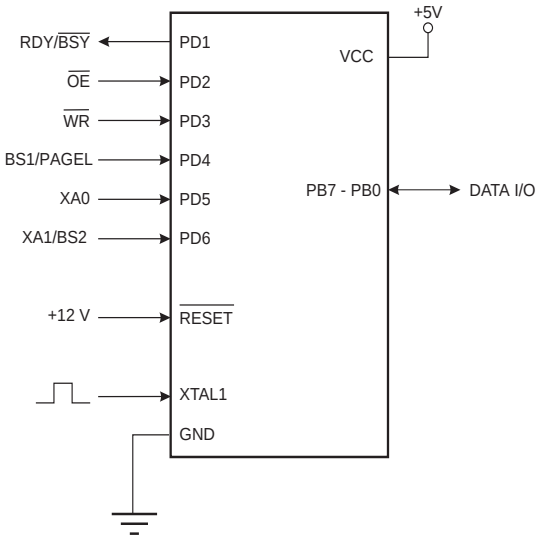


Table 71.

		I/O	
RDY/$\overline{BSY}$	PD1	O	0: , 1:
$\overline{OE}$	PD2	I	( ).
$\overline{WR}$	PD3	I	( ).
BS1/PAGEL	PD4	I	1(“0” , “1”).
XA0	PD5	I	XTAL 0
XA1/BS2	PD6	I	XTAL 1 2 (“0” , “1”)
DATA I/O	PB7-0	I/O	($\overline{OE}$)

Table 72.

XA1	Prog_enable[3]	0
XA0	Prog_enable[2]	0
BS1	Prog_enable[1]	0
$\overline{WR}$	Prog_enable[0]	0

Table 73. XA1 XA0

XA1	XA0	XTAL1
0	0	Flash EEPROM (BS1)
0	1	(BS1 Flash)
1	0	
1	1	

Table 74.

1000 0000	
0100 0000	
0010 0000	
0001 0000	Flash
0001 0001	EEPROM
0000 1000	
0000 0100	
0000 0010	Flash
0000 0011	EEPROM

Table 75.

		I/O	
MOSI	PB5	I	
MISO	PB6	O	t
SCK	PB7	I	

1. V_{CC} GND 4.5 - 5.5V
2. $\overline{\text{RESET}}$ XTAL1 6
3. P153Table 72 Prog_enable "0000" 100 ns
4. $\overline{\text{RESET}}$ 11.5 - 12.5V $\overline{\text{RESET}}$ +12V 100 ns Prog_enable
5. 50 µs

•
• 0xFF Flash EEPROM(EESAVE)

- Flash EEPROM 256

Flash EEPROM[1]

Flash /

EEPROM

Note: 1. EESAVE EEPRPOM

“ ”

1. XA1 XA0 “10”
2. BS1 “0”
3. DATA “1000 0000”
4. XTAL1
5. $\overline{\text{WR}}$ RDY/$\overline{\text{BSY}}$
6. RDY/$\overline{\text{BSY}}$

Flash Flash P152Table 69 Flash

Flash

A. “ Flash”
1. XA1 XA0 “10”
2. BS1 "0”
3. DATA “0001 0000” Flash
4. XTAL1

B.
1. XA1 XA0 “00”
2. BS1 “0”
3. DATA (0x00 - 0xFF)
4. XTAL1

C.
1. XA1 XA0 “01”
2. DATA (0x00 - 0xFF)
3. XTAL1

D.
1. BS1 “1”
2. XA1 XA0 “01”
3. DATA (0x00 - 0xFF)
4. XTAL1

E.
1. BS1 “1”
2. PAGEL (Figure 70)

F. B E

FLASH P157Figure 69
8 (< 256)

G.
1. XA1 XA0 “00”
2. BS1 “1”
3. DATA (0x00 - 0xFF)
4. XTAL1

H.
1. $\overline{WR}$ RDY/$\overline{BSY}$

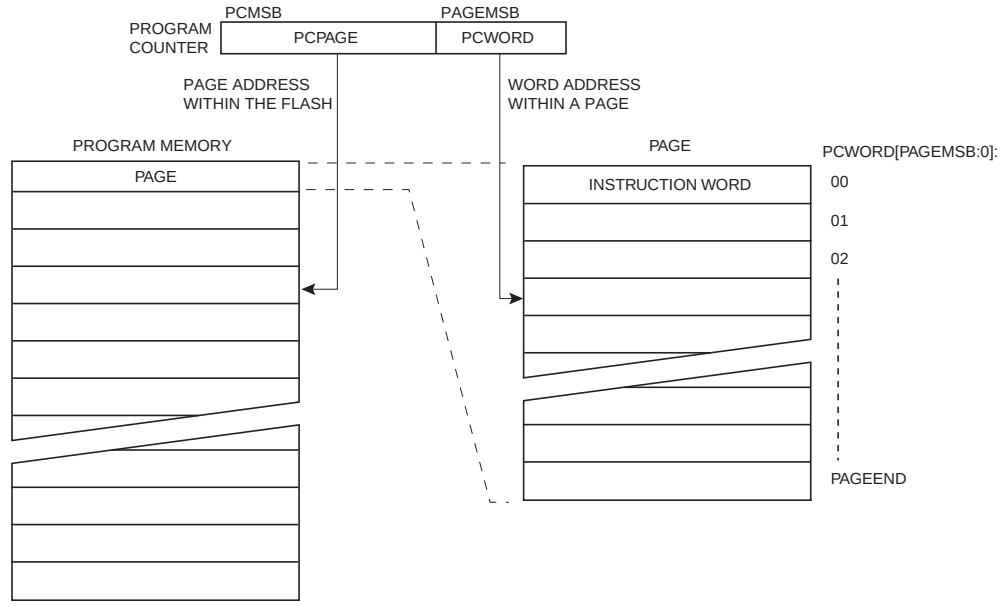
RDY/$\overline{BSY}$ (Figure 70)

I. B H Flash

J.
1. 1. XA1 XA0 “10”
2. DATA “0000 0000”

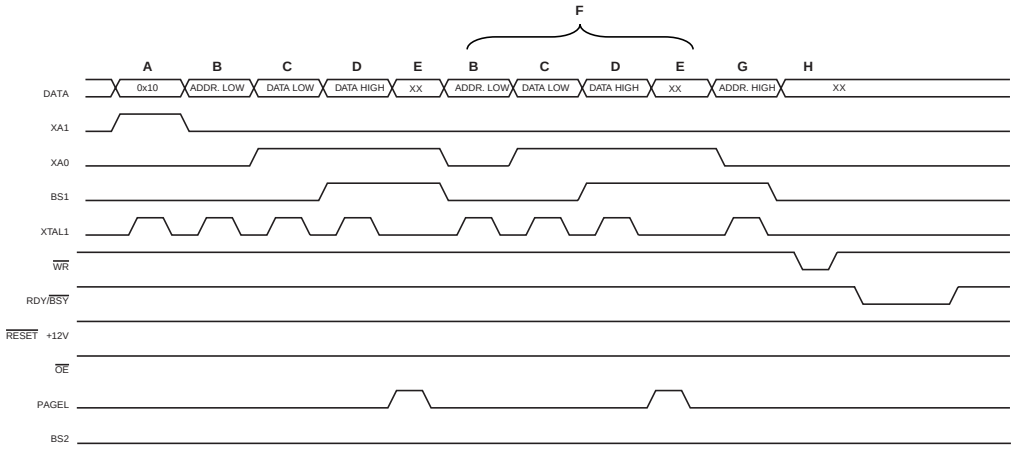
3. XTAL1

Figure 69. Flash (1)



Note: 1. PCPAGE PCWORD P152Table 69

Figure 70. Flash (1)



Note: 1. "XX" Flash

EEPROM P152Table 70 EEPROM EEPROM
EEPROM (
P156“ Flash ”)

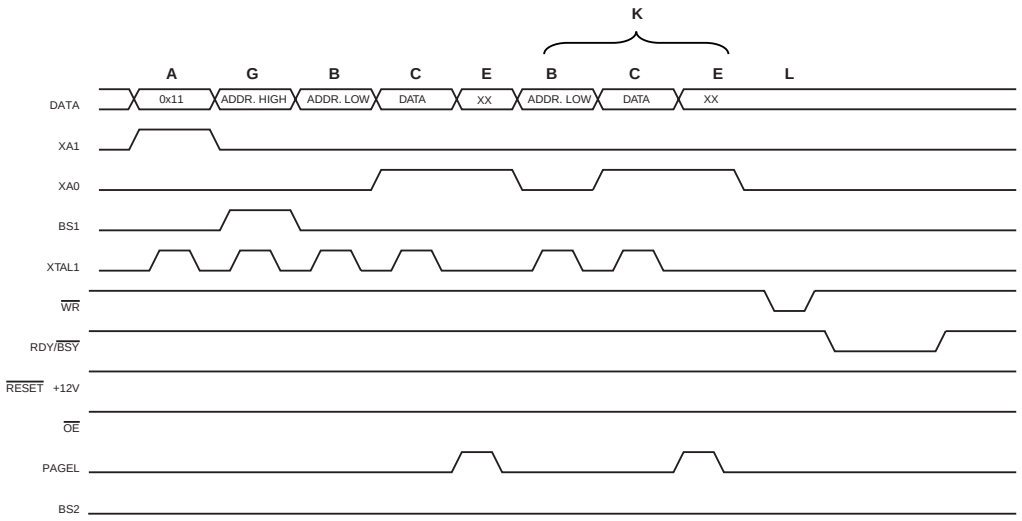
1. A “0001 0001”
2. G (0x00 - 0xFF)
3. B (0x00 - 0xFF)
4. C (0x00 - 0xFF)
5. E (PAGEL)

K 3 5

L EEPROM

1. BS “0”
2. $\overline{WR}$ EEPROM RDY/$\overline{BSY}$
3. RDY/$\overline{BSY}$ (Figure 71)

Figure 71. EEPROM



Flash Flash (P156“ Flash ”)

1. A “0000 0010”
2. G (0x00 - 0xFF)
3. B (0x00 - 0xFF)
4. $\overline{OE}$ “0” BS1 “0” DATA Flash
5. BS “1” DATA Flash
6. $\overline{OE}$ “1”

EEPROM (P156“ Flash ”)

1. A “0000 0011”
2. G (0x00 - 0xFF)
3. B (0x00 - 0xFF)
4. $\overline{OE}$ "0” BS1 "0” DATA EEPROM
5. $\overline{OE}$ ”1”

(P156“ Flash ”)

1. A “0100 0000”
2. C "0”
3. $\overline{WR}$ RDY/$\overline{BSY}$

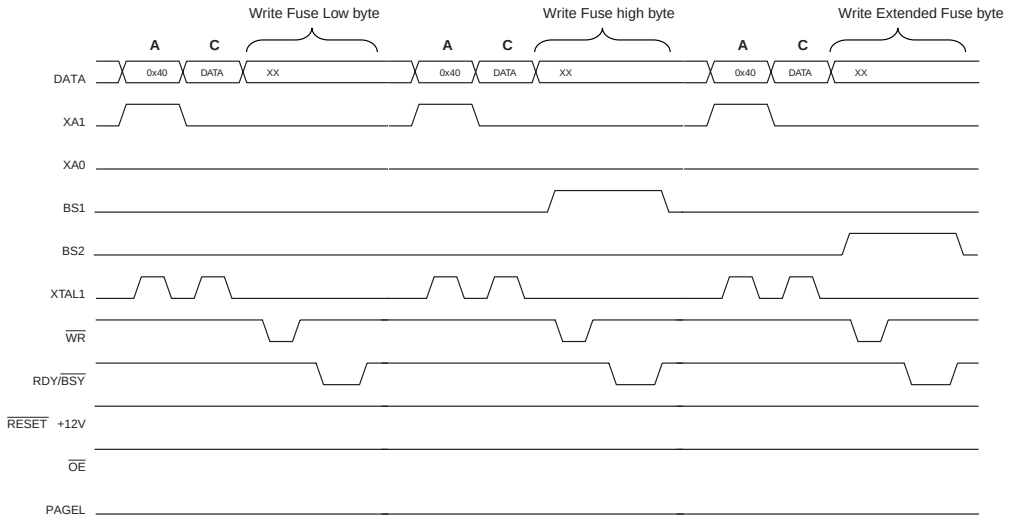
(P156“ Flash ”)

1. A “0100 0000”
2. C “0”
3. BS1 “1” BS2 “0”
4. $\overline{WR}$ RDY/$\overline{BSY}$
5. BS1 “0”

(P156“ Flash ”)

1. A “0100 0000”
2. C “0”
3. 3. BS1 “0” BS2 “1”
4. 4. $\overline{WR}$ RDY/$\overline{BSY}$
5. 5. BS2 “0”

Figure 72.



(P156“ Flash ”)

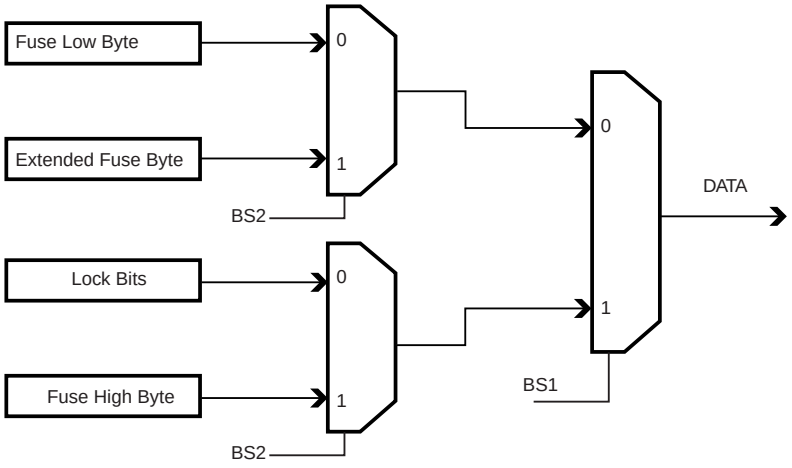
1. A “0010 0000”
2. C. n “0” LB 3(LB1 LB2)

3. $\overline{WR}$ RDY/$\overline{BSY}$

(P156“ Flash ”)

1. A “0000 0100”
2. $\overline{OE}$ BS2 BS1 “0” DATA (“0”)
3. $\overline{OE}$ “0” BS2 BS1 “1” DATA (“0”)
4. $\overline{OE}$ BS1 “0” BS2 “1” DATA (“0”)
5. $\overline{OE}$ “0” BS2 “0” BS1 “1” DATA (“0”)
6. $\overline{OE}$ “1”

Figure 73. BS1 BS2



(P156“ Flash ”)

1. A “0000 1000”
2. B 0x00 - 0x02
3. $\overline{OE}$ “0” BS1 “1” DATA
4. $\overline{OE}$ “1”

(P156“ Flash ”)

1. A “0000 1000”
2. B 0x00
3. $\overline{OE}$ “0” BS1 “1” DATA
4. $\overline{OE}$ “1”

Figure 74.

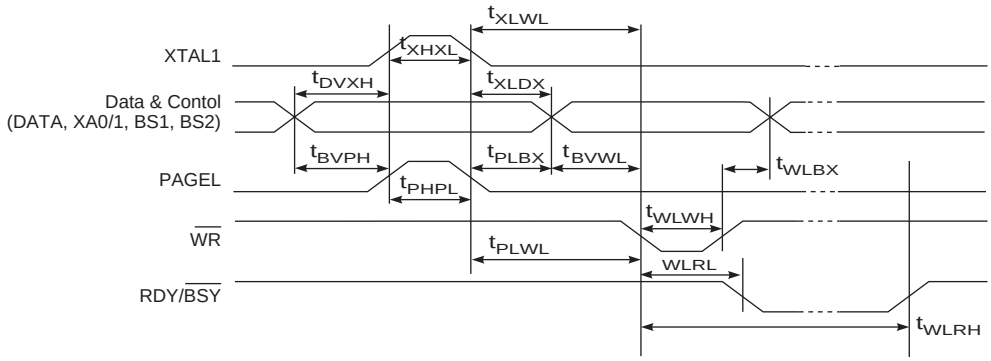
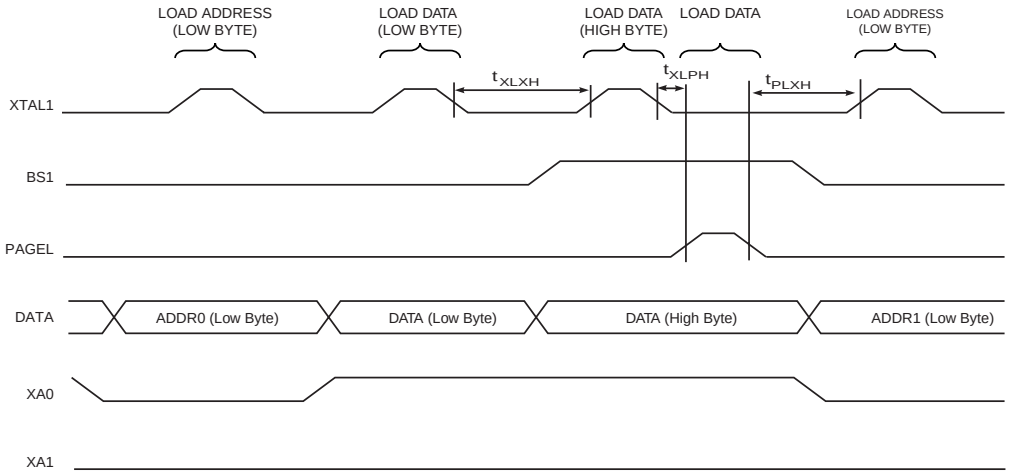
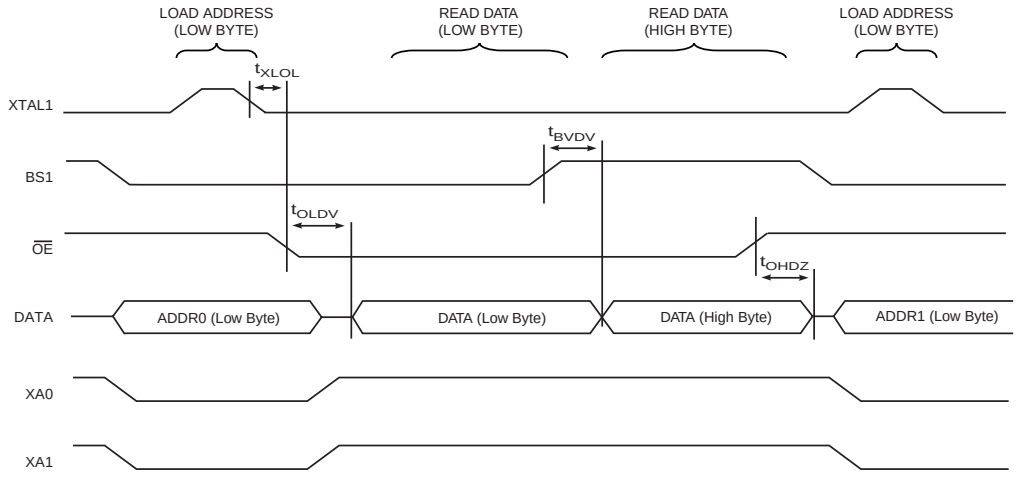


Figure 75. (1)



Note: 1. Figure 74 (t_{DVXH} t_{XHXL} t_{XLDX})

Figure 76. ( )[1]



Note: 1. Figure 74 (t_{DVXH} t_{XHXL} t_{XLDX})

Table 76. V_{CC} = 5V ± 10%

V_{PP}		11.5		12.5	V
I_{PP}				250	µA
t_{DVXH}	XTAL1	67			ns
t_{XLXH}	XTAL1 XTAL1	200			ns
t_{XHXL}	XTAL1	150			ns
t_{XLDX}	XTAL1	67			ns
t_{XLWL}	XTAL1 $\overline{WR}$	0			ns
t_{XLPH}	XTAL1 PAGEL	0			ns
t_{PLXH}	PAGEL XTAL1	150			ns
t_{BVPH}	PAGEL BS1	67			ns
t_{PHPL}	PAGEL	150			ns
t_{PLBX}	PAGEL BS1	67			ns
t_{WLBX}	$\overline{WR}$ BS2/1	67			ns
t_{PLWL}	PAGEL $\overline{WR}$	67			ns
t_{BVWL}	BS1 $\overline{WR}$	67			ns
t_{WLWH}	$\overline{WR}$	150			ns
t_{WLRL}	$\overline{WR}$ RDY/$\overline{BSY}$	0		1	µs
t_{WLRH}	$\overline{WR}$ RDY/$\overline{BSY}$ (1)	3.7		4.5	ms
t_{WLRH_CE}	$\overline{WR}$ RDY/$\overline{BSY}$ (2)	7.5		9	ms
t_{XLOL}	XTAL1 $\overline{OE}$	0			ns

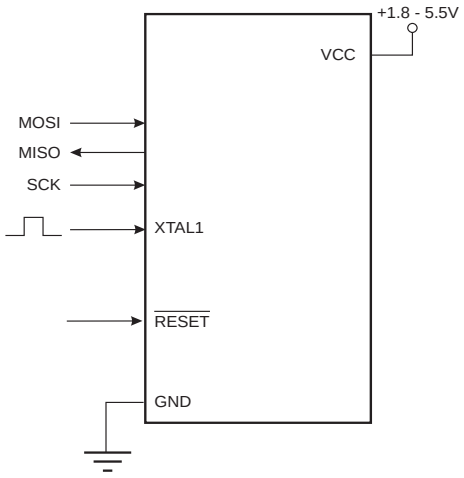
Table 76. V_{CC} = 5V ± 10%

t_{BVDV}	BS1 DATA	0		250	ns
t_{OLDV}	$\overline{OE}$ DATA			250	ns
t_{OHDZ}	$\overline{OE}$ DATA			250	ns

Notes: 1. Flash EEPROM t_{WLRH}
2. t_{WLRH_CE}

$\overline{RESET}$ SPI Flash EEPROM
SCK MOSI( ) MISO( ) $\overline{RESET}$
P154Table 75 SPI
SPI SPI

Figure 77. (1)



Notes: 1. XTAL1
2. V_{CC} - 0.3V < AVCC < V_{CC} + 0.3V AVCC 1.8 - 5.5V

EEPROM MCU
EEPROM 0xFF
CKSEL (SCK)

> f_{ck} < 12 MHz	2	CPU	f_{ck} >= 12 MHz	3	CPU
> f_{ck} < 12 MHz	2	CPU	f_{ck} >= 12 MHz	3	CPU

ATtiny2313 SCK

ATtiny2313 SCK Figure 78 Figure 79 Table 79

ATtiny2313 (P165Table 78 4)

1. $\overline{\text{RESET}}$ SCK "0" V_{CC} GND SCK SCK $\overline{\text{RESET}}$ 2 CPU
2. 20 ms MOSI
3. (0x53) 4 0x53 $\overline{\text{RESET}}$
4. Flash 4 LSB 8 t_{WD_FLASH} (P165Table 77.) Flash
5. **A:** EEPROM EEPROM t_{WD_EEPROM} (P165Table 77.) 0xFF
   B:EEPROM Load EEPROM 2 LSB EEPROM EEPROM 5 MSB EEPROM Load EEPROM t_{WD_FLASH} (P165Table 77) 0xFF
6. MISO
7. $\overline{\text{RESET}}$
8. ( ) $\overline{\text{RESET}}$ “1” V_{CC}

Table 77. Flash EEPROM

t_{WD_FLASH}	4.5 ms
t_{WD_EEPROM}	4.0 ms
t_{WD_ERASE}	4.0 ms
t_{WD_FUSE}	4.5 ms

Figure 78.

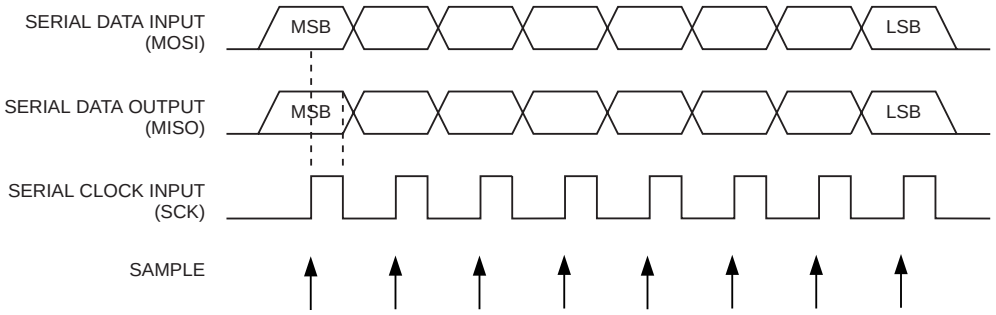


Table 78.

	1	**2**	**3**	**4**	
	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx	$\overline{\text{RESET}}$
	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	EEPROM Flash
	0010 **H**000	0000 00**aa**	**bbbb bbbb**	**oooo oooo**	**a**:**b** **H**( ) **o**
	0100 **H**000	000x xxxx	xxxx **bbbb**	**iiii iiii**	**b** **H**( ) **i**
	0100 1100	0000 00**aa**	**bbbb** xxxx	xxxx xxxx	**a**:**b**
EEPROM	1010 0000	000x xxxx	x**bbb bbbb**	**oooo oooo**	EEPROM **a**:**b** **o**
EEPROM	1100 0000	000x xxxx	x**bbb bbbb**	**iiii iiii**	EEPROM **b** **i**
EEPROM ( )	1100 0001	0000 0000	0000 00**bb**	**iiii iiii**	**i** EEPROM EEPROM
EEPROM ( )	1100 0010	00xx xxxx	x**bbb bb**00	xxxx xxxx	**b** EEPROM
	0101 1000	0000 0000	xxxx xxxx	xx**oo oooo**	”0” "1” P150Table 64
	1010 1100	111x xxxx	xxxx xxxx	11**ii iiii**	“0” P150Table 64
	0011 0000	000x xxxx	xxxx xx**bb**	**oooo oooo**	**b** **o**

Table 78.

	1	**2**	**3**	**4**	
	1010 1100	1010 0000	xxxx xxxx	**iiii iiii**	“0” “1” .
	1010 1100	1010 1000	xxxx xxxx	**iiii iiii**	“0” “1”
	1010 1100	1010 0100	xxxx xxxx	xxxx xxx**i**	“0” “1”
	0101 0000	0000 0000	xxxx xxxx	**oooo oooo**	“0” “1”
	0101 1000	0000 1000	xxxx xxxx	**oooo oooo**	“0” “1”
	0101 0000	0000 1000	xxxx xxxx	**oooo oooo**	“0” “1”
	0011 1000	000x xxxx	0000 000**b**	**oooo oooo**	**b**
RDY/$\overline{\text{BSY}}$	1111 0000	0000 0000	xxxx xxxx	xxxx xxx**o**	**o** = “1” “0”

Note: **a** = **b** = **H** = 0 - 1 - **o** = **i** = x =

Figure 79.

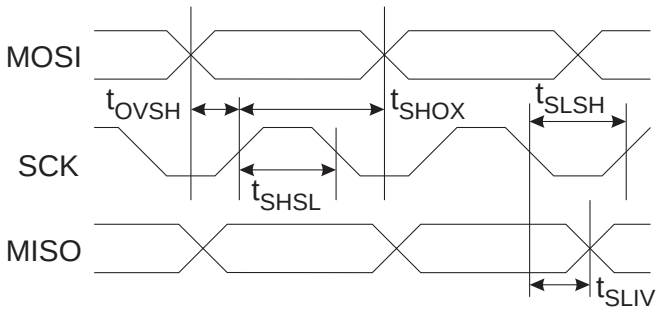


Table 79. T_A = -40°C 85°C, V_{CC} = 2.7V - 5.5V ( )

$1/t_{CLCL}$	(ATtiny2313L)	0		8	MHz
t_{CLCL}	(ATtiny2313L)	125			ns
$1/t_{CLCL}$	(ATtiny2313, V_{CC} = 4.5V - 5.5V)	0		16	MHz
t_{CLCL}	(ATtiny2313, V_{CC} = 4.5V - 5.5V)	67			ns
t_{SHSL}	SCK	2 t_{CLCL}*			ns
t_{SLSH}	SCK	2 t_{CLCL}*			ns
t_{OVSH}	MOSI SCK	t_{CLCL}			ns
t_{SHOX}	SCK MOSI	2 t_{CLCL}			ns
t_{SLIV}	SCK MISO	TBD	TBD	TBD	ns

Note: 1. f_{ck} < 12 MHz 2 t_{CLCL} f_{ck} >= 12 MHz 3 t_{CLCL}

*

.....	-55°C +125°C
.....	-65°C +150°C
$\overline{\text{RESET}}$	-0.5V V_{CC}+0.5V
$\overline{\text{RESET}}$	-0.5V +13.0V
.....	6.0V
I/O	40.0 mA
V_{CC} GND	200.0 mA

*NOTICE: " "

T_A = -40°C 85°C, V_{CC} = 1.8V 5.5V ( )[1]

V_{IL}			-0.5		$0.2V_{CC}$	V
V_{IH}		$\overline{\text{RESET}}$	$0.6V_{CC}$[3]		V_{CC} +0.5	V
V_{IH2}		$\overline{\text{RESET}}$	$0.9V_{CC}$[3]		V_{CC} +0.5	V
V_{OL}	[4] (B)	I_{OL} = 10 mA, V_{CC} = 5V I_{OL} = 5 mA, V_{CC} = 3V			0.7 0.5	V V
V_{OH}	[5] (B)	I_{OH} = -10 mA, V_{CC} = 5V I_{OH} = -5 mA, V_{CC} = 3V	4.2 2.5			V V
I_{IL}	I/O	Vcc = 5.5V, ( )			1	µA
I_{IH}	I/O	Vcc = 5.5V, ( )			1	µA
R_{RST}	Reset		30		60	kΩ
R_{pu}	I/O		20		50	kΩ
I_{CC}		1MHz, V_{CC} = 2V			0.35	mA
		4MHz, V_{CC} = 3V			2	mA
		8MHz, V_{CC} = 5V			6	mA
		1MHz, V_{CC} = 2V		0.08	0.2	mA
		4MHz, V_{CC} = 3V		0.41	1	mA
		8MHz, V_{CC} = 5V		1.6	3	mA
		WDT , V_{CC} = 3V		< 3	6	µA
		WDT , V_{CC} = 3V		< 0.5	2	µA

Notes: 1. AVR

2. " "
3. " "

4. ( ) I/O (20 mA V_{CC} = 5V 10 mA V_{CC} = 3V)

1] IOL 60 mA
IOL VOL

5. ( ) I/O (20 mA V_{CC} = 5V 10 mA V_{CC} = 3V)

1] IOH 60 mA
IOH VOH

Figure 80.

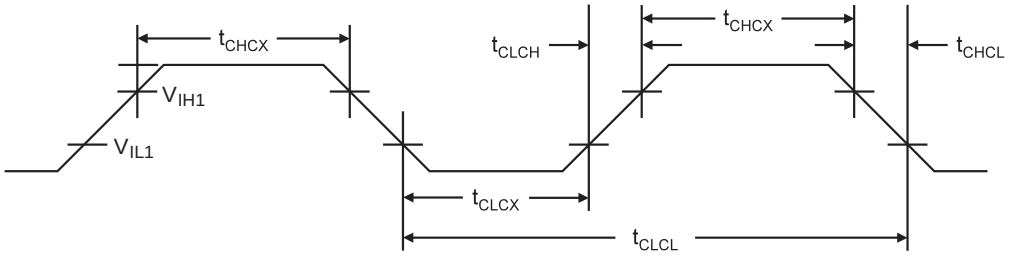


Table 80. ( )

		V_{CC}=1.8-5.5V				V_{CC}=4.5-5.5V		
$1/t_{CLCL}$		0	1	0	8	0	16	MHz
t_{CLCL}		1000		125		62.5		ns
t_{CHCX}		400		50		25		ns
t_{CLCX}		400		50		25		ns
t_{CLCH}			2.0		1.6		0.5	µs
t_{CHCL}			2.0		1.6		0.5	µs
Δt_{CLCL}			2		2		2	%

V_{CC} V_{CC} Figure 81 Figure 82 V_{CC} $1.8V < V_{CC} < 2.7V$ $2.7V < V_{CC} < 4.5V$

Figure 81. ATtiny2313V V_{CC}

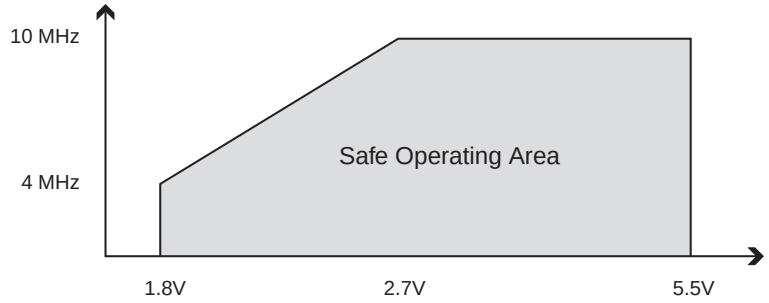
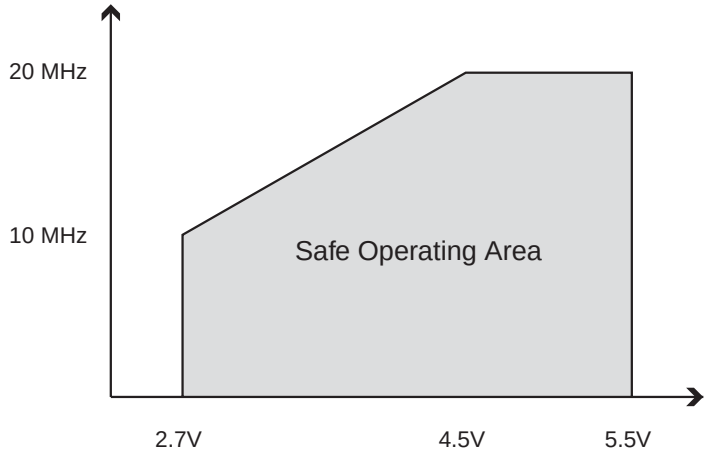


Figure 82. ATtiny2313 V_{CC}



ATtiny2313

I/O

I/O I/O

I/O $C_L*V_{CC}*f$ C_L = V_{CC} =
f = I/O

Figure 83. (0.1 - 1.0 MHz)

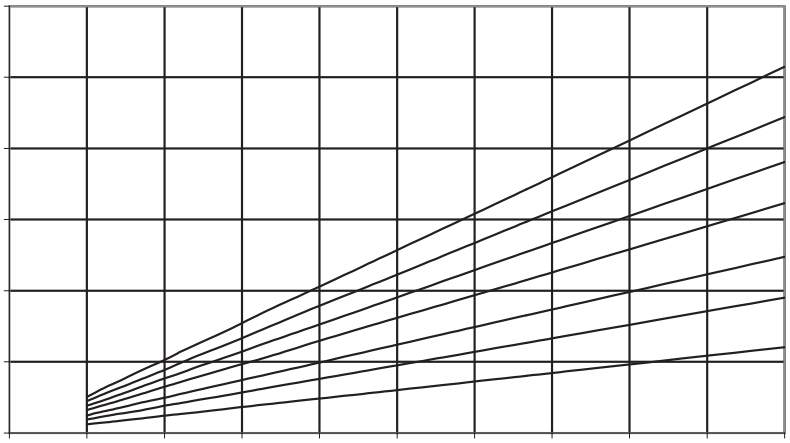


Figure 84. (1 - 20 MHz)

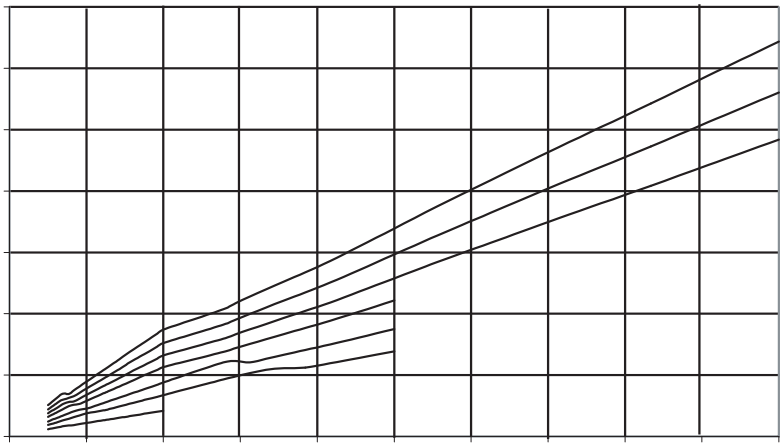


Figure 85. V_{CC} (RC 8 MHz)

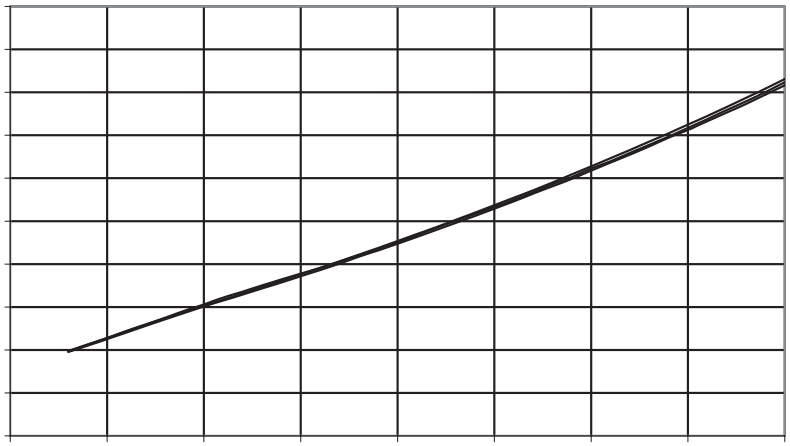


Figure 86. V_{CC} (RC 4 MHz)

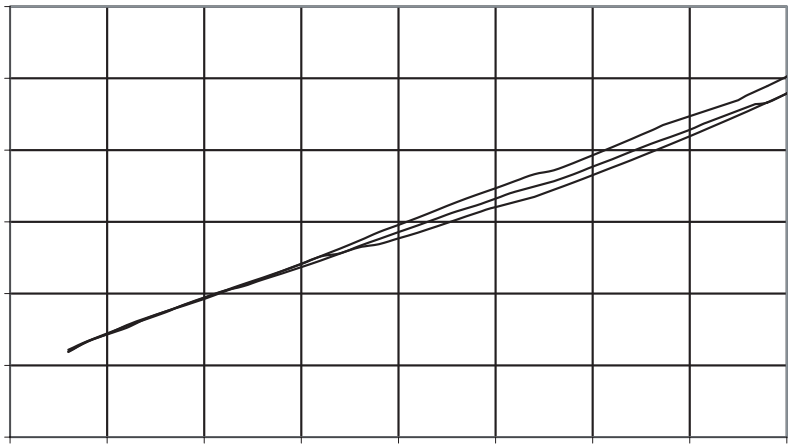


Figure 87. V_{CC} (RC 1 MHz)

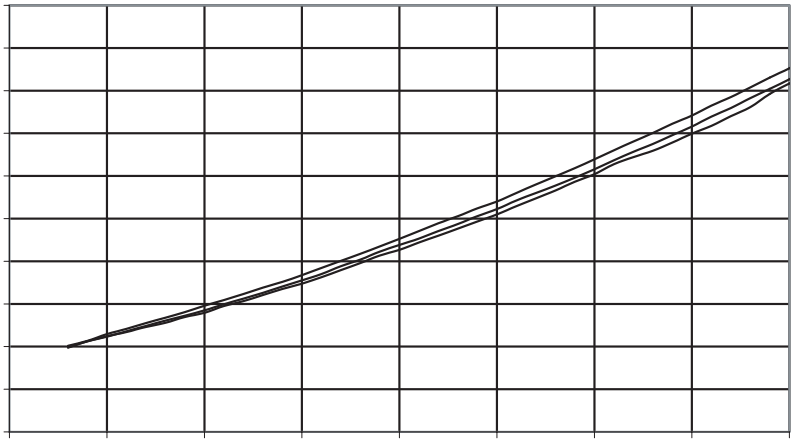


Figure 88. V_{CC} (RC 0.5 MHz)

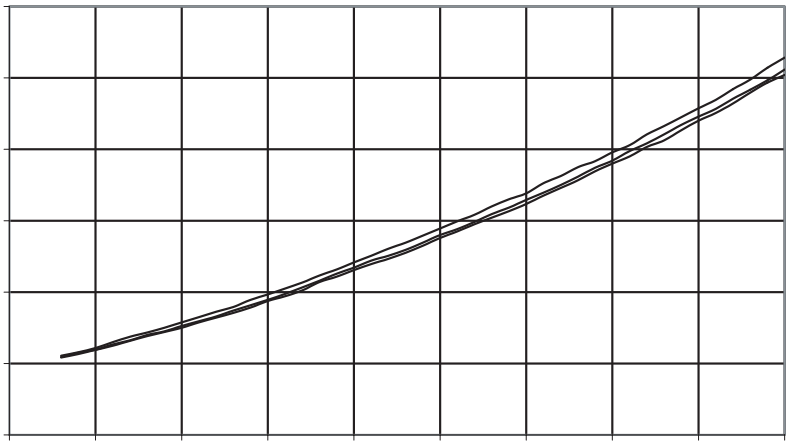


Figure 89. V_{CC} (RC 128 KHz)

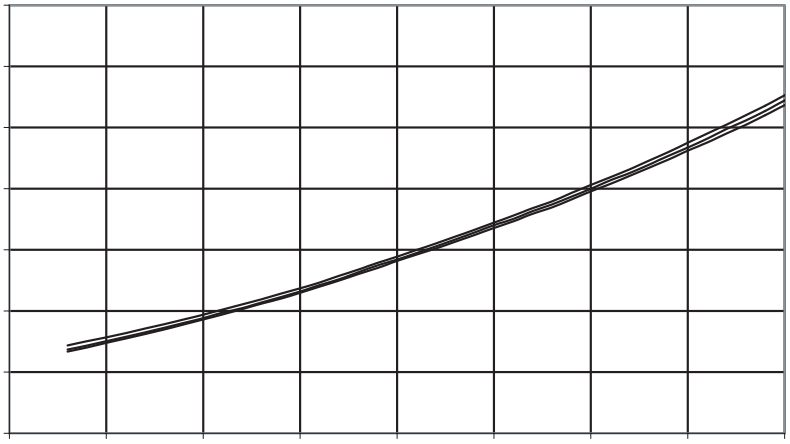


Figure 90. (0.1 - 1.0 MHz)

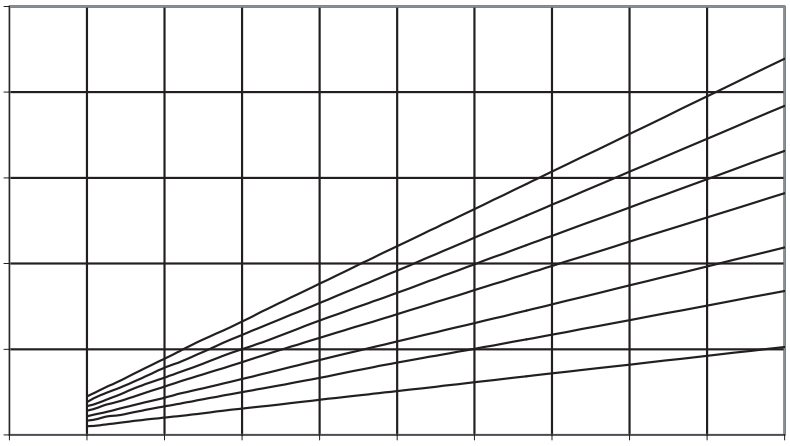


Figure 91. (1 - 20 MHz)

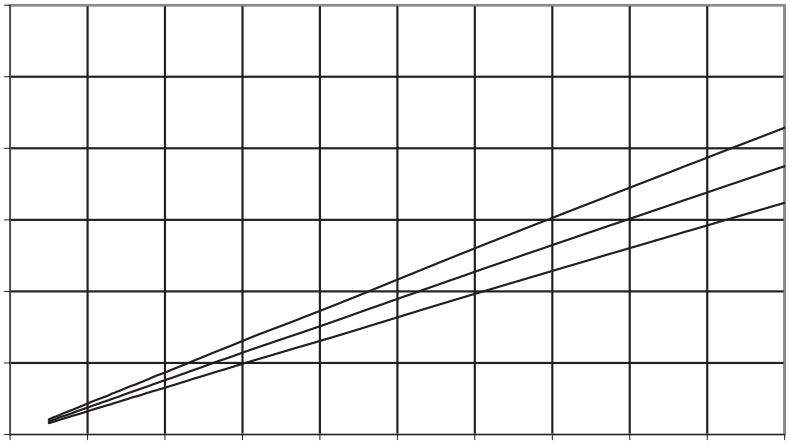


Figure 92. V_{CC} (RC 8 MHz)

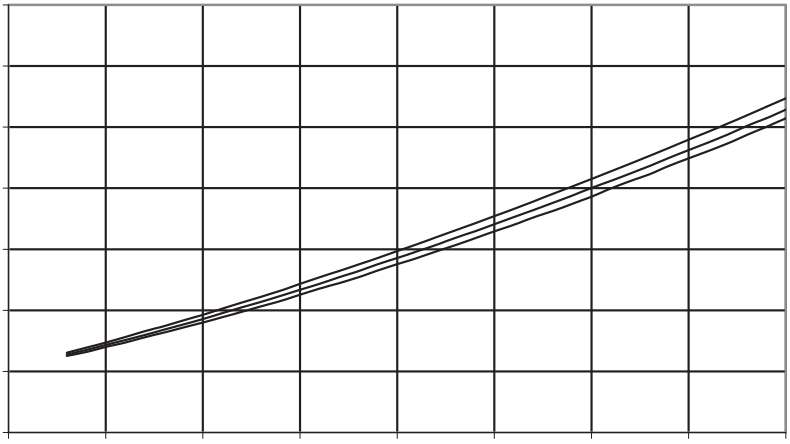


Figure 93. V_{CC} (RC 4 MHz)

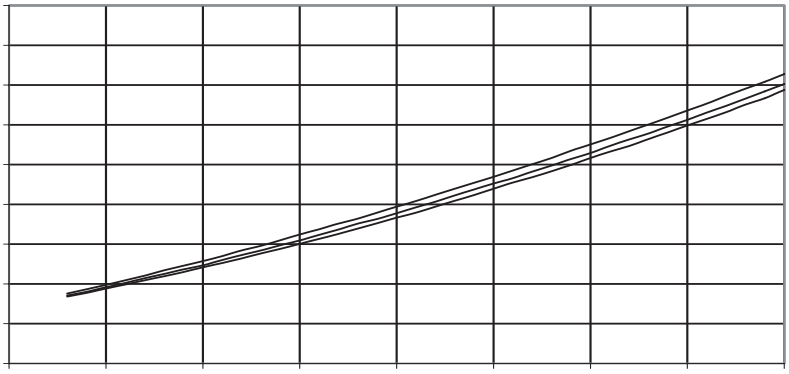


Figure 94. V_{CC} (RC 1 MHz)

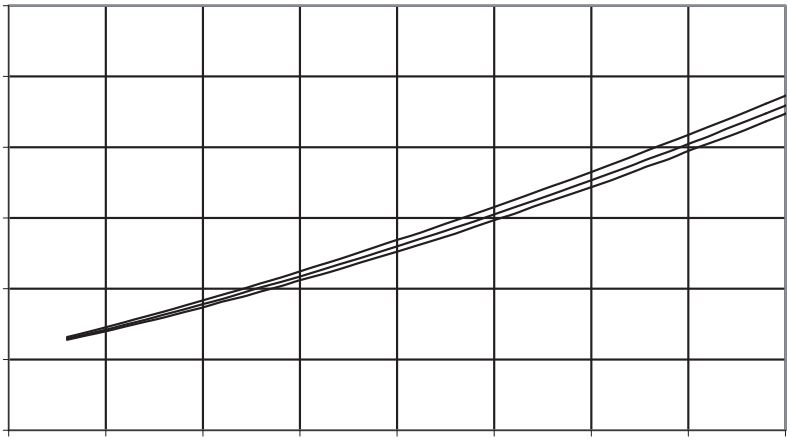


Figure 95. V_{CC} (RC 0.5 MHz)

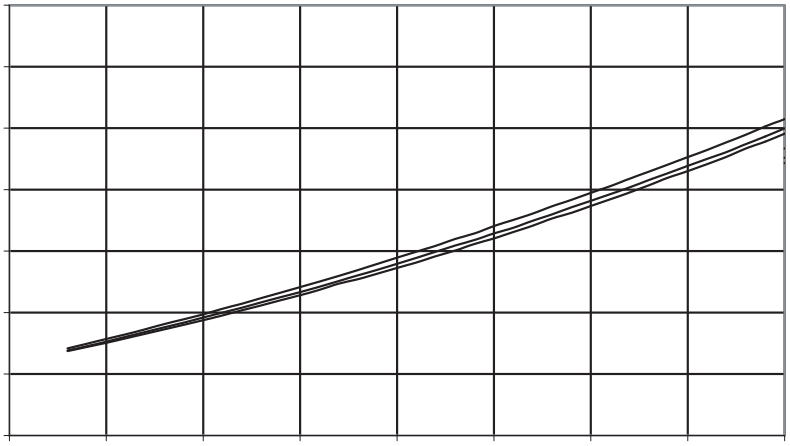


Figure 96. V_{CC} (RC 128 KHz)

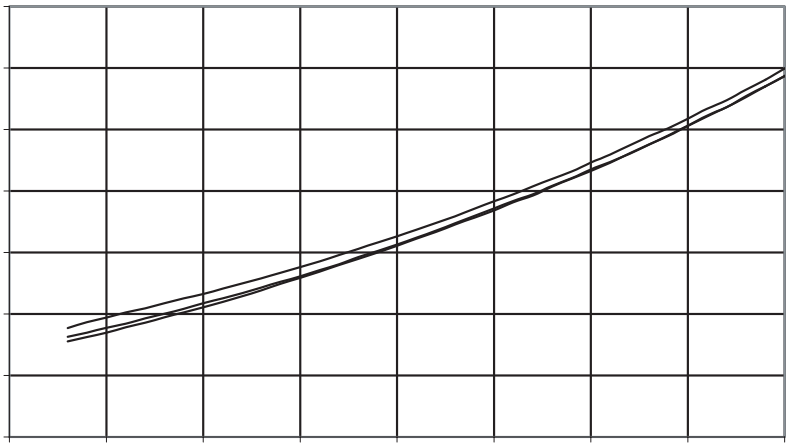


Figure 97. V_{CC} ( )

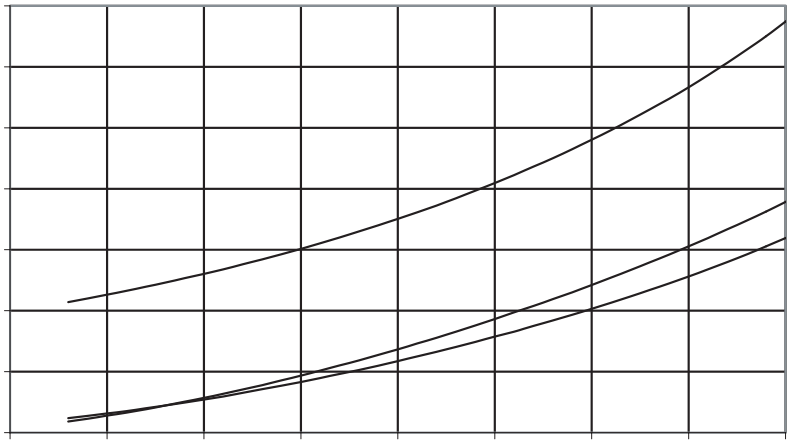
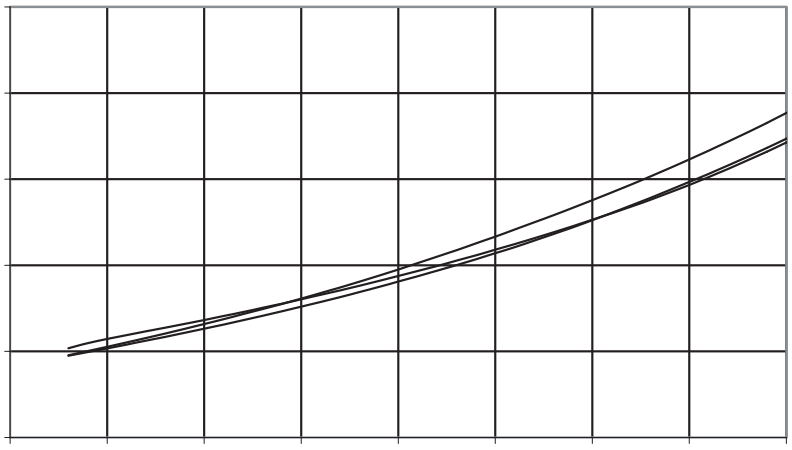


Figure 98. V_{CC} ( )



Standby

Figure 99. Standby V_{CC}

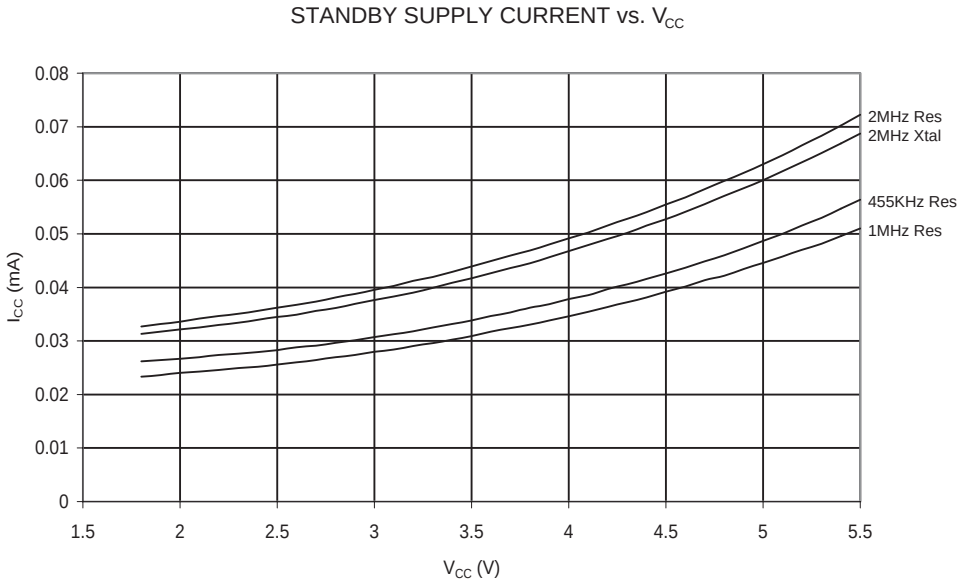


Figure 100. I/O (V_{CC} = 5V)

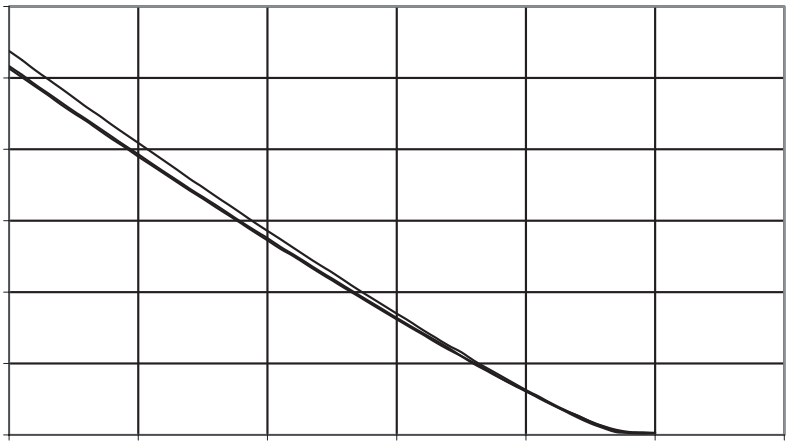


Figure 101. I/O (V_{CC} = 2.7V)

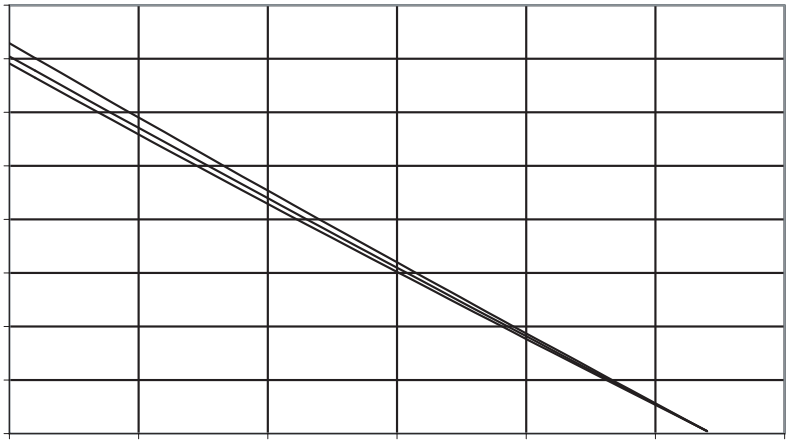


Figure 102. (Reset) Reset (V_{CC} = 5V)

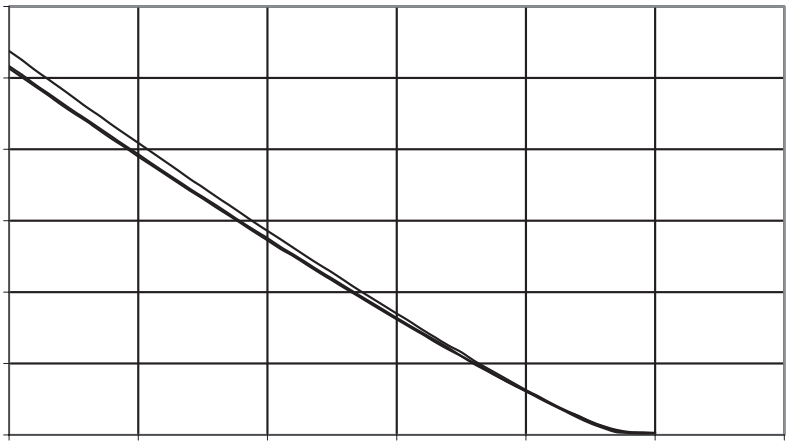


Figure 103. (Reset) Reset (V_{CC} = 2.7V)

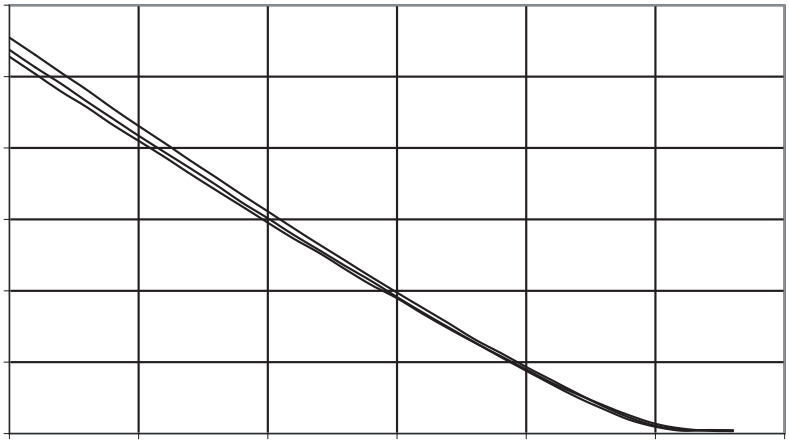


Figure 104. I/O (V_{CC} = 5V)

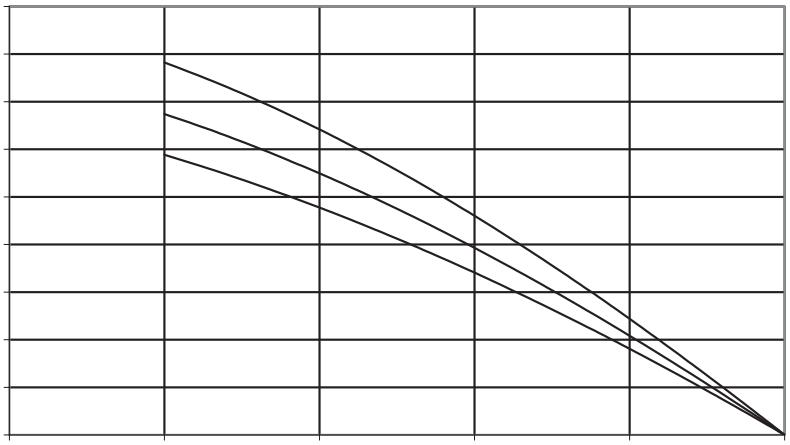


Figure 105. I/O (V_{CC} = 2.7V)

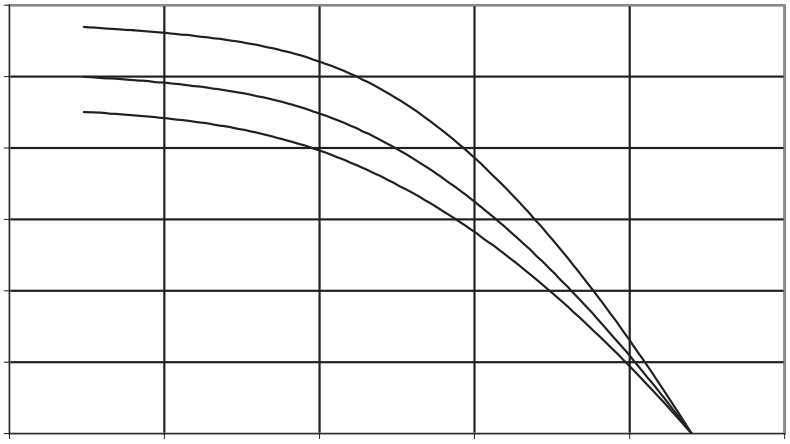


Figure 106. I/O (V_{CC} = 1.8V)

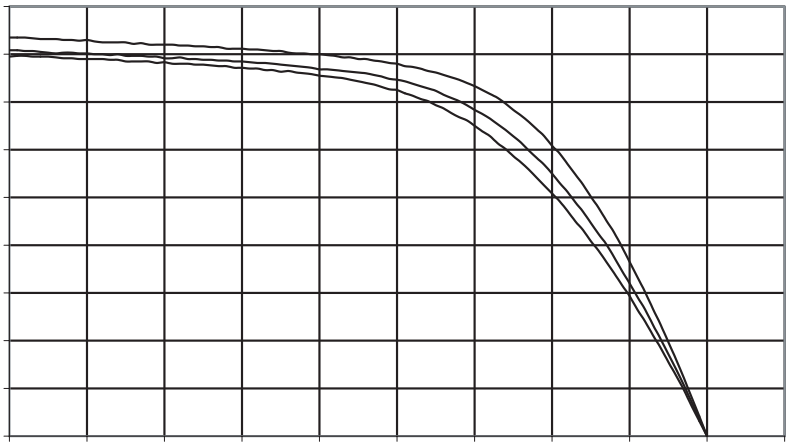


Figure 107. I/O (V_{CC} = 5V)

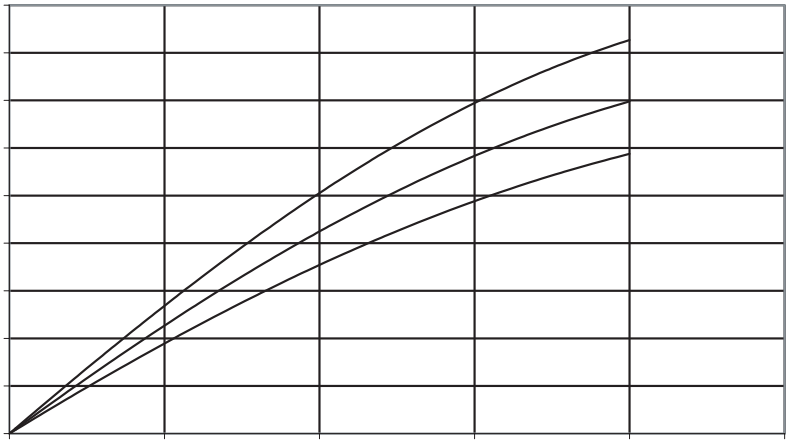


Figure 108. I/O (V_{CC} = 2.7V)

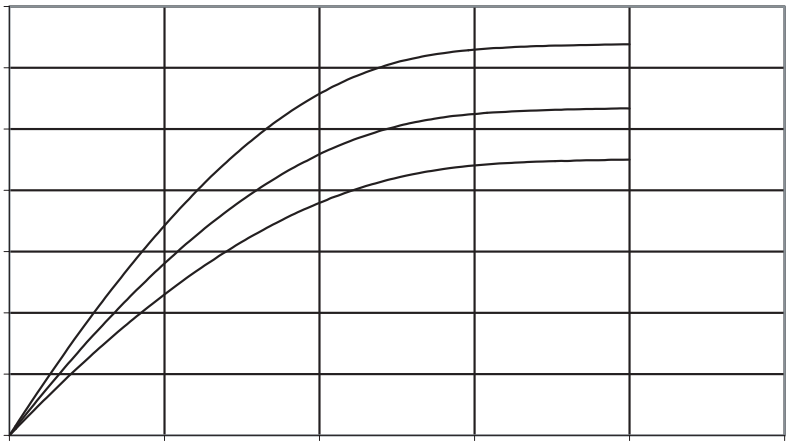


Figure 109. I/O (V_{CC} = 1.8V)

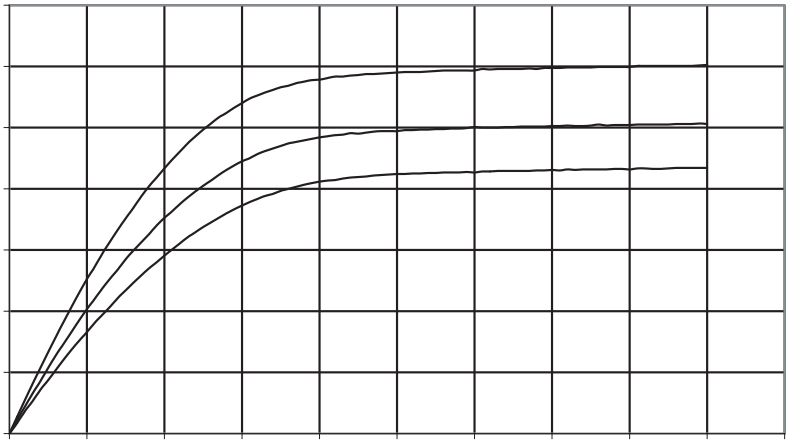


Figure 110. I/O (V_{CC} = 5V)

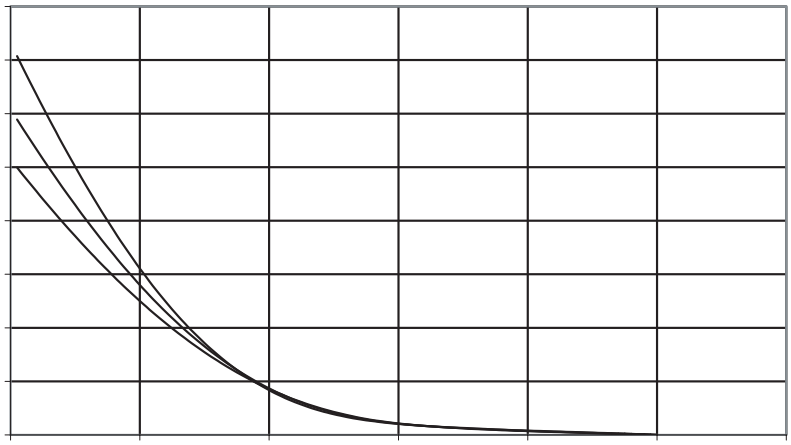


Figure 111. I/O (V_{CC} = 2.7V)

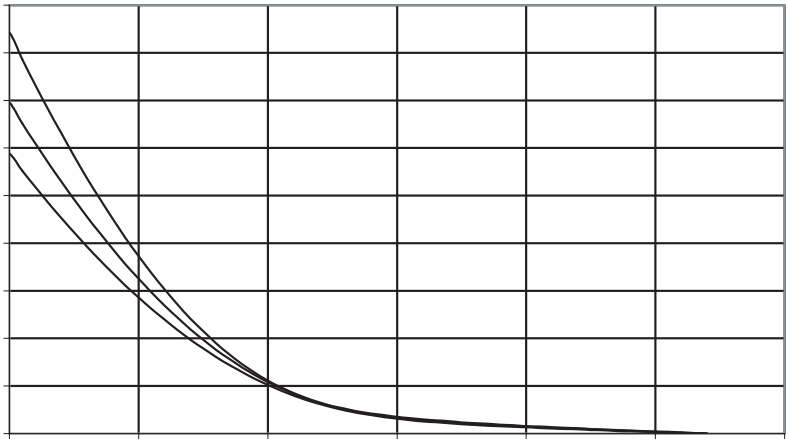


Figure 112. I/O (V_{CC} = 1.8V)

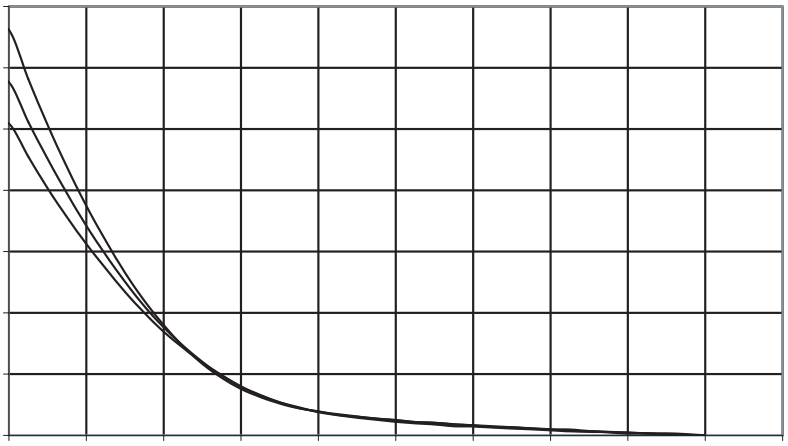


Figure 113. I/O (V_{CC} = 5V)

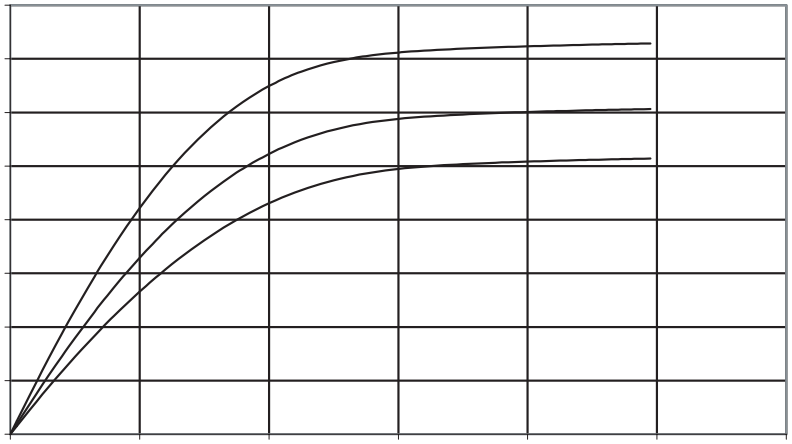


Figure 114. I/O (V_{CC} = 2.7V)

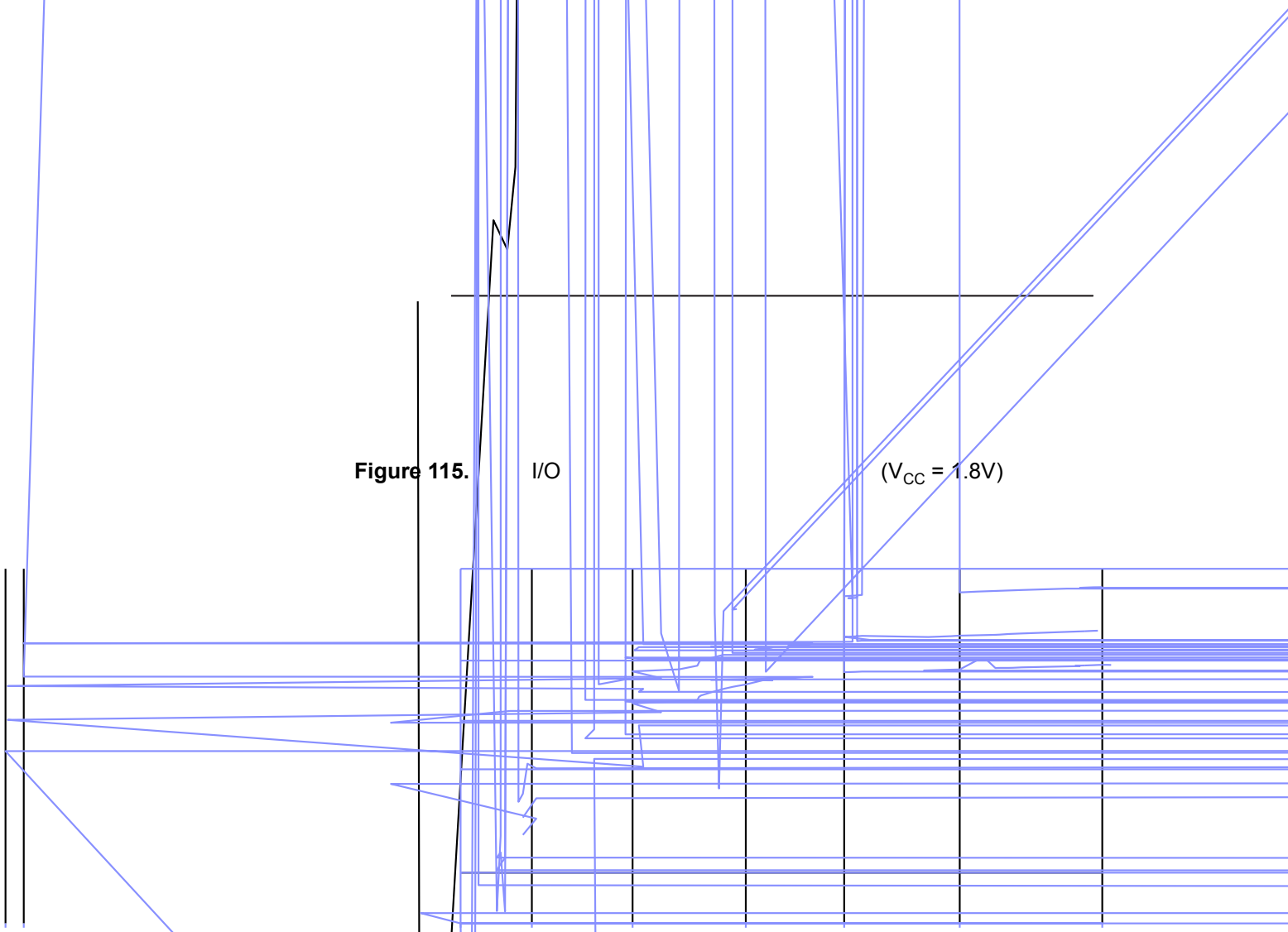


Figure 115. I/O (V_{CC} = 1.8V)

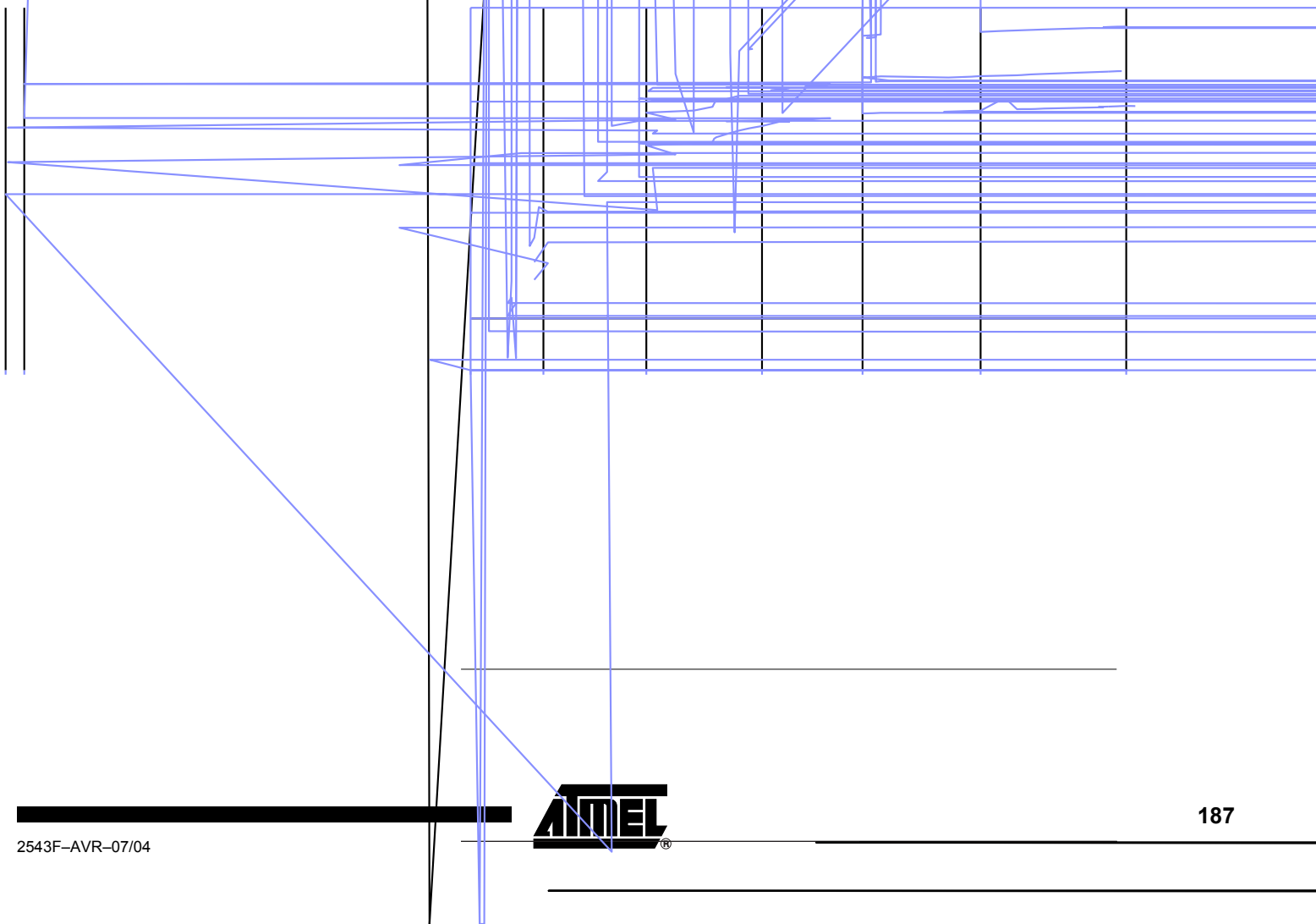


Figure 116. I/O V_{CC} (V_{IH}, I/O "1")

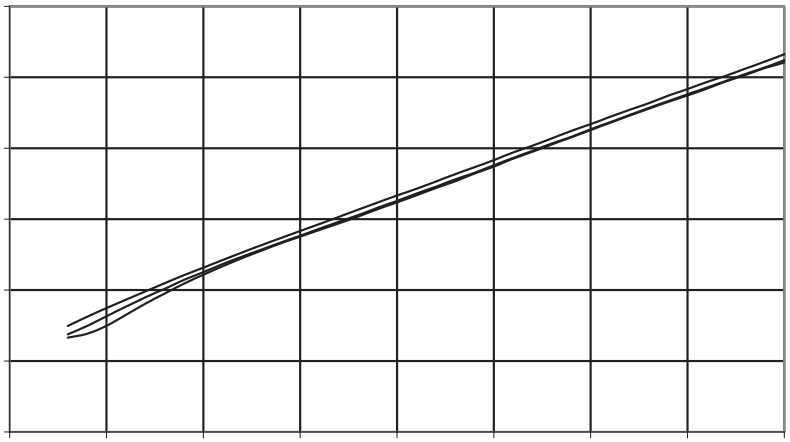


Figure 117. I/O V_{CC} (V_{IL}, I/O "0")

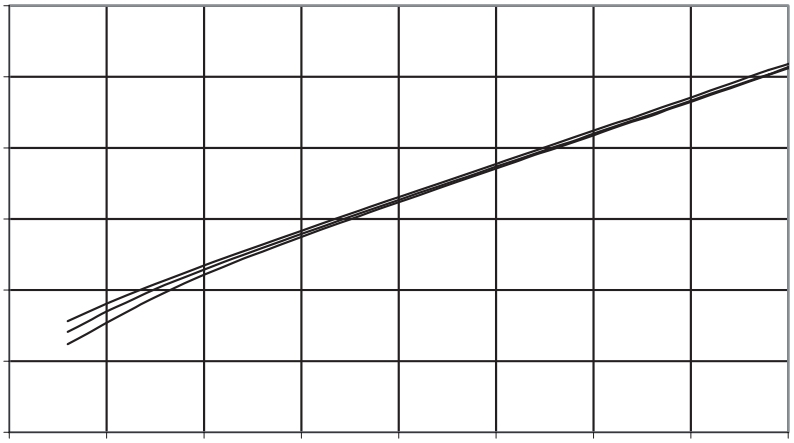


Figure 118. I/O V_{CC}

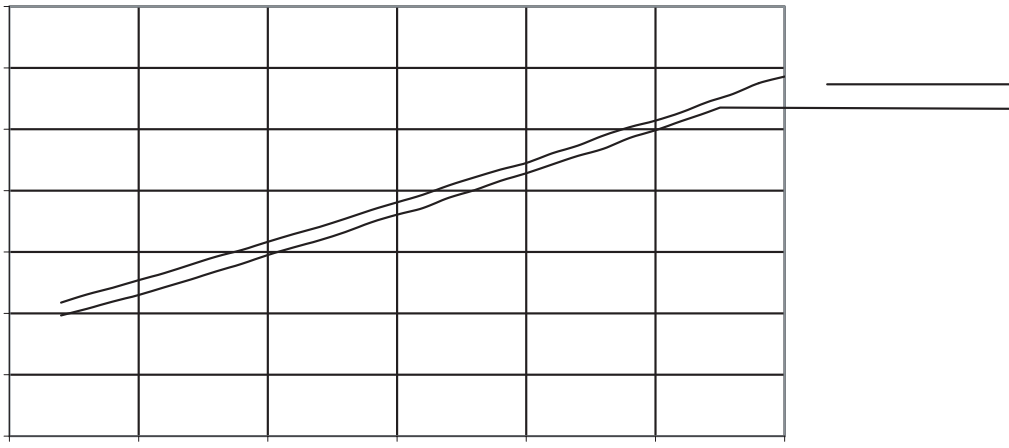


Figure 119. Reset I/O V_{CC} (V_{IH},Reset "1")

Figure 120. Reset I/O V_{CC} (V_{IL},Reset "0")

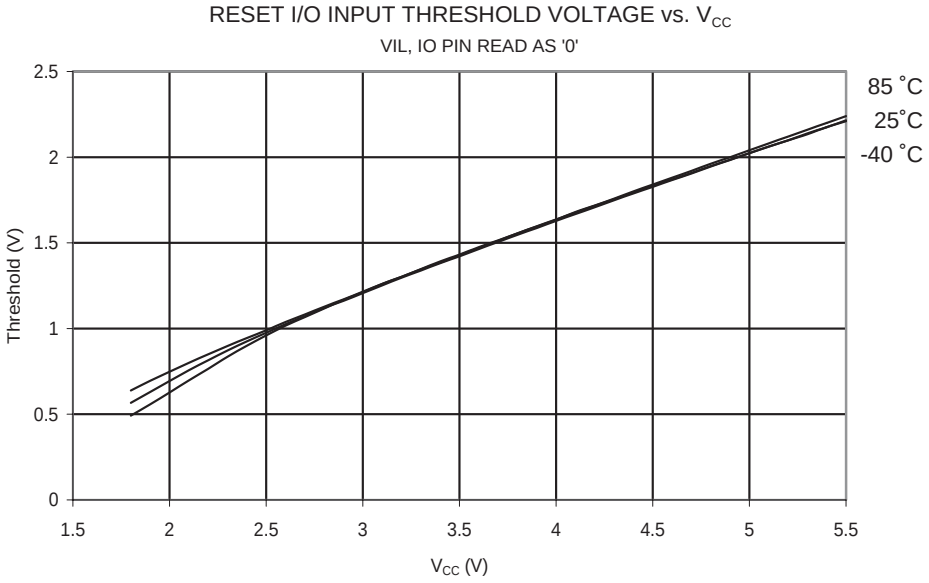


Figure 121. Reset I/O V_{CC}

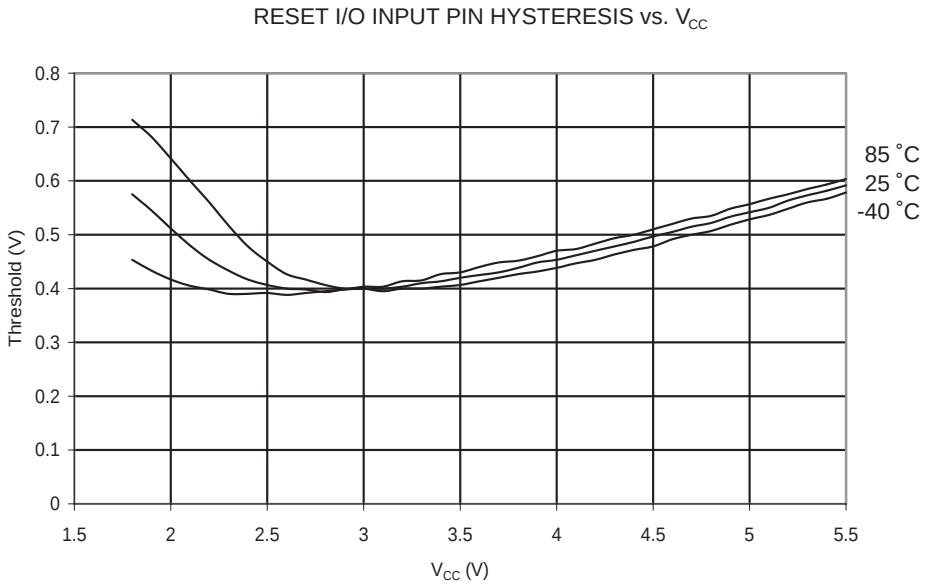


Figure 122. Reset V_{CC} (V_{IH},Reset "1")

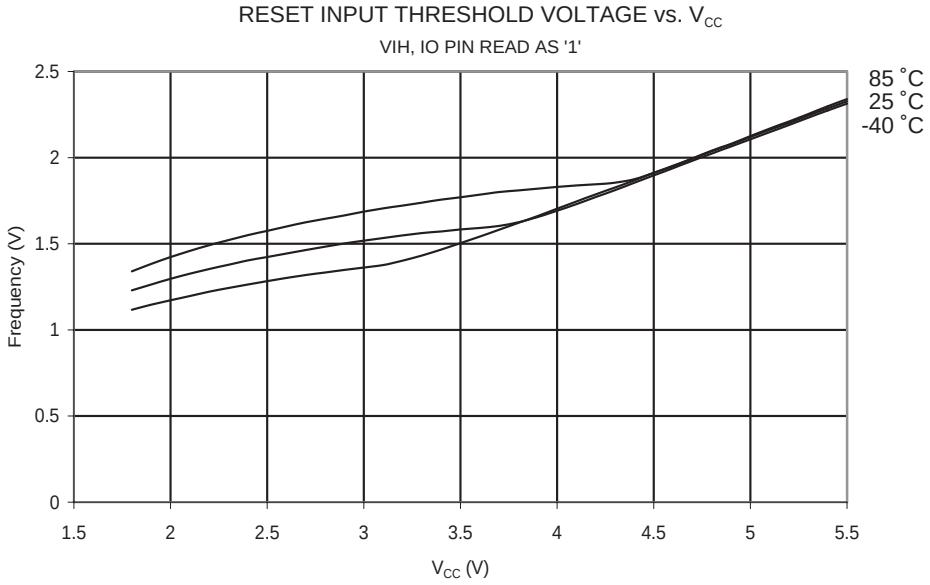


Figure 123. Reset V_{CC} (V_{IL},Reset "0")

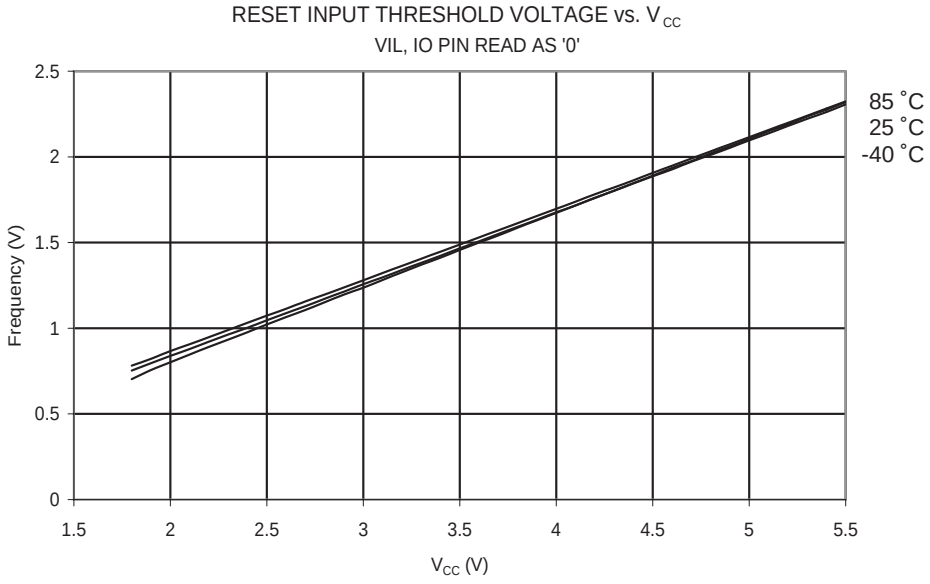
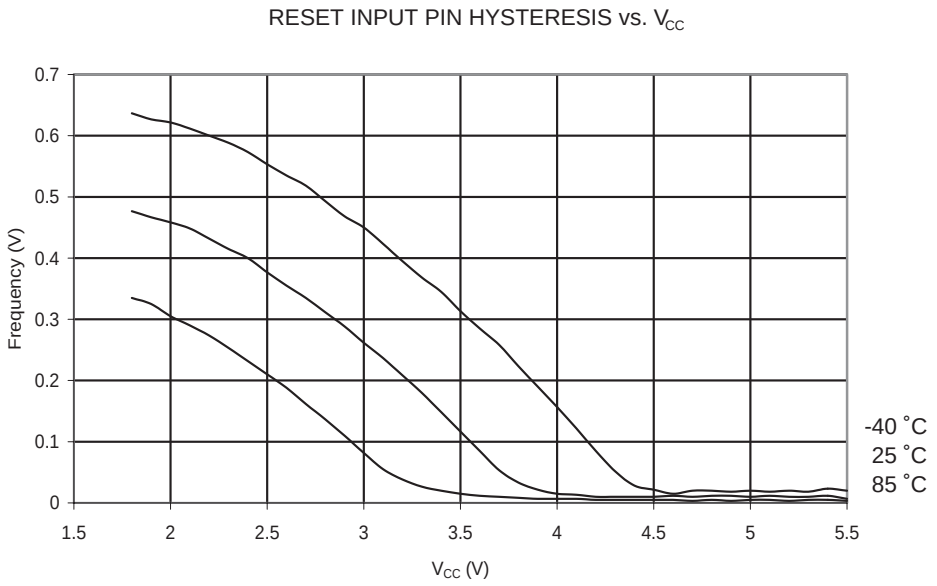


Figure 124. Reset V_{CC}



BOD

Figure 125. BOD (BOD 4.3V)

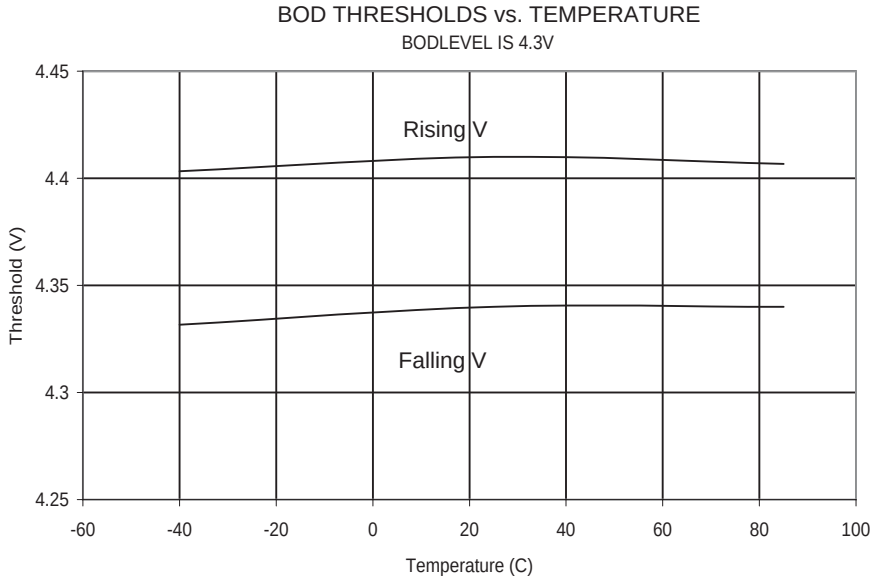


Figure 128. V_{CC}

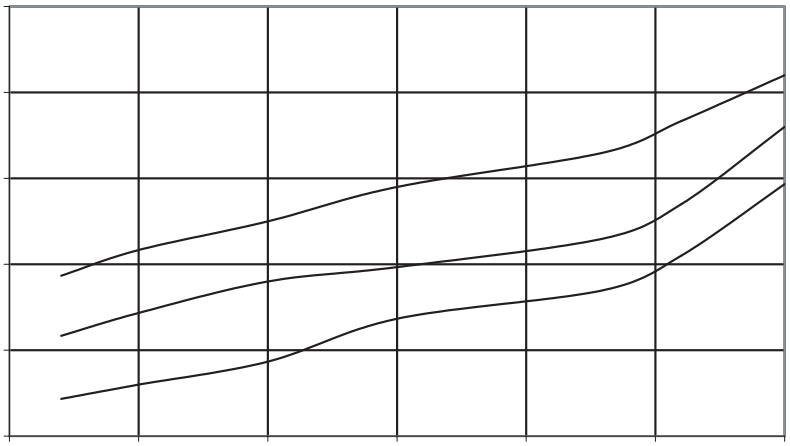


Figure 129. V_{CC}

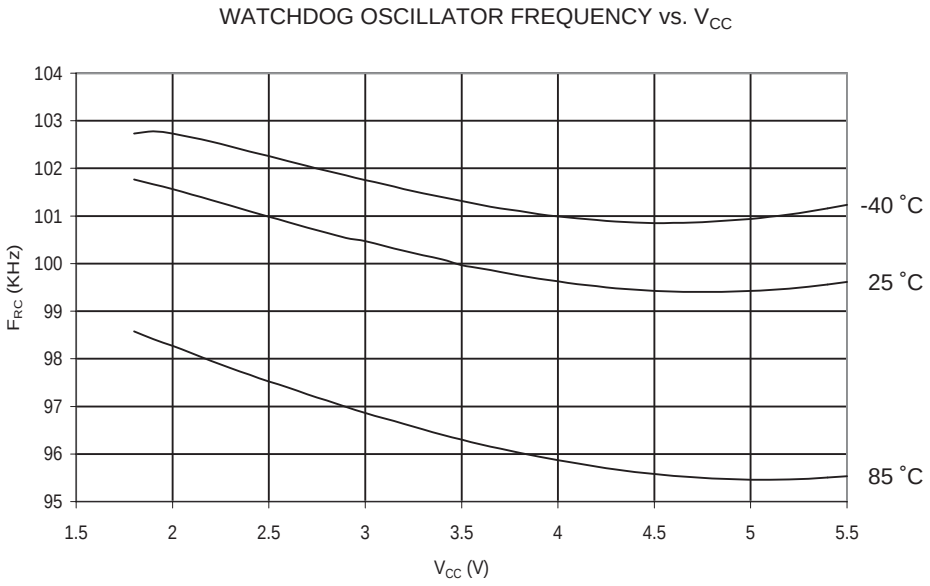


Figure 130.

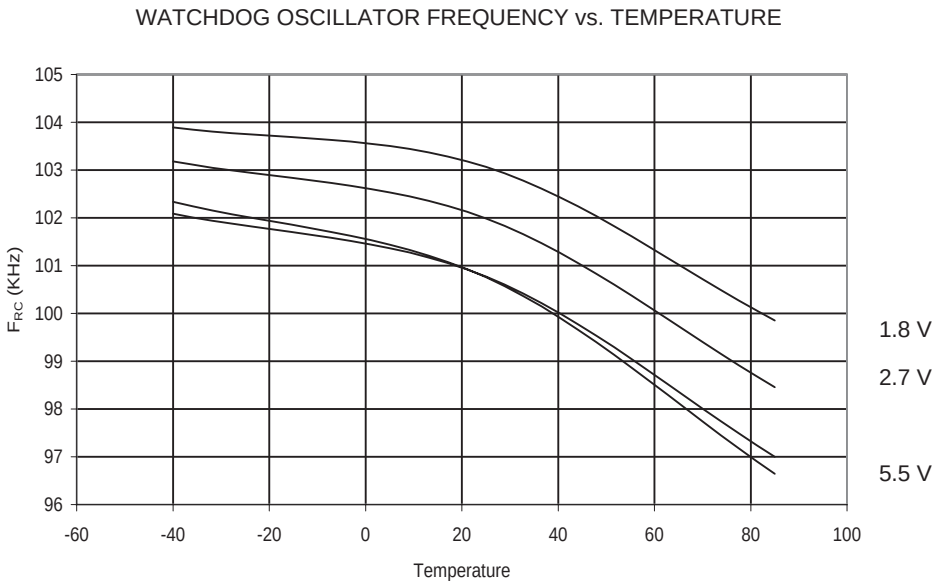


Figure 131. 8 MHz RC

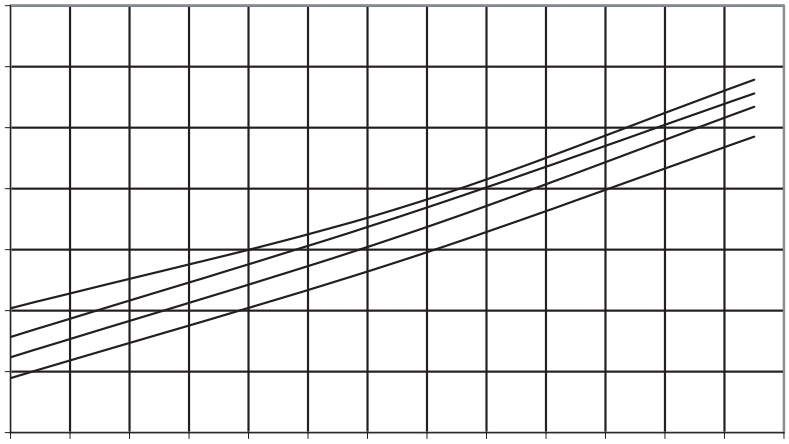


Figure 132. 8 MHz RC V_{CC}

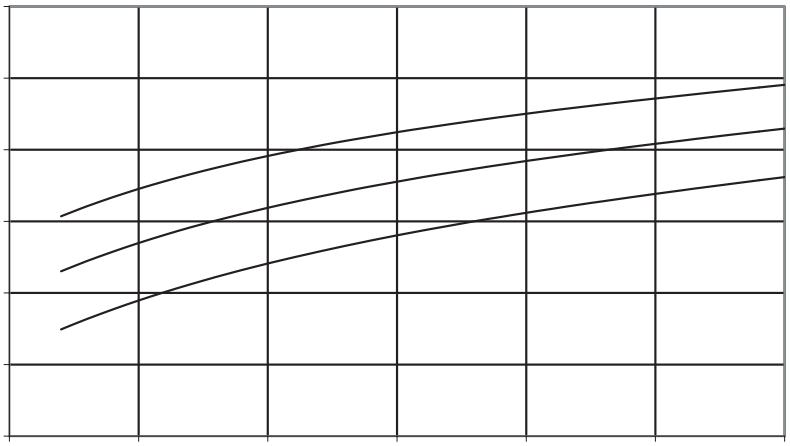


Figure 133. 8 MHz RC Osccal

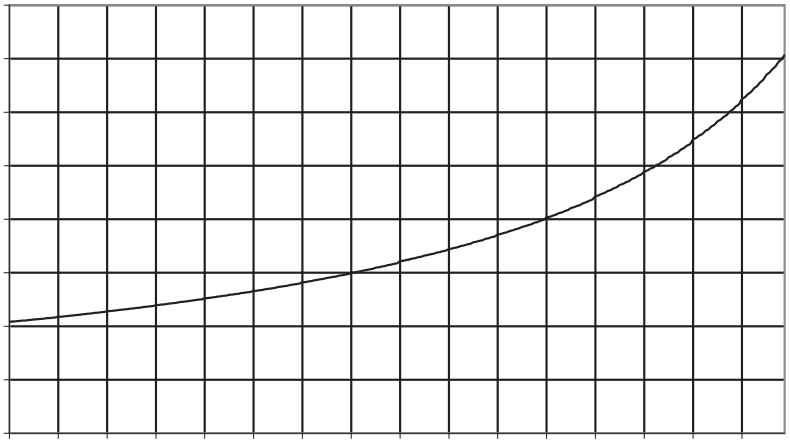


Figure 134. 4 MHz RC I

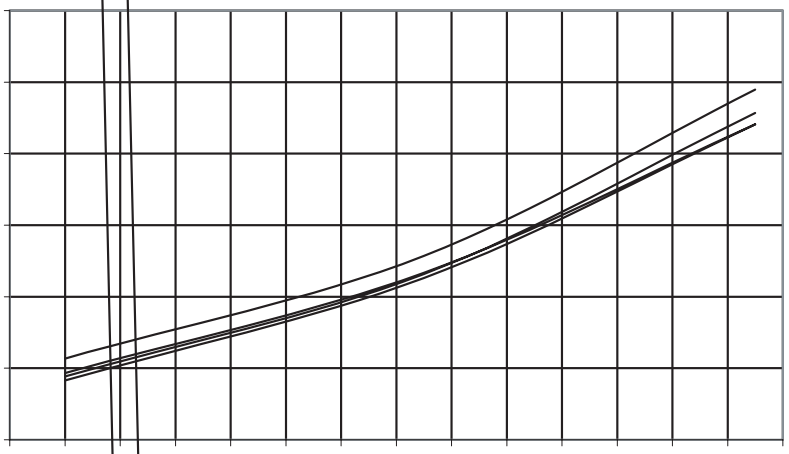


Figure 135. 4 MHz RC V_{CC}

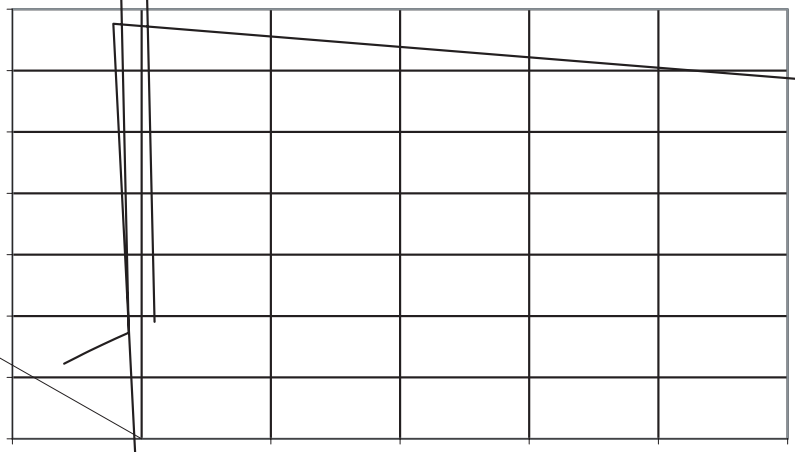


Figure 136. 4 MHz RC Osccal

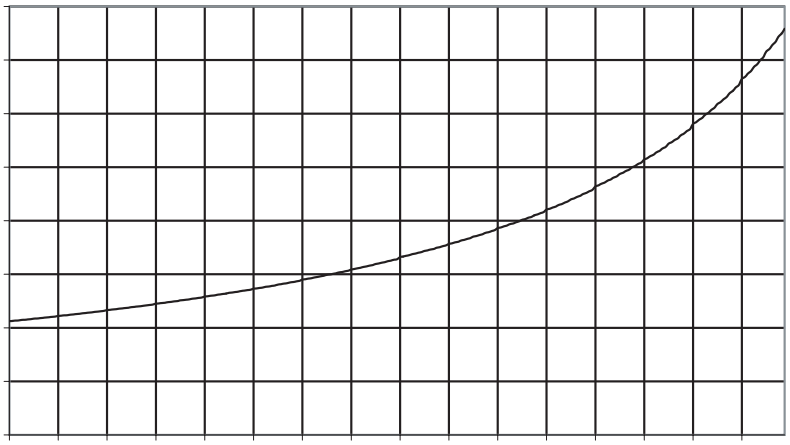


Figure 137. BOD V_{CC}

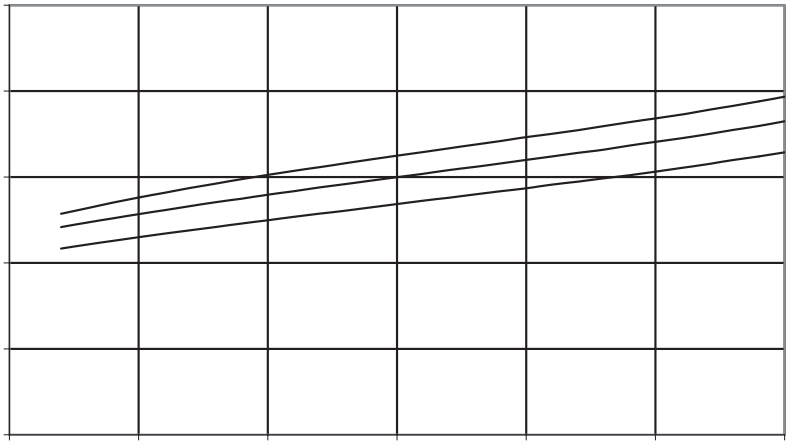


Figure 138. V_{CC}

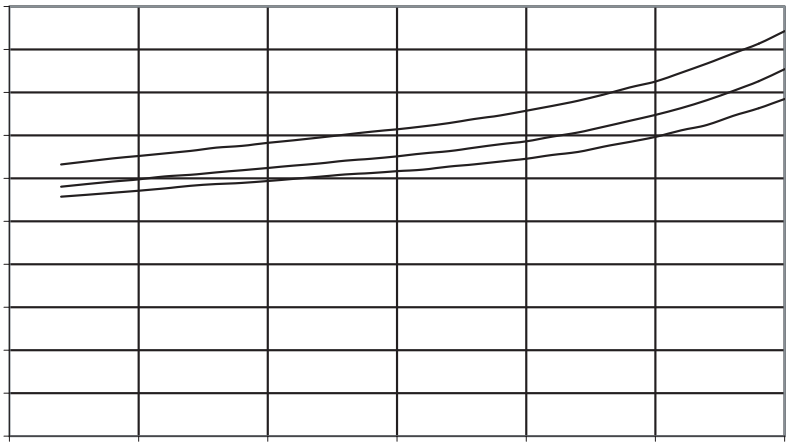


Figure 139. V_{CC}

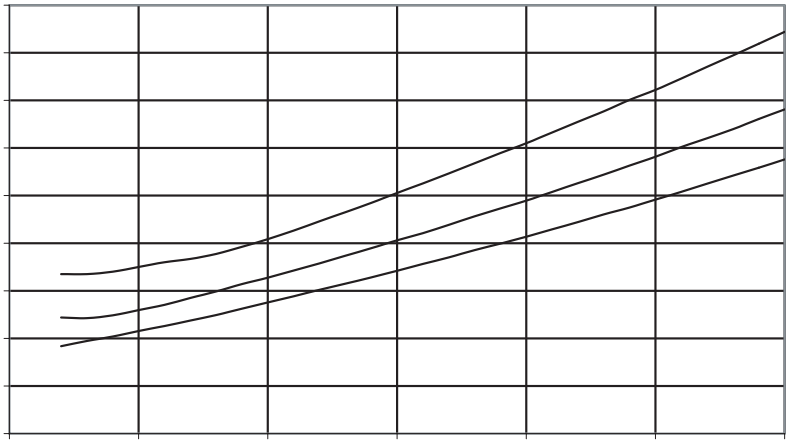


Figure 140. V_{CC} (0.1 - 1.0 MHz)

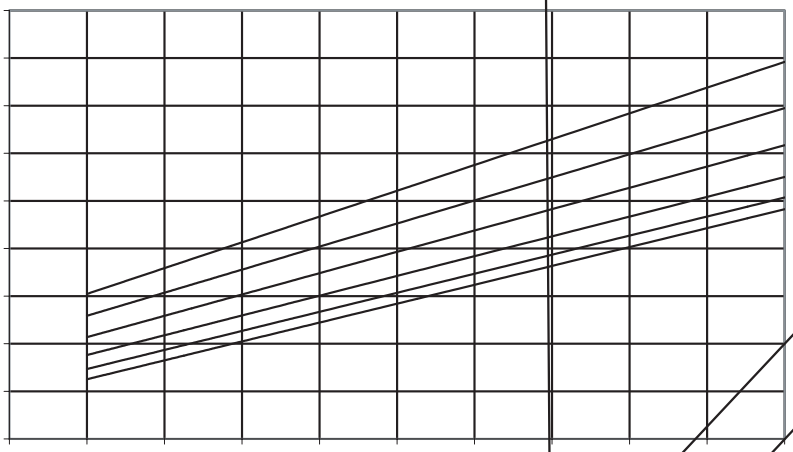
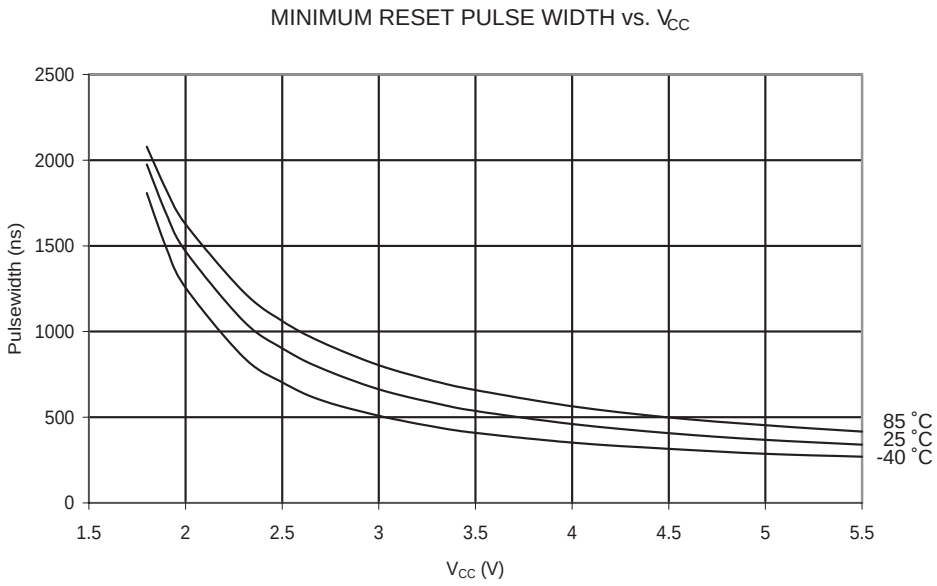


Figure 141. V_{CC} (1 - 20 MHz)

Figure 142. V_{CC}



		7	6	5	4	3	2	1	0	
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	7
0x3E (0x5E)		–	–	–	–	–	–	–	–	
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	10
0x3C (0x5C)	OCR0B	T/C0 B								73
0x3B (0x5B)	GIMSK	INT1	INT0	PCIE	–	–	–	–	–	58
0x3A (0x5A)	EIFR	INTF1	INTF0	PCIF	–	–	–	–	–	59
0x39 (0x59)	TIMSK	TOIE1	OCIE1A	OCIE1B	–	ICIE1	OCIE0B	TOIE0	OCIE0A	74, 102
0x38 (0x58)	TIFR	TOV1	OCF1A	OCF1B	–	ICF1	OCF0B	TOV0	OCF0A	74
0x37 (0x57)	SPMCSR	–	–	–	CTPB	RFLB	PGWRT	PGERS	SELFPRGEN	147
0x36 (0x56)	OCR0A	T/C0 A								73
0x35 (0x55)	MCUCR	PUD	SM1	SE	SM0	ISC11	ISC10	ISC01	ISC00	51
0x34 (0x54)	MCUSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	35
0x33 (0x53)	TCCR0B	FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00	72
0x32 (0x52)	TCNT0	T/C0 (8)								73
0x31 (0x51)	OSCCAL	–	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	25
0x30 (0x50)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	–	–	WGM01	WGM00	69
0x2F (0x4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1BO	–	–	WGM11	WGM10	97
0x2E (0x4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	100
0x2D (0x4D)	TCNT1H	T/C1 –								101
0x2C (0x4C)	TCNT1L	T/C1 –								101
0x2B (0x4B)	OCR1AH	T/C1 – A								101
0x2A (0x4A)	OCR1AL	T/C1 – A								101
0x29 (0x49)	OCR1BH	T/C1 – B								102
0x28 (0x48)	OCR1BL	T/C1 – B								102
0x27 (0x47)		–	–	–	–	–	–	–	–	
0x26 (0x46)	CLKPR	CLKPCE	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	27
0x25 (0x45)	ICR1H	T/C1 -								102
0x24 (0x44)	ICR1L	T/C1 -								102
0x23 (0x43)	GTCCR	–	–	–	–	–	–	–	PSR10	76
0x22 (0x42)	TCCR1C	FOC1A	FOC1B	–	–	–	–	–	–	100
0x21 (0x41)	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	40
0x20 (0x40)	PCMSK	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	59
0x1F (0x3F)		–	–	–	–	–	–	–	–	
0x1E (0x3E)	EEAR	–	EEPROM							15
0x1D (0x3D)	EEDR	EEPROM								16
0x1C (0x3C)	EECR	–	–	EEPM1	EEPM0	EERIE	EEMPE	EEPE	EERE	16
0x1B (0x3B)	PORTA	–	–	–	–	–	PORTR2	PORTA1	PORTA0	56
0x1A (0x3A)	DDRA	–	–	–	–	–	DDA2	DDA1	DDA0	56
0x19 (0x39)	PINA	–	–	–	–	–	PINA2	PINA1	PINA0	56
0x18 (0x38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	56
0x17 (0x37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	56
0x16 (0x36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	56
0x15 (0x35)	GPIOR2	I/O 2								20
0x14 (0x34)	GPIOR1	I/O 1								20
0x13 (0x33)	GPIOR0	I/O 0								20
0x12 (0x32)	PORTD	–	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	56
0x11 (0x31)	DDRD	–	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	56
0x10 (0x30)	PIND	–	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	56
0x0F (0x2F)	USIDR	USI								137
0x0E (0x2E)	USISR	USISIF	USIOIF	USIPF	USIDC	USICNT3	USICNT2	USICNT1	USICNT0	137
0x0D (0x2D)	USICR	USISIE	USIOIE	USIWM1	USIWM0	USICS1	USICS0	USICLK	USITC	138
0x0C (0x2C)	UDR	UART (8)								121
0x0B (0x2B)	UCSRA	RXC	TXC	UDRE	FE	DOR	UPE	U2X	MPCM	122
0x0A (0x2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8	124
0x09 (0x29)	UBRRL	UBRRH[7:0]								126
0x08 (0x28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	141
0x07 (0x27)		–	–	–	–	–	–	–	–	
0x06 (0x26)		–	–	–	–	–	–	–	–	
0x05 (0x25)		–	–	–	–	–	–	–	–	
0x04 (0x24)		–	–	–	–	–	–	–	–	
0x03 (0x23)	UCSRC	–	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	125
0x02 (0x22)	UBRRH	–	–	–	–	UBRRH[11:8]				126
0x01 (0x21)	DIDR	–	–	–	–	–	–	AIN1D	AIN0D	142
0x00 (0x20)		–	–	–	–	–	–	–	–	

Note: 1. "0" I/O

2. SBI CBI 0x00 - 0x1F I/O SBIS SBIC

3. "1" AVR CBI SBI CBI SBI 0x00 - 0x1F

4. I/O IN OUT 0x00 - 0x3F I/O LD ST I/O 0x20

					#
ADD	Rd, Rr		Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr		Rd ← Rd + Rr + C	Z,C,N,V,H	1
ADIW	Rdl,K		Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr		Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd, K		Rd ← Rd - K	Z,C,N,V,H	1
SBC	Rd, Rr		Rd ← Rd - Rr - C	Z,C,N,V,H	1
SBCI	Rd, K		Rd ← Rd - K - C	Z,C,N,V,H	1
SBIW	Rdl,K		Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr		Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K		Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr		Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K		Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr		Rd ← Rd ⊕ Rr	Z,N,V	1
COM	Rd	1	Rd ← 0xFF − Rd	Z,C,N,V	1
NEG	Rd	2	Rd ← 0x00 − Rd	Z,C,N,V,H	1
SBR	Rd,K		Rd ← Rd v K	Z,N,V	1
CBR	Rd,K		Rd ← Rd • (0xFF - K)	Z,N,V	1
INC	Rd		Rd ← Rd + 1	Z,N,V	1
DEC	Rd		Rd ← Rd − 1	Z,N,V	1
TST	Rd		Rd ← Rd • Rd	Z,N,V	1
CLR	Rd		Rd ← Rd ⊕ Rd	Z,N,V	1
SER	Rd		Rd ← 0xFF	None	1
RJMP	k		PC ← PC + k + 1	None	2
IJMP		(Z)	PC ← Z	None	2
RCALL	k		PC ← PC + k + 1	None	3
ICALL		(Z)	PC ← Z	None	3
RET			PC ← STACK	None	4
RETI			PC ← STACK	I	4
CPSE	Rd,Rr		if (Rd = Rr) PC ← PC + 2 or 3	None	1/2/3
CP	Rd,Rr		Rd − Rr	Z, N,V,C,H	1
CPC	Rd,Rr		Rd − Rr − C	Z, N,V,C,H	1
CPI	Rd,K		Rd − K	Z, N,V,C,H	1
SBRC	Rr, b	"0"	if (Rr(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBRS	Rr, b	"1"	if (Rr(b)=1) PC ← PC + 2 or 3	None	1/2/3
SBIC	P, b	I/O "0"	if (P(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBIS	P, b	I/O "1"	if (P(b)=1) PC ← PC + 2 or 3	None	1/2/3
BRBS	s, k	"1"	if (SREG(s) = 1) then PC←PC+k + 1	None	1/2
BRBC	s, k	"0"	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k		if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k		if (Z = 0) then PC ← PC + k + 1	None	1/2
BRCS	k	"1"	if (C = 1) then PC ← PC + k + 1	None	1/2
BRCC	k	"0"	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k		if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k		if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k		if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k		if (N = 0) then PC ← PC + k + 1	None	1/2
BRGE	k		if (N ⊕ V= 0) then PC ← PC + k + 1	None	1/2
BRLT	k		if (N ⊕ V= 1) then PC ← PC + k + 1	None	1/2
BRHS	k	"1"	if (H = 1) then PC ← PC + k + 1	None	1/2
BRHC	k	"0"	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	T "1"	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	T "0"	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	"1"	if (V = 1) then PC ← PC + k + 1	None	1/2
BRVC	k	"0"	if (V = 0) then PC ← PC + k + 1	None	1/2
BRIE	k		if (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k		if (I = 0) then PC ← PC + k + 1	None	1/2
SBI	P,b	I/O	I/O(P,b) ← 1	None	2
CBI	P,b	I/O	I/O(P,b) ← 0	None	2
LSL	Rd		Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd		Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd		Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V	1

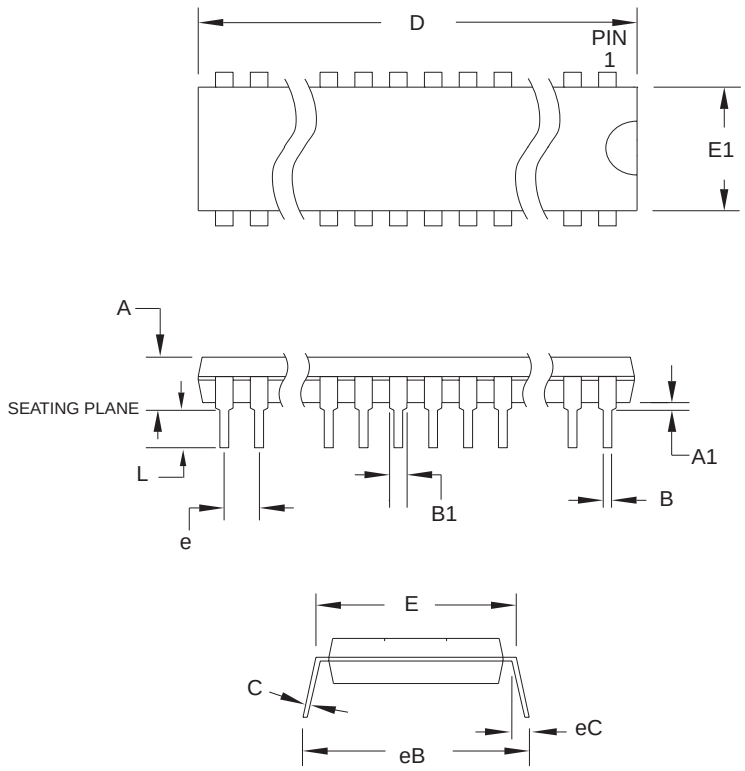
					#
ROR	Rd		Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
ASR	Rd		Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd		Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s		SREG(s) ← 1	SREG(s)	1
BCLR	s		SREG(s) ← 0	SREG(s)	1
BST	Rr, b	T	T ← Rr(b)	T	1
BLD	Rd, b	T	Rd(b) ← T	None	1
SEC			C ← 1	C	1
CLC			C ← 0	C	1
SEN			N ← 1	N	1
CLN			N ← 0	N	1
SEZ			Z ← 1	Z	1
CLZ			Z ← 0	Z	1
SEI			I ← 1	I	1
CLI			I ← 0	I	1
SES			S ← 1	S	1
CLS			S ← 0	S	1
SEV		2	V ← 1	V	1
CLV		2	V ← 0	V	1
SET		SREG T	T ← 1	T	1
CLT		SREG T	T ← 0	T	1
SEH		SREG	H ← 1	H	1
CLH		SREG	H ← 0	H	1
MOV	Rd, Rr		Rd ← Rr	None	1
MOVW	Rd, Rr		Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K		Rd ← K	None	1
LD	Rd, X		Rd ← (X)	None	2
LD	Rd, X+		Rd ← (X), X ← X + 1	None	2
LD	Rd, - X		X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y		Rd ← (Y)	None	2
LD	Rd, Y+		Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, - Y		Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd,Y+q		Rd ← (Y + q)	None	2
LD	Rd, Z		Rd ← (Z)	None	2
LD	Rd, Z+		Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z		Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q		Rd ← (Z + q)	None	2
LDS	Rd, k	SRAM	Rd ← (k)	None	2
ST	X, Rr		(X) ← Rr	None	2
ST	X+, Rr		(X) ← Rr, X ← X + 1	None	2
ST	- X, Rr		X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr		(Y) ← Rr	None	2
ST	Y+, Rr		(Y) ← Rr, Y ← Y + 1	None	2
ST	- Y, Rr		Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q,Rr		(Y + q) ← Rr	None	2
ST	Z, Rr		(Z) ← Rr	None	2
ST	Z+, Rr		(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr		Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q,Rr		(Z + q) ← Rr	None	2
STS	k, Rr	SRAM	(k) ← Rr	None	2
LPM			R0 ← (Z)	None	3
LPM	Rd, Z		Rd ← (Z)	None	3
LPM	Rd, Z+		Rd ← (Z), Z ← Z+1	None	3
SPM			(Z) ← R1:R0	None	-
IN	Rd, P	I/O	Rd ← P	None	1
OUT	P, Rr	I/O	P ← Rr	None	1
PUSH	Rr		STACK ← Rr	None	2
POP	Rd		Rd ← STACK	None	2
MCU					
NOP				None	1
SLEEP			(Sleep specific)	None	1
WDR			(WDR/timer specific)	None	1
BREAK				None	N/A

(MHz)			(1)	
10(3)	1.8 - 5.5V	ATtiny2313V-10PI ATtiny2313V-10PJ(2) ATtiny2313V-10SI ATtiny2313V-10SJ(2)	20P3 20P3 20S 20S	(-40°C 85°C)
20(3)	2.7 - 5.5V	ATtiny2313-20PI ATtiny2313-20PJ(2) ATtiny2313-20SI ATtiny2313-20SJ(2)	20P3 20P3 20S 20S	(-40°C 85°C)

Note: 1. wafer Atmel
2.
3. P170Figure 81 P170Figure 82

20P3	20	0.300"	PDIP
20S	20	0.300"	SOIC

20P3



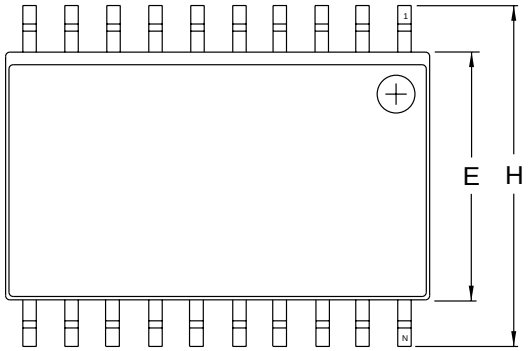
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	25.493	–	25.984	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.270	–	1.551	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

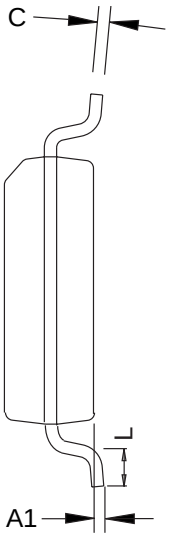
Notes: 1. This package conforms to JEDEC reference MS-001, Variation AD.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

1/12/04

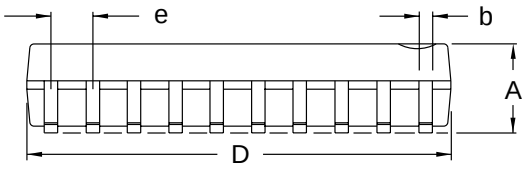
	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20P3**, 20-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	20P3	C



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.0926		0.1043	
A1	0.0040		0.0118	
b	0.0130		0.0200	4
C	0.0091		0.0125	
D	0.4961		0.5118	1
E	0.2914		0.2992	2
H	0.3940		0.4190	
L	0.0160		0.050	3
e	0.050 BSC			

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
2. Dimension "D" does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006") per side.
3. Dimension "E" does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010") per side.
4. "L" is the length of the terminal for soldering to a substrate.
5. The lead width "b", as measured 0.36 mm (0.014") or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024") per side.

1/9/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20S2**, 20-lead, 0.300" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)	20S2	A

ATtiny2313

ATtiny2313 Rev B

•
•
•

1.

2.7 V EEPROM 0x00

0xFF

2.

– (SPIEN)
– (RSTDISBL)

3.

ATtiny2313 Rev A

A

Rev. 2514E-04/04
Rev. 2514F-07/04

1. P1“ ”
2. P51“ B ”
3. P152“ ”
4. P152Table 69 P152Table 70 P152“ ”
5. P164“ ”
6. P165Table 78
7. P168“ ”
8. P171“ATtiny2313 ”
9. PCINT15 PCINT7, EEMWE EEMPE EEWE EEPE

Rev. 2514D-03/04
Rev. 2514E-04/04

1. - 12MHz 10MHz
   - 24MHz 20MHz
2. P2Figure 1
3. P206“ ”
4. P170“ V_{CC} ”
5. P171“ATtiny2313 ”

Rev. 2514C-12/03
Rev. 2514D-03/04

1. P21Table 2
2. P37“ ”
3. P170“ V_{CC} ”
4. P164“ ”
5. P198Figure 137 mA µA
6. P206“ ” MLF
7. P207“20P3”
8. C
9. SPMEN to SELFPRGEN

Rev. 2514B-09/03
Rev. 2514C-12/03

1. P24“ RC ”

Rev. 2514A-09/03
Rev. 2514B-09/03

1. UART USART P1“ ”
2. P2“ ”
3. P32Table 15 P169Table 80
4. P164“ ” 5
5. P168“ ”

6. P170Figure 81 P170Figure 82
7. P202“ ” SFIOR GTCCR
8. P206“ ”
9. P209“ ”

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Data-com

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests

www.atmel.com/literature

Printed on recycled paper.

2543F–AVR–07/04