MSP430x15x, MSP430x16x，MSP430x161x混合信号微控制器

- 低供电电压范围：1.8V…3.6V
- 超低功耗：
  - －活动模式：1MHz，2.2V 时为 280μA
  - －等待模式：1.6μA
  - －关闭模式（RAM 保持）：0.1μA
- 五种省电模式
- 6μS 内从等待状态唤醒
- 16 位精简指令结构，125 纳秒指令时间周期
- 三个内部 DMA 通道
- 具有内部参考电平、采样保持和自动扫描特性的 12 位 A/D 转换器
- 同步的双 12 位 D/A 转换器
- 带有三个捕捉/比较寄存器的 16 位定时器 A
- 带有三个或七个捕捉/比较影子寄存器的 16 位定时器 B
- 片内集成比较器
- 串行通讯接口（USART1），具有异步 UART 或者同步 SPI 接口的功能
- 串行通讯接口（USART0），具有异步 UART 或者同步 SPI 或者 I^2C 接口
- 具有可编程电平检测的供电电压管理器/监视器
- 欠电压检测器
- 串行在线编程，无需外部编程电压，可编程的安全熔丝代码保护
- Bootstrap Loader
- 器件系列包括：
  - －MSP430F155:
    16KB+256B flash 存储器
    512B RAM
  - －MSP430F156:
    24KB+256B flash 存储器
    1KB RAM
  - －MSP430F157:
    32KB+256B flash 存储器
    1KB RAM
  - －MSP430F167:
    32KB+256B flash 存储器
    1KB RAM
  - －MSP430F168:
    48KB+256B flash 存储器
    2KB RAM
  - －MSP430F169:
    60KB+256B flash 存储器
    2KB RAM
  - －MSP430F1610:
    32KB+256B flash 存储器 5KB RAM

－MSP430F1611

48KB+256B flash 存储器 ； 10KB RAM

- 64 引脚 Quad Flat Pack（QFP）封装
- 要获得完整的模块描述参见 MSP430x1xx 系列用户手册，文献号 SLAU049

说明

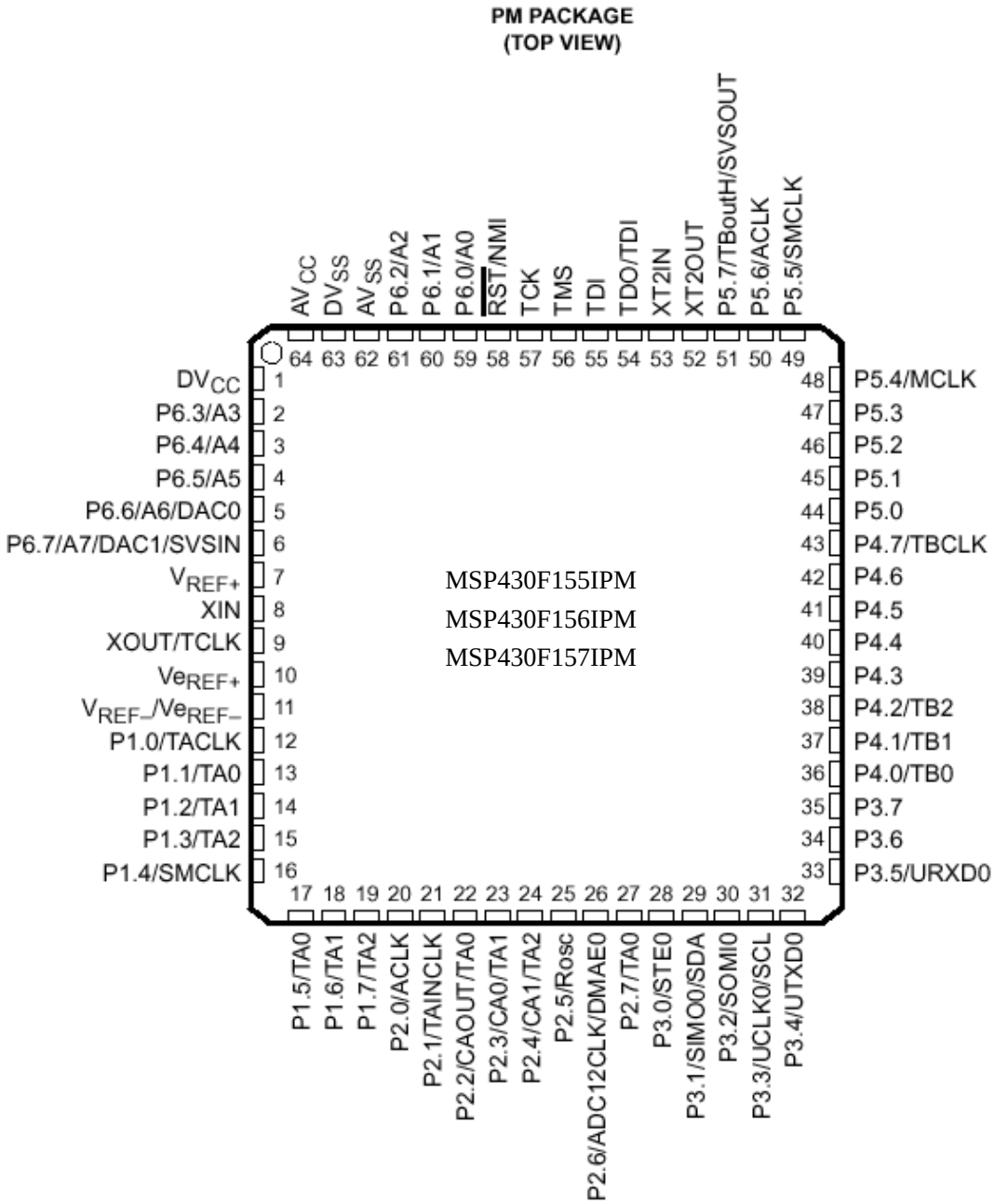
德州仪器公司的 MSP430 系列超低功耗微控制器，由针对各种不同应用目标具有不同外围设备的芯片系列组成。MSP430 的结构与五种低功耗模式相结合，最适用于在便携式测量设备中延长电池寿命。芯片具有一个强大的 16 位 RISC CPU，16 位的寄存器以及常数发生器，能够最大限度地提高代码的效率。数字控制的振荡器（DCO）允许在 6 微秒内从低功耗模式唤醒。MSP430x15x/16x/161x 系列是配置了内置 16 位定时器、12 位快速 A/D 转换器、双 12 位 D/A 转换器，一个或者两个通用同步/异步串行通讯接口（USART）、I^2C、DMA 和 48 个 I/O 引脚的微控制器。另外，MSP430x161x 系列为需要大存储器的应用和堆栈的要求提供扩展 RAM 寻址。

MSP430 的典型应用包括：测量系统、捕获模拟信号转换为数字值、然后处理数据用于显示或者传送到主系统。定时器使得其配置理想地使用在工业控制中，例如数字马达控制、手持式仪表、光网络中地 TEC 控制，等等。

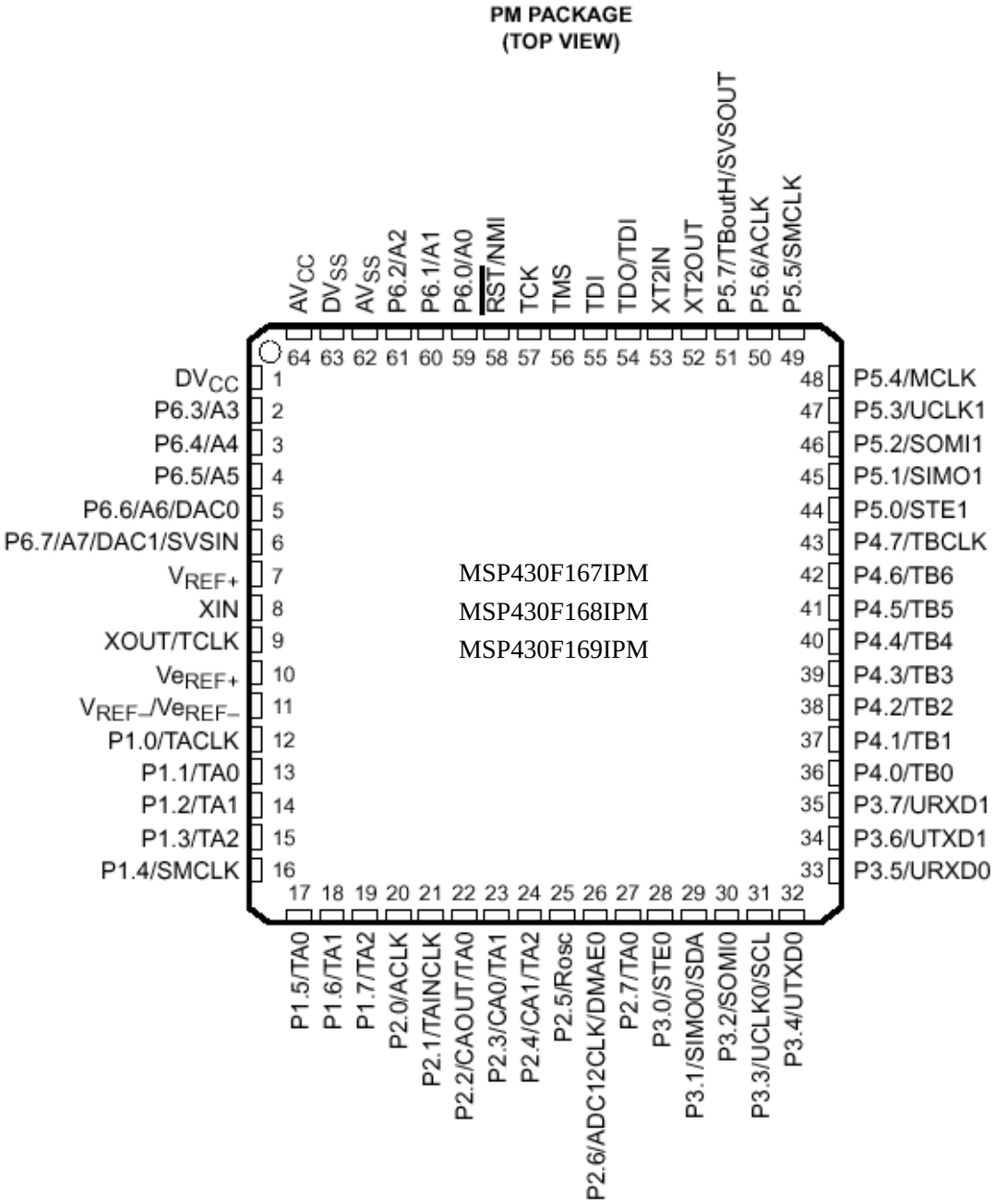
可选型号

TA	PACKAGED DEVICES
	PLASTIC 64-PIN QFP
-40℃ to 85℃	MSP430F155IPM MSP430F156IPM MSP430F157IPM MSP430F167IPM MSP430F168IPM MSP430F169IPM MSP430F1610IPM MSP430F1611IPM

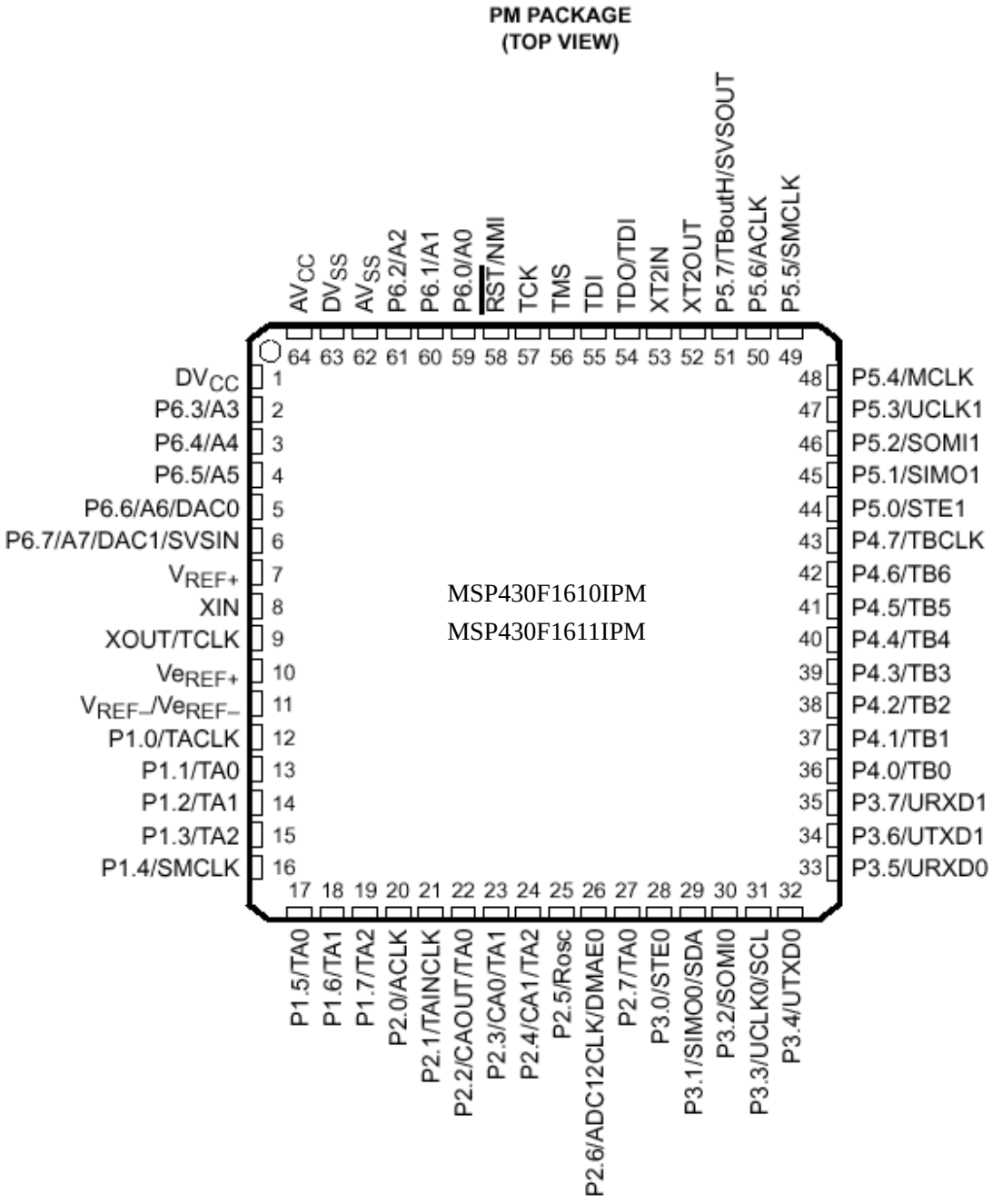
MSP430F155、MSP430F156、 MSP430F157的引脚定义



MSP430F167, MSP430F168, MSP430F169的引脚定义

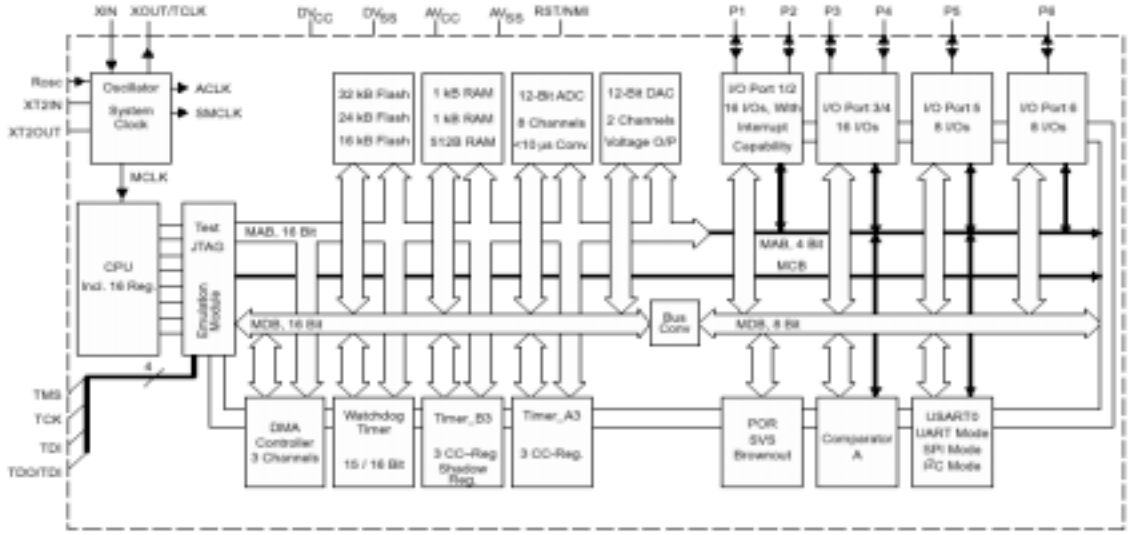


MSP430F1610, MSP430F1611的引脚定义

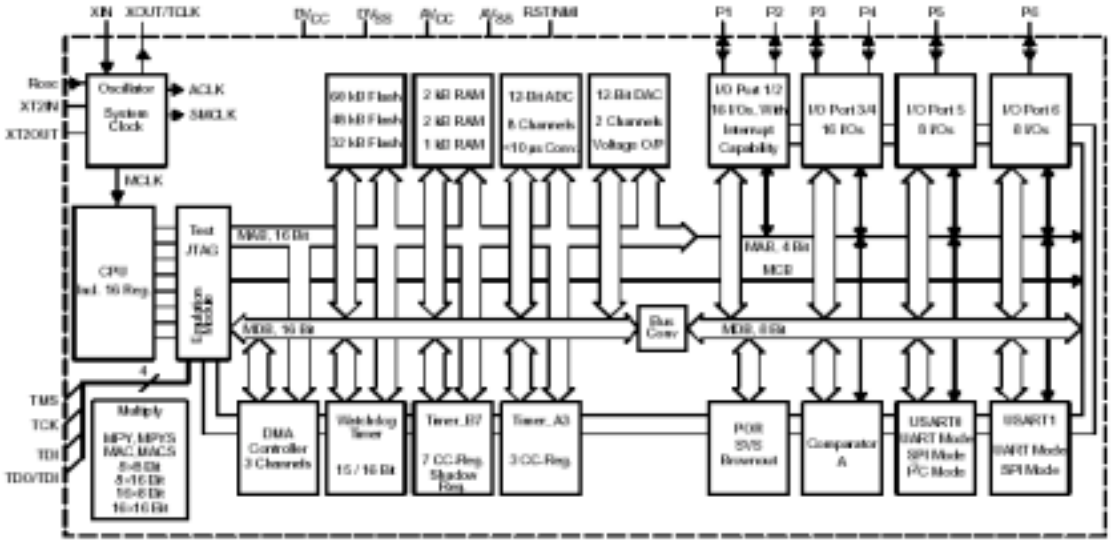


功能模块框图

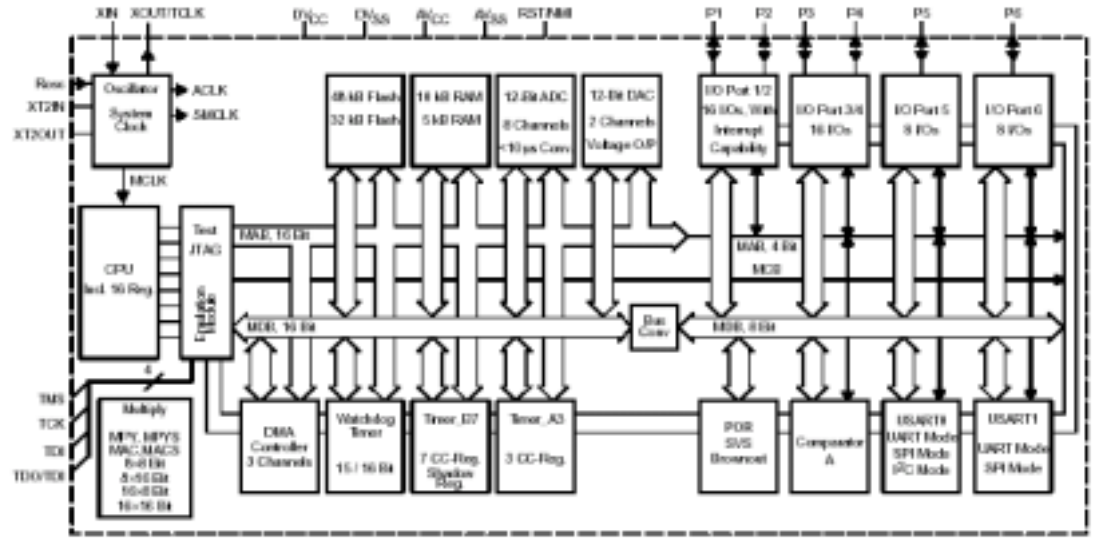
MSP430x15x



MSP430x16x



MSP430x161x



引脚功能

引脚名称	序号	I/O	说 明
Avcc	64		模拟供电电源正端.只为ADC和DAC的模拟部分供电
Avss	62		模拟供电电源负端.只为ADC和DAC的模拟部分供电
DVcc	1		数字供电电源正端.为所有数字部分供电
DVss	63		数字供电电源负端.为所有数字部分供电
P1.0/TACLK	12	I/O	通用数字I/O引脚/定时器A时钟信号TACLK输入
P1.1/TA0	13	I/O	通用数字I/O引脚/定时器A捕捉：CCI0A输入，比较：OUT0输出
P1.2/TA1	14	I/O	通用数字I/O引脚/定时器A捕捉：CCI1A输入，比较：OUT1输出
P1.3/TA2	15	I/O	通用数字I/O引脚/定时器A捕捉：CCI2A输入，比较：OUT2输出
P1.4/SMCLK	16	I/O	通用数字I/O引脚/SMCLK信号输出
P1.5/TA0	17	I/O	通用数字I/O引脚/定时器A，比较：OUT0输出
P1.6/TA1	18	I/O	通用数字I/O引脚/定时器A，比较：OUT1输出
P1.7/TA2	19	I/O	通用数字I/O引脚/定时器A，比较：OUT2输出
P2.0/ACLK	20	I/O	通用数字I/O引脚/ACLK输出
P2.1/TAINCLK	21	I/O	通用数字I/O引脚/定时器A，INCLK上的时钟信号
P2.2/CAOUT/TA0	22	I/O	通用数字I/O引脚/定时器A捕获：CCI0B输入/比较器输出
P2.3/CA0/TA1	23	I/O	通用数字I/O引脚/定时器A，比较：OUT1输出/比较器A输入
P2.4/CA1/TA2	24	I/O	通用数字I/O引脚/定时器A，比较：OUT2输出/比较器A输入
P2.5/Rosc	25	I/O	通用数字I/O引脚，定义DCO标称频率的外部电阻输入
P2.6/ADC12CLK/	26	I/O	通用数字I/O引脚，转换时钟－12位ADC，DMA通道0外部触发器
P2.7/TA0	27	I/O	通用数字I/O引脚/定时器A比较：OUT0输出
P3.0/STE0	28	I/O	通用数字I/O引脚，USART0/SPI模式从设备传输使能端
P3.1/SIMO0/SDA	29	I/O	通用数字I/O引脚，USART0/SPI模式的从入/主出，I^2C数据
P3.2/SOMI0	30	I/O	通用数字I/O引脚，USART0/SPI模式的从出/主入
P3.3/UCLK0/SCL	31	I/O	通用数字I/O引脚，USART0/SPI模式的外部时钟输入，USART0
P3.4/UTXD0	32	I/O	通用数字I/O引脚，USART0/UART模式的传输数据输出
P3.5/URXD0	33	I/O	通用数字I/O引脚，USART0/UART模式的接收数据输入
P3.6/UTXD1	34	I/O	通用数字I/O引脚，USI1/UART模式的发送数据输出
P3.7/URXD1	35	I/O	通用数字I/O引脚，USI1/UART模式的接收数据输入
P4.0/TB0	36	I/O	通用数字I/O引脚，捕获I/P或者PWM输出端口－定时器B7 CCR0
P4.1/TB1	37	I/O	通用数字I/O引脚，捕获I/P或者PWM输出端口－定时器B7 CCR1
P4.2/TB2	38	I/O	通用数字I/O引脚，捕获I/P或者PWM输出端口－定时器B7 CCR2
P4.3/TB3	39	I/O	通用数字I/O引脚，捕获I/P或者PWM输出端口－定时器B7 CCR3
P4.4/TB4	40	I/O	通用数字I/O引脚，捕获I/P或者PWM输出端口－定时器B7 CCR4
P4.5/TB5	41	I/O	通用数字I/O引脚，捕获I/P或者PWM输出端口－定时器B7 CCR5
P4.6/TB6	42	I/O	通用数字I/O引脚，捕获I/P或者PWM输出端口－定时器B7 CCR6
P4.7/TBCLK	43	I/O	通用数字I/O引脚，输入时钟TBCLK－定时器B7
P5.0/STE1	44	I/O	通用数字I/O引脚，USART1/SPI模式从设备传输使能端
P5.1/SIMO1	45	I/O	通用数字I/O引脚，USART1/SPI模式的从入/主出
P5.2/SOMI1	46	I/O	通用数字I/O引脚，USART1/SPI模式的从出/主入
P5.3/UCLK1	47	I/O	通用数字I/O引脚，USART1/SPI模式的外部时钟输入，USART0/SPI模式的时钟输出

P5.4/MCLK	48	I/O	通用数字I/O引脚，主系统时钟MCLK输出
P5.5/SMCLK	49	I/O	通用数字I/O引脚，子系统时钟SMCLK输出
P5.6/ACLK	50	I/O	通用数字I/O引脚，辅助时钟ACLK输出
P5.7/TboutH/	51	I/O	通用数字I/O引脚，将所有PWM数字输出端口为高阻态－定时器B7
P6.0/A0	59	I/O	通用数字I/O引脚，模拟量输入A0－12位ADC
P6.1/A1	60	I/O	通用数字I/O引脚，模拟量输入A1－12位ADC
P6.0/A2	61	I/O	通用数字I/O引脚，模拟量输入A2－12位ADC
P6.0/A3	2	I/O	通用数字I/O引脚，模拟量输入A3－12位ADC
P6.0/A4	3	I/O	通用数字I/O引脚，模拟量输入A4－12位ADC
P6.0/A5	4	I/O	通用数字I/O引脚，模拟量输入A5－12位ADC
P6.0/A6/DAC0	5	I/O	通用数字I/O引脚，模拟量输入A6－12位ADC，DAC.0输出
P6.0/A7/DAC1/	6	I/O	通用数字I/O引脚，模拟量输入A7－12位ADC，DAC.1输出，SVS输入
RST/NMI	58	I	复位输入，不可屏蔽中断输入端口或者Bootstrap Lload启动（FLASH
TCK	57	I	测试时钟，TCK是芯片编程测试和bootstrap loader启动的时钟输入端口
TDI	55	I	测试数据输入，TDI用作数据输入端口，芯片保护熔丝连接到TDI
TDO/TDI	54	I/O	测试数据输出端口，TDO/TDI数据输出或者编程数据输出引脚
TMS	56	I	测试模式选择，TMS用作芯片编程和测试的输入端口
VeREF+	10	I/P	外部参考电压的输入
VREF+	7	O	参考电压的正输出引脚
VREF-/VeREF-	11	O	内部参考电压或者外加参考电压的引脚
XIN	8	I	晶体振荡器XT1的输入端口，可连接标准晶振或者钟表晶振
XOUT/TCLK	9	I/O	晶体振荡器XT1的输出引脚或测试时钟输入
XT2IN	53	I	晶体振荡器XT2的输入端口，只能连接标准晶振
XT2OUT	52	O	晶体振荡器XT2的输出引脚

简要说明

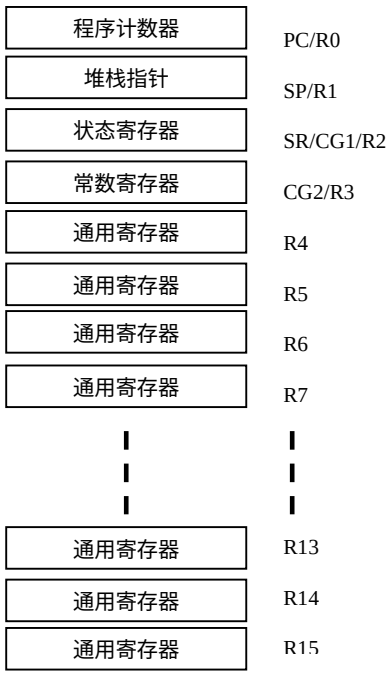
CPU

MSP430 CPU具有一个16位的精简指令计算机结构，对应用是高度透明的。所有的操作，除了程序流程指令，都是通过源操作数的7种寻址模式和目标操作数的四种寻址模式的组合对寄存器操作进行的。

CPU集成了16个寄存器，减小了指令执行时间。寄存器到寄存器操作的执行时间是一个CPU周期。

寄存器中的四个，R0到R3，相对地专用作程序计数器、堆栈指针、状态寄存器和常数发生器。其余寄存器是通用寄存器。

外围通过数据、地址和控制总线连接到CPU，可以通过所有指令处理。



指令集

指令集由三种格式和7种寻址模式的51条指令构成。每条指令可以操作一个字或者字节。表1的例子显示了三类指令格式，表2中列出了寻址模式。

表1 指令字格式

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 —–> R5
Single operands, destination only	e.g. CALL R8	PC —>(TOS), R8—> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

表2 寻址模式说明

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 —> R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)—> M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) —> M(TONI)
Absolute	✓	✓	MOV and MEM,and TCDAT		M(MEM) —> M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) —> M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) —> R11 R10 + 2—> R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 —> M(TONI)

NOTE: S = source D = destination

运行模式

MSP430具有一种活动模式和五种软件可选的低功耗运行模式。一个中断事件可以将芯片从五种低功耗模式中的任何一种唤醒，为请求服务并在从中断程序返回时恢复低功耗模式。

下列六种运行模式由软件配置：

- 活动模式AM：
  －所有时钟活动
- 低功耗模式0（LPM0）
  －CPU关闭
  ACLK和SMCLK保持活动，MCLK关闭
  如果DCO在活动模式中没有使用，DCO的直流发生器将关闭
- 低功耗模式1（LPM1）
  —CPU关闭
  ACLK和SMCLK保持活动，MCLK关闭
- 低功耗模式2（LPM2）
  －CPU关闭
  MCLK和SMCLK关闭
  DCO的直流发生器保持活动
  ACLK保持活动
- 低功耗模式3（LPM3）
  －CPU关闭
  MCLK和SMCLK关闭
  DCO的直流发生器关闭
  ACLK保持活动
- 低功耗模式4（LPM4）
  －CPU关闭
  ACLK关闭
  MCLK和SMCLK关闭
  DCO的直流发生器关闭
  晶体振荡器停止

中断向量地址

中断向量和上电起始地址位于地址范围0FFFFh－0FFE0h。这些向量包括相应中断处理指令序列的16位地址。

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External Reset Watchdog Flash memory	WDTIFG KEYV (see Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator Fault Flash memory access violation	NMIIFG (see Notes 1 & 3) OFIFG (see Notes 1 & 3) ACCVIFG (see Notes 1 & 3)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	14
Timer_B7 (see Note 5)	TBCCR0 CCIFG (see Note 2)	Maskable	0FFFAh	13
Timer_B7 (see Note 5)	TBCCR1 to TBCCR6 CCIFGs, TBIFG (see Notes 1 & 2)	Maskable	0FFF8h	12
Comparator_A	CAIFG	Maskable	0FFF6h	11
Watchdog timer	WDTIFG	Maskable	0FFF4h	10
USART0 receive I2C transmit/receive/others	URXIFG0, I2CIFG (see Note 4)	Maskable	0FFF2h	9
USART0 transmit	UTXIFG0	Maskable	0FFF0h	8
ADC12	ADC12IFG (see Notes 1 & 2)	Maskable	0FFEEh	7
Timer_A3	TACCR0 CCIFG (see Note 2)	Maskable	0FFECh	6
Timer_A3	TACCR1 and TACCR2 CCIFGs, TAIFG (see Notes 1 & 2)	Maskable	0FFEAh	5
I/O port P1 (eight flags)	P1IFG.0 (see Notes 1 & 2) To P1IFG.7 (see Notes 1 & 2)	Maskable	0FFE8h	4
USART1 receive	URXIFG1	Maskable	0FFE6h	3
USART1 transmit	UTXIFG1	Maskable	0FFE4h	2
I/O port P2 (eight flags)	P2IFG.0 (see Notes 1 & 2) To P2IFG.7 (see Notes 1 & 2)	Maskable	0FFE2h	1
DAC12 DMA	DAC12_0IFG, DAC12_1IFG DMA0IFG, DMA1IFG, DMA2IFG (see Notes 1 & 2)	Maskable	0FFE0h	0, lowest

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module.
3. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
4. I2C interrupt flags located in the module
5. Timer_B7 in MSP430x16x/161x family has 7 CCRs; Timer_B3 in MSP430x15x family has 3 CCRs; in Timer_B3 there are only interrupt flags TBCCR0, 1 and 2 CCIFGs and the interrupt-enable bits TBCCR0, 1 and 2 CCIEs.

专用功能寄存器

大部分中断和模块使能位集中在低地址空间。芯片物理上不存在没有分配功能目的的专用功能寄存器位。这种布局简化了软件处理。

中断使能寄存器1和2

Address	7	6	5	4	3	2	1	0
0h	UTXIE0	URXIE0	ACCVIE	NMIIE			OFIE	WDTIE
	rw-0	rw-0	rw-0	rw-0			rw-0	rw-0

WDTIE： 看门狗定时器中断使能。如果选择看门狗模式停止；如果看门狗定时器配置为通用定时器活动。

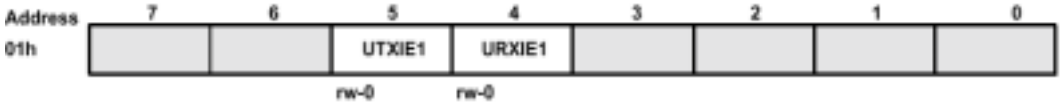
OFIE： 振荡器失效中断使能

NMIIE： 不可屏蔽中断使能

ACCVIE： Flash存储器处理出错中断使能

URXIE0： USART0，UART和SPI接收中断使能

UTXIE0： USART0，UART和SPI发送中断使能



URXIE1： USART1，UART和SPI接收中断使能

UTXIE1： USART1，UART和发送中断使能

URXIE1和UTXIE1在MSP430x15x芯片中不存在。

中断标志寄存器1和2

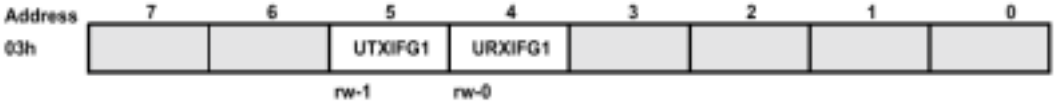
WDTIFG： 当看门狗定时器溢出（在看门狗模式）或者安全键值出错，当Vcc上电复位或者$\overline{\text{RST}}$/NMI引脚在复位模式满足复位条件时复位

OFIFG： 振荡器失效时标志置位

NMIIFG： 通过$\overline{\text{RST}}$/NMI引脚置位

URXIFG0： USART0，UART和SPI接收标志

UTXIFG0： USART0，UART和SPI发送标志



URXIFG1： USART1，UART和SPI接收标志

UTXIFG1： USART1，UART和SPI发送标志

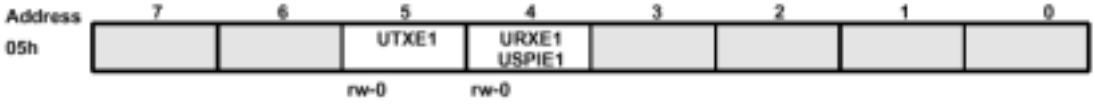
URXIFG1和UTXIFG1在MSP430x15x芯片中不存在。

模块使能寄存器1和2

URXE0： USART0，UART模式接收使能

UTXE0： USART0，UART模式发送使能

USPIE0： USART0，SPI模式发送和接收使能



URXE1： USART1，UART模式接收使能

UTXE1： USART1，UART模式发送使能

USPIE1： USART1，SPI模式发送和接收使能

图例：rw：位可读写

rw－0：位可读写，由PUC复位

： SFR位在芯片中不存在

存储器布局（MSP430F15x）

		MSP430F155	MSP430F156	MSP430F157
Memory Main: interrupt vector Main: code memory	Size Flash Flash	16kB 0FFFFh – 0FFE0h 0FFFFh – 0C000h	24kB 0FFFFh – 0FFE0h 0FFFFh – 0A000h	32kB 0FFFFh – 0FFE0h 0FFFFh – 08000h
Information memory	Size Flash	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h
Boot memory	Size ROM	1kB 0FFFh – 0C00h	1kB 0FFFh – 0C00h	1kB 0FFFh – 0C00h
RAM	Size	512B 03FFh – 0200h	1kB 05FFh – 0200h	1kB 05FFh – 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

存储器布局（MSP430F16x）

		MSP430F167	MSP430F168	MSP430F169
Memory Main: interrupt vector Main: code memory	Size Flash Flash	32kB 0FFFFh – 0FFE0h 0FFFFh – 08000h	48kB 0FFFFh – 0FFE0h 0FFFFh – 04000h	60kB 0FFFFh – 0FFE0h 0FFFFh – 01100h
Information memory	Size Flash	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h
Boot memory	Size ROM	1kB 0FFFh – 0C00h	1kB 0FFFh – 0C00h	1kB 0FFFh – 0C00h
RAM	Size	1kB 05FFh – 0200h	2kB 09FFh – 0200h	2kB 09FFh – 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

存储器布局（MSP430F161x）

		MSP430F1610	MSP430F1611
Memory Main: interrupt vector Main: code memory	Size Flash Flash	32kB 0FFFFh – 0FFE0h 0FFFFh – 08000h	48kB 0FFFFh – 0FFE0h 0FFFFh – 04000h
RAM	Size	5kB 024FFh – 01100h	8kB 038FFh – 01100h
Information memory	Size Flash	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h
Boot memory	Size ROM	1kB 0FFFh – 0C00h	1kB 0FFFh – 0C00h
RAM	Size	2kB 09FFh – 0200h	2kB 09FFh – 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

bootstrap loader（BSL）

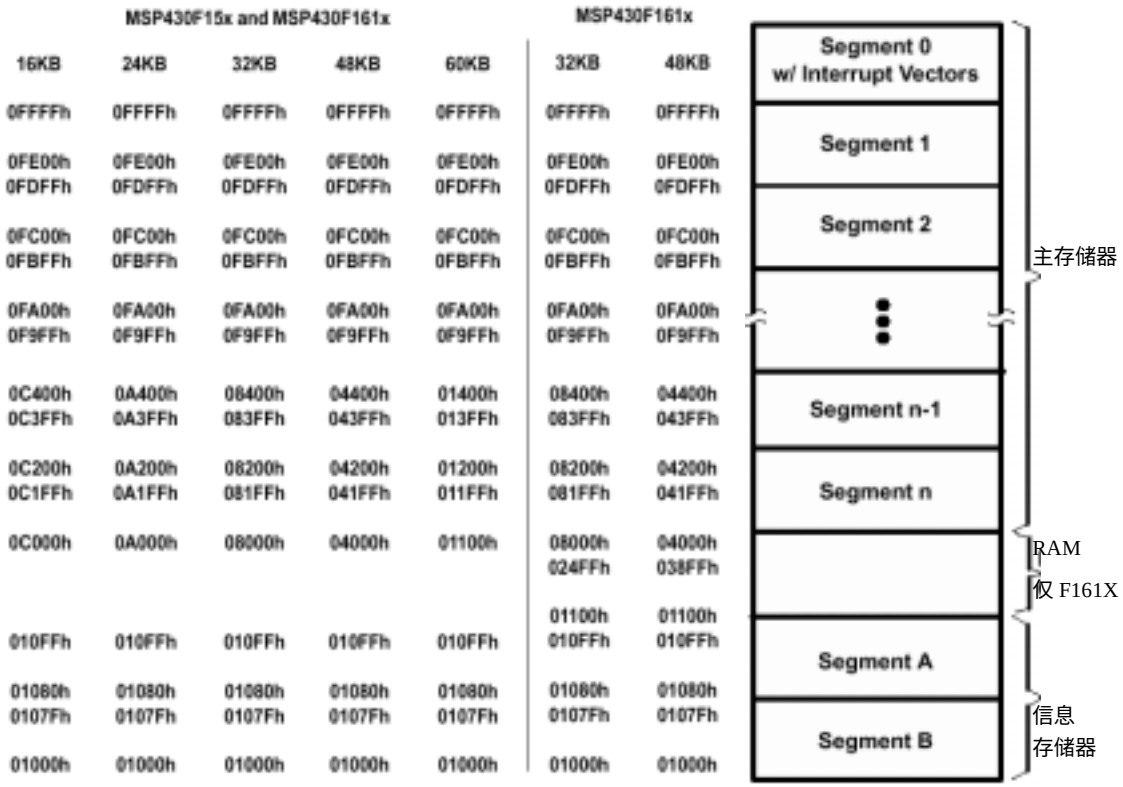
MSP430的bootstrap loader（BSL）使用户可以使用一个UART串行接口对Flash存储器或者RAM进行编程。通过BSL对MSP430存储器进行操作由用户定义的口令保护。完整的BSL特性说明和执行，可以参见应用报告MSP430的Bootstrap Loader的特性，文献号SLAA089。

Flash存储器

Flash存储器可以通过JTAG端口、bootstrap loader或者由CPU在系统编程。CPU可以执行单字节和单字写入Flash存储器。Flash存储器的特性包括：

- Flash存储器有n个主存储段和两个各为128各字节的信息存储段（A和B）。每个主存储段为512各字节。
- 段0到n可以一起擦除或者每个段单独擦除。
- 段A和B可以单独擦除或者与段0－n作为一个组擦除。
  段A和B也被称为信息存储器。

● 新芯片的信息存储器中的某些字节可能已经编程（制造过程中用于测试）。用户在初次使用前应进行一次信息存储器的擦除。



外围模块

外围模块通过数据、地址和控制总线连接到CPU，可以使用所有指令处理。

DMA控制器

DMA控制器允许数据从一个存储器地址移动到另外一个存储器地址无需CPU干预。例如，DMA控制器可以用于将数据从ADC12转换器存储器移动到RAM。使用DMA控制器可以外围模块的吞吐量。DMA控制器允许CPU保持在睡眠模式，无需唤醒来从外围移动数据，从而减小系统功耗。

振荡器和系统时钟

MSP430x15x和MSP430x16x（x）系列芯片的时钟系统支持基本时钟模块，包括支持32768Hz钟表晶振、一个内部数字控制的振荡器（DCO）和一个高频晶体振荡器。基本时钟模块的设计是为了同时满足低系统成本和低功耗的要求。内部DCO可以在6微秒内快速打开时钟源并稳定。基本时钟模块提供下列时钟信号：

● 辅助时钟（ACLK），来自32768Hz钟表晶振或者高频晶振
● 主时钟（MCLK），CPU使用的主时钟
● 次主时钟（SMCLK），由外围模块使用的子系统时钟

上电电路，供电电压管理器

上电电路是在上电和掉电时用于为芯片提供正确的内部复位信号。供电电压管理（SVS）电路检测供电电压是否下降到用户选择的电压以下，同时支持供电电压管理（芯片自动复位）和监测（SVM，芯片不自动复位）。

CPU在上电电路释放芯片复位后开始代码执行。不过Vcc不能下降到Vcc（min）。用户

必须确保缺省的FLL＋设定不会改变直至Vcc到达Vcc（min）。如果愿意，SVS电路可以用于监测Vcc何时到达Vcc（min）。

数字I/O

MSP430中有6个I/O端口—端口P1到P6:

- 所有I/O位可以独立编程
- 任何输入、输出和中断条件的组合都是可能的
- P1、P2端口的所有8位可以选择边缘中断输入
- 所有指令支持对端口控制寄存器的读/写

看门狗定时器

看门狗定时器模块（WDT）的主要功能是在发生软件问题后进行控制系统的重启。如果选定的时间间隔溢出，系统产生复位。如果看门狗功能在应用中不需要，这个模块可以配置位间隔定时器在选定的时间间隔产生中断。

乘法器（仅对MSP430x16x/161x）

乘法器操作由专用外围模块支持。这个模块进行16×16、16×8、8×16、8×8位的操作。这个模块能够同时支持带符号和不带符号的乘法和累加操作。操作结果可以在操作数装入外围寄存器后立即处理，无需额外的时钟周期。

USART0

MSP430x15x和MSP430x16x(x)有一个硬件通用同步/异步接收发送（USART0）外围模块用于串行数据通信。USART支持同步SPI（3或者4引脚）、异步UART和使用双缓冲发送和传输通道的I2C通讯协议。

USART1(仅对MSP43016x/161x)

MSP430x16x(x)芯片配有第二个硬件通用同步/异步接收发送（USART1）外围模块用于串行数据通信。USART支持同步SPI(3或4引脚)和异步UART通讯协议，使用双缓冲发送和接收通道。除了支持I2C，USART1的操作与USART0是一样的。

定时器A3

定时器A3是一个带有3个捕获/比较寄存器的定时器/计数器。定时器A3可以支持多个捕获/比较、PWM输出和内部时序。定时器A3也具有扩展中断能力。中断可以由计数器溢出条件或者每个捕获/比较寄存器产生。

定时器B7(仅对MSP43016x/161x)

定时器B7是一个带有7个捕获/比较寄存器的定时器/计数器。定时器B7可以支持多个捕获/比较、PWM输出和内部时序。定时器A3也具有扩展中断能力。中断可以由计数器溢出条件或者每个捕获/比较寄存器产生。

定时器B3(仅对MSP43015x)

定时器B3是一个带有3个捕获/比较寄存器的定时器/计数器。定时器B3可以支持多个捕获/比较、PWM输出和内部时序。定时器A3也具有扩展中断能力。中断可以由计数器溢出条件或者每个捕获/比较寄存器产生。

比较器A

比较器A模块的主要功能是支持精密的斜坡模拟/数字转换、电池电压管理和外部模拟信号的检测。

ADC12

ADC12模块支持快速12位模拟/数字转换。模块包括一个12位SAR内核、采样选择控制、参考电压发生器和一个16字的转换控制缓冲区。转换控制缓冲区允许多达16个独立ADC采样的转换和存储而无需CPU的干预。

DAC12

DAC12模块是一个12位的，R梯度的电压输出DAC。DAC12可用作8位或者12位模式，也可以与DMA控制器组合使用。当存在多路DAC12模块时，他们可以编成一组同时操作。

外围模块布局

PERIPHERAL FILE MAP			
DMA	DMA channel 2 transfer size	DMA2SZ	01F6h
	DMA channel 2 destination address	DMA2DA	01F4h
	DMA channel 2 source address	DMA2SA	01F2h
	DMA channel 2 control	DMA2CTL	01F0h
	DMA channel 1 transfer size	DMA1SZ	01EEh
	DMA channel 1 destination address	DMA1DA	01ECh
	DMA channel 1 source address	DMA1SA	01EAh
	DMA channel 1 control	DMA1CTL	01E8h
	DMA channel 0 transfer size	DMA0SZ	01E6h
	DMA channel 0 destination address	DMA0DA	01E4h
	DMA channel 0 source address	DMA0SA	01E2h
	DMA channel 0 control	DMA0CTL	01E0h
	DMA module control 1	DMACTL1	0124h
	DMA module control 0	DMACTL0	0122h
DAC12	DAC12_1 data	DAC12_1DAT	01CAh
	DAC12_1 control	DAC12_1CTL	01C2h
	DAC12_0 data	DAC12_0DAT	01C8h
	DAC12_0 control	DAC12_0CTL	01C0h
ADC12	Interrupt-vector-word register	ADC12IV	01A8h
	Inerrupt-enable register	ADC12IE	01A6h
	Inerrupt-flag register	ADC12IFG	01A4h
	Control register 1	ADC12CTL1	01A2h
	Control register 0	ADC12CTL0	01A0h
	Conversion memory 15	ADC12MEM15	015Eh
	Conversion memory 14	ADC12MEM14	015Ch
	Conversion memory 13	ADC12MEM13	015Ah
	Conversion memory 12	ADC12MEM12	0158h
	Conversion memory 11	ADC12MEM11	0156h
	Conversion memory 10	ADC12MEM10	0154h
	Conversion memory 9	ADC12MEM9	0152h
	Conversion memory 8	ADC12MEM8	0150h
	Conversion memory 7	ADC12MEM7	014Eh
	Conversion memory 6	ADC12MEM6	014Ch
	Conversion memory 5	ADC12MEM5	014Ah
	Conversion memory 4	ADC12MEM4	0148h
	Conversion memory 3	ADC12MEM3	0146h
	Conversion memory 2	ADC12MEM2	0144h
	Conversion memory 1	ADC12MEM1	0142h
	Conversion memory 0	ADC12MEM0	0140h

PERIPHERAL FILE MAP (CONTINUED)			
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control2	CACTL2	05Ah
	Comparator_A control1	CACTL1	059h
Basic Clock	Basic clock system control2	BCSCTL2	058h
	Basic clock system control1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
BrownOUT, SVS	SVS control register (reset by brownout signal)	SVSCTL	055h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag2	IFG2	003h
	SFR interrupt flag1	IFG1	002h
	SFR interrupt enable2	IE2	001h
	SFR interrupt enable1	IE1	000h

PERIPHERAL FILE MAP (CONTINUED)			
ADC12 (continued)	ADC memory-control register15	ADC12MCTL15	08Fh
	ADC memory-control register14	ADC12MCTL14	08Eh
	ADC memory-control register13	ADC12MCTL13	08Dh
	ADC memory-control register12	ADC12MCTL12	08Ch
	ADC memory-control register11	ADC12MCTL11	08Bh
	ADC memory-control register10	ADC12MCTL10	08Ah
	ADC memory-control register9	ADC12MCTL9	089h
	ADC memory-control register8	ADC12MCTL8	088h
	ADC memory-control register7	ADC12MCTL7	087h
	ADC memory-control register6	ADC12MCTL6	086h
	ADC memory-control register5	ADC12MCTL5	085h
	ADC memory-control register4	ADC12MCTL4	084h
	ADC memory-control register3	ADC12MCTL3	083h
	ADC memory-control register2	ADC12MCTL2	082h
	ADC memory-control register1	ADC12MCTL1	081h
	ADC memory-control register0	ADC12MCTL0	080h
Timer_B7/ Timer_B3 (see Note 6)	Capture/compare register 6	TBCCR6	019Eh
	Capture/compare register 5	TBCCR5	019Ch
	Capture/compare register 4	TBCCR4	019Ah
	Capture/compare register 3	TBCCR3	0198h
	Capture/compare register 2	TBCCR2	0196h
	Capture/compare register 1	TBCCR1	0194h
	Capture/compare register 0	TBCCR0	0192h
	Timer_B register	TBR	0190h
	Capture/compare control 6	TBCCTL6	018Eh
	Capture/compare control 5	TBCCTL5	018Ch
	Capture/compare control 4	TBCCTL4	018Ah
	Capture/compare control 3	TBCCTL3	0188h
	Capture/compare control 2	TBCCTL2	0186h
	Capture/compare control 1	TBCCTL1	0184h
	Capture/compare control 0	TBCCTL0	0182h
	Timer_B control	TBCTL	0180h
	Timer_B interrupt vector	TBIV	011Eh
Timer_A3	Reserved		017Eh
	Reserved		017Ch
	Reserved		017Ah
	Reserved		0178h
	Capture/compare register 2	TACCR2	0176h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 0	TACCR0	0172h
	Timer_A register	TAR	0170h
	Reserved		016Eh
	Reserved		016Ch
	Reserved		016Ah
	Reserved		0168h

NOTE 6: Timer_B7 in MSP430x16x/161x family has 7 CCR, Timer_B3 in MSP430x15x family has 3 CCR.

PERIPHERAL FILE MAP (CONTINUED)			
Timer_A3 (continued)	Capture/compare control 2	TACCTL2	0166h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 0	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Multiplier (MSP430x16x and MSP430x161x only)	Sum extend	SUMEXT	013Eh
	Result high word	RESHI	013Ch
	Result low word	RESLO	013Ah
	Second operand	OP2	0138h
	Multiply signed +accumulate/operand1	MACS	0136h
	Multiply+accumulate/operand1	MAC	0134h
	Multiply signed/operand1	MPYS	0132h
	Multiply unsigned/operand1	MPY	0130h
Flash	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog	Watchdog Timer control	WDTCTL	0120h
USART1 (MSP430x16x and MSP430x161x only)	Transmit buffer	U1TXBUF	07Fh
	Receive buffer	U1RXBUF	07Eh
	Baud rate	U1BR1	07Dh
	Baud rate	U1BR0	07Ch
	Modulation control	U1MCTL	07Bh
	Receive control	U1RCTL	07Ah
	Transmit control	U1TCTL	079h
	USART control	U1CTL	078h
USART0 (UART or SPI mode)	Transmit buffer	U0TXBUF	077h
	Receive buffer	U0RXBUF	076h
	Baud rate	U0BR1	075h
	Baud rate	U0BR0	074h
	Modulation control	U0MCTL	073h
	Receive control	U0RCTL	072h
	Transmit control	U0TCTL	071h
	USART control	U0CTL	070h
USART0 (I^2C mode)	I2C interrupt vector	I2CIV	011Ch
	I2C slave address	I2CSA	011Ah
	I2C own address	I2COA	0118h
	I2C data	I2CDR	076h
	I2C SCLL	I2CSCLL	075h
	I2C SCLH	I2CSCLH	074h
	I2C PSC	I2CPSC	073h
	I2C data control	I2CDCTL	072h
	I2C transfer control	I2CTCTL	071h
	USART control	U0CTL	070h
	I2C data count	I2CNDAT	052h
	I2C interrupt flag	I2CIFG	051h
	I2C interrupt enable	I2CIE	050h

最大绝对额定值

作用于 Vcc 到 Vss 的电压……-0.3V 到 4.1V

作用于任何引脚的电压（相对于 Vss）……-0.3V 到 Vcc＋0.3V

芯片终端的二极管电流……±2mA

储存温度，Tstg（未编程芯片）……..…-55℃到 150℃

储存温度，Tstg（已编程芯片）……..…..…-40℃到 85℃

超过最大绝对额定值中列出的条件可能引起芯片永久性的损坏。这些只是额定的极限，并不代表芯片在超出“ 推荐运行条件 ”之外的条件下芯片能够正常运行。在一段时期内暴露在最大绝对额定值将影响芯片的可靠性。（**注意：所有电压以地为参考。）**

推荐运行条件

			MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC} (AV_{CC} = DV_{CC} = V_{CC})		MSP430F15x/F16x /161x	1.8		3.6	V
Supply voltage during flash memory programming, V_{CC} (AV_{CC} = DV_{CC} = V_{CC})		MSP430F15x/16x/ 161x	2.7		3.6	V
Supply voltage during program execution, SVS enabled (see Note 1), V_{CC} (AV_{CC} = DV_{CC} = V_{CC})		MSP430F15x/16x/ 161x	2		3.6	V
Supply voltage, V_{SS} (AV_{SS} = DV_{SS} = V_{SS})			0		0	V
Operating free-air temperature range, T_A		MSP430F161x	–40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Notes 2 and 3)	LF selected, XTS=0	Watch crystal		32.768		kHz
	XT1 selected, XTS=1	Ceramic resonator	450		8000	kHz
	XT1 selected, XTS=1	Crystal	1000		8000	kHz
XT2 crystal frequency, $f_{(XT2)}$		Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	
Processor frequency (signal MCLK), $f_{(System)}$		V_{CC} = 1.8 V	DC		4.15	MHz
		V_{CC} = 3.6 V	DC		8	
Flash-timing-generator frequency, $f_{(FTG)}$		MSP430F15x/16x/ 161x	257		476	kHz
Cumulative program time, $t_{(CPT)}$ (see Note 4)		V_{CC} = 2.7 V/3.6 V MSP430F15x/16x/ 161x			3	ms
Mass erase time, t(MEras) (See the *flash memory, timing generator, control register FCTL2* section and Note 5)		V_{CC} = 2.7 V/3.6 V	200			ms
Low-level input voltage (TCK, TMS, TDI, RST/NMI), V_{IL} (excluding Xin, Xout)		V_{CC} = 2.2 V/3 V	V_{SS}		V_{SS} + 0.6	V
High-level input voltage (TCK, TMS, TDI, RST/NMI), V_{IH} (excluding Xin, Xout)		V_{CC} = 2.2 V/3 V	0.8 × V_{CC}		V_{CC}	V
Input levels at Xin and Xout	$V_{IL(Xin, Xout)}$	V_{CC} = 2.2 V/3 V	V_{SS}		0.2 × V_{CC}	V
	$V_{IH(Xin, Xout)}$		0.8 × V_{CC}		V_{CC}	

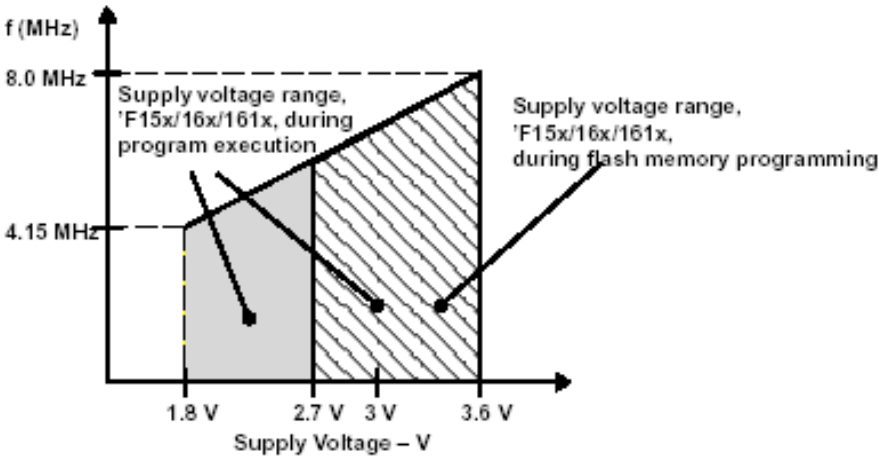


图 1 频率和供电电压　MSP430F15x/16x/161x

在推荐的供电电压和运行温度范围内时的电气特性（除非另有说明）
除外部电流外的供电电流（到 Vcc）（f（system）＝1MHz）

PARAMETER			TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)} = 1$ MHz, $f_{(ACLK)} = 32.768$ Hz XTS=0, SELM=(0,1)	F15x, F16x, F161x	T_A = –40°C to 85°C	V_{CC} = 2.2 V		280	350	µA
				V_{CC} = 3 V		420	560	
	Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)} = 4{,}096$ Hz, $f_{(ACLK)} = 4{,}096$ Hz XTS=0, SELM=3	F15x, F16x, F161x	T_A = –40°C to 85°C	V_{CC} = 2.2 V		2.5	7	µA
				V_{CC} = 3 V		9	20	
$I_{(LPM0)}$	Low-power mode, (LPM0) (see Note 1)	F161x	T_A = –40°C to 85°C	V_{CC} = 2.2 V		32	45	µA
				V_{CC} = 3 V		55	70	
$I_{(LPM2)}$	Low-power mode, (LPM2), f(MCLK) = f (SMCLK) = 0 MHz, f(ACLK) = 32.768 Hz, SCG0 = 0		T_A = –40°C to 85°C	V_{CC} = 2.2 V		11	14	µA
				V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode, (LPM3) $f_{(MCLK)} = f_{(SMCLK)} = 0$ MHz, $f_{(ACLK)} = 32{,}768$ Hz, SCG0 = 1 (see Note 2)		T_A = –40°C	V_{CC} = 2.2 V		0.8	1.5	µA
			T_A = 25°C			0.9	1.5	
			T_A = 85°C			1.6	2.8	
			T_A = –40°C	V_{CC} = 3 V		1.8	2.2	µA
			T_A = 25°C			1.6	1.9	
			T_A = 85°C			2.3	3.9	
$I_{(LPM4)}$	Low-power mode, (LPM4) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1		T_A = –40°C	V_{CC} = 2.2 V		0.1	0.5	µA
			T_A = 25°C			0.1	0.5	
			T_A = 85°C			0.8	2.5	
			T_A = –40°C	V_{CC} = 3 V		0.1	0.5	µA
			T_A = 25°C			0.1	0.5	
			T_A = 85°C			0.8	2.5	

活动模式电流消耗相对于系统频率, F 版本

IAM = IAM[1 MHz] · fsystem [MHz]

活动模式电流消耗相对于供电电压，F 版本

IAM = I（AM）[3 V] + 175 µA/V · (VCC–3 V)

施密特触发器输入端口P1到P2；P1.0到P1.7,P2.0到P2.5

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.5	V
		V_{CC} = 3 V	1.5		1.9	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	0.90		1.3	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	V_{CC} = 2.2 V	0.3		1.1	V
		V_{CC} = 3 V	0.5		1	

标准输入－RST/NMI;JTAG;TCK,TMS,TDI,TDO/TDI

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage	V_{CC} = 2.2 V / 3 V	V_{SS}		V_{SS}+0.6	V
V_{IH}	High-level input voltage		0.8×V_{CC}		V_{CC}	V

输出－端口 P1，P2，P3，P4，P5，P6

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –1 mA,	V_{CC} = 2.2 V,	See Note 1	V_{CC}–0.25		V_{CC}	V
		$I_{OH(max)}$ = –3.4 mA,	V_{CC} = 2.2 V,	See Note 2	V_{CC}–0.6		V_{CC}	
		$I_{OH(max)}$ = –1 mA,	V_{CC} = 3 V,	See Note 1	V_{CC}–0.25		V_{CC}	
		$I_{OH(max)}$ = –3.4 mA,	V_{CC} = 3 V,	See Note 2	V_{CC}–0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{SS}		V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{SS}		V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{SS}		V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V,	See Note 2	V_{SS}		V_{SS}+0.6	

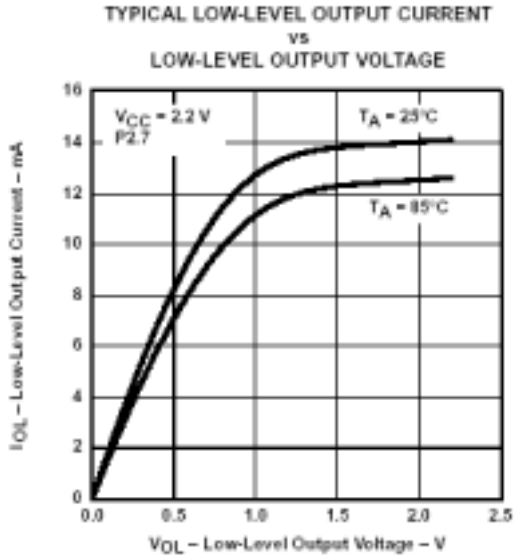


图 2

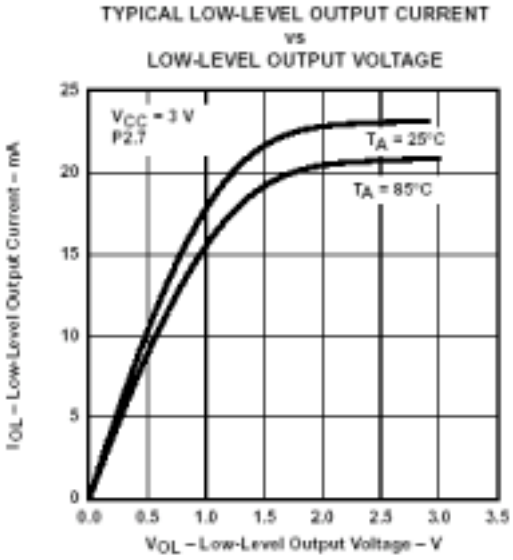


图 3

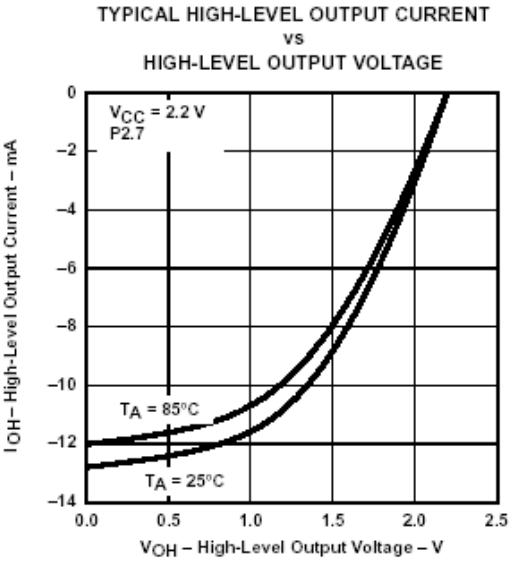


图 4

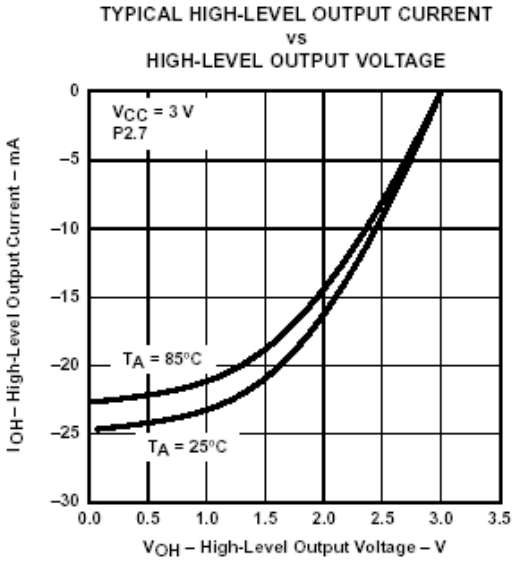


图 5

输出频率

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(Px.y)}$	(1 ≤ x ≤ 6, 0 ≤ y ≤ 7)	C_L = 20 pF, I_L = ±1.5 mA	V_{CC} = 2.2 V	DC		5	MHz
			V_{CC} = 3 V	DC		7.5	
$f_{(ACLK)}$ $f_{(MCLK)}$ $f_{(SMCLK)}$	P2.0/ACLK, P5.6/ACLK P5.4/MCLK, P1.4/SMCLK, P5.5/SMCLK	C_L = 20 pF	V_{CC} = 2.2 V V_{CC} = 3 V	DC DC		5 7.5	MHz
$t_{(Xdc)}$	Duty cycle of output frequency	P1.0/TACLK C_L = 20 pF V_{CC} = 2.2 V / 3 V	$f_{(ACLK)} = f_{(LFXT1)} = f_{(XT1)}$	40%		60%	
			$f_{(ACLK)} = f_{(LFXT1)} = f_{(LF)}$	30%		70%	
			$f_{(ACLK)} = f_{(LFXT1)}$		50%		
		P1.1/TA0/MCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{(MCLK)} = f_{(XT1)}$	40%		60%	
			$f_{(MCLK)} = f_{(DCOCLK)}$	50%–15 ns	50%	50%+15 ns	
		P1.4/TBCLK/SMCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{(SMCLK)} = f_{(XT2)}$	40%		60%	
			$f_{(SMCLK)} = f_{(DCOCLK)}$	50%–15 ns	50%	50%+15 ns	

输入 Px.x、Tax、TBx

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag, (see Note 1)	2.2 V/3 V	1.5			cycle
			2.2 V	62			ns
			3 V	50			
$t_{(cap)}$	Timer_A, Timer_B capture timing	TA0, TA1, TA2 (see Note 2)	2.2 V/3 V	1.5			cycle
			2.2 V	62			ns
		TB0, TB1, TB2, TB3, TB4, TB5, TB6 (see Note 3)	3 V	50			
$f_{(TAext)}$	Timer_A, Timer_B clock frequency externally applied to pin	TACLK, TBCLK, INCLK: $t_{(H)} = t_{(L)}$	2.2 V			8	MHz
$f_{(TBext)}$			3 V			10	
$f_{(TAint)}$	Timer_A, Timer_B clock frequency	SMCLK or ACLK signal selected	2.2 V			8	MHz
$f_{(BTAint)}$			3 V			10	

唤醒 LPM3

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(LPM3)}$	Delay time	V_{CC} = 2.2 V/3 V			6	µs

漏电流

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{lkg(P1.x)}$	Leakage current	Port P1	Port 1: $V_{(P1.x)}$ (see Note 2)	V_{CC} = 2.2 V/3 V			±50	nA
$I_{lkg(P2.x)}$		Port P2	Port 2: $V_{(P2.3)}$ $V_{(P2.4)}$ (see Note 2)				±50	
$I_{lkg(P6.x)}$		Port P6	Port 6: $V_{(P6.x)}$ (see Note 2)				±50	

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input and there must be no optional pullup or pulldown resistor.

RAM

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VRAMh	CPU HALTED (see Note 1)	1.6			V

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

比较器 A

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON=1, CARSEL=0, CAREF=0	V_{CC} = 2.2 V		25	40	µA
			V_{CC} = 3 V		45	60	
$I_{(Refladder/Refdiode)}$		CAON=1, CARSEL=0, CAREF=1/2/3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V		30	50	µA
			V_{CC} = 3 V		45	71	
$V_{(IC)}$	Common-mode input voltage	CAON =1	V_{CC} = 2.2 V/3 V	0		V_{CC}–1	V
$V_{(Ref025)}$	Voltage @ 0.25 V_{CC} node / V_{CC}	PCA0=1, CARSEL=1, CAREF=1, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V/3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	Voltage @ 0.5V_{CC} node / V_{CC}	PCA0=1, CARSEL=1, CAREF=2, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V/3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	See Figure 7.	PCA0=1, CARSEL=1, CAREF=3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2 T_A = 85°C	V_{CC} = 2.2 V	390	480	540	mV
			V_{CC} = 3 V	400	490	550	
$V_{(offset)}$	Offset voltage	See Note 2	V_{CC} = 2.2 V/3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON=1	V_{CC} = 2.2 V/3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$		T_A = 25°C, Overdrive 10 mV, Without filter: CAF=0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF=1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$		T_A = 25°C, Overdrive 10 mV, without filter: CAF=0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, with filter: CAF=1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	

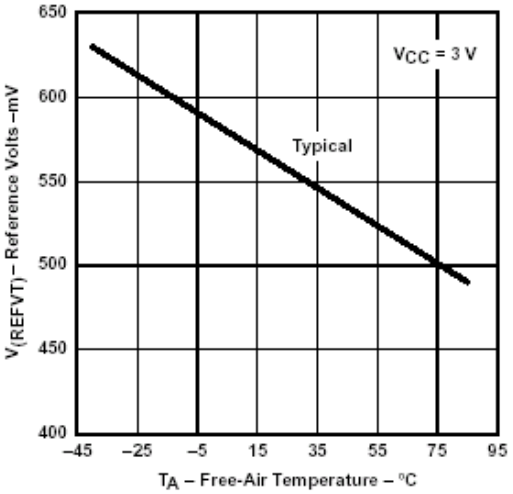


图6 V(RefVT) vs Temperature, VCC = 3 V

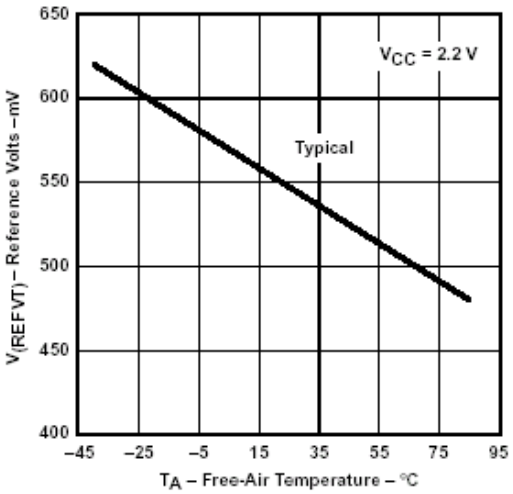


图7 V(RefVT) vs Temperature, VCC = 2.2 V

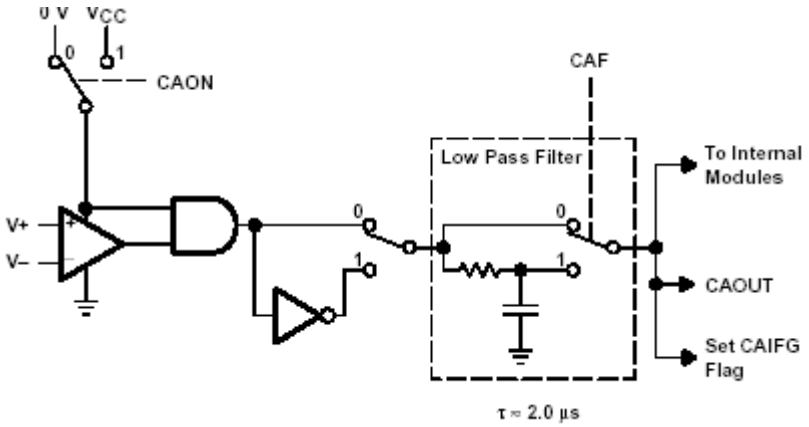


图 8 比较器 A 模块的结构框图

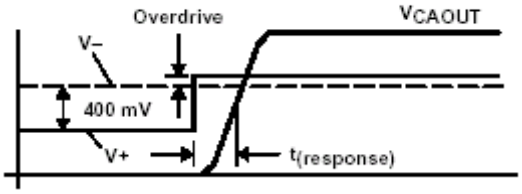


图 9 过驱动定义

POR/上电复位（BOR）（见 note1 和 2）

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout				2000	µs
$V_{CC(Start)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10)		$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10 through Figure 12)			1.71	V
$V_{hys(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10)	70	130	180	mV
$t_{(reset)}$		Pulse length needed at RST/NMI pin to accepted reset internally, V_{CC} = 2.2 V/3 V	2			µs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.

2. During power up, the CPU begins code execution following a period of $t_{BOR(delay)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \ge V_{CC(min)}$. See the *MSP430x1xx Family User's Guide* (SLAU049) for more information on the brownout/SVS circuit.

特性曲线

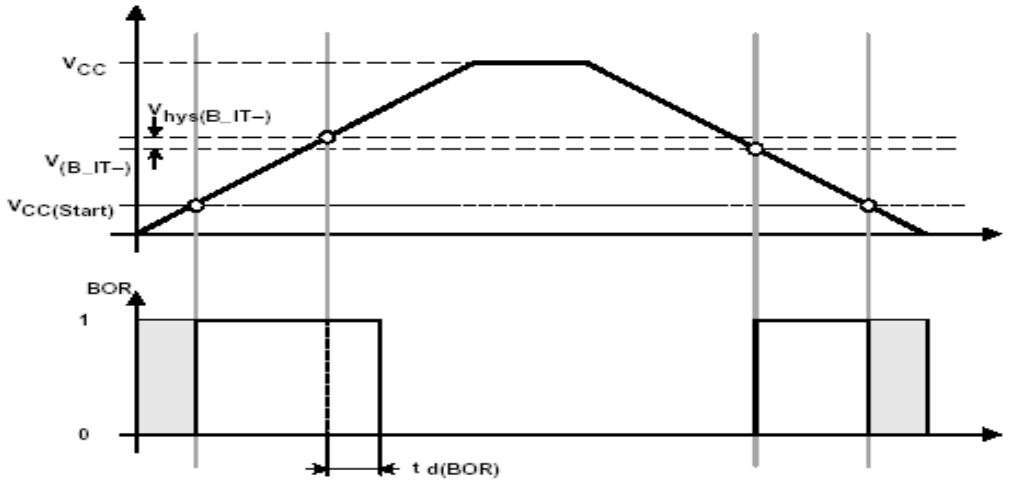


图 10 POR/上电复位与供电电压

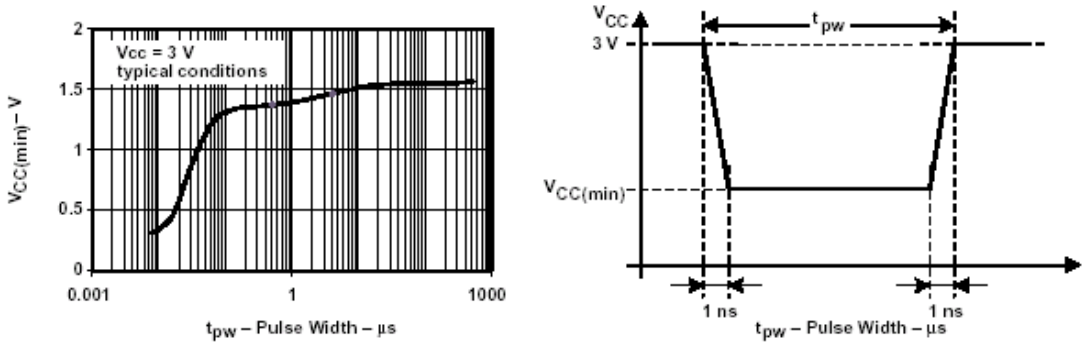


图 11 Vcc(min)上的方形电压降产生一个 POR/掉电信号

SVS（供电电压管理/监测）

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
$t_{(SVSR)}$	dV_{CC}/dt > 30 V/ms (see Figure 13)		5		150	µs
	dV_{CC}/dt ≤ 30 V/ms				2000	µs
$t_{d(SVSon)}$	SVSON, switch from VLD = 0 to VLD ≠ 0, V_{CC} = 3 V		20		150	µs
t_{settle}	VLD ≠ 0‡				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, V_{CC}/dt ≤ 3 V/s (see Figure 13)			1.55	1.7	V
$V_{hys(B\_IT-)}$	V_{CC}/dt ≤ 3 V/s (see Figure 13)	VLD = 1	70	120	155	mV
		VLD = 2 .. 14	$V_{(SVS\_IT-)}$ x 0.004		$V_{(SVS\_IT-)}$ x 0.008	
	V_{CC}/dt ≤ 3 V/s (see Figure 13), External voltage applied on A7	VLD = 15	4.4		10.4	mV
$V_{(SVS\_IT-)}$	V_{CC}/dt ≤ 3 V/s (see Figure 13 and Figure 14)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.25	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.6	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61†	
		VLD = 13	3.24	3.5	3.76†	
		VLD = 14	3.43	3.7†	3.99†	
	V_{CC}/dt ≤ 3 V/s (see Figure 13 and Figure 14), External voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (see Note 1)	VLD ≠ 0, V_{CC} = 2.2 V/3 V			10	15	µA

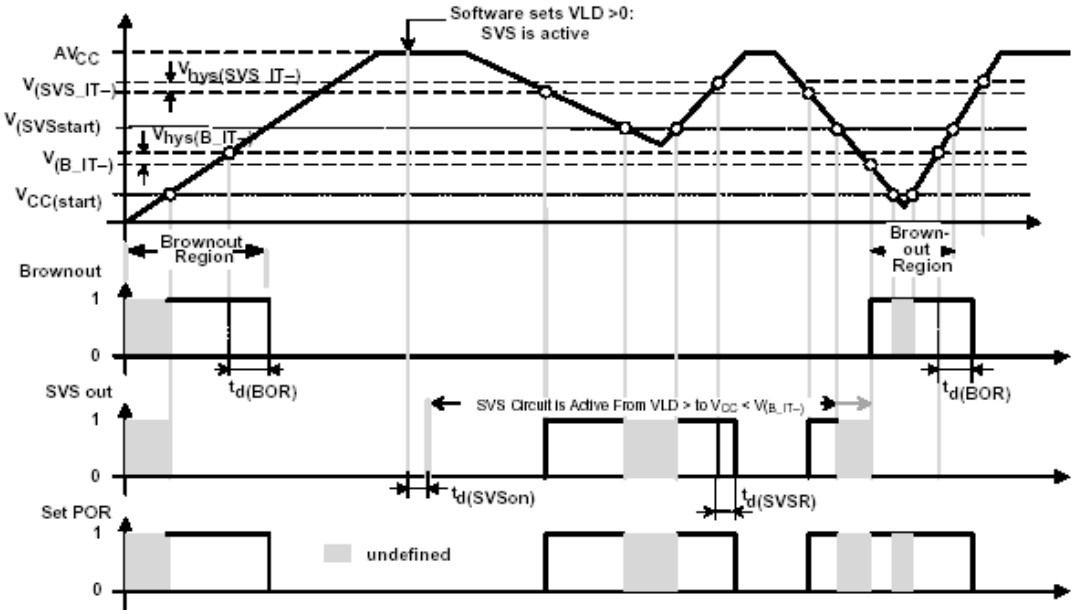


图 13　SVS 复位（SVSR）与供电电压

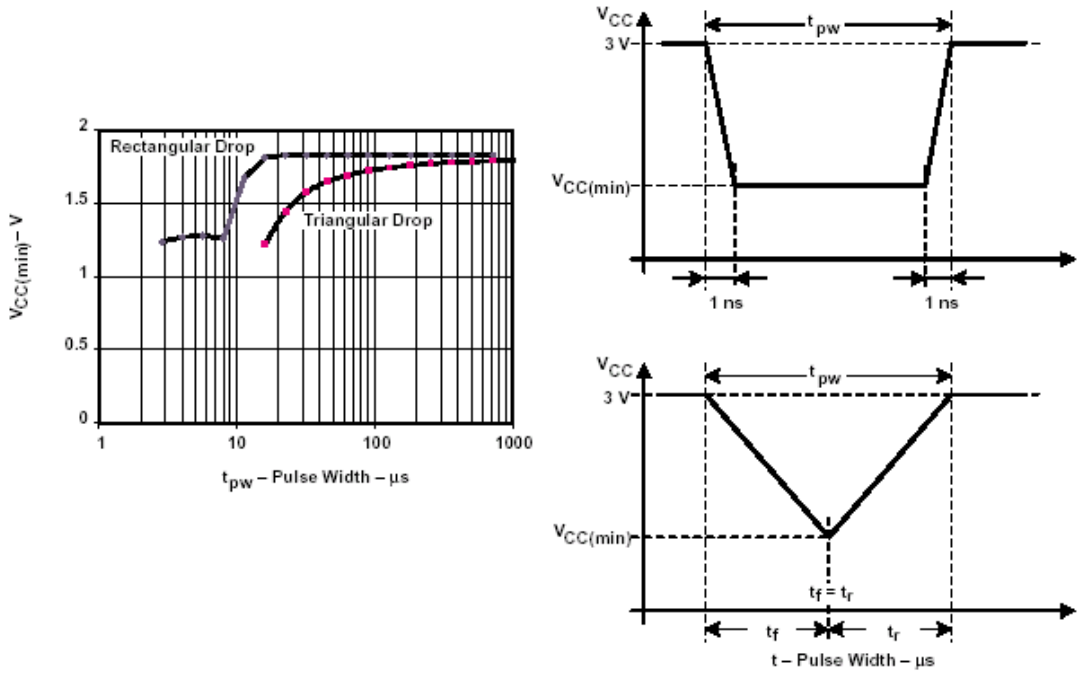


图 14　Vcc(min):产生一个 SVS 信号的方形电压降和三角形电压降（VLD=1）

DC0

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{(DCO03)}$	R_{sel} = 0, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.08	0.12	0.15	MHz
		V_{CC} = 3 V	0.08	0.13	0.16	
$f_{(DCO13)}$	R_{sel} = 1, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.14	0.19	0.23	MHz
		V_{CC} = 3 V	0.14	0.18	0.22	
$f_{(DCO23)}$	R_{sel} = 2, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.22	0.30	0.36	MHz
		V_{CC} = 3 V	0.22	0.28	0.34	
$f_{(DCO33)}$	R_{sel} = 3, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.37	0.49	0.59	MHz
		V_{CC} = 3 V	0.37	0.47	0.56	
$f_{(DCO43)}$	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.61	0.77	0.93	MHz
		V_{CC} = 3 V	0.61	0.75	0.90	
$f_{(DCO53)}$	R_{sel} = 5, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	1	1.2	1.5	MHz
		V_{CC} = 3 V	1	1.3	1.5	
$f_{(DCO63)}$	R_{sel} = 6, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	1.6	1.9	2.2	MHz
		V_{CC} = 3 V	1.69	2.0	2.29	
$f_{(DCO73)}$	R_{sel} = 7, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	2.4	2.9	3.4	MHz
		V_{CC} = 3 V	2.7	3.2	3.65	
$f_{(DCO47)}$	R_{sel} = 4, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V/3 V	f_{DCO40} × 1.7	f_{DCO40} × 2.1	f_{DCO40} × 2.5	MHz
$f_{(DCO77)}$	R_{sel} = 7, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	4	4.5	4.9	MHz
		V_{CC} = 3 V	4.4	4.9	5.4	
$S_{(Rsel)}$	$S_R = f_{Rsel+1} / f_{Rsel}$	V_{CC} = 2.2 V/3 V	1.35	1.65	2	
$S_{(DCO)}$	$S_{DCO} = f_{DCO+1} / f_{DCO}$	V_{CC} = 2.2 V/3 V	1.07	1.12	1.16	
D_T	Temperature drift, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 2)	V_{CC} = 2.2 V	–0.31	–0.36	–0.40	%/°C
		V_{CC} = 3 V	–0.33	–0.38	–0.43	
D_V	Drift with V_{CC} variation, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 2)	V_{CC} = 2.2 V/3 V	0	5	10	%/V

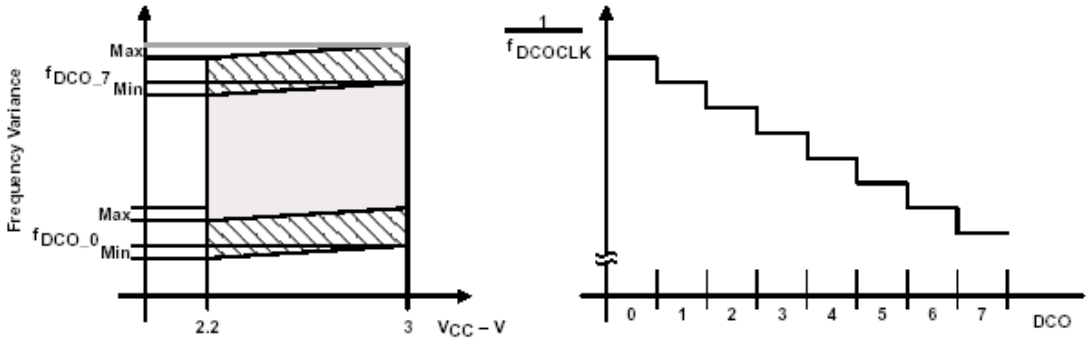


图 15 DCO 特性

DCO 的主要特性

- 单个芯片有最大和最小运行频率，fDCOx0 到 fDCOx0 的详细参数对所有芯片都存在。
- 所有由 Rsel(n)选择的范围与 Rsel(n+1)交叠，Rsel0 与 Rsel1 交叠…Rsel6 与 Rsel7 交叠。
- DCO 控制位 DCO0、DCO1 和 DCO2 具有由参数 SDCO 定义的台阶。
- 调制控制位 MOD0 到 MOD4 选择在 32 个 DCOCLK 周期多久使用 Fdco+1。频率是平均＝fdco×（2MOD/32）。

晶体振荡器，LFXT1 振荡器

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
X_{CIN}	Integrated input capacitance	XTS=0; LF oscillator selected, V_{CC} = 2.2 V/3 V		12		pF
		XTS=1; XT1 oscillator selected, V_{CC} = 2.2 V/3 V		2		
X_{COUT}	Integrated output capacitance	XTS=0; LF oscillator selected, V_{CC} = 2.2 V/3 V		12		pF
		XTS=1; XT1 oscillator selected, V_{CC} = 2.2 V/3 V		2		
X_{INL}	Input levels at XIN, XOUT	V_{CC} = 2.2 V/3 V	V_{SS}		$0.2 \times V_{CC}$	V
X_{INH}		V_{CC} = 2.2 V/3 V	$0.8 \times V_{CC}$		V_{CC}	V

晶体振荡器，XT2 振荡器

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
X_{CIN}	Integrated input capacitance	V_{CC} = 2.2 V/3 V		2		pF
X_{COUT}	Integrated output capacitance	V_{CC} = 2.2 V/3 V		2		pF
X_{INL}	Input levels at XIN, XOUT	V_{CC} = 2.2 V/3 V	V_{SS}		$0.2 \times V_{CC}$	V
X_{INH}		V_{CC} = 2.2 V/3 V	$0.8 \times V_{CC}$		V_{CC}	V

USART0,USART1

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(\tau)}$	USART0/USART1: deglitch time	V_{CC} = 2.2 V	200	430	800	ns
		V_{CC} = 3 V	150	280	500	

12 位 ADC，供电和输入条件范围

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together AV_{SS} and DV_{SS} are connected together $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
V_{REF+}	Positive built-in reference voltage output	REF2_5 V = 1 for 2.5 V built-in reference REF2_5 V = 0 for 1.5 V built-in reference $I_{V(REF+)} \le I_{(VREF+)max}$	3 V	2.4	2.5	2.6	
			2.2 V/ 3 V	1.44	1.5	1.56	
	Positive built-in reference, AVcc minimum voltage	REF2_5V = 0, $I_{VREF+} \le$ 1mA		2.2			
		REF2_5V = 1, $I_{VREF+} \le$ 0.5mA		V_{REF+} + 0.15			
		REF2_5V = 1, $I_{VREF+} \le$ 1mA		V_{REF+} + 0.15			
I_{VREF+}	Load-current out of V_{REF+} terminal		2.2 V	0.01		–0.5	mA
			3 V			–1	
$I_{L(VREF)+}$	Load-current regulation V_{REF+} terminal	$I_{V(REF)+}$ = 500 µA +/– 100 µA Analog input voltage ~0.75 V; REF2_5 V = 0	2.2 V			±2	LSB
			3 V			±2	
		$I_{V(REF)+}$ = 500 µA ± 100 µA Analog input voltage ~1.25 V; REF2_5 V = 1	3 V			±2	LSB
$I_{DL(VREF)+}$	Load current regulation V_{REF+} terminal	$I_{V(REF)+}$ =100 µA → 900 µA, VCC=3 V, ax ~0.5 x V_{REF+} Error of conversion result ≤ 1 LSB	C_{VREF+} =5 µF			20	ns
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 2)		1.4		V_{AVCC}	V
V_{REF-}/V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 3)		0		1.2	V
$(V_{eREF+} - V_{REF-}/V_{eREF-})$	Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 4)		1.4		V_{AVCC}	V
$V_{(P6.x/Ax)}$	Analog input voltage range (see Note 5)	All P6.0/A0 to P6.7/A7 terminals. Analog inputs selected in ADC12MCTLx register and P6Sel.x=1 $0 \le x \le 7$; $V_{(AVSS)} \le V_{P6.x/Ax} \le V_{(AVCC)}$		0		V_{AVCC}	V
I_{ADC12}	Operating supply current into AV_{CC} terminal (see Note 6)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 1, REFON = 0 SHT0=0, SHT1=0, ADC12DIV=0	2.2 V		0.65	1.3	mA
			3 V		0.8	1.6	
I_{REF+}	Operating supply current into AV_{CC} terminal (see Note 7)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, REF2_5V = 1	3 V		0.5	0.8	mA
I_{REF+}	Operating supply current (see Note 7)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, REF2_5V = 0	2.2 V		0.5	0.8	mA
			3 V		0.5	0.8	

12 位 ADC，内置参考电压

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
I_{VeREF+}	Static input current (see Note 2)	$0V \le V_{eREF+} \le V_{AVCC}$	2.2 V/3 V			±1	µA
$I_{VREF-/VeREF-}$	Static input current (see Note 2)	$0V \le V_{eREF-} \le V_{AVCC}$	2.2 V/3 V			±1	µA
C_{VREF+}	Capacitance at pin V_{REF+} (see Note 3)	REFON =1, $0 mA \le I_{VREF+} \le I_{V(REF)+(max)}$	2.2 V/3 V	5	10		µF
C_i	Input capacitance (see Note 4)	Only one terminal can be selected at one time, P6.x/Ax	2.2 V			40	pF
Z_i	Input MUX ON resistance(see Note 4)	$0V \le V_{Ax} \le V_{AVCC}$	3 V			2000	Ω
T_{REF+}	Temperature coefficient of built-in reference	$I_{V(REF)+}$ is a constant in the range of $0 mA \le I_{V(REF)+} \le 1 mA$	2.2 V/3 V			±100	ppm/°C

12 位 ADC，时序参数

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$t_{REF(ON)}$	Settle time of internal reference voltage (see Figure 16 and Note 1)	$I_{V(REF)+} = 0.5 mA$, $C_{V(REF)+} = 10 µF$, $V_{REF+} = 1.5 V$, $V_{AVCC} = 2.2 V$				17	ms
f(ADC12CLK)		Error of conversion result ≤ ±2 LSB (vs. the conversion result taken with f(ADC12CLK) = 5MHz)	2.2V/ 3V		5		MHz
f(ADC12OSC)		ADC12DIV=0 [f(ADC12CLK) =f(ADC12OSC)]	2.2V/ 3V	3.7		6.3	MHz
$t_{CONVERT}$	Conversion time	$AV_{CC(min)} \le V_{AVCC} \le AV_{CC(max)}$, $C_{VREF+} \ge 5 µF$, Internal oscillator, $f_{OSC} = 3.7 MHz$ to 6.3 MHz	2.2V/ 3V	2.06		3.51	µs
	Conversion time	$A_{VCC(min)} \le V_{AVCC} \le A_{VCC(max)}$, External $f_{ADC12CLK}$ from ACLK or MCLK or SMCLK: ADC12SSEL ≠ 0			13×ADC12DIV× $1/f_{ADC12CLK}$		µs
$t_{ADC12ON}$	Settle time of the ADC	$A_{VCC(min)} \le V_{AVCC} \le A_{VCC(max)}$ (see Note 2)				100	ns
t_{Sample}	Sampling time	$V_{AVCC(min)} \le V_{AVCC} \le V_{AVCC(max)}$, $R_{i(source)} = 400 Ω$, $Z_i = 1000 Ω$, $C_i = 30 pF$, $τ = [R_{i(source)} + Z_i] \times C_i$ (see Note 3)	3V	1220			ns
			2.2V	1400			

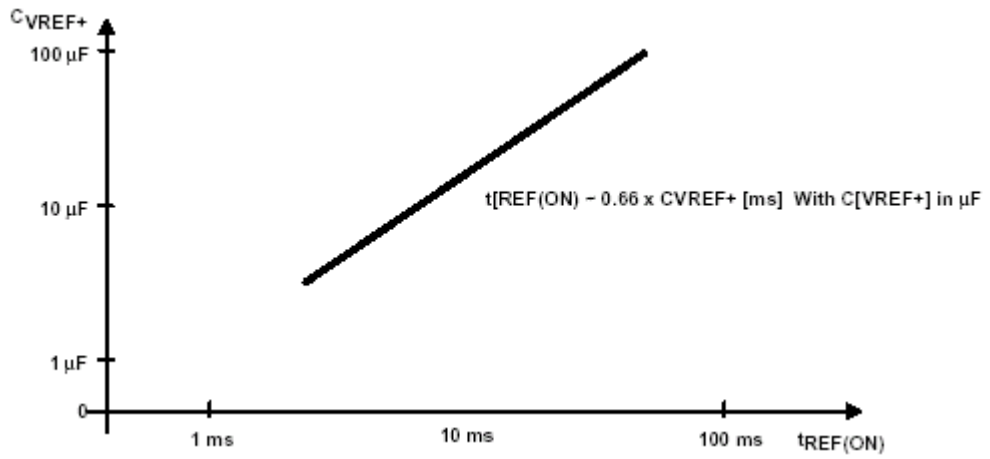


图 16 典型内部参考电压建立时间 Tref(ON)与 VREF+上的外部电容

12 位 ADC，线性参数

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$E_{(I)}$	Integral linearity error	1.4 V ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}) min ≤ 1.6 V	2.2 V/3 V			±2	LSB
		1.6 V < [V_{eREF+} – V_{REF-}/V_{eREF-}] min ≤ [V(AV_{CC})]				±1.7	
E_D	Differential linearity error	(V_{eREF+} – V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}), $C(V_{REF+})$ = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V			±1	LSB
E_O	Offset error	(V_{eREF+} – V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}), Internal impedance of source R_i < 100 Ω, $C(V_{REF+})$ = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±4	LSB
E_G	Gain error	(V_{eREF+} – V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}), $C(V_{REF+})$ = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±1.1	±2	LSB
E_T	Total unadjusted error	(V_{eREF+} – V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}), $C(V_{REF+})$ = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±5	LSB

12 位 ADC，温度传感器和内置 Vmid

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal (see Note 1)	V_{REFON} = 0, INCH = 0Ah, ADC12ON=NA, T_A = 25°C	2.2 V		40	120	µA
			3 V		60	160	
V_{SENSOR}		ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		986	986±5%	mV
			3 V		986	986±5%	
TC_{SENSOR}		ADC12ON = 1, INCH = 0Ah	2.2 V		3.55	3.55±3%	mV/°C
			3 V		3.55	3.55±3%	
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected (see Note 2)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30			µs
			3 V	30			
I_{VMID}	Current into divider at channel 11	ADC12ON = 1, INCH = 0Bh, (see Note 3)	2.2 V			NA	µA
			3 V			NA	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, V_{MID} is ~0.5 x V_{AVCC}	2.2 V		1.1	1.1±0.04	V
			3 V		1.5	1.50±0.04	
$t_{ON(VMID)}$	On-time if channel 11 is selected (see Note 4)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V			NA	ns
			3 V			NA	

12 位 DAC，电源说明

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} = DV_{CC}, AV_{SS} = DV_{SS} = 0 V		2.20		3.60	V
I_{DD}	Supply Current (see Notes 1 and 2)	DAC12AMPx=[0,1], DAC12IR=0, DAC12_xDAT=0800h	2.2V/3V		TBD	TBD	µA
		DAC12AMPx=2, DAC12IR=0, DAC12_xDAT=0800h	2.2V/3V		120	TBD	
		DAC12AMPx=[2, 3, 4], DAC12IR=1, DAC12_xDAT=0800h , V_{eREF+}='V_{REF+}='AV_{CC}	2.2V/3V		160	TBD	
		DAC12AMPx=[5, 6], DAC12IR=1, DAC12_xDAT=0800h, V_{eREF+}='V_{REF+}='AV_{CC}	2.2V/3V		275	TBD	
		DAC12AMPx=7, DAC12IR=1, DAC12_xDAT=0800h, V_{eREF+}='V_{REF+}='AV_{CC}	2.2V/3V		725	TBD	
PSRR	Power supply sensitivity (see Notes 3 and 4)	DAC12_xDAT = 800h, V_{REF} = 1.5 V ΔAV_{CC} = 100mV	2.2V		~70		dB
		DAC12_xDAT = 800h, V_{REF} = 1.5 V or 2.5 V ΔAV_{CC} = 100mV	3V				

12 位 DAC，线性度说明

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Resolution		(12-bit Monotonic)		12			bits
INL	Integral nonlinearity (see Note 1)	V_{ref} = 1.5 V or AV_{CC} DAC12AMPx = 7, DAC12IR = 1	2.2V		±4.0	±8.0	LSB
		V_{ref} = 1.5 V, 2.5 V or AV_{CC} DAC12AMPx = 7, DAC12IR = 1	3V				
DNL	Differential nonlinearity (see Note 1)	V_{ref} = 1.5 V or AV_{CC} DAC12AMPx = 7, DAC12IR = 1	2.2V			±1.0	LSB
		V_{ref} = 1.5 V, 2.5 V or AV_{CC} DAC12AMPx = 7, DAC12IR = 1	3V				
E_O	Offset voltage w/o calibration (see Notes 1, 2)	V_{ref} = 1.5 V or AV_{CC} DAC12AMPx = 7, DAC12IR = 1	2.2V			±21	mV
		V_{ref} = 1.5 V, 2.5 V or AV_{CC} DAC12AMPx = 7, DAC12IR = 1	3V				
	Offset voltage with calibration (see Notes 1, 2)	V_{ref} = 1.5 V or AV_{CC} DAC12AMPx = 7, DAC12IR = 1	2.2V			±1.5	
		V_{ref} = 1.5 V, 2.5 V or AV_{CC} DAC12AMPx = 7, DAC12IR = 1	3V				
$d_{E(ZS)}/d_T$	Zero–scale error temperature coefficient (see Note 1)		2.2V/3V		30		uV/C
E_G	Gain error (see Note 1)		2.2V/3V			±3.50	% FS
$d_{E(G)}/d_T$	Gain temperature coefficient (see Note 1)		2.2V/3V		10		ppm/°C
t_{Offset_Cal}	Time for offset calibration (see Note 3)	DAC12.xAmp=2	2.2V/3V			25.0	ms
		DAC12.xAmp=3,5	2.2V/3V			8.0	
		DAC12.xAmp=4,6,7	2.2V/3V			1.5	

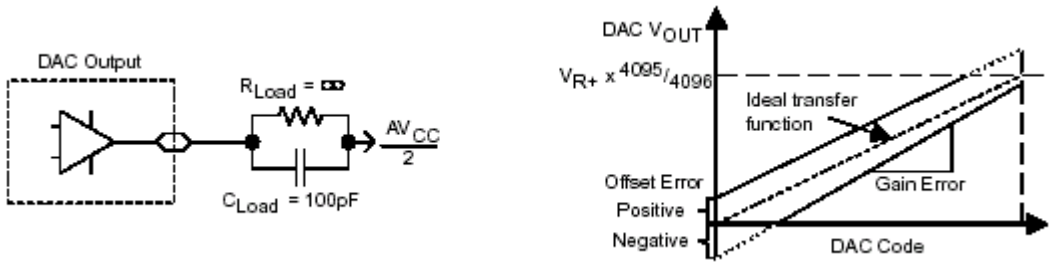


图 17 线性度测试负荷条件和增益/偏置定义

12 位 DAC，输出说明

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
V_O	Output voltage range (see Note 1)	R_{Load}= 3 kΩ, Ve_{REF+} = AV_{CC}, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	AV_{CC}–0.13		AV_{CC}	V
		No Load, Ve_{REF+} = AV_{CC}, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	0		0.025	
		No Load, Ve_{REF+} = AV_{CC}, DAC12.xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	AV_{CC} –0.1		AV_{CC}	
$C_{L(DAC12)}$	DAC12 load capacitance		2.2V/3V			100	pF
$R_{L(DAC12)}$	DAC12 load resistance		2.2V/3V	2.2			kΩ
$R_{O/P(DAC12)}$ (see Figure 18)	Output Resistance V_{OUT}<0.3V or V_{OUT}>AV_{CC}–0.3V	R_{Load}= 3 kΩ, $V_{O/P(DAC12)}$< 0.3V, DAC12AMPx = 2	2.2V/3V			200	Ω
		R_{Load}= 3 kΩ$V_{O/P(DAC12)}$>AV_{CC}–0.3V	2.2V/3V			200	
	Output Resistance 0.3V<V_{OUT}<AV_{CC}–0.3V	R_{Load}= 3 kΩ, 0.3V ≤ $V_{O/P(DAC12)}$ ≤ AV_{CC} – 0.3V	2.2V/3V			4	

NOTES: 1. Data is valid after the offset calibration of the output amplifier.

12 位 DAC，参考输入说明

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
V_{eREF+}	Reference input voltage range	DAC12.xIR=0, (see Notes 1 and 2)	2.2V/3V		AV_{CC} /3	AV_{CC} + 0.2	V
		DAC12.xIR=1, (see Notes 3 and 4)	2.2V/3V		AVcc	AVcc + 0.2	
$R_{I(VREF+)}$, $R_{I(VeREF+)}$	Reference input resistance (see Figure 18)	DAC12_0 IR=1, DAC12_1 IR = 0	2.2V/3V	40	48	56	kΩ
		DAC12_0 IR=0, DAC12_1 IR = 1	2.2V/3V				
		DAC12_0 IR=DAC12_1 IR =0	2.2V/3V	20			MΩ

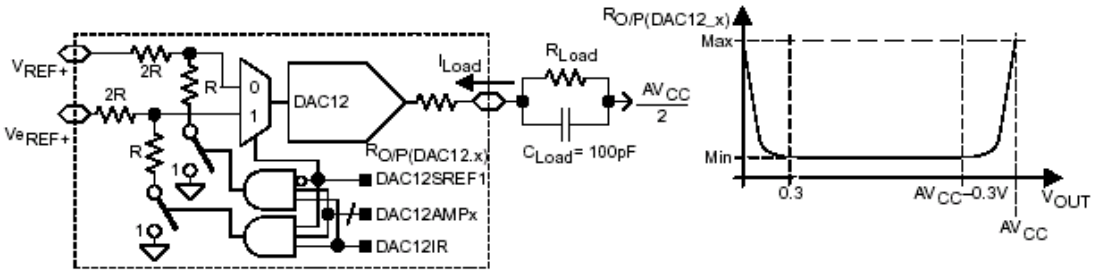


图 18　DAC12_x 参考输入和 DAC 输出电阻测试

12 位 DAC 动态说明（TA=25℃除非另有说明）（见图 19）

PARAMETER		TEST CONDITIONS		VCC	MIN	TYP	MAX	UNIT
t_{ON}	DAC12 on-time	DAC12_xDAT = 800h, Error$_{V(O)}$ < ±0.5 LSB	DAC12.xAmp=0 → {2, 3, 4}	2.2V/3V		TBD	TBD	µs
			DAC12.xAmp=0 → {5, 6}	2.2V/3V		TBD	TBD	
			DAC12.xAmp=0 → 7	2.2V/3V		TBD	TBD	
$t_{S(FS)}$	Settling time, full-scale	DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12.xAmp=2	2.2V/3V		TBD	TBD	µs
			DAC12.xAmp=3,5	2.2V/3V		TBD	TBD	
			DAC12.xAmp=4,6,7	2.2V/3V		TBD	TBD	
$t_{S(C-C)}$	Settling time, code to code	DAC12_xDAT = 3F8h→ 408h→ 3F8h BF8h→ C08h→ BF8h	DAC12.xAmp=2	2.2V/3V			TBD	µs
			DAC12.xAmp=3,5	2.2V/3V			TBD	
			DAC12.xAmp=4,6,7	2.2V/3V			TBD	
SR	Slew Rate	DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12.xAmp=2	2.2V/3V	0.08			V/µs
			DAC12.xAmp=3,5	2.2V/3V	0.50			
			DAC12.xAmp=4,6,7	2.2V/3V	2.00			
Glitch energy: code-to-code		DAC12_xDAT = 3F8h→ 408h→ 3F8h BF8h→ C08h→ BF8h	DAC12.xAmp=2	2.2V/3V		25		nV-s
			DAC12.xAmp=3,5	2.2V/3V		25		
			DAC12.xAmp=4,6,7	2.2V/3V		25		

NOTES: 1. Slew rate applies to output voltage steps >= 200mV.

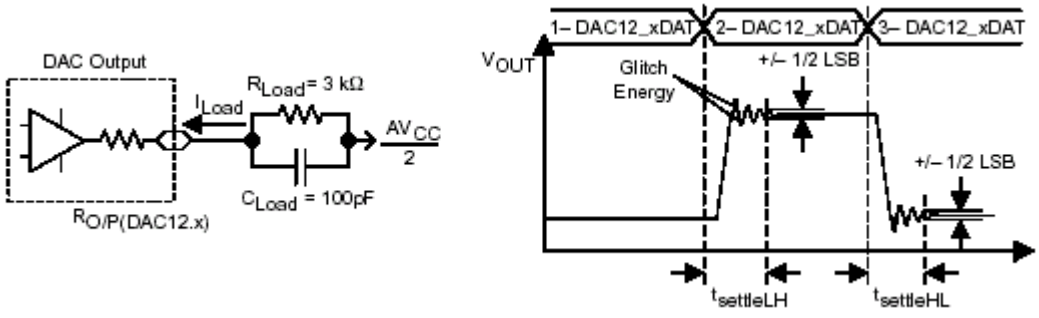


图 19 建立时间和短时脉冲波形干扰能量测试

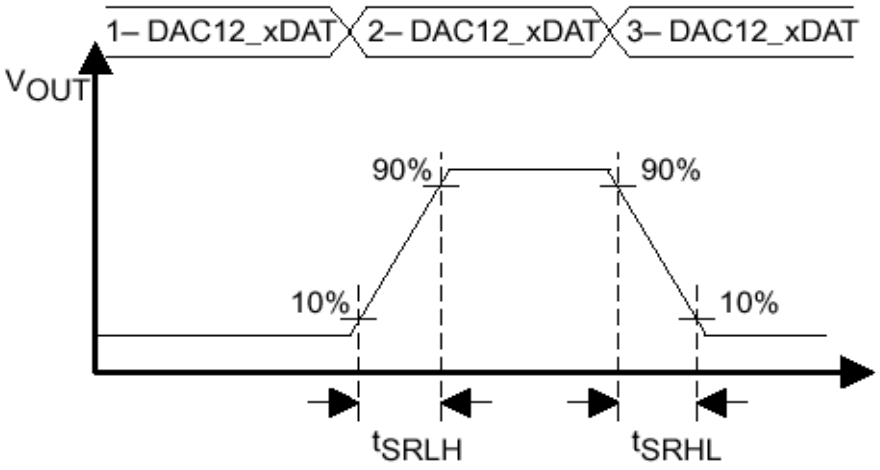


图 20 回转率测试

12 位 DAC 动态说明（TA=25℃除非另有说明）（见图 19）

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
SNR	Signal to noise ratio	DAC12AMPx = 2 (see Notes 1, 3, 5)	2.2V/3V		72		dB
		DAC12AMPx = (3, 5) (see Notes 1, 4, 5)	2.2V/3V		72		
		DAC12AMPx = (4, 6, 7) (see Notes 1, 4, 5)	2.2V/3V		72		
SINAD	Signal to noise and distortion	DAC12AMPx = 2 (see Notes 1, 2, 3, 5)	2.2V/3V		60		dB
		DAC12AMPx = (3, 5) (see Notes 1, 2, 4, 5)	2.2V/3V		60		
		DAC12AMPx = (4, 6, 7) (see Notes 1, 2, 4, 5)	2.2V/3V		60		
THD	Total harmonic distortion	DAC12AMPx = 2 (see Note 3, 5)	2.2V/3V		–60		dB
		DAC12AMPx = (3, 5) (see Note 4, 5)	2.2V/3V		–60		
		DAC12AMPx = (4, 6, 7) (see Note 4, 5)	2.2V/3V		–60		
SFDR	Spurious free dynamic range	DAC12AMPx = 2 (see Note 3, 5)	2.2V/3V		76		dB
		DAC12AMPx = (3, 5) (see Note 4, 5)	2.2V/3V		76		
		DAC12AMPx = (4, 6, 7) (see Note 4, 5)	2.2V/3V		76		

BW_{-3dB}	3-dB bandwidth, V_{DC}=1.5V, V_{AC}=0.1Vpp (see Figure 21)	DAC12AMPx = (2, 3, 4), DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2V/3V	40.0		kHz
		DAC12AMPx = (5, 6), DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2V/3V	180.0		
		DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2V/3V	584.0		
Channel to channel crosstalk (see Note 1 and Figure 22)		DAC12_0DAT = 800h, No Load, DAC12_1DAT = 80h<–>F7Fh, R_{Load} = 3kΩ f_{DAC12_1OUT} = 10kHz @ 50/50 duty cycle	2.2V/3V		–80	dB
		DAC12_0DAT = 80h<–>F7Fh, R_{Load} = 3kΩ, DAC12_1DAT = 800h, No Load f_{DAC12_0OUT} = 10kHz @ 50/50 duty cycle	2.2V/3V		–80	

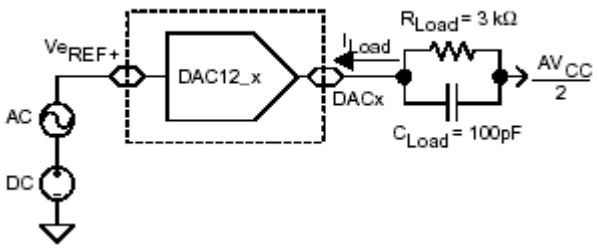


图 21 3dB 带宽规范的测试条件

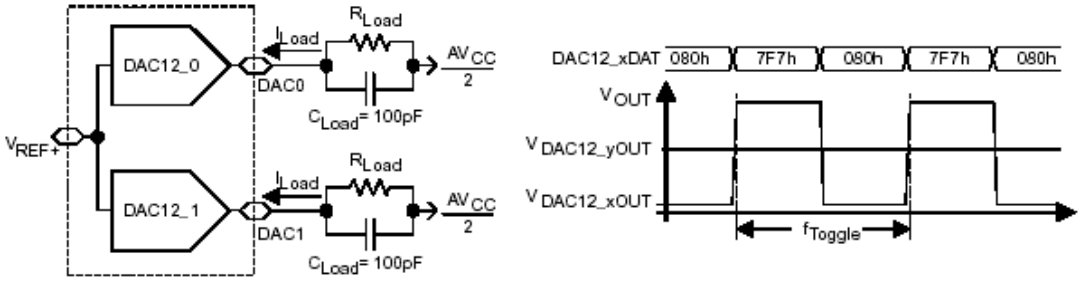


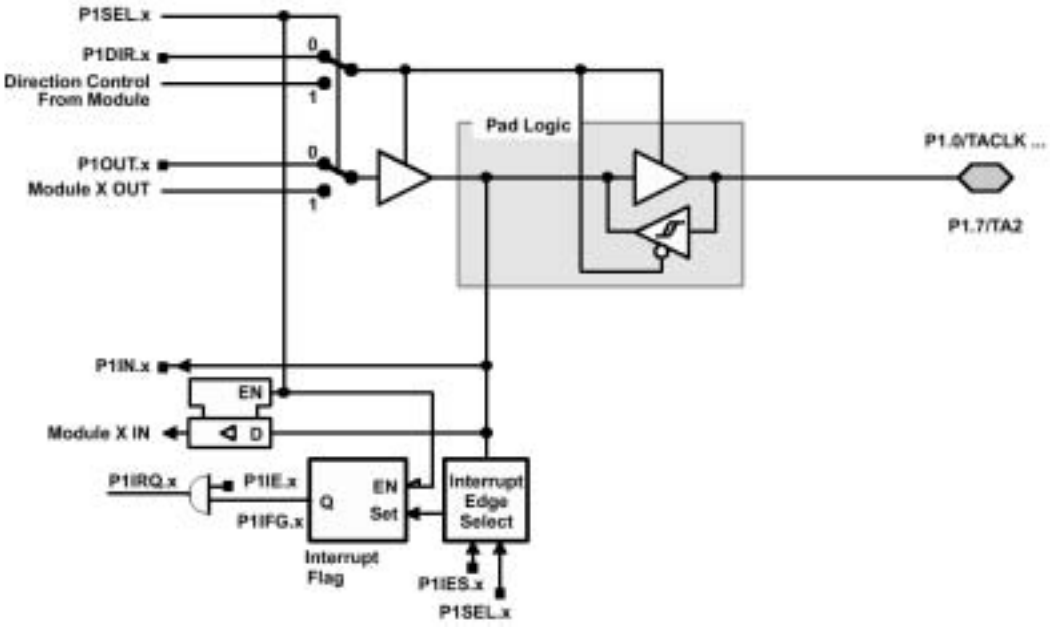
图 22 串扰测试条件

JTAG，编程存储器和熔丝

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$f_{(TCK)}$	JTAG/Test (see Note 4)	TCK frequency	2.2 V	DC		5	MHz
			3 V	DC		10	
		Pullup resistors on TMS, TCK, TDI (see Note 1)	2.2 V/ 3V	25	60	90	kΩ
$V_{CC(FB)}$	JTAG/fuse (see Note 2)	Supply voltage during fuse-blow condition, $T_{(A)}$ = 25°C		2.5			V
V_{FB}		Fuse-blow voltage, F versions (see Note 3)		6.0		7.0	V
I_{FB}		Supply current on TDI with fuse blown				100	mA
		Time to blow the fuse				1	ms
$I_{(DD-PGM)}$	F-versions only (see Note 4)	Current from DV_{CC} when programming is active	2.7 V/3.6 V		3	5	mA
$I_{(DD-Erase)}$		Current from DV_{CC} when erase is active	2.7 V/3.6 V		3	5	mA
$N_{(retention)}$	F-versions only	Write/erase cycles		10^4	10^5		cycles
		Data retention T_J = 25°C		100			years

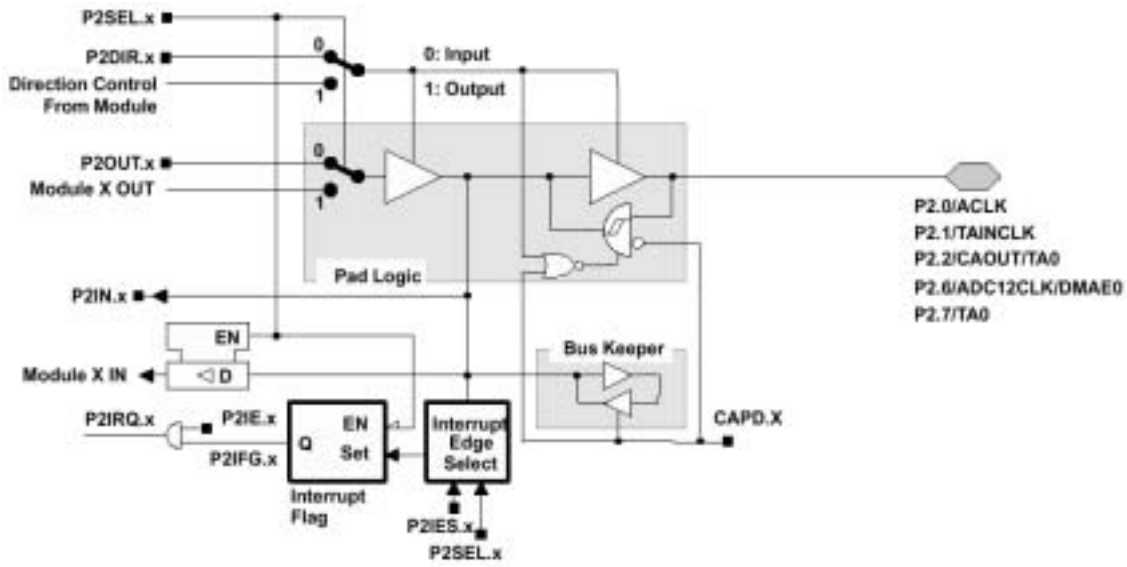
输入输出电路

（端口 P1，P1.0 到 P1.7，带施密特触发器的输入/输出）



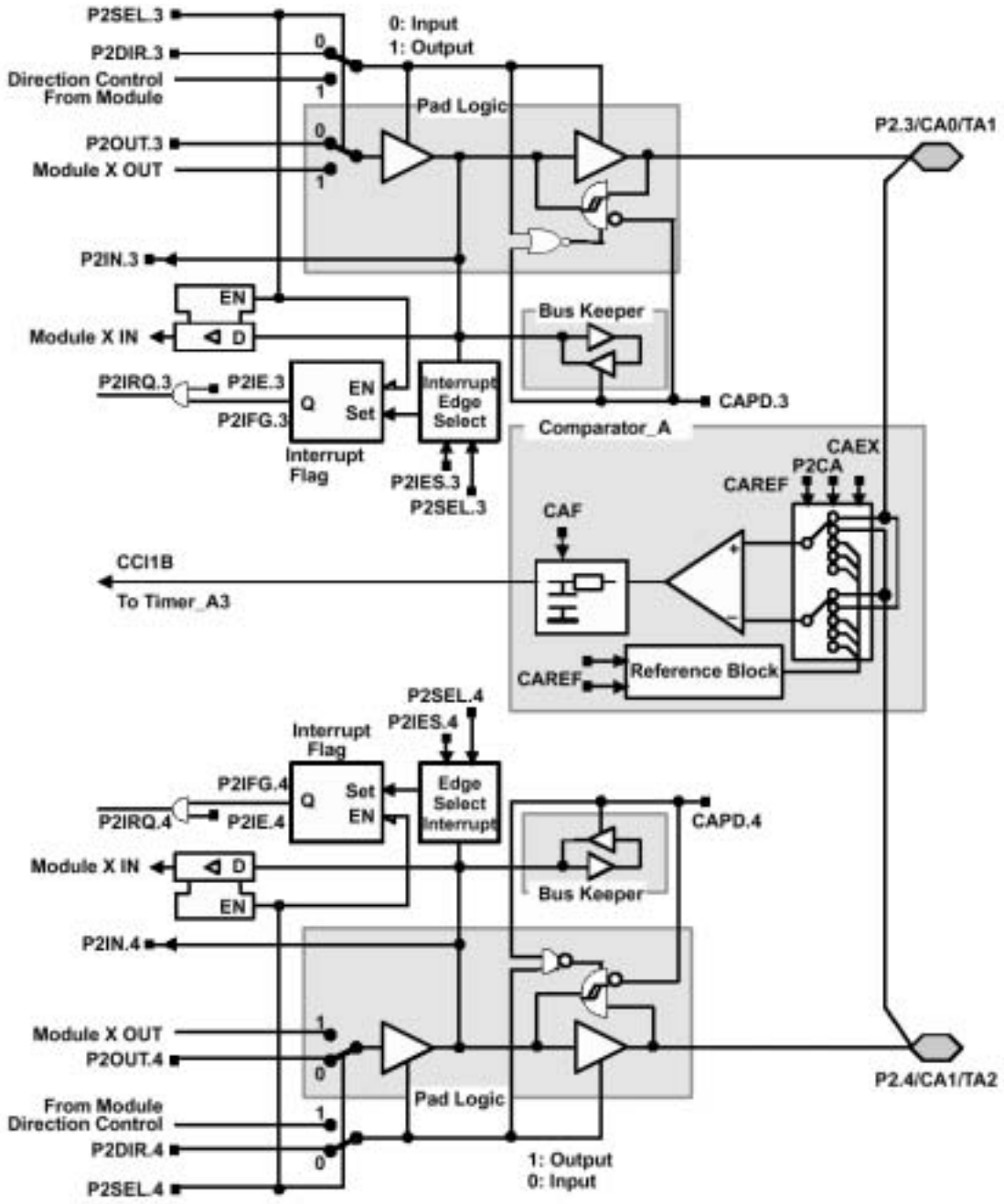
PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.0	P1DIR.0	P1DIR.0	P1OUT.0	DV_{SS}	P1IN.0	TACLK†	P1IE.0	P1IFG.0	P1IES.0
P1Sel.1	P1DIR.1	P1DIR.1	P1OUT.1	Out0 signal†	P1IN.1	CCI0A†	P1IE.1	P1IFG.1	P1IES.1
P1Sel.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 signal†	P1IN.2	CCI1A†	P1IE.2	P1IFG.2	P1IES.2
P1Sel.3	P1DIR.3	P1DIR.3	P1OUT.3	Out2 signal†	P1IN.3	CCI2A†	P1IE.3	P1IFG.3	P1IES.3
P1Sel.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	unused	P1IE.4	P1IFG.4	P1IES.4
P1Sel.5	P1DIR.5	P1DIR.5	P1OUT.5	Out0 signal†	P1IN.5	unused	P1IE.5	P1IFG.5	P1IES.5
P1Sel.6	P1DIR.6	P1DIR.6	P1OUT.6	Out1 signal†	P1IN.6	unused	P1IE.6	P1IFG.6	P1IES.6
P1Sel.7	P1DIR.7	P1DIR.7	P1OUT.7	Out2 signal†	P1IN.7	unused	P1IE.7	P1IFG.7	P1IES.7

端口 P2，P2.0 到 P2.2，P2.6 和 P2.7，带施密特触发器的输入/输出



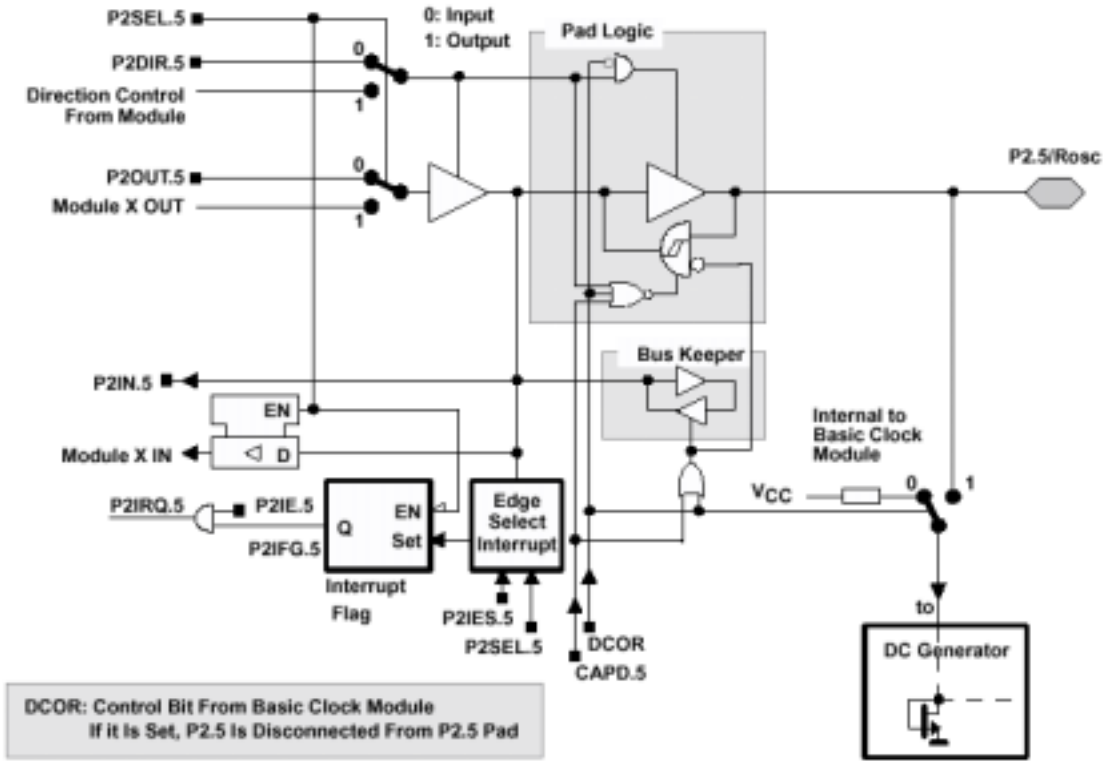
PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	ACLK	P2IN.0	unused	P2IE.0	P2IFG.0	P2IES.0
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	DV_{SS}	P2IN.1	INCLK‡	P2IE.1	P2IFG.1	P2IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	CAOUT†	P2IN.2	CCI0B‡	P2IE.2	P2IFG.2	P2IES.2
P2Sel.6	P2DIR.6	P2DIR.6	P2OUT.6	ADC12CLK¶	P2IN.6	DMAE0#	P2IE.6	P2IFG.6	P2IES.6
P2Sel.7	P2DIR.7	P2DIR.7	P2OUT.7	Out0 signal§	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7

端口 P2，P2.3 到 P2.4，带施密特触发器的输入/输出



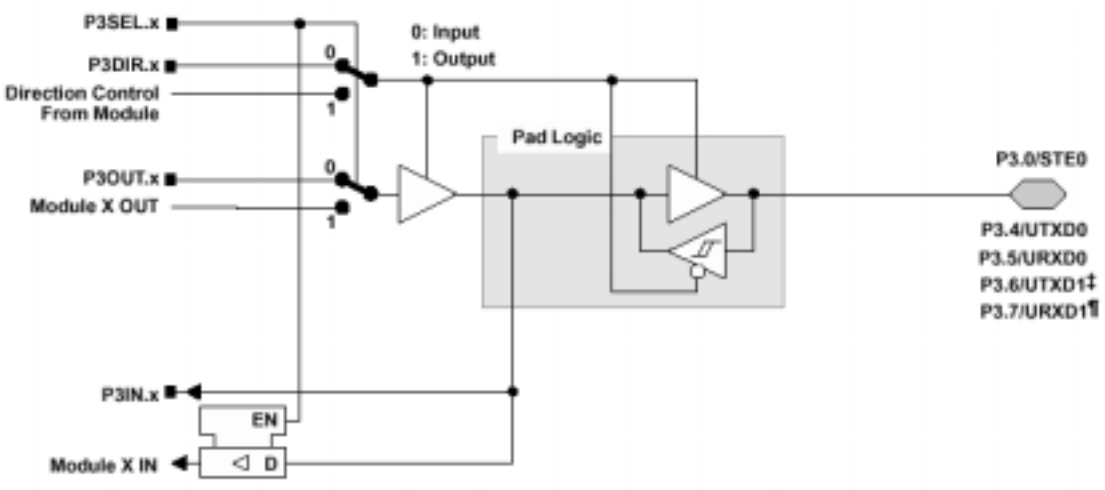
PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out1 signal†	P2IN.3	unused	P2IE.3	P2IFG.3	P2IES.3
P2Sel.4	P2DIR.4	P2DIR.4	P2OUT.4	Out2 signal†	P2IN.4	unused	P2IE.4	P2IFG.4	P2IES.4

端口 P2，P2.5，带施密特触发器的输入/输出和基本时钟模块的 Rosc 功能



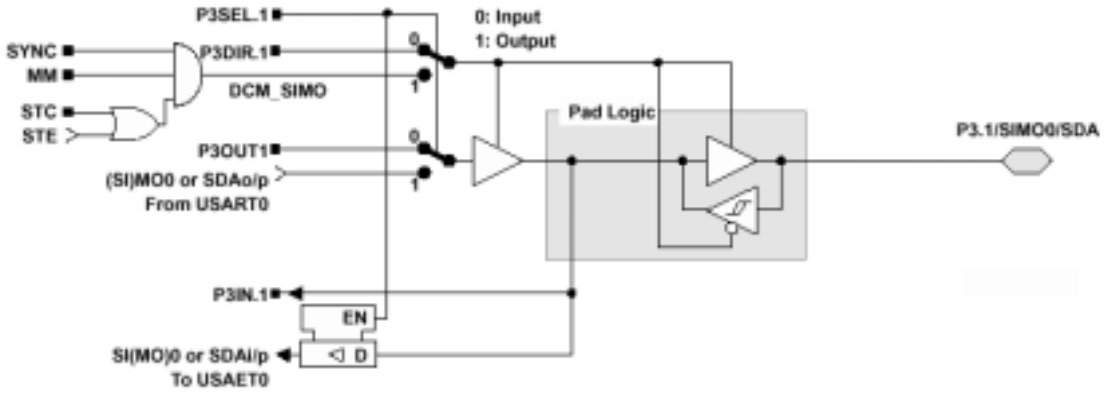
PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.5	P2DIR.5	P2DIR.5	P2OUT.5	DV_{SS}	P2IN.5	unused	P2IE.5	P2IFG.5	P2IES.5

端口 P3，P3.0 和 P3.4 到 P3.7，带施密特触发器的输入/输出

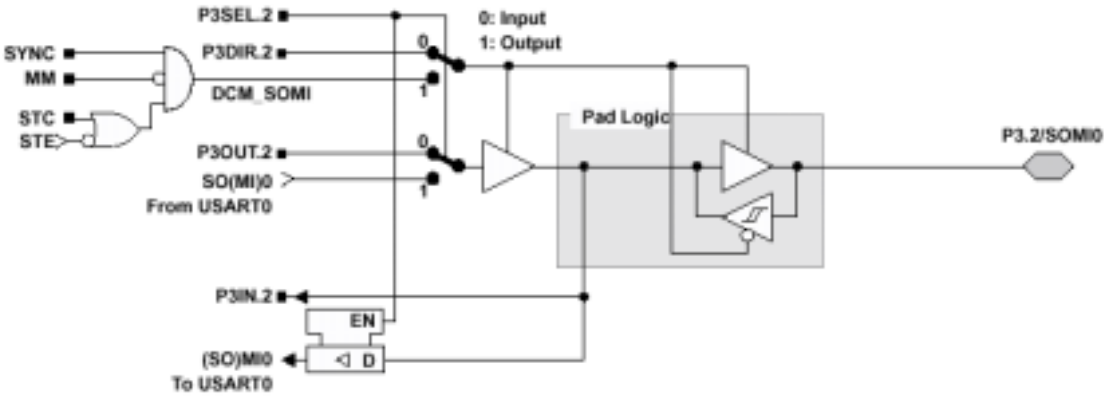


PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P3Sel.0	P3DIR.0	DV_{SS}	P3OUT.0	DV_{SS}	P3IN.0	STE0
P3Sel.4	P3DIR.4	DV_{CC}	P3OUT.4	UTXD0†	P3IN.4	Unused
P3Sel.5	P3DIR.5	DV_{SS}	P3OUT.5	DV_{SS}	P3IN.5	URXD0§
P3Sel.6	P3DIR.6	DV_{CC}	P3OUT.6	UTXD1‡	P3IN.6	Unused
P3Sel.7	P3DIR.7	DV_{SS}	P3OUT.7	DV_{SS}	P3IN.7	URXD1¶

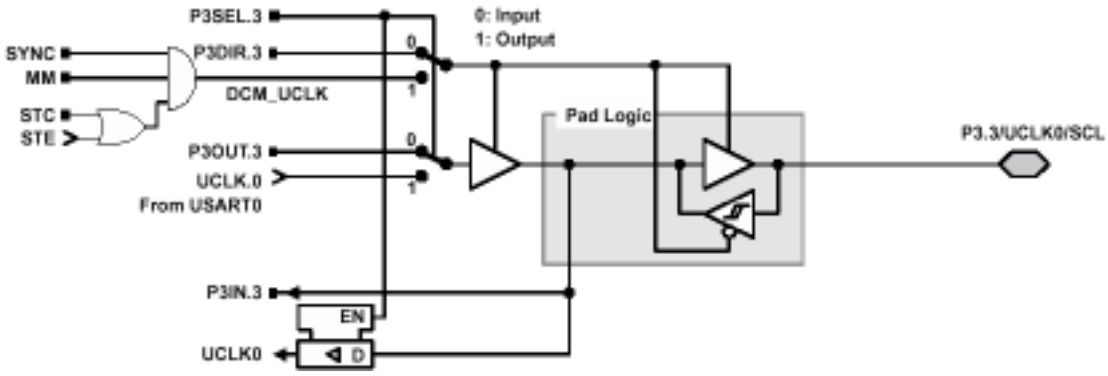
端口 P3，P3.1，带施密特触发器的输入/输出



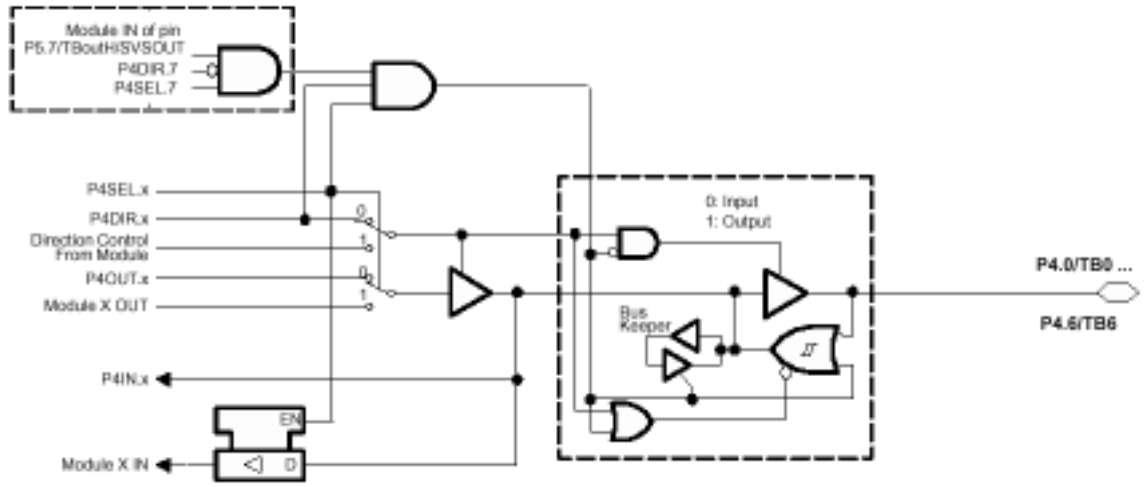
端口 P3，P3.2，带施密特触发器的输入/输出



端口 P3，P3.3，带施密特触发器的输入/输出

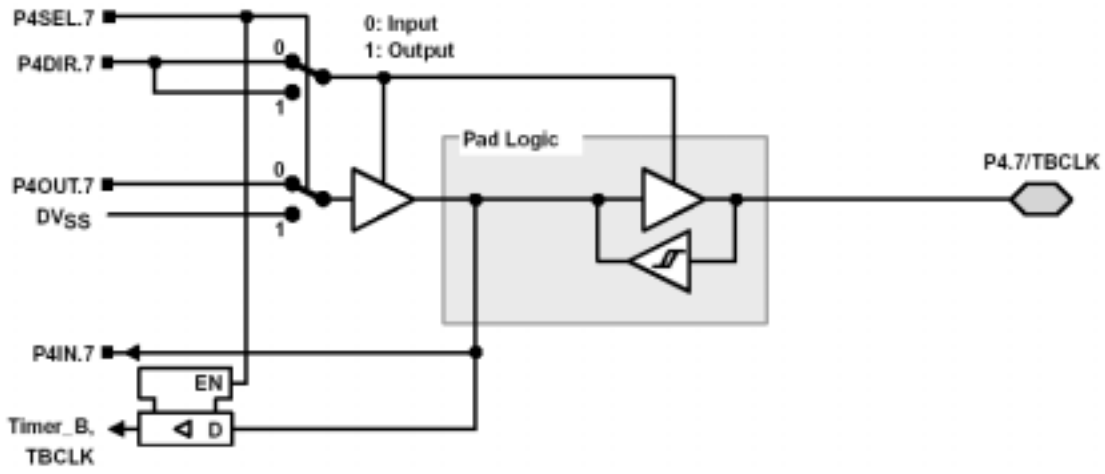


端口 P4，P4.0 到 P4.6，带施密特触发器的输入/输出



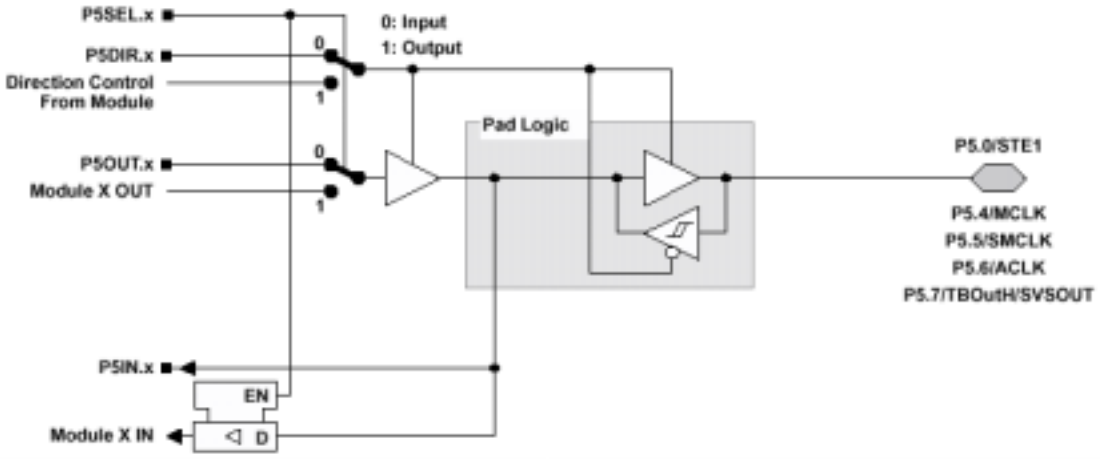
PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P4Sel.0	P4DIR.0	P4DIR.0	P4OUT.0	Out0 signal†	P4IN.0	CCI0A / CCI0B‡
P4Sel.1	P4DIR.1	P4DIR.1	P4OUT.1	Out1 signal†	P4IN.1	CCI1A / CCI1B‡
P4Sel.2	P4DIR.2	P4DIR.2	P4OUT.2	Out2 signal†	P4IN.2	CCI2A / CCI2B‡
P4Sel.3	P4DIR.3	P4DIR.3	P4OUT.3	Out3 signal†	P4IN.3	CCI3A / CCI3B‡
P4Sel.4	P4DIR.4	P4DIR.4	P4OUT.4	Out4 signal†	P4IN.4	CCI4A / CCI4B‡
P4Sel.5	P4DIR.5	P4DIR.5	P4OUT.5	Out5 signal†	P4IN.5	CCI5A / CCI5B‡
P4Sel.6	P4DIR.6	P4DIR.6	P4OUT.6	Out6 signal†	P4IN.6	CCI6A

端口 P4，P4.7，带施密特触发器的输入/输出

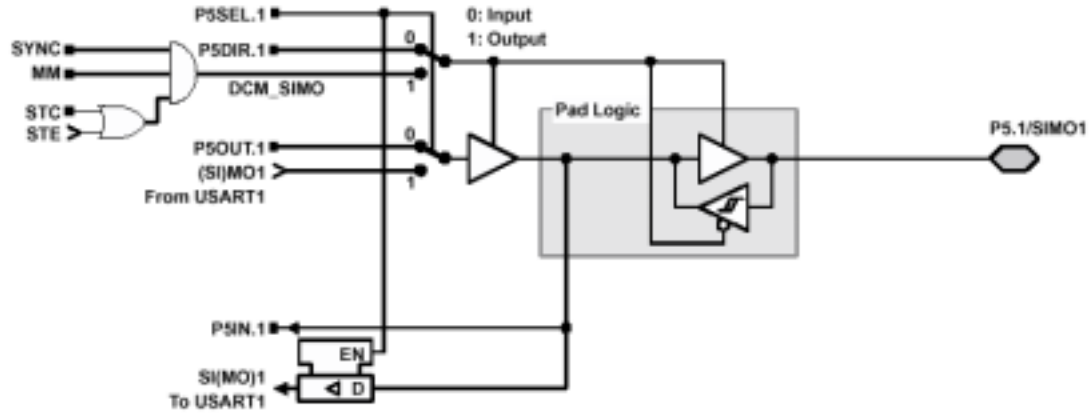


PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P5Sel.0	P5DIR.0	DV_{SS}	P5OUT.0	DV_{SS}	P5IN.0	STE.1
P5Sel.4	P5DIR.4	DV_{CC}	P5OUT.4	MCLK	P5IN.4	unused
P5Sel.5	P5DIR.5	DV_{CC}	P5OUT.5	SMCLK	P5IN.5	unused
P5Sel.6	P5DIR.6	DV_{CC}	P5OUT.6	ACLK	P5IN.6	unused
P5Sel.7	P5DIR.7	DV_{SS}	P5OUT.7	SVSOUT	P5IN.7	TBoutHiZ

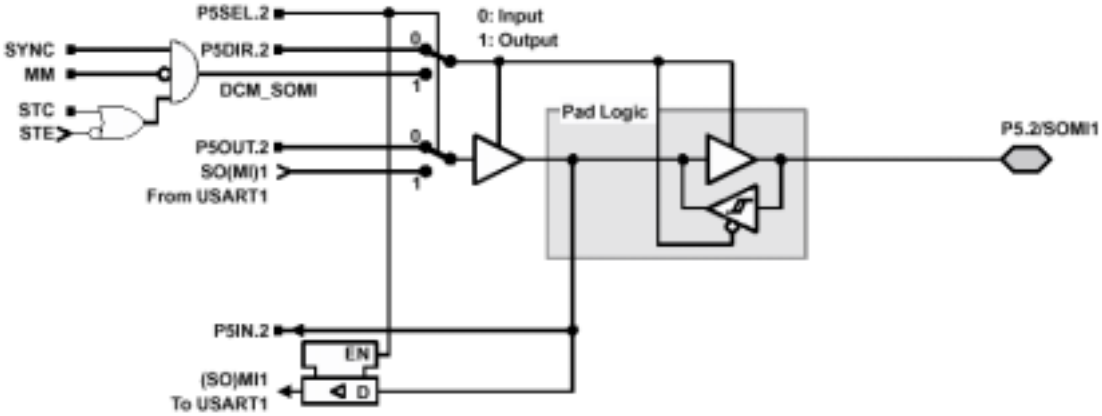
端口 P5，P5.0，P5.4 到 P5.7 带施密特触发器的输入/输出



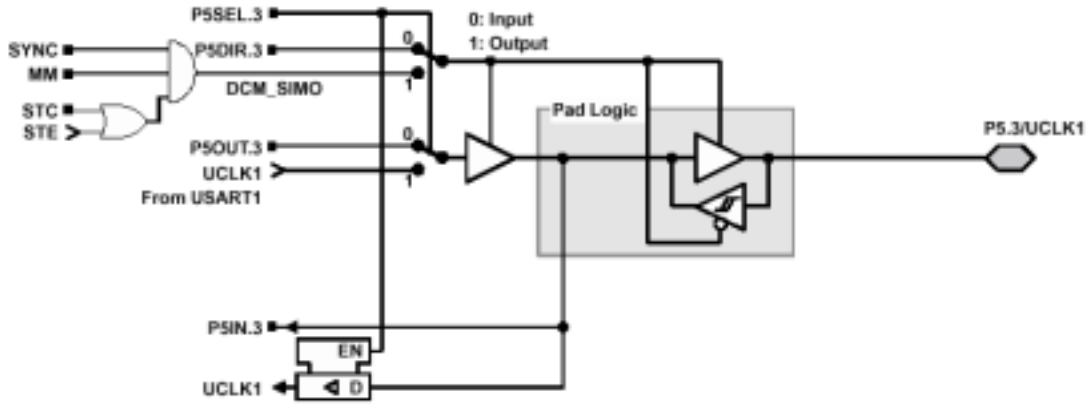
端口 P5，P5.1，带施密特触发器的输入/输出



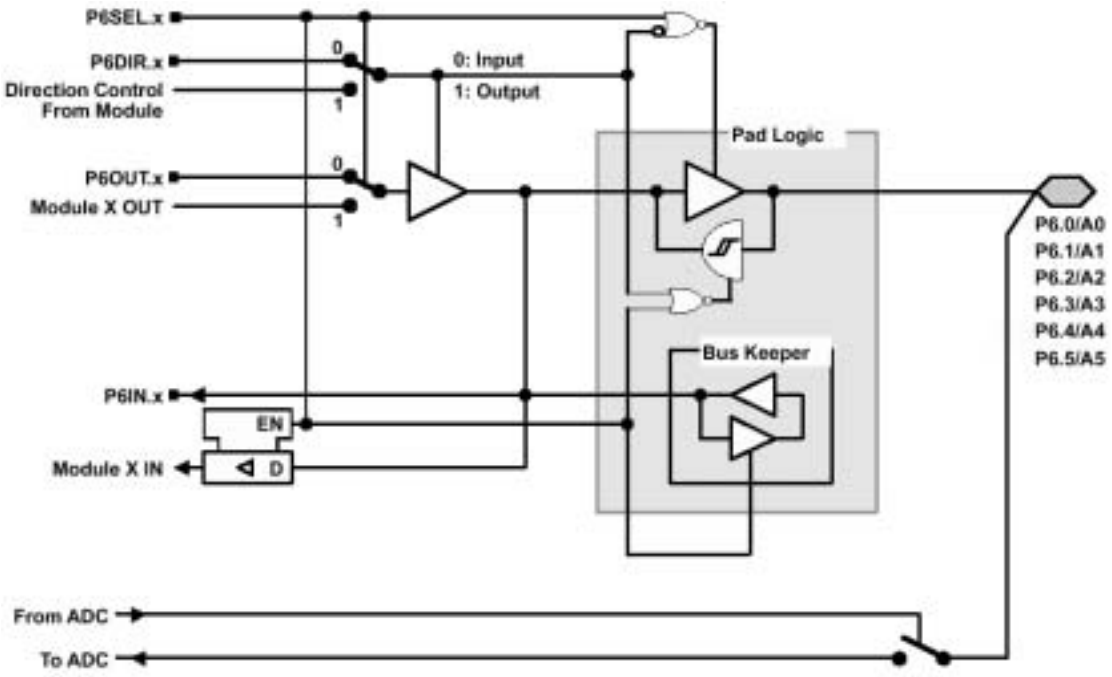
端口 P5，P5.2，带施密特触发器的输入/输出



端口 P5，P5.3，带施密特触发器的输入/输出

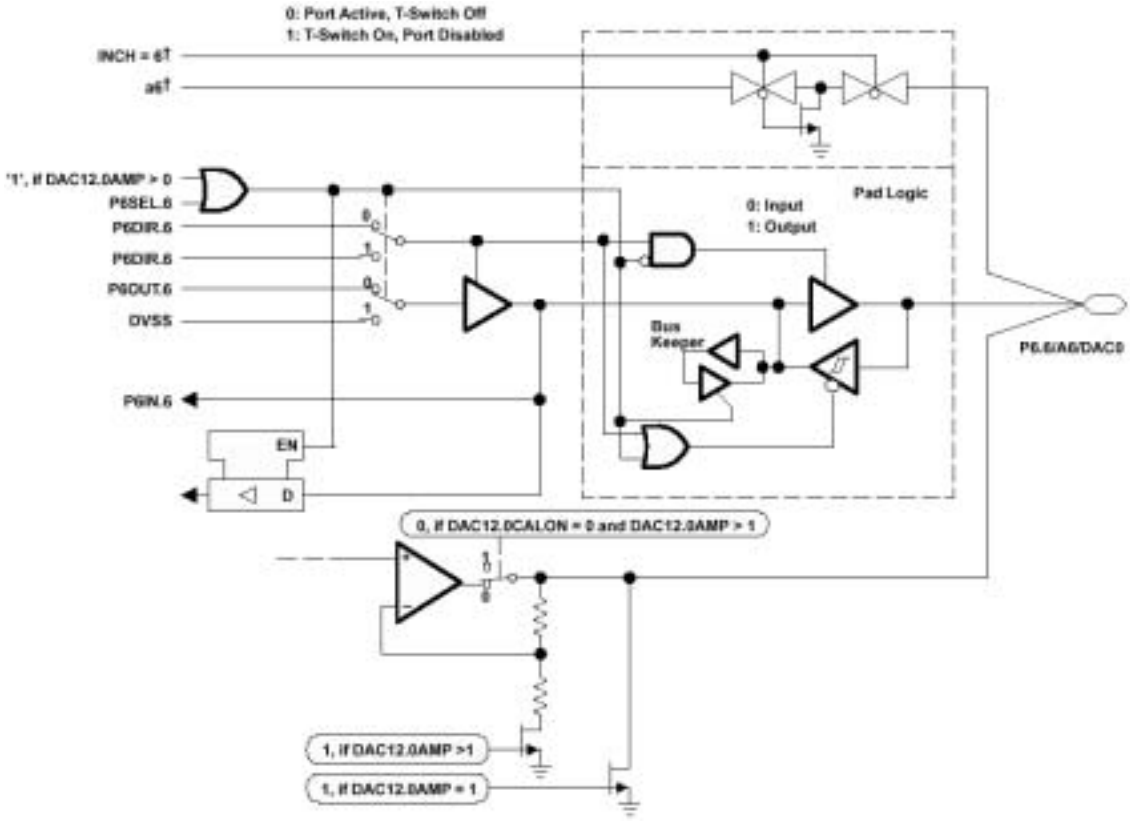


端口 P6，P6.0 到 P6.5，带施密特触发器的输入/输出

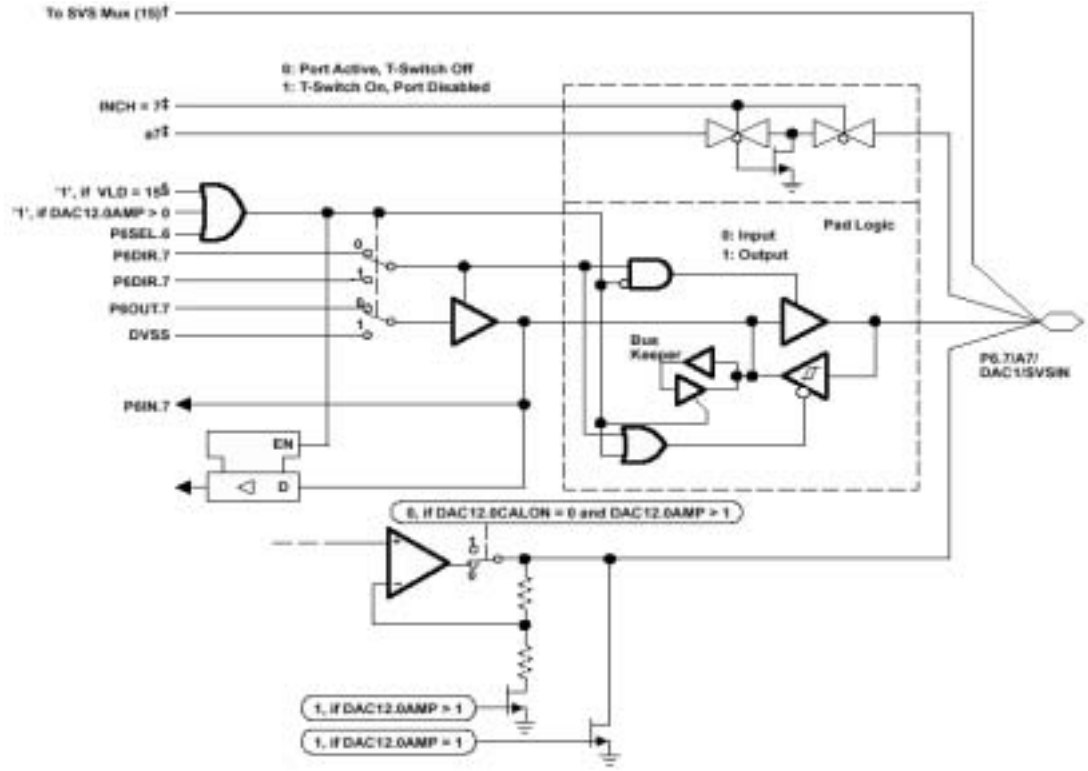


PnSel.x	PnDIR.x	DIR. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P6Sel.0	P6DIR.0	P6DIR.0	P6OUT.0	DV_{SS}	P6IN.0	unused
P6Sel.1	P6DIR.1	P6DIR.1	P6OUT.1	DV_{SS}	P6IN.1	unused
P6Sel.2	P6DIR.2	P6DIR.2	P6OUT.2	DV_{SS}	P6IN.2	unused
P6Sel.3	P6DIR.3	P6DIR.3	P6OUT.3	DV_{SS}	P6IN.3	unused
P6Sel.4	P6DIR.4	P6DIR.4	P6OUT.4	DV_{SS}	P6IN.4	unused
P6Sel.5	P6DIR.5	P6DIR.5	P6OUT.5	DV_{SS}	P6IN.5	unused

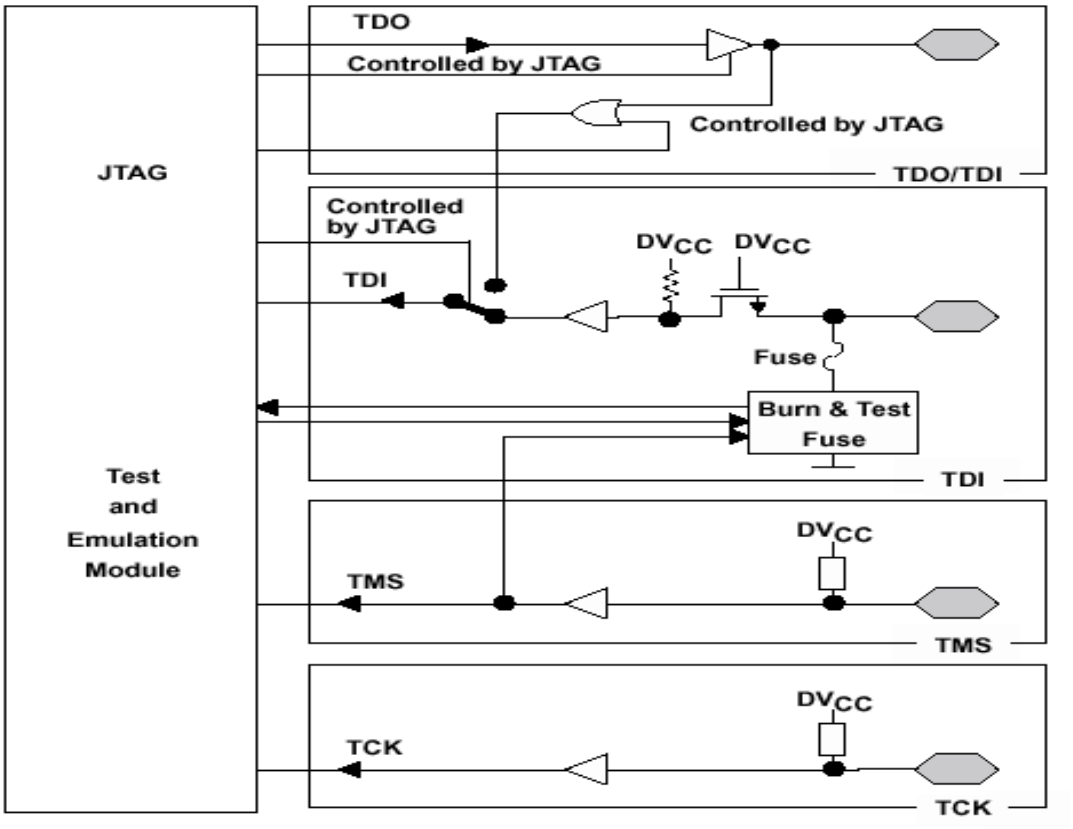
端口 P6，P6.6，带施密特触发器的输入/输出



端口 P6，P6.7，带施密特触发器的输入/输出



JTAG 引脚 TCK、TDI、TMS、TDI/TDO，带施密特触发器的输入/输出



JTAG 熔丝检查模式

MSP430 芯片在 TDI 引脚上有熔丝及在 JTAG 端口在上电复位（POR）后初次处理 JTAG 端口时检测熔丝得连续性的熔丝检查模式。当激活时，熔丝检查电流 ITF，在 3V 时为 1mA，在 5V 时为 2.5mA，如果熔丝没有烧掉将从 TDI 引脚流向地。必须注意避免意外地激活熔丝检查模式而增大整个系统地功耗。熔丝检查模式地激活发生在上电后 TMS 引脚的第一个下降沿或者上电时 TMS 保持为低。TMS 引脚上的第二个上升沿关闭熔丝检查模式。关闭后，熔丝检查模式保持停止直到发生另一个 POR。

熔丝检查电流仅当熔丝检查模式激活以及 TMS 引脚处于低状态时才流过（见图 23）。因此，额外的电流流过可以通过将 TMS 引脚拉高（缺省条件）避免。

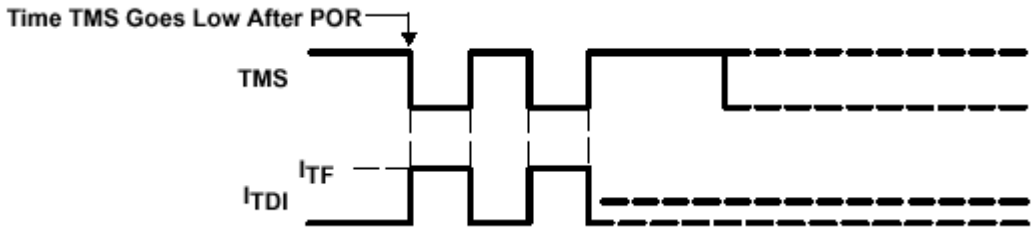


图 23 熔丝检查模式电流 MSP430x15/16x/161x