深圳市明微电子有限公司
SM SHENZHEN SUNMOON MICROELECTRONICS CO.,LTD.

地址：深圳市高新技术产业园南区高新南一道国微大厦 5 层
Add： SSMEC Bldg., South Area, Shenzhen High-tech Industrial Park, Shenzhen, P.R.China
电 话 Tel ： 86-755-26983951 传 真 Fax ： 86-755-26991336
邮编 Zip：518057
网址/Web: http://www.chinaasic.com 电子邮件/Email: sunmoon@ssmec.com

一、概述：

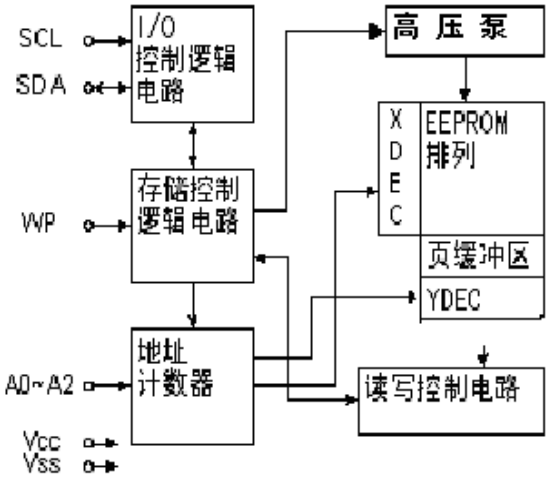
SM24C02 是一种电可擦除只读存储器 (EEPROM)，它内含 256×8 位存储空间，具有工作电压宽，擦写次数多，写入速度快等特点。可多达 8 个该器件同时连接到二线制总线，通过 SDA（串行数据线）及 SCL（串行时钟线）在连接总线上的器件之间传送数据，并根据地址识别每个器件（如：单片机、存储器、LCD 驱动器还是键盘接口）。SM24C02 采用 CMOS 浮栅工艺，内置有高压泵，可在单电压供电条件下工作。该存储器可重复擦写 1 兆次，并有 40 年数据保存功能。应用范围广，如 IC 卡，CPU 卡，解码设备，加密卡，视频处理，移动通信，计算机，自动控制系统等领域都普遍采用此种 I2C 总线接口器件。

二、特点

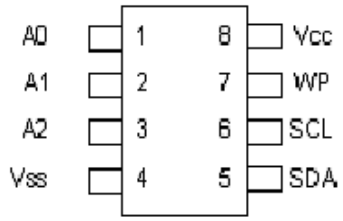
1、 工作电压：5V±10%
2、 低功耗：
最大工作电流：5mA
最大待机电流：5uA
3、 内部存储单元 2K:256*8byte
4、 二线制串行接口
5、 最大写入周期 5ms
6、 自动写前擦除功能
7、 部分页写模式
8、 8 字节页写模式
9、 内置写操作定时器
10、 硬件控制写保护模式
11、 40 年数据保存能力
12、 每字节可重复擦写 1M 次
13、 工作温度：0^{o}C to +70^{o}C
14、 封装形式：**8-pin SOP/DIP**

三、内部结构及引脚定义

内部结构



引脚说明



8 Pin PDIP/SOP

Pin Name	I/O	Description
A0~A2	I	Address inputs
SDA	I/O	Serial data inputs/output
SCL	I	Serial clock data input
WP	I	Write protect
Vss	—	Negative power supply
Vcc	I	Positive power supply

四、工作条件

Operation Temperature(comercial).....0°C to 70°C
Storage Temperature ..... –50°C to 125°C
Applied V_{CC} Voltage with Respect to V_{SS} ..... –0.3V to 6.0V
Applied Voltage on any Pin with Respect to V_{SS} ..... –0.3V to V_{CC}+

五、直流特性（Ta=0°C to 70°C）

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage	—	2.7	—	5.5	V
I_{CC1}	Operating Current	Read at 100KHz	—	—	2	mA
I_{CC2}	Operating Current	Write at 100KHz	—	—	5	mA
V_{IL}	Input Low Voltage	—	–1	—	0.3Vcc	V
V_{IH}	Input High Voltage	—	$0.7V_{CC}$	—	Vcc+0.5	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{LI}	Input Leakage Current	V_{IN}=0 or Vcc	—	—	1	uA

I_{LO}	Output Leakage Current	V_{OUT}=0 or Vcc	—	—	1	uA
I_{STB1}	Standby Current	V_{IN}=0 or Vcc	—	—	5	uA
C_{IN}	Input Capacitance (See Note)	f=1MHz 25°C	—	—	6	pF
C_{OUT}	Output Capacitance (See Note)	f=1MHz 25°C	—	—	8	pF

Note: These parameters are periodically sampled but not 100% tested

六、交流特性（Ta=0°C to 70°C）

Symbol	Parameter	Remark	Vcc=5V+10%		Unit
			Min.	Max.	
f_{SK}	Clock Frequency	—	—	400	KHz
t_{HIGH}	Clock High Time	—	600	—	ns
t_{LOW}	Clock Low Time	—	1200	—	ns
t_R	SDA and SCL Rise Time	Note	—	300	ns
t_F	SDA and SCL Fall Time	Note	—	300	ns
$t_{HD:STA}$	START Condition Hold Time	After this period the first clock pulse is generated	600	—	ns
$t_{SU:STA}$	START Condition Setup Time	Only relevant for repeated START condition	600	—	ns
$t_{HD:DAT}$	Data Input Hold Time	—	0	—	ns
$t_{SU:DAT}$	Data Input Setup Time	—	100	—	ns
$t_{SU:STO}$	STOP Condition Setup Time	—	600	—	ns
t_{AA}	Output Valid from Clock	—	—	900	ns
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	1200	—	ns
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	50	ns
t_{WR}	Write Cycle Time	—	—	5	ms

Notes: These parameters are periodically sampled but not 100% tested; for relative timing, refer to timing diagrams.

七、功能描述

（1）I/O 口说明

- Serial clock (SCL)

The SCL input is used for positive edge clock data into each EEPROM device and negative edge clock data out of each device.

- Serial data (SDA)

The SDA pin is bidirectional for serial data transfer. The pin is open-drain driven and may be wired-OR with any number of other open- drain or open collector devices.

- A0, A1, A2

The A2,A1 and A0 pins are device address inputs that are hard wired for the SM24C02.As many as eight 2K devices may be addressed on a single bus system (The device addressing is discussed in detail under the Device Ad- dressing section).

- Write protect（WP）

The SM24C02 has a write protect pin that provides hardware data protection. The write protect pin allows normal read/write operations when connected to the Vss. When the write protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following table.

WP Pin Status	Protect Array
At Vcc	Full Array (2K)
At Vss	Normal Read/Write Operations

（2）存储单元

- SM24C02,2K Serial EEPROM

Internally organized with 256 8-bit words, the 2K requires an 8-bit data word address for random word addressing.

（3）工作过程

- Clock and data transition

Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is high. Changes in data line while the clock line is high will be interpreted as a START or STOP condition.

- Start condition

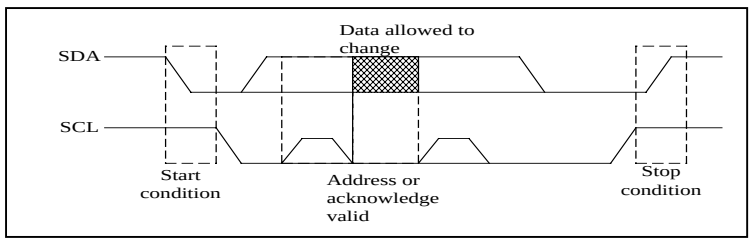
A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Defini- tion Timing diagram).

- Stop condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition Timing Diagram).

- Acknowledge

All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowl- edge that it has received each word. This happens during the ninth clock cycle.



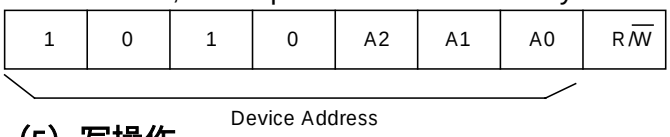
（4）寻址方式

The 2K EEPROM devices require an 8-bit device address word following a start condition to enable the chip for a read or write operation. The device address word consist of a mandatory one, zero sequence for the first four most significant bits (refer to diagram showing the Device Address). This is common to all the EEPROM device.

The next three bits are the A2, A1 and A0 device address bits for the 2K EEPROM. These three bits must compare to their corresponding hard-wired input pins.

The 8th bit of device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

If the comparison of the device address succeed the EEPROM will output a zero at ACK bit. If not, the chip will return to a standby state.



（5）写操作

● Byte write

A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. After receiving the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a micro- controller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle to the non-volatile memory. All inputs are disabled during this write cycle and EEPROM will not respond until the write is completed (refer to Byte write timing).

● Page write

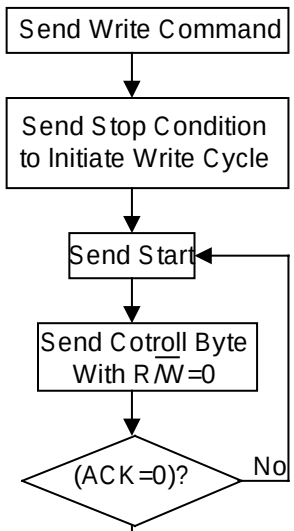
The 2K EEPROM is capable of 8-byte page writes.

A page write is initiated the same as byte write, but the micro controller does not sand a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges the receipt of the first data word, the micro controller can transmit up to seven more data words. The EEPROM will respond with a zero after each data word received. The micro controller must terminate the page write sequence with a stop condition.

The data word address lower three (2K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location (refer to Page write timing).

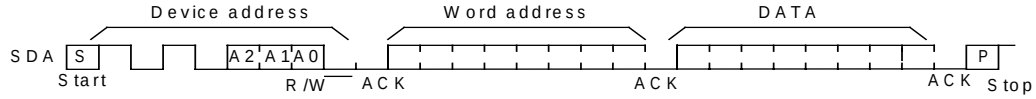
● Acknowledge polling

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a

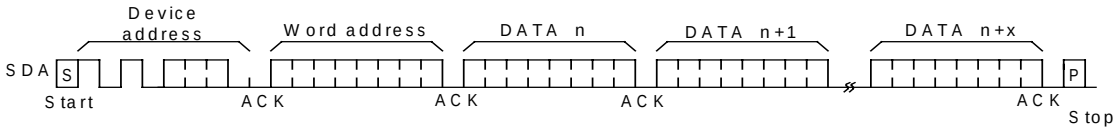


start condition followed by the control byte for a write command (R/W=0).
If the device is still busy with the write cycle, then no ACK will be returned.
If the cycle is completed, then the device will return the ACK and the master can then proceed with the next read or write command.

Byte write timing



Page write timing



● Write protect

The SM24C02 can be used as a serial ROM when the WP pin is connected to Vcc. Pro- gramming will be inhibited and the entire memory will be write protected.

（6）读操作

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

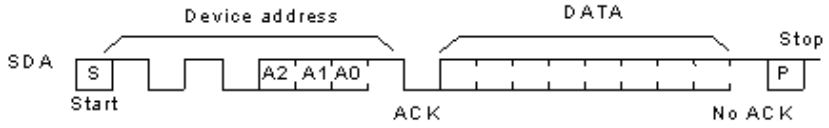
● Current address read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll over during read from the last byte of the last memory page to the first byte of the first page. The address roll over during write from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The micro controller does not respond with an input zero but generates a following stop condition (refer to Current read timing).

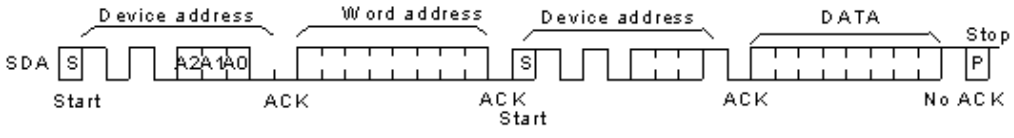
● Random read

A random read requires a dummy byte write sequence to load in the data word address which is then clocked in and acknowledged by the EEPROM. The micro controller must then generate another start condition. The micro controller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The micro controller does not respond with a zero but does generate a following stop condition (refer to Random read timing).

Current read timing



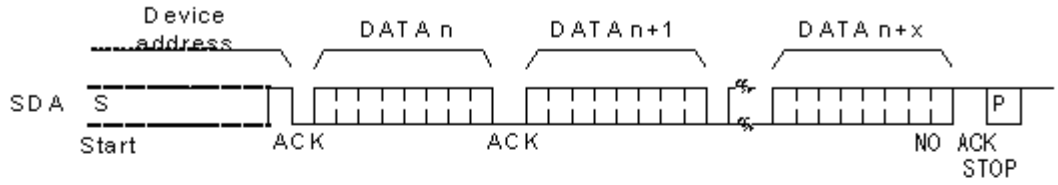
Random read timing



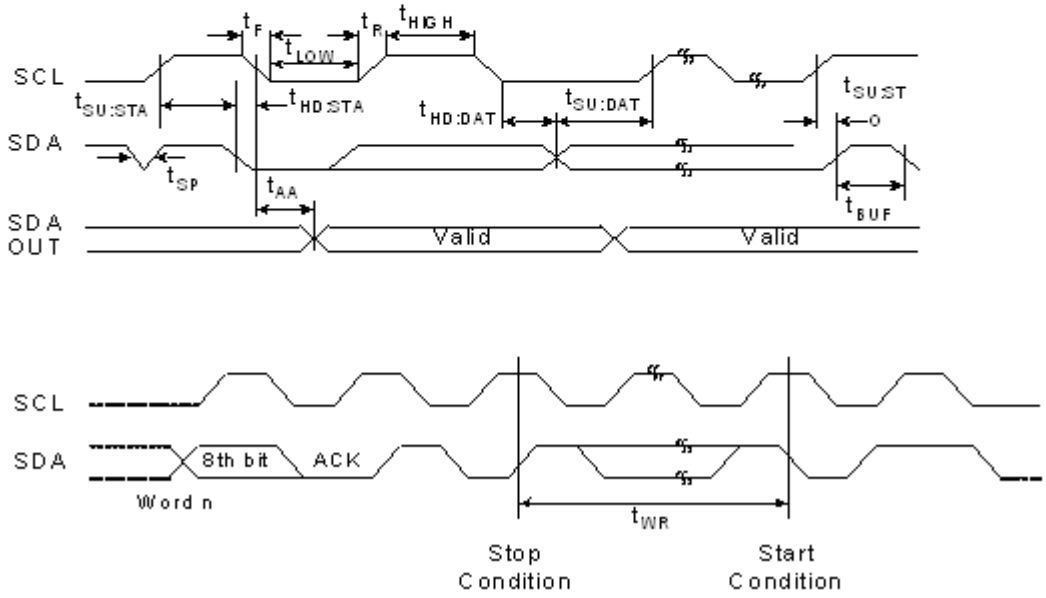
● Sequential read

Sequential reads are initiated by either a current address read or a random address read. After the micro controller receives a data word, it responds with an acknowledgment. As long as the EEPROM receives an acknowledgment, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll over and the sequential read continues. The sequential read operation is terminated when the micro controller does not respond with a zero but generates a following stop condition.

Sequential read timing



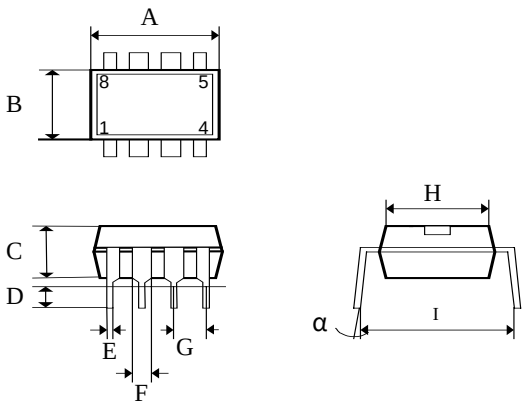
Timing Diagrams



Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the valid start condition of sequential command.

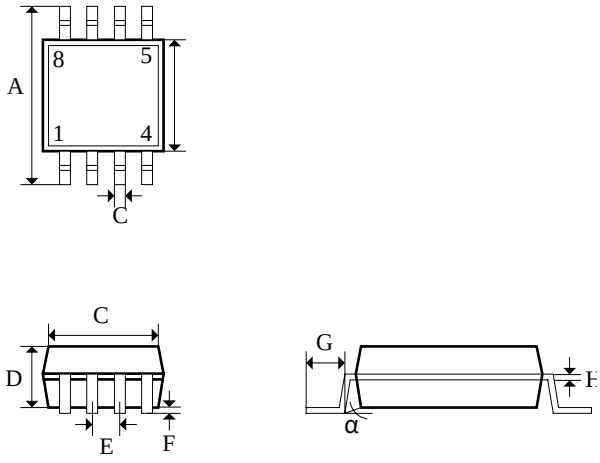
八、封装形式

8-pin DIP (300mil) Outline



Symbol	Dimensions in mil		
	Min.	Nom	Max
A	355	-	375
B	240	-	260
C	125	-	135
D	125	-	145
E	16	-	20
F	50	-	70
G	-	100	-
H	295	-	315
I	335	-	375
α	0°	-	15°

8-pin SOP (150mil) Outline



Symbol	Dimensions in mil		
	Min.	**Nom**	**Max**
A	228	-	244
B	149	-	157
C	14	-	20
C ′	189	-	197
D	53	-	69
E	-	50	-
F	4	-	10
G	22	-	28
H	4	-	12
α	0°	-	10°