MP3 音讯解码芯片

产品介绍

演算 A3200A MP3 音讯解码芯片是针对可携式 MP3 播放器应用市场所研发的高集成度特殊应用音讯处理芯片。演算提供的单一芯片解决方案可支持 MP3、WMA、WAV、AAC 及其它数字音讯格式，并应用在 USB 接口的相关产品。

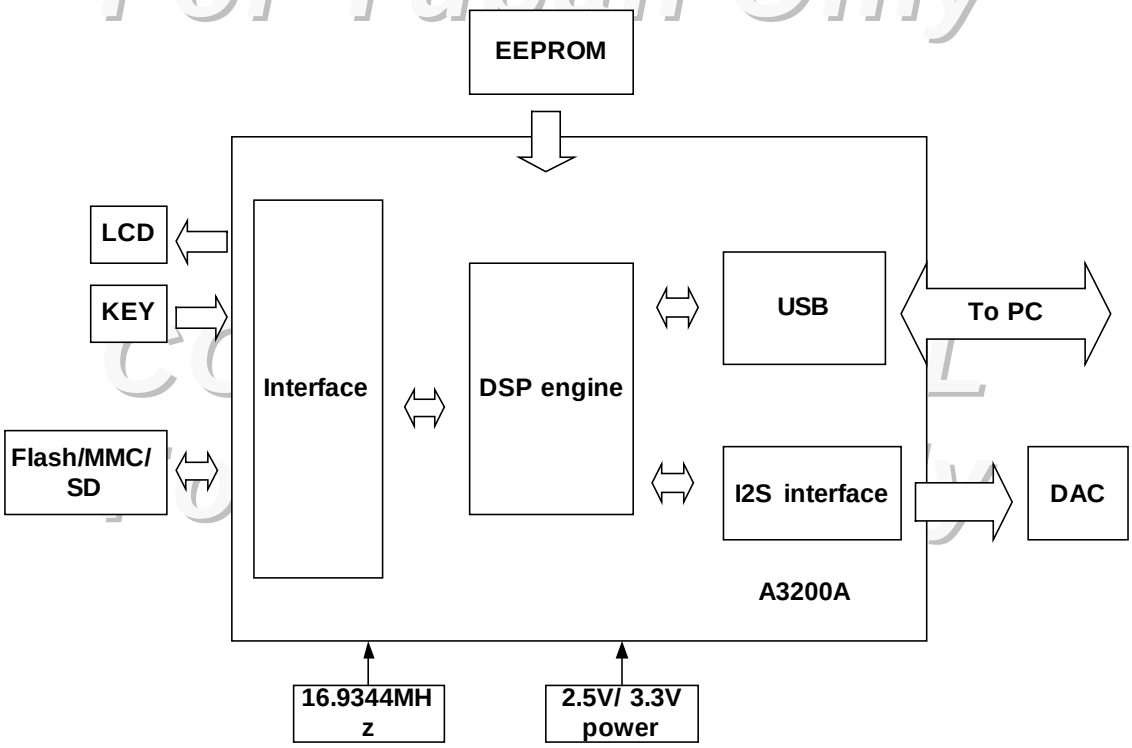
A3200A 解码芯片内建 USB 接口，可直接与电脑连结，以支持 MP3 音乐档案上传及下载至电脑。在闪存应用中，已压缩的 MP3 语音信号数据流可透过电脑 USB 接口下载，并且将档案储存到 PCB 上的闪存芯片中，或者直接储存至可插式多媒体卡(MMC/SD)甚至其它内存装置。A3200A 解码芯片不需特殊应用线路，即可支持最高至 512MB 以上的闪存。A3200A 除了支持闪存及可插式多媒体卡之外，尚提供 LED, LCD, LCM 显示屏幕，按键，开关输入，耳机，麦克风, FM 收音…等应用功能，透过数字模拟转换器即可播放 CD 音质的音乐。

特色

- 具有 MPEG Layer 1, Layer 2, Layer 3 等级之译码功能
- 24 位/80 兆数字讯号处理核心
- 内建数字讯号处理程序内存：16K×16 Byte
- 内建数字讯号处理资料内存：16K×24 Byte
- 內建 USB1.1，提供资料下载及上传功能
- 具有 I^2S 输出格式以接音频数字模拟转换器
- 具有 I^2S 输入格式可作语音录音(选择性)
- 16 bits PCM 资料
- 取样频率：8 - 48 KHz
- 比特率：8K - 320K
- 讯噪比：92dB
- 支持变动位速率（Variable Bit Rate，VBR）
- 外部 ROM 供程序下载，不掉程序
- 毋须额外的开机程序以及闪存接口
- 支持最高至 512MB 以上的闪存
- 支持可插式多媒体卡(MMC/SD)
- 提供直接的数字模拟转换器(DAC)及模拟数字转换器(ADC)接口
- 低操作电流、低闲置电流

- 动态功耗管理
- 核心电压 2.5 伏；外围接口脚位电压 3.3 伏（可依需求微调）
- 制造工艺技术为 0.18 微米至 0.25 微米
- 封装方式:128 个脚位 (LQFP)，可接受客戶需求選擇 100 腳, 80 腳, 64 腳

架构图解



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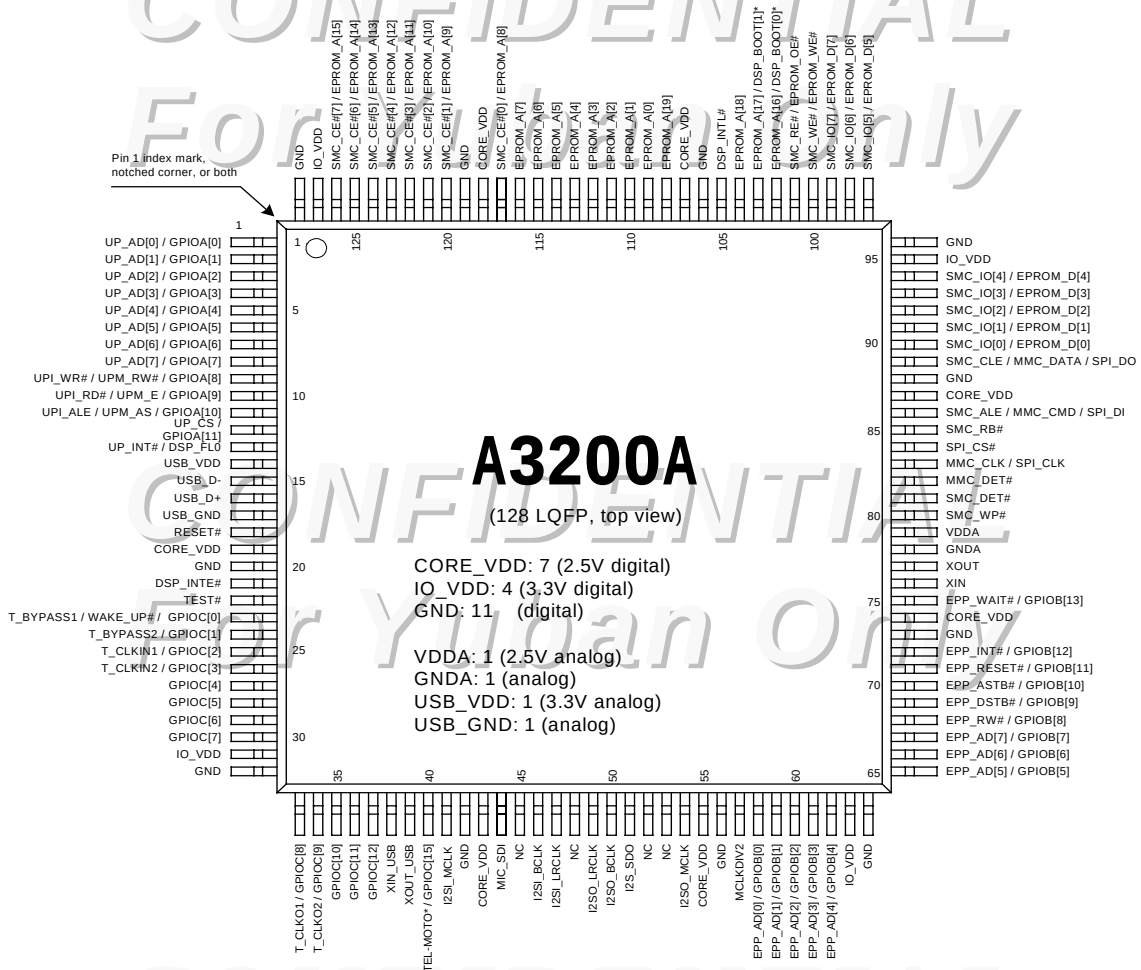
脚位定义图



脚位详叙

注意： I – input, O – output, B – bi-directional, T – tri-state, # low active,
* power-strapping pin

Pin Name	Pin Number	Direction	Description
UP_AD[7:0] / GPIOA[7:0]	8, 7, 6, 5, 4, 3, 2, 1	B / B	µP Address / Data / GPIOA[7:0]
UPI_WR# / UPM_RW# / GPIOA[8]	9	I / I / B	Intel 8051 – WR# - 1: Non-Write 0: Write / Motorola 68HC11 - 1: Read 0: Write / GPIOA[8]
UPI_RD# / UPM_E / GPIOA[9]	10	I / I / B	Intel 8051 – RD# - 1: Non-Read 0: Read / Motorola 68HC11 - 1: Data access 0: Non-Data / GPIOA[9]
UPI_ALE / UPM_AS / GPIOA[10]	11	I / I / B	Intel 8051 – Address Latch Enable / Motorola 68HC11 – Address Select / GPIOA[10]
UP_CS / GPIOA[11]	12	I / B	Chip Select / GPIOA[11]
UP_INT# / DSP_FL0	13	OT / O	Interrupt output to host / DSP core's FL0 output
USB_VDD	14	I	3.3V analog power pin for internal USB transceiver
USB_D-	15	B	USB data signal
USB_D+	16	B	USB data signal
USB_GND	17	I	Analog ground pin for internal USB transceiver
RESET#	18	I	Device reset
CORE_VDD	19	I	2.5V digital power pin for core

GND	20	I	Digital ground pin for core
DSP_INTE#	21	I	DSP edge trigger interrupt
TEST#	22		Set this pin low to move the device into test mode. When in test mode, both PLL clock outputs will be observable from T_CLKO1 and T_CLKO2.
T_BYPASS1 / WAKE_UP# / GPIOC[0]	23	I	DSP PLL bypass enable / Wake-up pin to restart DSP
T_BYPASS2 / GPIOC[1]	24		Audio PLL bypass enable
T_CLKIN1 / GPIOC[2]	25		DSP PLL bypass clock input
T_CLKIN2 / GPIOC[3]	26		Audio PLL bypass clock input
GPIOC[7:4]	30, 29, 28, 27	B	1: Intel 8051 0: Motorola 68HC11
IO_VDD	31	I	3.3V digital power pin for IO pads
GND	32	I	Digital ground pin for IO pads
T_CLKO1 / GPIOC[8]	33		DSP PLL clock out
T_CLKO2 / GPIOC[9]	34		Audio PLL clock out
GPIOC[12:10]	37, 36, 35	B	1: Intel 8051 0: Motorola 68HC11
XIN_USB	38	I	48 MHz crystal (or clock in) for USB
XOUT_USB	39	O	48 MHz crystal for USB
INTEL-MOTO* / GPIOC[15]	40	I	Power-strap pin for µP type 1: Intel 8051 0: Motorola 68HC11
I^2SI_MCLK	41	I	I^2S In – MCLK (CS 8412/8414)
GND	42	I	Digital ground pin for core
CORE_VDD	43	I	2.5V digital power pin for core
MIC_SDI	44	I	MIC – serial data in from ADC

NC	45		
I^2SI_BCLK	46	I	I^2S In – bit clock
I^2SI_LRCLK	47	I	I^2S IN – LEFT/RIGHT CHANNEL CLOCK
NC	48		
I^2SO_LRCLK	49	O	I^2S Out – left/right channel clock
I^2SO_BCLK	50	O	I^2S Out – serial bit clock
I^2S_SDO	51	O	I^2S Out – serial data
NC	53, 52		
I^2SO_MCLK	54	O	I^2S Out – MCLK out to DAC/ADC
CORE_VDD	55	I	2.5V digital power pin for core
GND	56	I	Digital ground pin for core
MCLKDIV2	57	O	I^2S Out – MCLK out divided by 2
EPP_AD[4:0] / GPIOB[4:0]	62, 61, 60, 59, 58	B / B	EPP Address – Data bus / GPIOB[4:0]
IO_VDD	63	I	3.3V digital power pin for IO pads
GND	64	I	Digital ground pin for IO pads
EPP_AD[7:5] / GPIOB[7:5]	67, 66, 65	B / B	EPP Address – Data bus / GPIOB[7:5]
EPP_RW# / GPIOB[8]	68	I / B	EPP Read/Write / GPIOB[8]
EPP_DSTB# / GPIOB[9]	69	I / B	EPP Data Strobe / GPIOB[9]
EPP_ASTB# / GPIOB[10]	70	I / B	EPP Address Strobe / GPIOB[10]
EPP_RESET# / GPIOB[11]	71	I / B	EPP Reset / GPIOB[11]
EPP_INT# / GPIOB[12]	72	O / B	EPP Interrupt / GPIOB[12]
GND	73	I	Digital ground pin for core
CORE_VDD	74	I	2.5V digital power pin for core
EPP_WAIT# /	75	O / B	EPP Wait /

GPIOB[13]			GPIOB[13]
XIN	76	I	Crystal in Pins 76 and 77 are crystal oscillation pads.
XOUT	77	B	Crystal out or external clock input
GNDA	78	I	Analog GND, ground pins for PLL block Do not connect to digital GND.
VDDA	79	I	2.5V analog VDD, power pin for PLL block Do not connect to digital VDD.
SMC_WP#	80	O	Smart Media Flash – Write Protection
SMC_DET#	81	I	Smart Media Flash – Detect
MMC_DET#	82	I	Multi-Media Card – Detect
MMC_CLK / SPI_CLK	83	O	Multi-Media Card Clock / SPI Clock
SPI_CS#	84	O	SPI Chip Select
SMC_RB#	85	I	Smart Media Flash – Ready/Busy
SMC_ALE / MMC_CMD / SPI_DI	86	O / B / I	Smart Media Flash – Address Latch Enable / Multi-Media Card – serial command in/out / SPI serial data in
CORE_VDD	87	I	2.5V digital power pin for core
GND	88	I	Digital ground pin for core
SMC_CLE / MMC_DATA / SPI_DO	89	O / B / O	Smart Media Flash – Command Latch Enable / Multi-Media Card – serial data in/out / SPI serial data out
SMC_IO[4:0] / EPROM_D[4:0]	94, 93, 92, 91, 90	B / B	Smart Media Flash – IO[4:0] / EPROM Data[4:0]
IO_VDD	95	I	3.3V digital power pin for IO pads
GND	96	I	Digital ground pin for IO pads
SMC_IO[7:5] /	99, 98, 97	B / B	Smart Media Flash – IO[7:5] /

EPROM_D[7:5]			EPROM Data[7:0]
SMC_WE# / EPROM_WE#	100	O / O	Smart Media Flash – Write Enable / EPROM – Write Enable
SMC_RE# / EPROM_OE	101	O / O	Smart Media Flash – Read Enable / EPROM – Output Enable
EPROM_A[17:16] / DSP_BOOT[1:0]*	103, 102	O / I	EPROM Address[17:16] / DSP boot source select[1:0], 00: boot from external byte memory 01: boot from external µP 1x: boot from internal code in PM
EPROM_A[18]	104	O	EPROM Address[18]
DSP_INTL#	105	I	DSP level trigger interrupt
GND	106	I	Digital ground pin for core
CORE_VDD	107	I	2.5V digital power pin for core
EPROM_A[19]	108	O	EPROM Address[19]
EPROM_A[7:0]	116, 115, 114, 113, 112, 111, 110, 109	O	EPROM Address[7:0]
SMC_CE#[0] / EPROM_A [8]	117	O / O	Smart Media Flash – Chip Enable[0] / EPROM Address[8]
CORE_VDD	118	I	2.5V digital power pin for core
GND	119	I	Digital ground pin for core
SMC_CE#[7:1] / EPROM_A [15:9]	126, 125, 124, 123, 122, 121, 120	O / O	Smart Media Flash – Chip Enable[7:1] / EPROM Address[15:9]
IO_VDD	127	I	3.3V digital power pin for IO pads
GND	128	I	Digital ground pin for IO pads

操作环境所需要的绝对最大功率条件值建议

供应电伏范围, VddA (PLL), Vdd (Core+I/O)	2.4V to 4.3V***
输入电伏范围	- 0.3V to 5.5V***
输出电伏范围	- 0.3V to Vdd***
畜电温度 (Tstorage)	- 55°C to 150°C***

***注意:

1) 所有功能所需的最大功率是经过评估而非预期值
2) 所有指定的电压都与 VSS 相关
3) 温度或电压超过绝对最大功率可负荷时可能导致装置永久损坏

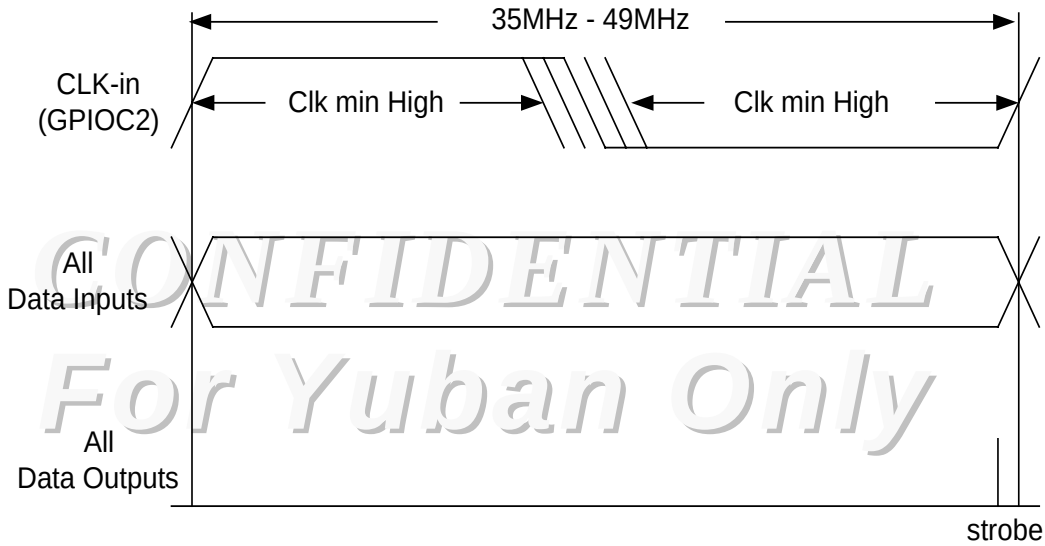
操作环境条件建议

		MIN	NOM	MAX	UNIT
VddA	PLL supply	2.4	2.5 / 3.3	3.6	V
Vdd	Core+I/O supply	2.4	2.5 / 3.3	3.6	V
Vss	Common Ground	0	0	0	V
VIH	High level Input	Vdd/2 +0.3V	Vdd	5.0V	V
VIL	Low level Input	-0.3	0	0.8	V
IOH	High level Output Current			-300	uA
IOL	Low level Output Current	2			mA
VOH	High level Output Voltage	Vdd-0.3			V
VOL	Low level Output Voltage			0.4	V
IIH Vin = Vdd	Input Leakage Current			10	uA
IIL Vin = 0V	Input Leakage Current	-50			uA
Idd (Pll+Core+I/O)	Operating Current at 40MHz Vdd=2.5V & Tj = 35^{o}C			80	mA
Pd (Pll+Core+I/O)	Operating Power at 40MHz, Vdd=2.5V & Tj = 35^{o}C			200	mW
Idds (Pll+Core+I/O)	Power Down Standby @ 2.5V & Tj=35^{o}C			600	uA
Theta-ja	Thermal resistance 0 m/s air flow 1 m/s air flow 2 m/s air flow			 55 45 41	 ^{o}/W ^{o}/W ^{o}/W
Ci	Input capacitance			< 10	pF (DUT only)
Co	Output capacitance			< 10	pF (DUT only)

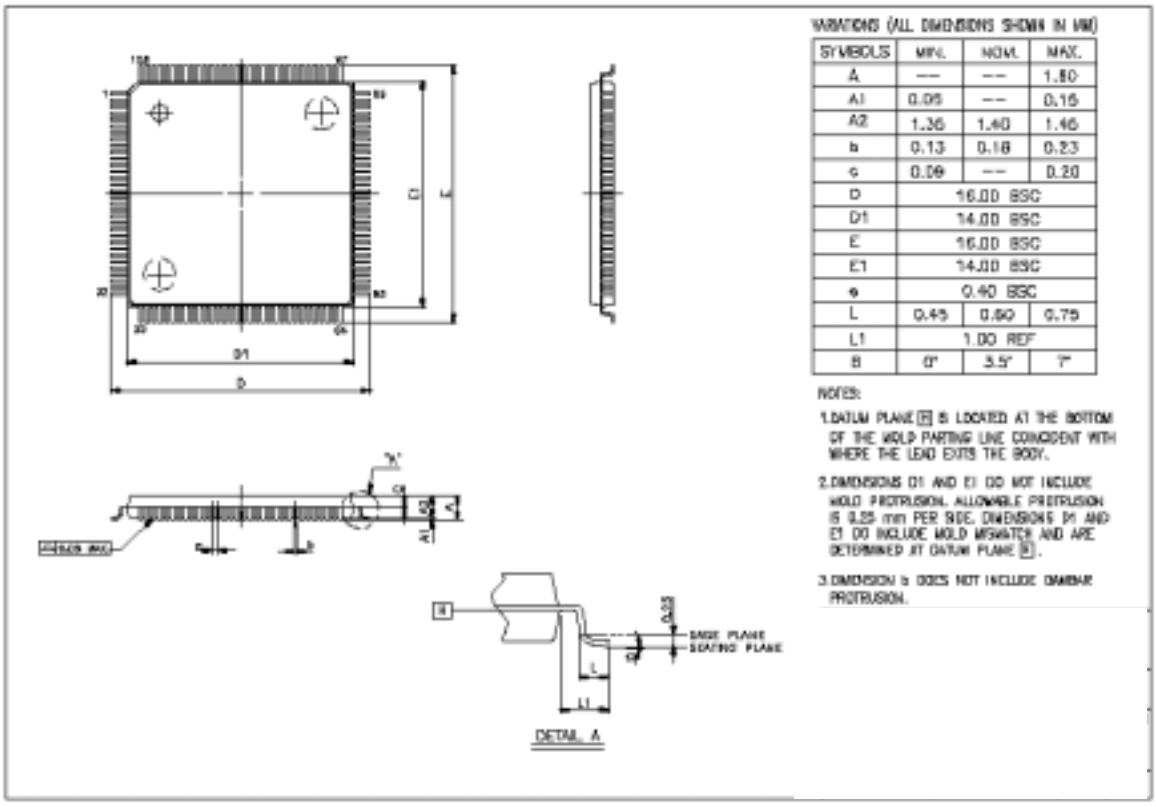
在操作环境下的时序特色

参数:	MIN	NOM	MAX	UNIT
Normal Operating Frequency (PLL driven) - CLKin at Crystal = 16.9445MHz	35	40	49	MHz
Test-Mode Operating Frequency - CLKin at GPIOC2 input	35	40	49	MHz
Tsu (1) Valid Data to CLK Rising		0		nS
Tsu (2) Valid Data to CLK Falling		Tcy/2		nS
Tpd (1) CLK Falling to Compare Strobe		Tcy		nS
CLKh Min-CLK-high	8			nS
CLKl Min-CLK-low	8			nS

在測試模式上的運作時序



封装大小规格



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	---	---	1.60
A1	0.05	---	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	---	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

NOTES:

1. DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

产品记号规格定义

标记: 封装正面

公司名/标志:

ATCHIP: 演算科技股份有限公司

产品型号:

A3200A:

A = 公司英文名称的第一个字母 (AT CHIP Co,)

3 = 多媒体类 IC

2 = CMOS 制程技术

0 = MP3 子类别 IC

0 = 产品序号

A = 设计修正版本

日期编码:

0420 :

04 = 2004 年

20 = 周数

销售服务点

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