Cyclone Device Handbook, Volume 2

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Contents

Chapter 6. Package Information for Cyclone Devices

Chapter 7. Designing with FineLine BGA Packages

Chapter Revision Dates

The chapters in this book, *Cyclone Device Handbook, Volume 2*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Cyclone EP1C3T100 Device Pin Information
Revised: *May 2003*
Part number: *C52001-1.0*

Chapter 2. Cyclone EP1C3T144 Device Pin Information
Revised: *May 2003*
Part number: *C52002-1.0*

Chapter 3. Cyclone EP1C6 Device Pin Information
Revised: *May 2003*
Part number: *C52003-1.0*

Chapter 4. Cyclone EP1C12 Device Pin Information
Revised: *May 2003*
Part number: *C52004-1.0*

Chapter 5. Cyclone EP1C20 Device Pin Information
Revised: *May 2003*
Part number: *C52005-1.0*

Chapter 6. Package Information for Cyclone Devices
Revised: *May 2003*
Part number: *C52006-1.0*

Chapter 7. Designing with FineLine BGA Packages
Revised: *May 2003*
Part number: *C52007-1.0*

About this Handbook

This handbook provides comprehensive information about the Altera® Cyclone family of devices.

How to Find Information

You can find more information in the following ways:

- The Adobe Acrobat Find feature, which searches the text of a PDF document. Click the binoculars toolbar icon to open the Find dialog box.
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- Numerous links, shown in green text, which allow you to jump to related information.

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This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Section I. PCB Layout Guidelines

This section provides information for board layout designers to successfully layout their boards for Cyclone devices. It contains the required PCB layout guidelines, device pin tables, and package specifications.

This section includes the following chapters:

- Chapter 1. Cyclone EP1C3T100 Device Pin Information
- Chapter 2. Cyclone EP1C3T144 Device Pin Information
- Chapter 3. Cyclone EP1C6 Device Pin Information
- Chapter 4. Cyclone EP1C12 Device Pin Information
- Chapter 5. Cyclone EP1C20 Device Pin Information
- Chapter 6. Package Information for Cyclone Devices
- Chapter 7. Designing with FineLine BGA Packages

Revision History

The table below shows the revision history for Chapter 7.

Chapter(s)	Date / Version	Changes Made
12	May 2003 v1.0	Updated Table 7–6.
	v1.03	Updated the "PCB Layout for FineLine BGA Packages" section and Table 7–6.
	v1.02	Minor updates.
	v1.01	Updated Table 7–6.

1. Cyclone EP1C3T100 Device Pin Information

C52001-1.0

Introduction

The following tables contain pin information for the Cyclone EP1C3T100 device, organized into the following sections:

Pin List

Table 1–1 shows the complete pin list for the Cyclone EP1C3T100 device:

Table 1–1. Pin List for the Cyclone EP1C3T100 Device (Part 1 of 5)

Device					Package	DQS for X8 in 100-Pin Thin Quad Flat Pack
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	100-Pin Thin Quad Flat Pack	
IO		INIT_DONE	B1	VREF0B1	1	
IO			B1	VREF0B1	2	
IO		CLKUSR	B1	VREF0B1	3	
IO	VREF0B1		B1	VREF0B1	4	
VCCIO1			B1	VREF0B1		
GND			B1	VREF0B1		
IO	VREF1B1		B1	VREF1B1	5	
IO		nCSO	B1	VREF1B1	6	
DATA0		DATA0	B1	VREF1B1	7	
nCONFIG		nCONFIG	B1	VREF1B1	8	
VCCA_PLL1				VREF1B1	9	
CLK0			B1	VREF1B1	10	
GNDA_PLL1				VREF1B1	11	
nCEO		nCEO	B1	VREF1B1	12	
nCE		nCE	B1	VREF1B1	13	
MSEL0		MSEL0	B1	VREF1B1	14	
MSEL1		MSEL1	B1	VREF1B1	15	
DCLK		DCLK	B1	VREF1B1	16	
IO		ASDO	B1	VREF1B1	17	
VCCIO1			B1	VREF2B1	18	
GND			B1	VREF2B1	19	

Table 1–1. Pin List for the Cyclone EP1C3T100 Device (Part 2 of 5)

Device					Package	DQS for X8 in 100-Pin Thin Quad Flat Pack
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	100-Pin Thin Quad Flat Pack	
IO	VREF2B1		B1	VREF2B1	20	
IO			B1	VREF2B1	21	
IO			B1	VREF2B1	22	
IO			B1	VREF2B1	23	
IO			B1	VREF2B1	24	
IO			B1	VREF2B1	25	
IO			B4	VREF2B4	26	
IO			B4	VREF2B4	27	DQ1B7
IO			B4	VREF2B4	28	DQ1B6
IO			B4	VREF2B4	29	DQ1B5
GND			B4	VREF2B4	30	
VCCIO4			B4	VREF2B4	31	
GND				VREF2B4	32	
VCCINT				VREF2B4	33	
IO	DPCLK7		B4	VREF2B4	34	DQS1B
IO	VREF2B4		B4	VREF2B4	35	
IO			B4	VREF2B4	36	DQ1B4
IO			B4	VREF1B4	37	
IO	VREF1B4		B4	VREF1B4	38	
IO			B4	VREF1B4	39	DM1B
IO			B4	VREF1B4	40	
IO	VREF0B4		B4	VREF0B4	41	
IO	DPCLK6		B4	VREF0B4	42	

Table 1–1. Pin List for the Cyclone EP1C3T100 Device (Part 3 of 5)

Device					Package	DQS for X8 in 100-Pin Thin Quad Flat Pack
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	100-Pin Thin Quad Flat Pack	
GND				VREF0B4	43	
VCCINT				VREF0B4	44	
GND			B4	VREF0B4	45	
VCCIO4			B4	VREF0B4	46	
IO			B4	VREF0B4	47	DQ1B3
IO			B4	VREF0B4	48	DQ1B2
IO			B4	VREF0B4	49	DQ1B1
IO			B4	VREF0B4	50	DQ1B0
IO			B3	VREF2B3	51	
IO			B3	VREF2B3	52	
IO			B3	VREF2B3	53	DQ0R7
IO			B3	VREF2B3	54	DQ0R6
IO			B3	VREF2B3	55	DQ0R5
IO			B3	VREF2B3	56	DQ0R4
IO	VREF2B3		B3	VREF2B3	57	
GND			B3	VREF2B3	58	
VCCIO3			B3	VREF2B3	59	
CONF_DONE		CONF_DONE	B3	VREF1B3	60	
nSTATUS		nSTATUS	B3	VREF1B3	61	
TCK		TCK	B3	VREF1B3	62	
TMS		TMS	B3	VREF1B3	63	
TDO		TDO	B3	VREF1B3	64	
IO			B3	VREF1B3	65	DM0R

Table 1–1. Pin List for the Cyclone EP1C3T100 Device (Part 4 of 5)

Device					Package	DQS for X8 in 100-Pin Thin Quad Flat Pack
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	100-Pin Thin Quad Flat Pack	
CLK2			B3	VREF1B3	66	
TDI		TDI	B3	VREF1B3	67	
IO	VREF1B3		B3	VREF1B3	68	
IO			B3	VREF0B3	69	DQ0R3
IO			B3	VREF0B3	70	DQ0R2
IO			B3	VREF0B3	71	DQ0R1
IO	DPCLK4		B3	VREF0B3	72	DQS0R
GND			B3	VREF0B3		
VCCIO3			B3	VREF0B3		
IO	VREF0B3		B3	VREF0B3	73	
IO			B3	VREF0B3	74	DQ0R0
IO			B3	VREF0B3	75	
IO			B2	VREF0B2	76	DQ1T0
IO			B2	VREF0B2	77	DQ1T1
IO			B2	VREF0B2	78	DQ1T2
IO			B2	VREF0B2	79	DQ1T3
VCCIO2			B2	VREF0B2	80	
GND			B2	VREF0B2	81	
VCCINT				VREF0B2	82	
GND				VREF0B2	83	
IO	DPCLK3		B2	VREF0B2	84	
IO	VREF0B2		B2	VREF0B2	85	
IO			B2	VREF1B2	86	

Table 1–1. Pin List for the Cyclone EP1C3T100 Device (Part 5 of 5)

Device					Package	DQS for X8 in 100-Pin Thin Quad Flat Pack
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	100-Pin Thin Quad Flat Pack	
IO			B2	VREF1B2	87	
IO	VREF1B2		B2	VREF1B2	88	
IO			B2	VREF1B2	89	
IO			B2	VREF2B2	90	DM1T
IO	VREF2B2		B2	VREF2B2	91	
IO	DPCLK2		B2	VREF2B2	92	DQS1T
VCCINT				VREF2B2	93	
GND				VREF2B2	94	
VCCIO2			B2	VREF2B2	95	
GND			B2	VREF2B2	96	
IO			B2	VREF2B2	97	DQ1T4
IO			B2	VREF2B2	98	DQ1T5
IO		DEV_OE	B2	VREF2B2	99	DQ1T6
IO		DEV_CLRn	B2	VREF2B2	100	DQ1T7

Pin Definitions

Table 1–2 shows pin definitions for the EP1C3T100 device.

Table 1–2. Pin Definitions for the Cyclone EP1C3T100 Device (Part 1 of 3)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
Supply and Reference Pins		
VCCIO[1..4]	Power	These are I/O supply voltage pins for banks 1 through 4. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, and 3.3-V PCI I/O standards.
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, SSTL2, and SSTL3 I/O standards.
VREF[0..2]B[1..4]	I/O, Input	Input reference voltage for banks 1-4. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
VCCA_PLL[1..2]	Power	Analog power for PLLs[1..2]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1..2]	Ground	Analog ground for PLLs[1..2]. The designer can connect this pin to the GND plane on the board.
Configuration and JTAG Pins		
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input (PS mode), Output (AS mode)	In passive serial configuration mode, DCLK is a clock input used to clock configuration data from an external source into the Cyclone device. In active serial configuration mode, DCLK is a clock output from the Cyclone device (the Cyclone device acts as master in this mode). This is a dedicated pin used for configuration.
DATA0	Input	Dedicated configuration data input pin.

Table 1–2. Pin Definitions for the Cyclone EP1C3T100 Device (Part 2 of 3)		
Pin Name	**Pin Type (1st, 2nd, & 3rd Function)**	**Pin Description**
nCE	Input	Active-low chip enable. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
ASDO	I/O, Output	Active serial data output from the Cyclone device. This output pin is utilized during active serial configuration mode. The Cyclone device controls configuration and drives address and control information out on ASDO. In passive serial configuration, this pin is available as a user I/O pin.
nCSO	I/O, Output	Chip select output that enables/disables a serial configuration device. This output is utilized during active serial configuration mode. The Cyclone device controls configuration and enables the serial configuration device by driving nCSO low. In passive serial configuration, this pin is available as a user I/O pin.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. This pin can be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Dual-purpose pin that can override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the design.
DEV_OE	I/O, Input	Dual-purpose pin that can override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
MSEL[1..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG output pin.

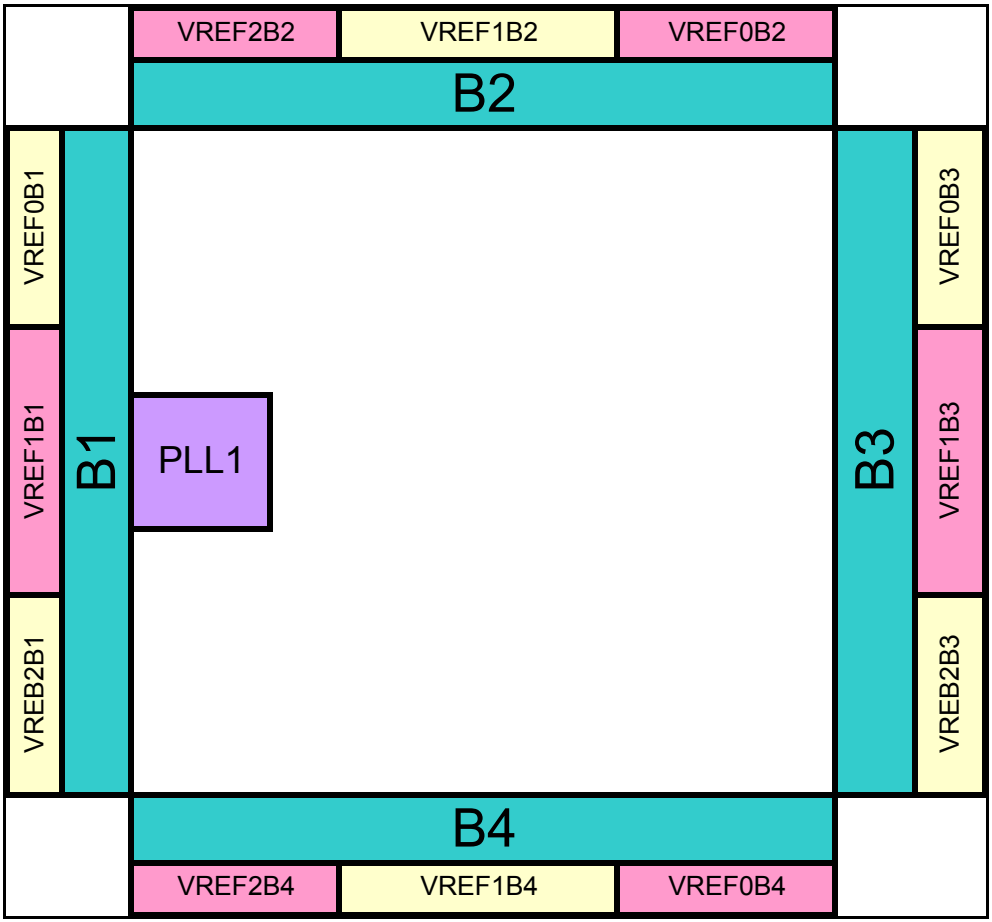
Table 1–2. Pin Definitions for the Cyclone EP1C3T100 Device (Part 3 of 3)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
Clock and PLL Pins		
CLK0	Input	Dedicated global clock input. The dual-function of CLK0 is LVDSCLK1p, which is used for differential input to PLL1.
CLK2	Input	Dedicated global clock input. The dual-function of CLK2 is LVDSCLK2p, which is used for differential input to PLL2.
DPCLK[7..0]	I/O	Dual-purpose clock pins that can connect to the global clock network. These pins can be used for high fan-out control signals, such as clocks, clears, IRDY, TRDY, or DQS signals. These pins are also available as user I/O pins.
Dual-Purpose External Memory Interface Pins		
DQS[0..1][L,R,T,B]	I/O	Optional data strobe signal for use in external memory interfacing. These pins also function as DPCLK pins; therefore, the DQS signals can connect to the global clock network. A programmable delay chain is used to shift the DQS signals by 90 or 72 degrees.
DQ[0..7][L,R,T,B]	I/O	Optional data signal for use in external memory interfacing.
DM[0..1][L,R,T,B]	I/O	Optional data mask output signal for use in external memory interfacing.

PLL & Bank Diagram

Figure 1–1 shows the PLL and Bank locations for the EP1C3T100 device.

Figure 1–1. PLL and Bank Diagram (1), (2)



Notes for Figure 1–1:

(1) This is a top view of the silicon die.

(2) This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and

2. Cyclone EP1C3T144 Device Pin Information

C52002-1.0

Introduction

The following tables contain pin information for the Cyclone EP1C3T144 device, organized into the following sections:

Pin List

Table 2–1 shows the complete pin list for the Cyclone EP1C3T144 device:

Table 2–1. Pin List for the Cyclone EP1C3T144 Device (Part 1 of 7)

Device					Package	DQS for X8 in 144-Pin Thin Quad Flat Pack
Pin Name/ Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin Thin Quad Flat Pack	
IO	LVDS4p	INIT_DONE	B1	VREF0B1	1	DM1L
IO	LVDS4n		B1	VREF0B1	2	DQ1L0
IO	LVDS3p	CLKUSR	B1	VREF0B1	3	DQ1L1
IO	LVDS3n		B1	VREF0B1	4	
IO	VREF0B1		B1	VREF0B1	5	
IO	LVDS2p		B1	VREF0B1	6	DQ1L2
IO	LVDS2n		B1	VREF0B1	7	DQ1L3
VCCIO1			B1	VREF0B1	8	
GND			B1	VREF0B1	9	
IO	DPCLK1		B1	VREF0B1	10	
IO	VREF1B1		B1	VREF1B1	11	
IO		nCSO	B1	VREF1B1	12	
DATA0		DATA0	B1	VREF1B1	13	
nCONFIG		nCONFIG	B1	VREF1B1	14	
VCCA_PLL1				VREF1B1	15	
CLK0	LVDSCLK1p		B1	VREF1B1	16	
CLK1	LVDSCLK1n		B1	VREF1B1	17	
GNDA_PLL1				VREF1B1	18	
GNDG_PLL1				VREF1B1	19	
nCEO		nCEO	B1	VREF1B1	20	
nCE		nCE	B1	VREF1B1	21	

Table 2–1. Pin List for the Cyclone EP1C3T144 Device (Part 2 of 7)

Device					Package	DQS for X8 in 144-Pin Thin Quad Flat Pack
Pin Name/ Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin Thin Quad Flat Pack	
MSEL0		MSEL0	B1	VREF1B1	22	
MSEL1		MSEL1	B1	VREF1B1	23	
DCLK		DCLK	B1	VREF1B1	24	
IO		ASDO	B1	VREF1B1	25	
IO	PLL1_OUTp		B1	VREF1B1	26	
IO	PLL1_OUTn		B1	VREF1B1	27	
IO	DPCLK0		B1	VREF2B1	28	DQS1L
VCCIO1			B1	VREF2B1	29	
GND			B1	VREF2B1	30	
IO	VREF2B1		B1	VREF2B1	31	
IO			B1	VREF2B1	32	DQ1L4
IO	LVDS1p		B1	VREF2B1	33	DQ1L5
IO	LVDS1n		B1	VREF2B1	34	DQ1L6
IO	LVDS0p		B1	VREF2B1	35	DQ1L7
IO	LVDS0n		B1	VREF2B1	36	
IO	LVDS33p		B4	VREF2B4	37	
IO	LVDS33n		B4	VREF2B4	38	
IO	LVDS32p		B4	VREF2B4	39	DQ1B7
IO	LVDS32n		B4	VREF2B4	40	DQ1B6
IO	LVDS31p		B4	VREF2B4	41	DQ1B5
IO	LVDS31n		B4	VREF2B4	42	DQ1B4
GND			B4	VREF2B4	43	
VCCIO4			B4	VREF2B4	44	

Table 2–1. Pin List for the Cyclone EP1C3T144 Device (Part 3 of 7)

Device					Package	DQS for X8 in 144-Pin Thin Quad Flat Pack
Pin Name/ Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin Thin Quad Flat Pack	
GND				VREF2B4	45	
VCCINT				VREF2B4	46	
IO	DPCLK7		B4	VREF2B4	47	DQS1B
IO	VREF2B4		B4	VREF2B4	48	
IO			B4	VREF2B4	49	
IO	LVDS30p		B4	VREF2B4	50	
IO	LVDS30n		B4	VREF2B4	51	
IO	LVDS29p		B4	VREF1B4	52	
IO	LVDS29n		B4	VREF1B4	53	
IO	LVDS28p		B4	VREF1B4	54	
IO	LVDS28n		B4	VREF1B4	55	
IO	VREF1B4		B4	VREF1B4	56	
IO	LVDS27p		B4	VREF1B4	57	DM1B
IO	LVDS27n		B4	VREF1B4	58	
IO	LVDS26p		B4	VREF1B4	59	
IO	LVDS26n		B4	VREF0B4	60	
IO	VREF0B4		B4	VREF0B4	61	
IO	DPCLK6		B4	VREF0B4	62	
GND				VREF0B4	63	
VCCINT				VREF0B4	64	
GND			B4	VREF0B4	65	
VCCIO4			B4	VREF0B4	66	
IO	LVDS25p		B4	VREF0B4	67	DQ1B3

Table 2–1. Pin List for the Cyclone EP1C3T144 Device (Part 4 of 7)

Device					Package	DQS for X8 in 144-Pin Thin Quad Flat Pack
Pin Name/ Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin Thin Quad Flat Pack	
IO	LVDS25n		B4	VREF0B4	68	DQ1B2
IO	LVDS24p		B4	VREF0B4	69	DQ1B1
IO	LVDS24n		B4	VREF0B4	70	DQ1B0
IO	LVDS23p		B4	VREF0B4	71	
IO	LVDS23n		B4	VREF0B4	72	
IO	LVDS22n		B3	VREF2B3	73	
IO	LVDS22p		B3	VREF2B3	74	
IO	LVDS21n		B3	VREF2B3	75	
IO	LVDS21p		B3	VREF2B3	76	
IO	LVDS20n		B3	VREF2B3	77	DQ1R7
IO	LVDS20p		B3	VREF2B3	78	DQ1R6
IO	VREF2B3		B3	VREF2B3	79	
GND			B3	VREF2B3	80	
VCCIO3			B3	VREF2B3	81	
IO	DPCLK5		B3	VREF2B3	82	DQS1R
IO	LVDS19n		B3	VREF2B3	83	DQ1R5
IO	LVDS19p		B3	VREF2B3	84	DQ1R4
IO			B3	VREF2B3	85	DM1R
CONF_DONE		CONF_DONE	B3	VREF1B3	86	
nSTATUS		nSTATUS	B3	VREF1B3	87	
TCK		TCK	B3	VREF1B3	88	
TMS		TMS	B3	VREF1B3	89	
TDO		TDO	B3	VREF1B3	90	

Table 2–1. Pin List for the Cyclone EP1C3T144 Device (Part 5 of 7)

Device					Package	DQS for X8 in 144-Pin Thin Quad Flat Pack
Pin Name/ Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin Thin Quad Flat Pack	
IO			B3	VREF1B3	91	
CLK3	LVDSCLK2n		B3	VREF1B3	92	
CLK2	LVDSCLK2p		B3	VREF1B3	93	
IO			B3	VREF1B3	94	
TDI		TDI	B3	VREF1B3	95	
IO	VREF1B3		B3	VREF1B3	96	
IO			B3	VREF0B3	97	DQ1R3
IO	LVDS18n		B3	VREF0B3	98	DQ1R2
IO	LVDS18p		B3	VREF0B3	99	DQ1R1
IO	DPCLK4		B3	VREF0B3	100	
GND			B3	VREF0B3	101	
VCCIO3			B3	VREF0B3	102	
IO			B3	VREF0B3	103	DQ1R0
IO	VREF0B3		B3	VREF0B3	104	
IO	LVDS17n		B3	VREF0B3	105	
IO	LVDS17p		B3	VREF0B3	106	
IO	LVDS16n		B3	VREF0B3	107	
IO	LVDS16p		B3	VREF0B3	108	
IO	LVDS15n		B2	VREF0B2	109	
IO	LVDS15p		B2	VREF0B2	110	
IO	LVDS14n		B2	VREF0B2	111	DQ0T0
IO	LVDS14p		B2	VREF0B2	112	DQ0T1
IO	LVDS13n		B2	VREF0B2	113	DQ0T2

Table 2–1. Pin List for the Cyclone EP1C3T144 Device (Part 6 of 7)

Device					Package	DQS for X8 in 144-Pin Thin Quad Flat Pack
Pin Name/ Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin Thin Quad Flat Pack	
IO	LVDS13p		B2	VREF0B2	114	DQ0T3
VCCIO2			B2	VREF0B2	115	
GND			B2	VREF0B2	116	
VCCINT				VREF0B2	117	
GND				VREF0B2	118	
IO	DPCLK3		B2	VREF0B2	119	DQS0T
IO	VREF0B2		B2	VREF0B2	120	
IO	LVDS12n		B2	VREF0B2	121	
IO	LVDS12p		B2	VREF1B2	122	
IO	LVDS11n		B2	VREF1B2	123	DM0T
IO	LVDS11p		B2	VREF1B2	124	
IO	VREF1B2		B2	VREF1B2	125	
IO	LVDS10n		B2	VREF1B2	126	
IO	LVDS10p		B2	VREF1B2	127	
IO	LVDS9n		B2	VREF1B2	128	
IO	LVDS9p		B2	VREF1B2	129	
IO	LVDS8n		B2	VREF2B2	130	
IO	LVDS8p		B2	VREF2B2	131	
IO			B2	VREF2B2	132	
IO	VREF2B2		B2	VREF2B2	133	
IO	DPCLK2		B2	VREF2B2	134	
VCCINT				VREF2B2	135	
GND				VREF2B2	136	

Table 2–1. Pin List for the Cyclone EP1C3T144 Device (Part 7 of 7)

Device					Package	DQS for X8 in 144-Pin Thin Quad Flat Pack
Pin Name/ Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin Thin Quad Flat Pack	
VCCIO2			B2	VREF2B2	137	
GND			B2	VREF2B2	138	
IO	LVDS7n		B2	VREF2B2	139	DQ0T4
IO	LVDS7p		B2	VREF2B2	140	DQ0T5
IO	LVDS6n		B2	VREF2B2	141	DQ0T6
IO	LVDS6p		B2	VREF2B2	142	DQ0T7
IO	LVDS5n	DEV_OE	B2	VREF2B2	143	
IO	LVDS5p	DEV_CLRn	B2	VREF2B2	144	

Pin Definitions

Table 2–2 shows pin definitions for the EP1C3T144 device.

Table 2–2. Pin Definitions for the EP1C3T144 Device (Part 1 of 4)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
Supply and Reference Pins		
VCCIO[1..4]	Power	These are I/O supply voltage pins for banks 1 through 4. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, and 3.3-V PCI I/O standards.
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, SSTL2, and SSTL3 I/O standards.
VREF[0..2]B[1..4]	I/O, Input	Input reference voltage for banks 1-4. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
VCCA_PLL[1..2]	Power	Analog power for PLLs[1..2]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1..2]	Ground	Analog ground for PLLs[1..2]. The designer can connect this pin to the GND plane on the board.
GNDG_PLL[1..2]	Ground	Guard ring ground for PLLs[1..2]. The designer can connect this pin to the GND plane on the board.
Configuration and JTAG Pins		
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input (PS mode), Output (AS mode)	In passive serial configuration mode, DCLK is a clock input used to clock configuration data from an external source into the Cyclone device. In active serial configuration mode, DCLK is a clock output from the Cyclone device (the Cyclone device acts as master in this mode). This is a dedicated pin used for configuration.

Table 2–2. Pin Definitions for the EP1C3T144 Device (Part 2 of 4)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
DATA0	Input	Dedicated configuration data input pin.
nCE	Input	Active-low chip enable. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
ASDO	I/O, Output	Active serial data output from the Cyclone device. This output pin is utilized during active serial configuration mode. The Cyclone device controls configuration and drives address and control information out on ASDO. In passive serial configuration, this pin is available as a user I/O pin.
nCSO	I/O, Output	Chip select output that enables/disables a serial configuration device. This output is utilized during active serial configuration mode. The Cyclone device controls configuration and enables the serial configuration device by driving nCSO low. In passive serial configuration, this pin is available as a user I/O pin.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. This pin can be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Dual-purpose pin that can override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the design.
DEV_OE	I/O, Input	Dual-purpose pin that can override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
MSEL[1..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.

Table 2–2. Pin Definitions for the EP1C3T144 Device (Part 3 of 4)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
TDO	Output	This is a dedicated JTAG output pin.
Clock and PLL Pins		
CLK0	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK0 is LVDSCLK1p, which is used for differential input to PLL1.
CLK1	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK1 is LVDSCLK1n, which is used for differential input to PLL1. The EP1C3T100 does not support this clock pin.
CLK2	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK2 is LVDSCLK2p, which is used for differential input to PLL2.
CLK3	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK3 is LVDSCLK2n, which is used for differential input to PLL2. The EP1C3T100 does not support this clock pin.
DPCLK[7..0]	I/O	Dual-purpose clock pins that can connect to the global clock network. These pins can be used for high fan-out control signals, such as clocks, clears, IRDY, TRDY, or DQS signals. These pins are also available as user I/O pins.
PLL1_OUTp	I/O, Output	External clock output from PLL 1. This pin can be used with differential or single ended I/O standards. If clock output from PLL1 is not used, this pin is available as a user I/O pin. The EP1C3T100 does not support this output pin.
PLL1_OUTn	I/O, Output	Negative terminal for external clock output from PLL1. If the clock output is single ended, this pin is available as a user I/O pin. The EP1C3T100 does not support this output pin.

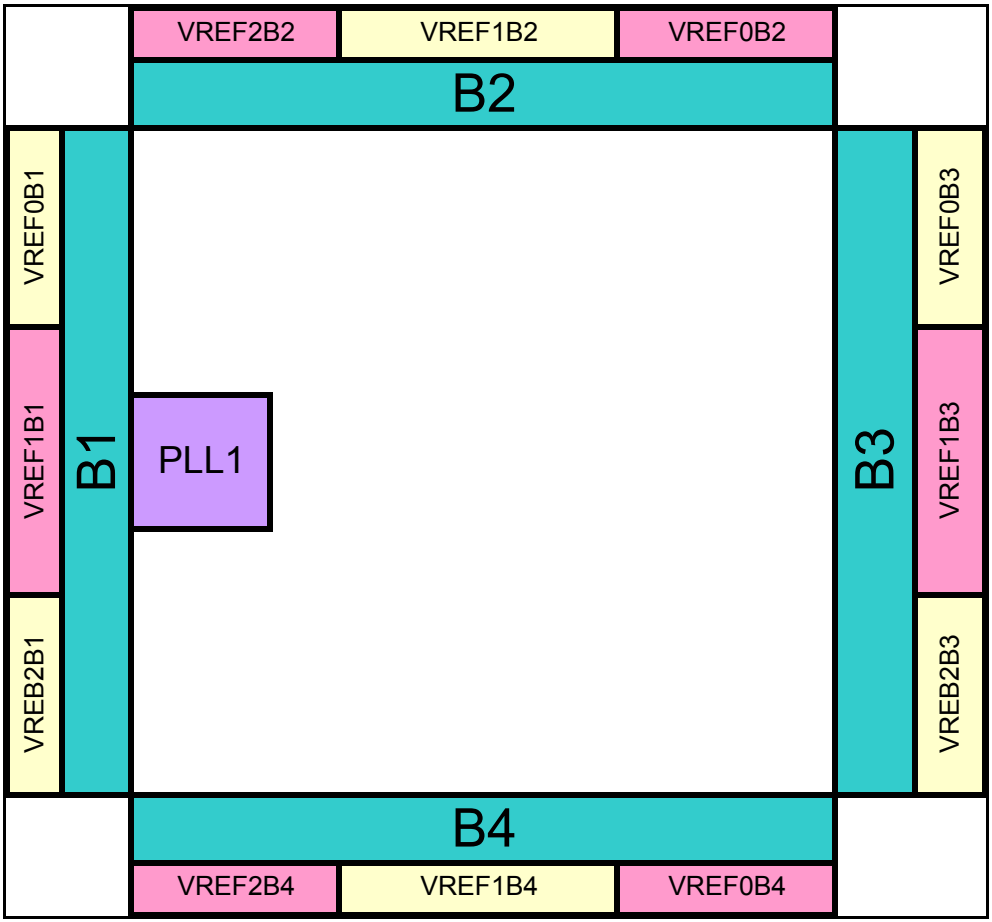
Table 2–2. Pin Definitions for the EP1C3T144 Device (Part 4 of 4)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
Dual-Purpose LVDS & External Memory Interface Pins		
LVDS[0..33]p	I/O, LVDS RX or TX	Dual-purpose LVDS I/O channels 0 to 33. These channels can be used for receiving or transmitting LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for LVDS interfacing, these pins are available as user I/O pins. The EP1C3T100 does not support LVDS I/O interfacing.
LVDS[0..33]n	I/O, LVDS RX or TX	Dual-purpose LVDS I/O channels 0 to 33. These channels can be used for receiving or transmitting LVDS compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for LVDS interfacing, these pins are available as user I/O pins. The EP1C3T100 does not support LVDS I/O interfacing.
LVDSCLK1p	Input, LVDS Input	Dual-purpose LVDS clock input to PLL1. If differential input to PLL1 is not required, this pin is available as the CLK0 input pin.
LVDSCLK1n	Input, LVDS Input	Dual-purpose LVDS clock input to PLL1. If differential input to PLL1 is not required, this pin is available as the CLK1 input pin. The EP1C3T100 does not support this clock pin.
LVDSCLK2p	Input, LVDS Input	Dual-purpose LVDS clock input to PLL2. If differential input to PLL2 is not required, this pin is available as the CLK2 input pin.
LVDSCLK2n	Input, LVDS Input	Dual-purpose LVDS clock input to PLL2. If differential input to PLL2 is not required, this pin is available as the CLK3 input pin. The EP1C3T100 does not support this clock pin.
DQS[0..1][L,R,T,B]	I/O	Optional data strobe signal for use in external memory interfacing. These pins also function as DPCLK pins; therefore, the DQS signals can connect to the global clock network. A programmable delay chain is used to shift the DQS signals by 90 or 72 degrees.
DQ[0..7][L,R,T,B]	I/O	Optional data signal for use in external memory interfacing.
DM[0..1][L,R,T,B]	I/O	Optional data mask output signal for use in external memory interfacing.

PLL & Bank Diagram

Figure 2–1 shows the PLL and Bank locations for the EP1C3T144 device.

Figure 2–1. PLL and Bank Diagram (1), (2)



Notes for Figure 2–1:

(1) This is a top view of the silicon die.

(2) This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and

3. Cyclone EP1C6 Device Pin Information

C52003-1.0

Introduction

The following tables contain pin information for the Cyclone EP1C6 device, organized into the following sections:

Pin List

Table 3–1 shows the complete pin list for the device Cyclone EP1C6 device:

Table 3–1. Pin List for the Cyclone EP1C6 Device (Part 1 of 14)

Device					Package			DQS for X8 in 144-Pin TQFP	DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA			
IO	LVDS14p	INIT_DONE	B1	VREF0B1	1	1	D4	DM1L		
IO	LVDS14n		B1	VREF0B1	2	2	C3	DQ1L0		
IO	LVDS13p	CLKUSR	B1	VREF0B1	3	3	C2	DQ1L1		
IO	LVDS13n		B1	VREF0B1	4	4	B1			
IO	VREF0B1		B1	VREF0B1	5	5	G5			
IO			B1	VREF0B1	6	6	F4	DQ1L2		
IO	LVDS12p		B1	VREF0B1	7	7	D3	DQ1L3	DQ0L0	DQ0L0
IO	LVDS12n		B1	VREF0B1		8	E4		DQ0L1	DQ0L1
VCCIO1			B1	VREF0B1	8	9				
GND			B1	VREF0B1	9	10				
IO	DPCLK1		B1	VREF0B1	10	11	F5		DQS0L	DQS0L
IO	LVDS11p		B1	VREF0B1		12	E3		DQ0L2	DQ0L2
IO	LVDS11n		B1	VREF0B1		13	D2		DQ0L3	DQ0L3
IO	LVDS10p		B1	VREF0B1		14	E2			
IO	LVDS10n		B1	VREF0B1		15	D1			
IO	LVDS9p		B1	VREF0B1		16	F3			
IO	LVDS9n		B1	VREF0B1		17	G3			
IO	LVDS8p		B1	VREF0B1		18	F2			
IO	LVDS8n		B1	VREF0B1		19	E1			
IO	LVDS7p		B1	VREF0B1		20	G2			

Table 3–1. Pin List for the Cyclone EP1C6 Device (Part 2 of 14)

Device					Package			DQS for X8 in 144-Pin TQFP	DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA			
IO	LVDS7n		B1	VREF0B1		21	F1		DM0L	DM0L
VCCIO1			B1	VREF0B1		22				
IO	VREF1B1		B1	VREF1B1	11	23	H5			
IO		nCSO	B1	VREF1B1	12	24	G4			
DATA0		DATA0	B1	VREF1B1	13	25	H2			
nCONFIG		nCONFIG	B1	VREF1B1	14	26	H3			
VCCA_PLL1				VREF1B1	15	27	H6			
CLK0	LVDSCLK1p		B1	VREF1B1	16	28	G1			
CLK1	LVDSCLK1n		B1	VREF1B1	17	29	H1			
GNDA_PLL1				VREF1B1	18	30	J6			
GNDG_PLL1				VREF1B1	19	31	J5			
nCEO		nCEO	B1	VREF1B1	20	32	H4			
nCE		nCE	B1	VREF1B1	21	33	J4			
MSEL0		MSEL0	B1	VREF1B1	22	34	J3			
MSEL1		MSEL1	B1	VREF1B1	23	35	J2			
DCLK		DCLK	B1	VREF1B1	24	36	K4			
IO		ASDO	B1	VREF1B1	25	37	K3			
IO	PLL1_OUTp		B1	VREF1B1	26	38	J1			
IO	PLL1_OUTn		B1	VREF1B1	27	39	K2			
GND			B1	VREF2B1		40				
IO			B1	VREF2B1		41	L3			
IO	LVDS6p		B1	VREF2B1		42	K1			

Table 3–1. Pin List for the Cyclone EP1C6 Device (Part 3 of 14)

Device					Package			DQS for X8 in 144-Pin TQFP	DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA			
IO	LVDS6n		B1	VREF2B1		43	L1			
IO	LVDS5p		B1	VREF2B1		44	L2			
IO	LVDS5n		B1	VREF2B1		45	M1			
IO	LVDS4p		B1	VREF2B1		46	N1			
IO	LVDS4n		B1	VREF2B1		47	M2			
IO	LVDS3p		B1	VREF2B1		48	N2		DQ0L4	DQ0L4
IO	LVDS3n		B1	VREF2B1		49	M3		DQ0L5	DQ0L5
IO	DPCLK0		B1	VREF2B1	28	50	L5	DQS1L		
VCCIO1			B1	VREF2B1	29	51				
GND			B1	VREF2B1	30	52				
IO	LVDS2p		B1	VREF2B1		53	M4		DQ0L6	DQ0L6
IO	LVDS2n		B1	VREF2B1		54	N3		DQ0L7	DQ0L7
IO	VREF2B1		B1	VREF2B1	31	55	K5			
IO			B1	VREF2B1	32	56	L4	DQ1L4		
IO	LVDS1p		B1	VREF2B1	33	57	R1	DQ1L5		
IO	LVDS1n		B1	VREF2B1	34	58	P2	DQ1L6		
IO	LVDS0p		B1	VREF2B1	35	59	P3	DQ1L7		
IO	LVDS0n		B1	VREF2B1	36	60	N4			
IO	LVDS71p		B4	VREF2B4	37	61	R2			
IO	LVDS71n		B4	VREF2B4	38	62	T2			
IO	LVDS70p		B4	VREF2B4		63	R3			
IO	LVDS70n		B4	VREF2B4		64	P4			

Table 3–1. Pin List for the Cyclone EP1C6 Device (Part 4 of 14)

Device					Package			DQS for X8 in 144-Pin TQFP	DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA			
IO	LVDS69p		B4	VREF2B4	39	65	R4	DQ1B7		
IO	LVDS69n		B4	VREF2B4	40	66	T4	DQ1B6		
IO	LVDS68p		B4	VREF2B4	41	67	R5	DQ1B5	DQ1B7	DQ1B7
IO	LVDS68n		B4	VREF2B4	42	68	P5	DQ1B4	DQ1B6	DQ1B6
GND			B4	VREF2B4	43	69				
VCCIO4			B4	VREF2B4	44	70				
GND				VREF2B4	45	71				
VCCINT				VREF2B4	46	72				
IO	DPCLK7		B4	VREF2B4	47	73	M5	DQS1B	DQS1B	DQS1B
IO	VREF2B4		B4	VREF2B4	48	74	M6			
IO	LVDS67p		B4	VREF2B4	49	75	N5			
IO	LVDS67n		B4	VREF2B4		76	N6		DQ1B5	DQ1B5
IO	LVDS66p		B4	VREF2B4		77	P6		DQ1B4	DQ1B4
IO	LVDS66n		B4	VREF2B4		78	R6			
IO			B4	VREF2B4		79	M7			
IO	LVDS65p		B4	VREF2B4		80	T6			
IO	LVDS65n		B4	VREF2B4		81	R7			
IO	LVDS64p		B4	VREF2B4		82	P7			
IO	LVDS64n		B4	VREF2B4		83	N7			
IO	LVDS63p		B4	VREF2B4	50	84	R8			
IO	LVDS63n		B4	VREF2B4	51	85	T8			
IO	LVDS62p		B4	VREF1B4	52	86	N8			

Table 3–1. Pin List for the Cyclone EP1C6 Device (Part 5 of 14)

Device					Package			DQS for X8 in 144-Pin TQFP	DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA			
IO	LVDS62n		B4	VREF1B4	53	87	P8			
IO			B4	VREF1B4		88	M8			
GND				VREF1B4	54	89				
VCCINT				VREF1B4	55	90				
GND			B4	VREF1B4		91				
VCCIO4			B4	VREF1B4		92				
IO	VREF1B4		B4	VREF1B4	56	93	M10			
IO	LVDS61p		B4	VREF1B4	57	94	R9	DM1B	DM1B	DM1B
IO	LVDS61n		B4	VREF1B4	58	95	T9			
IO	LVDS60p		B4	VREF1B4		96	P9			
IO	LVDS60n		B4	VREF1B4		97	N9			
IO	LVDS59p		B4	VREF1B4		98	R10			
IO	LVDS59n		B4	VREF1B4	59	99	T11			
IO	LVDS58p		B4	VREF1B4		100	N10			
IO	LVDS58n		B4	VREF1B4		101	P10			
IO	LVDS57p		B4	VREF0B4		102	R11			
IO	LVDS57n		B4	VREF0B4		103	P11			
IO	LVDS56p		B4	VREF0B4		104	N11			
IO	LVDS56n		B4	VREF0B4		105	N12			
IO			B4	VREF0B4	60	106	M9			
IO	VREF0B4		B4	VREF0B4	61	107	M11			
IO	DPCLK6		B4	VREF0B4	62	108	M12			

Table 3–1. Pin List for the Cyclone EP1C6 Device (Part 6 of 14)

Device					Package			DQS for X8 in 144-Pin TQFP	DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA			
GND				VREF0B4	63	109				
VCCINT				VREF0B4	64	110				
GND			B4	VREF0B4	65	111				
VCCIO4			B4	VREF0B4	66	112				
IO	LVDS55p		B4	VREF0B4	67	113	P12	DQ1B3	DQ1B3	DQ1B3
IO	LVDS55n		B4	VREF0B4	68	114	R12	DQ1B2	DQ1B2	DQ1B2
IO	LVDS54p		B4	VREF0B4	69	115	T13	DQ1B1	DQ1B1	DQ1B1
IO	LVDS54n		B4	VREF0B4	70	116	R13	DQ1B0	DQ1B0	DQ1B0
IO	LVDS53p		B4	VREF0B4		117	R14			
IO	LVDS53n		B4	VREF0B4		118	P13			
IO	LVDS52p		B4	VREF0B4	71	119	T15			
IO	LVDS52n		B4	VREF0B4	72	120	R15			
IO	LVDS51n		B3	VREF2B3	73	121	N13			
IO	LVDS51p		B3	VREF2B3	74	122	P14			
IO	LVDS50n		B3	VREF2B3	75	123	P15			
IO	LVDS50p		B3	VREF2B3	76	124	R16			
IO	LVDS49n		B3	VREF2B3	77	125	N15	DQ1R7	DQ1R7	DQ1R7
IO	LVDS49p		B3	VREF2B3	78	126	N16	DQ1R6		
IO	VREF2B3		B3	VREF2B3	79	127	K12			
IO			B3	VREF2B3		128	K14		DQ1R6	DQ1R6
GND			B3	VREF2B3	80	129				
VCCIO3			B3	VREF2B3	81	130				

Table 3–1. Pin List for the Cyclone EP1C6 Device (Part 7 of 14)

Device					Package			DQS for X8 in 144-Pin TQFP	DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA			
IO	DPCLK5		B3	VREF2B3	82	131	L12	DQS1R	DQS1R	DQS1R
IO	LVDS48n		B3	VREF2B3	83	132	N14	DQ1R5	DQ1R5	DQ1R5
IO	LVDS48p		B3	VREF2B3	84	133	M13	DQ1R4	DQ1R4	DQ1R4
IO	LVDS47n		B3	VREF2B3	85	134	M14	DM1R		
IO	LVDS47p		B3	VREF2B3		135	L13			
IO	LVDS46n		B3	VREF2B3		136	M15			
IO	LVDS46p		B3	VREF2B3		137	M16			
IO	LVDS45n		B3	VREF2B3		138	L14			
IO	LVDS45p		B3	VREF2B3		139	L15			
IO	LVDS44n		B3	VREF2B3		140	L16			
IO	LVDS44p		B3	VREF2B3		141	K16			
GND			B3	VREF2B3		142				
IO	PLL2_OUTn		B3	VREF1B3		143	K15			
IO	PLL2_OUTp		B3	VREF1B3		144	J16			
CONF_DONE		CONF_DONE	B3	VREF1B3	86	145	K13			
nSTATUS		nSTATUS	B3	VREF1B3	87	146	J13			
TCK		TCK	B3	VREF1B3	88	147	J14			
TMS		TMS	B3	VREF1B3	89	148	J15			
TDO		TDO	B3	VREF1B3	90	149	H15			
GNDG_PLL2				VREF1B3	91	150	J12			
GNDA_PLL2				VREF1B3		151	J11			
CLK3	LVDSCLK2n		B3	VREF1B3	92	152	H16			

Table 3–1. Pin List for the Cyclone EP1C6 Device (Part 8 of 14)

Device					Package			DQS for X8 in 144-Pin TQFP	DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA			
CLK2	LVDSCLK2p		B3	VREF1B3	93	153	G16			
VCCA_PLL2				VREF1B3	94	154	H11			
TDI		TDI	B3	VREF1B3	95	155	H14			
IO	VREF1B3		B3	VREF1B3	96	156	H12			
VCCIO3			B3	VREF0B3		157				
IO	LVDS43n		B3	VREF0B3		158	G14		DM1R	DM1R
IO	LVDS43p		B3	VREF0B3		159	G13			
IO	LVDS42n		B3	VREF0B3		160	G15			
IO	LVDS42p		B3	VREF0B3		161	F16			
IO	LVDS41n		B3	VREF0B3		162	F14			
IO	LVDS41p		B3	VREF0B3		163	F13			
IO	LVDS40n		B3	VREF0B3		164	F15			
IO	LVDS40p		B3	VREF0B3		165	E16			
IO	LVDS39n		B3	VREF0B3		166	E15			
IO	LVDS39p		B3	VREF0B3	97	167	D16	DQ1R3		
IO	LVDS38n		B3	VREF0B3	98	168	D15	DQ1R2		
IO	LVDS38p		B3	VREF0B3	99	169	E14	DQ1R1	DQ1R3	DQ1R3
IO	DPCLK4		B3	VREF0B3	100	170	F12			
GND			B3	VREF0B3	101	171				
VCCIO3			B3	VREF0B3	102	172				
IO	LVDS37n		B3	VREF0B3		173	E13		DQ1R2	DQ1R2
IO	LVDS37p		B3	VREF0B3		174	D14		DQ1R1	DQ1R1

Table 3–1. Pin List for the Cyclone EP1C6 Device (Part 9 of 14)

Device					Package			DQS for X8 in 144-Pin TQFP	DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA			
IO			B3	VREF0B3	103	175	H13	DQ1R0	DQ1R0	DQ1R0
IO	VREF0B3		B3	VREF0B3	104	176	G12			
IO	LVDS36n		B3	VREF0B3	105	177	B16			
IO	LVDS36p		B3	VREF0B3	106	178	C15			
IO	LVDS35n		B3	VREF0B3	107	179	C14			
IO	LVDS35p		B3	VREF0B3	108	180	D13			
IO	LVDS34n		B2	VREF0B2	109	181	B15			
IO	LVDS34p		B2	VREF0B2	110	182	A15			
IO	LVDS33n		B2	VREF0B2		183	B14			
IO	LVDS33p		B2	VREF0B2		184	C13			
IO	LVDS32n		B2	VREF0B2	111	185	B13	DQ0T0	DQ0T0	DQ0T0
IO	LVDS32p		B2	VREF0B2	112	186	A13	DQ0T1	DQ0T1	DQ0T1
IO	LVDS31n		B2	VREF0B2	113	187	B12	DQ0T2	DQ0T2	DQ0T2
IO	LVDS31p		B2	VREF0B2	114	188	C12	DQ0T3	DQ0T3	DQ0T3
VCCIO2			B2	VREF0B2	115	189				
GND			B2	VREF0B2	116	190				
VCCINT				VREF0B2	117	191				
GND				VREF0B2	118	192				
IO	DPCLK3		B2	VREF0B2	119	193	E12	DQS0T	DQS0T	DQS0T
IO	VREF0B2		B2	VREF0B2	120	194	E11			
IO			B2	VREF0B2	121	195	E9			
IO	LVDS30n		B2	VREF0B2		196	D12			

Table 3–1. Pin List for the Cyclone EP1C6 Device (Part 10 of 14)

Device					Package			DQS for X8 in 144-Pin TQFP	DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA			
IO	LVDS30p		B2	VREF0B2		197	D11			
IO	LVDS29n		B2	VREF0B2		198	C11			
IO	LVDS29p		B2	VREF0B2		199	B11			
IO	LVDS28n		B2	VREF1B2		200	A11			
IO	LVDS28p		B2	VREF1B2		201	B10			
IO	LVDS27n		B2	VREF1B2	122	202	C10			
IO	LVDS27p		B2	VREF1B2		203	D10			
IO	LVDS26n		B2	VREF1B2		204	A9			
IO	LVDS26p		B2	VREF1B2		205	B9			
IO	LVDS25n		B2	VREF1B2	123	206	D9	DM0T	DM0T	DM0T
IO	LVDS25p		B2	VREF1B2	124	207	C9			
IO	VREF1B2		B2	VREF1B2	125	208	E10			
VCCIO2			B2	VREF1B2		209				
GND			B2	VREF1B2		210				
VCCINT				VREF1B2	126	211				
GND				VREF1B2	127	212				
IO			B2	VREF1B2		213	E8			
IO	LVDS24n		B2	VREF1B2	128	214	C8			
IO	LVDS24p		B2	VREF1B2	129	215	D8			
IO	LVDS23n		B2	VREF2B2	130	216	A8			
IO	LVDS23p		B2	VREF2B2	131	217	B8			
IO	LVDS22n		B2	VREF2B2		218	D7			

Table 3–1. Pin List for the Cyclone EP1C6 Device (Part 11 of 14)

Device					Package			DQS for X8 in 144-Pin TQFP	DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA			
IO	LVDS22p		B2	VREF2B2		219	C7			
IO	LVDS21n		B2	VREF2B2		220	B7			
IO	LVDS21p		B2	VREF2B2		221	A6			
IO			B2	VREF2B2		222	E7			
IO	LVDS20n		B2	VREF2B2		223	B6			
IO	LVDS20p		B2	VREF2B2		224	C6			
IO	LVDS19n		B2	VREF2B2		225	D6			
IO	LVDS19p		B2	VREF2B2	132	226	D5			
IO	VREF2B2		B2	VREF2B2	133	227	E6			
IO	DPCLK2		B2	VREF2B2	134	228	E5			
VCCINT				VREF2B2	135	229				
GND				VREF2B2	136	230				
VCCIO2			B2	VREF2B2	137	231				
GND			B2	VREF2B2	138	232				
IO	LVDS18n		B2	VREF2B2	139	233	C5	DQ0T4	DQ0T4	DQ0T4
IO	LVDS18p		B2	VREF2B2	140	234	B5	DQ0T5	DQ0T5	DQ0T5
IO	LVDS17n		B2	VREF2B2	141	235	A4	DQ0T6	DQ0T6	DQ0T6
IO	LVDS17p		B2	VREF2B2	142	236	B4	DQ0T7	DQ0T7	DQ0T7
IO	LVDS16n		B2	VREF2B2		237	C4			
IO	LVDS16p		B2	VREF2B2		238	B3			
IO	LVDS15n	DEV_OE	B2	VREF2B2	143	239	A2			
IO	LVDS15p	DEV_CLRn	B2	VREF2B2	144	240	B2			

Table 3–1. Pin List for the Cyclone EP1C6 Device (Part 12 of 14)

Device					Package			DQS for X8 in 144-Pin TQFP	DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA			
VCCINT							A7			
VCCINT							A10			
VCCINT							G8			
VCCINT							G10			
VCCINT							H7			
VCCINT							H9			
VCCINT							J8			
VCCINT							J10			
VCCINT							K7			
VCCINT							K9			
VCCINT							T7			
VCCINT							T10			
VCCIO1							C1			
VCCIO1							G6			
VCCIO1							P1			
VCCIO4							T3			
VCCIO4							L7			
VCCIO4							L10			
VCCIO4							T14			
VCCIO3							P16			
VCCIO3							K11			
VCCIO3							C16			

Table 3–1. Pin List for the Cyclone EP1C6 Device (Part 13 of 14)

Device					Package			DQS for X8 in 144-Pin TQFP	DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA			
VCCIO2							A14			
VCCIO2							F10			
VCCIO2							F7			
VCCIO2							A3			
GND							A1			
GND							A16			
GND							A5			
GND							A12			
GND							F6			
GND							F8			
GND							F9			
GND							F11			
GND							G7			
GND							G9			
GND							G11			
GND							H8			
GND							H10			
GND							J7			
GND							J9			
GND							K6			
GND							K8			
GND							K10			

Table 3–1. Pin List for the Cyclone EP1C6 Device (Part 14 of 14)

Device					Package			DQS for X8 in 144-Pin TQFP	DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA			
GND							L6			
GND							L8			
GND							L9			
GND							L11			
GND							T1			
GND							T5			
GND							T12			
GND							T16			

Pin Definitions

Table 3–2 shows pin definitions for the EP1C6 device.

Table 3–2. Pin Definitions for the EP1C6 Device (Part 1 of 4)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
Supply and Reference Pins		
VCCIO[1..4]	Power	These are I/O supply voltage pins for banks 1 through 4. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, and 3.3-V PCI I/O standards.
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, SSTL2, and SSTL3 I/O standards.
VREF[0..2]B[1..4]	I/O, Input	Input reference voltage for banks 1-4. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
VCCA_PLL[1..2]	Power	Analog power for PLLs[1..2]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1..2]	Ground	Analog ground for PLLs[1..2]. The designer can connect this pin to the GND plane on the board.
GNDG_PLL[1..2]	Ground	Guard ring ground for PLLs[1..2]. The designer can connect this pin to the GND plane on the board.
Configuration and JTAG Pins		
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input (PS mode), Output (AS mode)	In passive serial configuration mode, DCLK is a clock input used to clock configuration data from an external source into the Cyclone device. In active serial configuration mode, DCLK is a clock output from the Cyclone device (the Cyclone device acts as master in this mode). This is a dedicated pin used for configuration.

Table 3–2. Pin Definitions for the EP1C6 Device (Part 2 of 4)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
DATA0	Input	Dedicated configuration data input pin.
nCE	Input	Active-low chip enable. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
ASDO	I/O, Output	Active serial data output from the Cyclone device. This output pin is utilized during active serial configuration mode. The Cyclone device controls configuration and drives address and control information out on ASDO. In passive serial configuration, this pin is available as a user I/O pin.
nCSO	I/O, Output	Chip select output that enables/disables a serial configuration device. This output is utilized during active serial configuration mode. The Cyclone device controls configuration and enables the serial configuration device by driving nCSO low. In passive serial configuration, this pin is available as a user I/O pin.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. This pin can be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Dual-purpose pin that can override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the design.
DEV_OE	I/O, Input	Dual-purpose pin that can override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
MSEL[1..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG output pin.

Table 3–2. Pin Definitions for the EP1C6 Device (Part 3 of 4)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
Clock and PLL Pins		
CLK0	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK0 is LVDSCLK1p, which is used for differential input to PLL1.
CLK1	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK1 is LVDSCLK1n, which is used for differential input to PLL1.
CLK2	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK2 is LVDSCLK2p, which is used for differential input to PLL2.
CLK3	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK3 is LVDSCLK2n, which is used for differential input to PLL2.
DPCLK[7..0]	I/O	Dual-purpose clock pins that can connect to the global clock network. These pins can be used for high fan-out control signals, such as clocks, clears, IRDY, TRDY, or DQS signals. These pins are also available as user I/O pins.
PLL1_OUTp	I/O, Output	External clock output from PLL 1. This pin can be used with differential or single ended I/O standards. If clock output from PLL1 is not used, this pin is available as a user I/O pin.
PLL1_OUTn	I/O, Output	Negative terminal for external clock output from PLL1. If the clock output is single ended, this pin is available as a user I/O pin.
PLL2_OUTp	I/O, Output	External clock output from PLL 2. This pin can be used with differential or single ended I/O standards. If clock output from PLL2 is not used, this pin is available as a user I/O pin. The EP1C6T144 does not support this output pin.
PLL2_OUTn	I/O, Output	Negative terminal for external clock output from PLL2. If the clock output is single ended, this pin is available as a user I/O pin. The EP1C6T144 does not support this output pin.
Dual-Purpose LVDS & External Memory Interface Pins		
LVDS[0..71]p	I/O, LVDS RX or TX	Dual-purpose LVDS I/O channels 0 to 71. These channels can be used for receiving or transmitting LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for LVDS interfacing, these pins are available as user I/O pins.

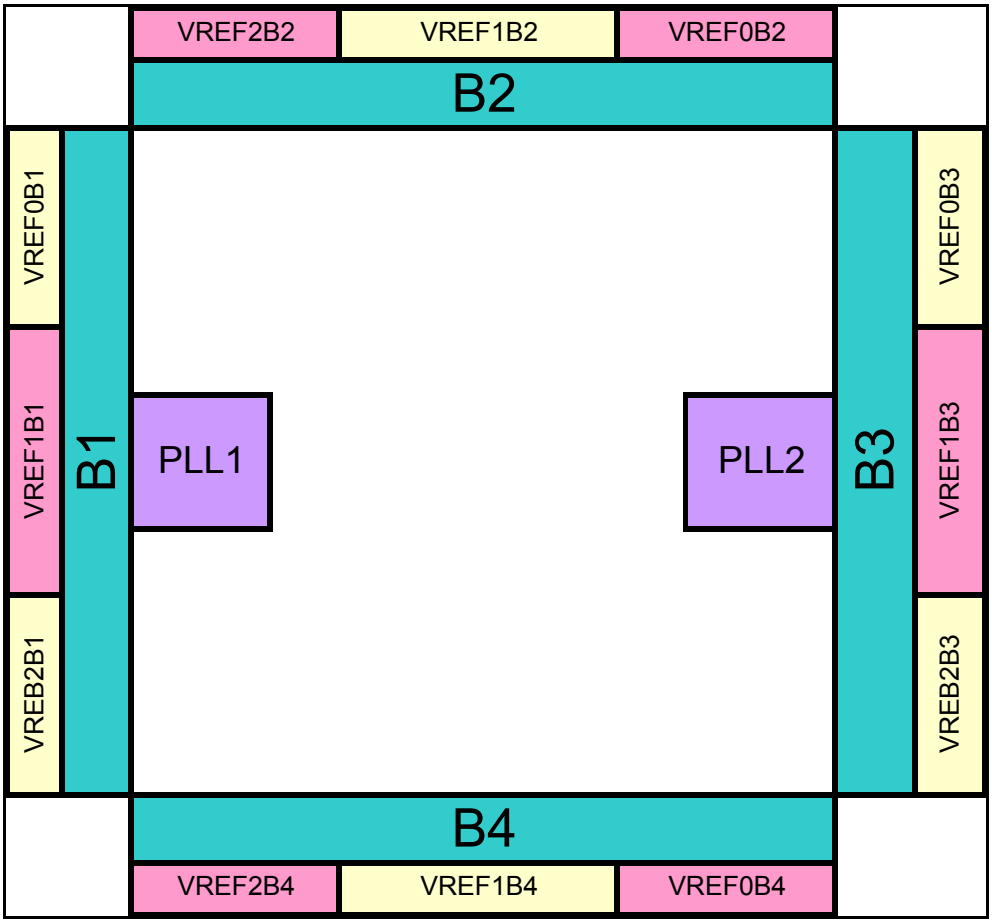
Table 3–2. Pin Definitions for the EP1C6 Device (Part 4 of 4)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
LVDS[0..71]n	I/O, LVDS RX or TX	Dual-purpose LVDS I/O channels 0 to 71. These channels can be used for receiving or transmitting LVDS compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for LVDS interfacing, these pins are available as user I/O pins.
LVDSCLK1p	Input, LVDS Input	Dual-purpose LVDS clock input to PLL1. If differential input to PLL1 is not required, this pin is available as the CLK0 input pin.
LVDSCLK1n	Input, LVDS Input	Dual-purpose LVDS clock input to PLL1. If differential input to PLL1 is not required, this pin is available as the CLK1 input pin.
LVDSCLK2p	Input, LVDS Input	Dual-purpose LVDS clock input to PLL2. If differential input to PLL2 is not required, this pin is available as the CLK2 input pin.
LVDSCLK2n	Input, LVDS Input	Dual-purpose LVDS clock input to PLL2. If differential input to PLL2 is not required, this pin is available as the CLK3 input pin.
DQS[0..1][L,R,T,B]	I/O	Optional data strobe signal for use in external memory interfacing. These pins also function as DPCLK pins; therefore, the DQS signals can connect to the global clock network. A programmable delay chain is used to shift the DQS signals by 90 or 72 degrees.
DQ[0..7][L,R,T,B]	I/O	Optional data signal for use in external memory interfacing.
DM[0..1][L,R,T,B]	I/O	Optional data mask output signal for use in external memory interfacing.

PLL & Bank Diagram

Figure shows the PLL and Bank locations for the EP1C6 device.

Figure 3–1. PLL and Bank Diagram *(1), (2)*



Notes for Figure:
(1) This is a top view of the silicon die.
(2) This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and

4. Cyclone EP1C12 Device Pin Information

C52004-1.0

Introduction

The following tables contain pin information for the Cyclone EP1C12 device, organized into the following sections:

Pin List

Table 4–1 shows the complete pin list for the device Cyclone EP1C12 device:

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 1 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
IO	LVDS23p	INIT_DONE	B1	VREF0B1	1	D4	C3			
IO	LVDS23n		B1	VREF0B1	2	C3	C2			
IO	LVDS22p	CLKUSR	B1	VREF0B1	3	C2	D3			
IO	LVDS22n		B1	VREF0B1	4	B1	D2			
IO	VREF0B1		B1	VREF0B1	5	G5	D4			
IO			B1	VREF0B1	6	F4	D1			
IO	LVDS21p		B1	VREF0B1	7	D3	E3	DQ0L0	DQ0L0	DQ0L0
IO	LVDS21n		B1	VREF0B1	8	E4	E2	DQ0L1	DQ0L1	DQ0L1
VCCIO1			B1	VREF0B1	9					
GND			B1	VREF0B1	10					
IO	DPCLK1		B1	VREF0B1	11	F5	F1	DQS0L	DQS0L	DQS0L
IO	LVDS20p		B1	VREF0B1	12	E3	E4	DQ0L2	DQ0L2	DQ0L2
IO	LVDS20n		B1	VREF0B1	13	D2	E5	DQ0L3	DQ0L3	DQ0L3
IO	LVDS19p		B1	VREF0B1	14	E2	F2			
IO	LVDS19n		B1	VREF0B1	15	D1	F3			
IO	LVDS18p		B1	VREF0B1	16	F3	F4			
IO	LVDS18n		B1	VREF0B1	17	G3	F5			
IO	LVDS17p		B1	VREF0B1	18	F2	G1			
IO	LVDS17n		B1	VREF0B1	19	E1	G2			
IO	LVDS16p		B1	VREF0B1	20	G2	F6			

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 2 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
IO	LVDS16n		B1	VREF0B1	21	F1	F7	DM0L	DM0L	
IO	LVDS15p		B1	VREF0B1			G3			
IO	LVDS15n		B1	VREF0B1			G4			DQ0L4
IO	LVDS14p		B1	VREF0B1			G5			DQ0L5
IO	LVDS14n		B1	VREF0B1			G6			DQ0L6
IO			B1	VREF0B1			H1			DQ0L7
VCCIO1			B1	VREF0B1	22					
GND			B1	VREF0B1						
IO	LVDS13p		B1	VREF1B1			H2			
IO	LVDS13n		B1	VREF1B1			H3			
IO	LVDS12p		B1	VREF1B1			H4			
IO	LVDS12n		B1	VREF1B1			H5			DM0L
IO	VREF1B1		B1	VREF1B1	23	H5	H6			
IO		nCSO	B1	VREF1B1	24	G4	J1			
DATA0		DATA0	B1	VREF1B1	25	H2	H7			
nCONFIG		nCONFIG	B1	VREF1B1	26	H3	J2			
VCCA_PLL1				VREF1B1	27	H6	J5			
CLK0	LVDSCLK1p		B1	VREF1B1	28	G1	J3			
CLK1	LVDSCLK1n		B1	VREF1B1	29	H1	J4			
GNDA_PLL1				VREF1B1	30	J6	K1			
GNDG_PLL1				VREF1B1	31	J5	J6			
nCEO		nCEO	B1	VREF1B1	32	H4	K2			

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 3 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
nCE		nCE	B1	VREF1B1	33	J4	J7			
MSEL0		MSEL0	B1	VREF1B1	34	J3	K3			
MSEL1		MSEL1	B1	VREF1B1	35	J2	K7			
DCLK		DCLK	B1	VREF1B1	36	K4	L1			
IO		ASDO	B1	VREF1B1	37	K3	K6			
IO	PLL1_OUTp		B1	VREF1B1	38	J1	K4			
IO	PLL1_OUTn		B1	VREF1B1	39	K2	K5			
IO	LVDS11p		B1	VREF1B1			L7			DM1L
IO	LVDS11n		B1	VREF1B1			L6			
IO	LVDS10p		B1	VREF1B1			L2			
IO	LVDS10n		B1	VREF1B1			L3			
IO	LVDS9p		B1	VREF1B1			L5			
IO	LVDS9n		B1	VREF1B1			L4			
VCCIO1			B1	VREF2B1						
GND			B1	VREF2B1	40					
IO			B1	VREF2B1			M1			DQ1L0
IO	LVDS8p		B1	VREF2B1			M3			DQ1L1
IO	LVDS8n		B1	VREF2B1			M2			DQ1L2
IO	LVDS7p		B1	VREF2B1			M5			DQ1L3
IO	LVDS7n		B1	VREF2B1	41	L3	M4			
IO	LVDS6p		B1	VREF2B1	42	K1	N1			
IO	LVDS6n		B1	VREF2B1	43	L1	N2			

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 4 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
IO	LVDS5p		B1	VREF2B1	44	L2	M6			
IO	LVDS5n		B1	VREF2B1	45	M1	N7			
IO	LVDS4p		B1	VREF2B1	46	N1	N5			
IO	LVDS4n		B1	VREF2B1	47	M2	N6			
IO	LVDS3p		B1	VREF2B1	48	N2	N3	DQ0L4	DQ0L4	DQ1L4
IO	LVDS3n		B1	VREF2B1	49	M3	N4	DQ0L5	DQ0L5	DQ1L5
IO	DPCLK0		B1	VREF2B1	50	L5	P5			DQS1L
VCCIO1			B1	VREF2B1	51					
GND			B1	VREF2B1	52					
IO	LVDS2p		B1	VREF2B1	53	M4	P2	DQ0L6	DQ0L6	DQ1L6
IO	LVDS2n		B1	VREF2B1	54	N3	P3	DQ0L7	DQ0L7	DQ1L7
IO	VREF2B1		B1	VREF2B1	55	K5	R1			
IO			B1	VREF2B1	56	L4	P4			
IO	LVDS1p		B1	VREF2B1	57	R1	R2			
IO	LVDS1n		B1	VREF2B1	58	P2	R3			
IO	LVDS0p		B1	VREF2B1	59	P3	T2			
IO	LVDS0n		B1	VREF2B1	60	N4	T3			
IO	LVDS102p		B4	VREF2B4	61	R2	U3			
IO	LVDS102n		B4	VREF2B4	62	T2	V4			
IO	LVDS101p		B4	VREF2B4	63	R3	M8			
IO	LVDS101n		B4	VREF2B4	64	P4	N8			
IO	LVDS100p		B4	VREF2B4	65	R4	T4			

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 5 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
IO	LVDS100n		B4	VREF2B4	66	T4	U4			
IO	LVDS99p		B4	VREF2B4	67	R5	T5	DQ1B7	DQ1B7	DQ1B7
IO	LVDS99n		B4	VREF2B4	68	P5	U5	DQ1B6	DQ1B6	DQ1B6
GND			B4	VREF2B4	69					
VCCIO4			B4	VREF2B4	70					
GND				VREF2B4	71					
VCCINT				VREF2B4	72					
IO	DPCLK7		B4	VREF2B4	73	M5	R4	DQS1B	DQS1B	DQS1B
IO	VREF2B4		B4	VREF2B4	74	M6	R5			
IO	LVDS98p		B4	VREF2B4	75	N5	V6			
IO	LVDS98n		B4	VREF2B4	76	N6	U6	DQ1B5	DQ1B5	DQ1B5
IO	LVDS97p		B4	VREF2B4	77	P6	P6	DQ1B4	DQ1B4	DQ1B4
IO	LVDS97n		B4	VREF2B4	78	R6	P7			
IO	LVDS96p		B4	VREF2B4	79	M7	T6			
IO	LVDS96n		B4	VREF2B4			R6			
GND				VREF2B4	80					
VCCINT				VREF2B4	81					
IO	LVDS95p		B4	VREF2B4	82	T6	U7			DQ1B3
IO	LVDS95n		B4	VREF2B4	83	R7	V7			DQ1B2
IO	LVDS94p		B4	VREF2B4	84	P7	T7			DQ1B1
IO	LVDS94n		B4	VREF2B4	85	N7	R7			DQ1B0
IO	LVDS93p		B4	VREF1B4	86	R8	U8			

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 6 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
IO	LVDS93n		B4	VREF1B4	87	T8	V8			
IO	LVDS92p		B4	VREF1B4	88	M8	T8			
IO	LVDS92n		B4	VREF1B4			R8			
GND				VREF1B4	89					
VCCINT				VREF1B4	90					
GND			B4	VREF1B4	91					
VCCIO4			B4	VREF1B4	92					
IO	LVDS91p		B4	VREF1B4			U9			
IO	LVDS91n		B4	VREF1B4			V9			
IO	LVDS90p		B4	VREF1B4		N8	R9			DM1B
IO	LVDS90n		B4	VREF1B4		P8	T9			
IO	LVDS89p		B4	VREF1B4			M9			
IO	LVDS89n		B4	VREF1B4			N9			
IO	VREF1B4		B4	VREF1B4	93	M10	P9			
IO	LVDS88p		B4	VREF1B4			U10			
IO	LVDS88n		B4	VREF1B4			V10			
IO	LVDS87p		B4	VREF1B4	94	R9	T10	DM1B	DM1B	
IO	LVDS87n		B4	VREF1B4	95	T9	R10			
GND				VREF1B4	96					
VCCINT				VREF1B4	97					
IO			B4	VREF1B4			P10			
IO	LVDS86p		B4	VREF1B4	98	P9	R11			

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 7 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
IO	LVDS86n		B4	VREF1B4	99	N9	T11			
IO	LVDS85p		B4	VREF1B4	100	R10	U11			DM0B
IO	LVDS85n		B4	VREF1B4	101	T11	V11			
GND			B4	VREF1B4						
VCCIO4			B4	VREF1B4						
IO	LVDS84p		B4	VREF1B4		N10	V12			
IO	LVDS84n		B4	VREF1B4		P10	U12			
GND				VREF0B4	102					
VCCINT				VREF0B4	103					
IO	LVDS83p		B4	VREF0B4		R11	T12			DQ0B7
IO	LVDS83n		B4	VREF0B4		P11	R12			DQ0B6
IO	LVDS82p		B4	VREF0B4			V13			DQ0B5
IO	LVDS82n		B4	VREF0B4			U13			DQ0B4
IO	LVDS81p		B4	VREF0B4			T13			
IO	LVDS81n		B4	VREF0B4			R13			
IO	LVDS80p		B4	VREF0B4	104	N11	N10			
IO	LVDS80n		B4	VREF0B4	105	N12	M10			
IO			B4	VREF0B4	106	M9	P12			
IO	VREF0B4		B4	VREF0B4	107	M11	P13			
IO	DPCLK6		B4	VREF0B4	108	M12	U14			DQS0B
GND				VREF0B4	109					
VCCINT				VREF0B4	110					

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 8 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
GND			B4	VREF0B4	111					
VCCIO4			B4	VREF0B4	112					
IO	LVDS79p		B4	VREF0B4	113	P12	T14	DQ1B3	DQ1B3	DQ0B3
IO	LVDS79n		B4	VREF0B4	114	R12	R14	DQ1B2	DQ1B2	DQ0B2
IO	LVDS78p		B4	VREF0B4	115	T13	V15	DQ1B1	DQ1B1	DQ0B1
IO	LVDS78n		B4	VREF0B4	116	R13	U15	DQ1B0	DQ1B0	DQ0B0
IO	LVDS77p		B4	VREF0B4	117	R14	N11			
IO	LVDS77n		B4	VREF0B4	118	P13	M11			
IO	LVDS76p		B4	VREF0B4	119	T15	U16			
IO	LVDS76n		B4	VREF0B4	120	R15	T15			
IO	LVDS75n		B3	VREF2B3	121	N13	T16			
IO	LVDS75p		B3	VREF2B3	122	P14	T17			
IO	LVDS74n		B3	VREF2B3	123	P15	R17			
IO	LVDS74p		B3	VREF2B3	124	R16	R18			
IO	LVDS73n		B3	VREF2B3	125	N15	R15	DQ1R7	DQ1R7	DQ1R7
IO	LVDS73p		B3	VREF2B3	126	N16	R16			
IO	VREF2B3		B3	VREF2B3	127	K12	P16			
IO			B3	VREF2B3	128	K14	P17	DQ1R6	DQ1R6	DQ1R6
GND			B3	VREF2B3	129					
VCCIO3			B3	VREF2B3	130					
IO	DPCLK5		B3	VREF2B3	131	L12	P15	DQS1R	DQS1R	DQS1R
IO	LVDS72n		B3	VREF2B3	132	N14	P14	DQ1R5	DQ1R5	DQ1R5

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 9 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
IO	LVDS72p		B3	VREF2B3	133	M13	N14	DQ1R4	DQ1R4	DQ1R4
IO	LVDS71n		B3	VREF2B3	134	M14	N18			
IO	LVDS71p		B3	VREF2B3	135	L13	N17			
IO	LVDS70n		B3	VREF2B3	136	M15	N13			
IO	LVDS70p		B3	VREF2B3	137	M16	N12			
IO	LVDS69n		B3	VREF2B3	138	L14	N16			
IO	LVDS69p		B3	VREF2B3	139	L15	N15			
IO	LVDS68n		B3	VREF2B3	140	L16	M18			
IO	LVDS68p		B3	VREF2B3	141	K16	M17			DQ1R3
IO	LVDS67n		B3	VREF2B3			M14			DQ1R2
IO	LVDS67p		B3	VREF2B3			M15			DQ1R1
IO			B3	VREF2B3			M16			DQ1R0
GND			B3	VREF2B3	142					
VCCIO3			B3	VREF2B3						
IO	LVDS66n		B3	VREF1B3			L18			
IO	LVDS66p		B3	VREF1B3			L17			
IO	LVDS65n		B3	VREF1B3			M13			
IO	LVDS65p		B3	VREF1B3			L13			
IO	LVDS64n		B3	VREF1B3			L16			DM1R
IO	LVDS64p		B3	VREF1B3			L15			
IO			B3	VREF1B3			L14			
IO	PLL2_OUTn		B3	VREF1B3	143	K15	K16			

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 10 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
IO	PLL2_OUTp		B3	VREF1B3	144	J16	K15			
CONF_DONE		CONF_DONE	B3	VREF1B3	145	K13	K17			
nSTATUS		nSTATUS	B3	VREF1B3	146	J13	L12			
TCK		TCK	B3	VREF1B3	147	J14	K18			
TMS		TMS	B3	VREF1B3	148	J15	K14			
TDO		TDO	B3	VREF1B3	149	H15	K13			
GNDG_PLL2				VREF1B3	150	J12	J18			
GNDA_PLL2				VREF1B3	151	J11	K12			
CLK3	LVDSCLK2n		B3	VREF1B3	152	H16	J16			
CLK2	LVDSCLK2p		B3	VREF1B3	153	G16	J15			
VCCA_PLL2				VREF1B3	154	H11	J12			
TDI		TDI	B3	VREF1B3	155	H14	J17			
IO	VREF1B3		B3	VREF1B3	156	H12	J14			
IO	LVDS63n		B3	VREF1B3			J13			
IO	LVDS63p		B3	VREF1B3			H13			DM0R
IO	LVDS62n		B3	VREF1B3			H14			
IO	LVDS62p		B3	VREF1B3			H15			
IO	LVDS61n		B3	VREF1B3			H16			
IO	LVDS61p		B3	VREF1B3			H17			
GND			B3	VREF0B3						
VCCIO3			B3	VREF0B3	157					
IO			B3	VREF0B3			H18			DQ0R7

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 11 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
IO	LVDS60n		B3	VREF0B3			G18			DQ0R6
IO	LVDS60p		B3	VREF0B3			G17			DQ0R5
IO	LVDS59n		B3	VREF0B3	158	G14	G13	DM1R	DM1R	DQ0R4
IO	LVDS59p		B3	VREF0B3	159	G13	G14			
IO	LVDS58n		B3	VREF0B3	160	G15	G15			
IO	LVDS58p		B3	VREF0B3	161	F16	G16			
IO	LVDS57n		B3	VREF0B3	162	F14	G12			
IO	LVDS57p		B3	VREF0B3	163	F13	F12			
IO	LVDS56n		B3	VREF0B3	164	F15	F18			
IO	LVDS56p		B3	VREF0B3	165	E16	F17			
IO	LVDS55n		B3	VREF0B3	166	E15	F13			
IO	LVDS55p		B3	VREF0B3	167	D16	F14			
IO	LVDS54n		B3	VREF0B3	168	D15	F16			
IO	LVDS54p		B3	VREF0B3	169	E14	F15	DQ1R3	DQ1R3	DQ0R3
IO	DPCLK4		B3	VREF0B3	170	F12	E17			DQS0R
GND			B3	VREF0B3	171					
VCCIO3			B3	VREF0B3	172					
IO	LVDS53n		B3	VREF0B3	173	E13	E16	DQ1R2	DQ1R2	DQ0R2
IO	LVDS53p		B3	VREF0B3	174	D14	E15	DQ1R1	DQ1R1	DQ0R1
IO			B3	VREF0B3	175	H13	D18	DQ1R0	DQ1R0	DQ0R0
IO	VREF0B3		B3	VREF0B3	176	G12	E14			
IO	LVDS52n		B3	VREF0B3	177	B16	D16			

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 12 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
IO	LVDS52p		B3	VREF0B3	178	C15	D15			
IO	LVDS51n		B3	VREF0B3	179	C14	C17			
IO	LVDS51p		B3	VREF0B3	180	D13	D17			
IO	LVDS50n		B2	VREF0B2	181	B15	C16			
IO	LVDS50p		B2	VREF0B2	182	A15	B16			
IO	LVDS49n		B2	VREF0B2	183	B14	G11			
IO	LVDS49p		B2	VREF0B2	184	C13	F11			
IO	LVDS48n		B2	VREF0B2	185	B13	B15	DQ0T0	DQ0T0	DQ0T0
IO	LVDS48p		B2	VREF0B2	186	A13	A15	DQ0T1	DQ0T1	DQ0T1
IO	LVDS47n		B2	VREF0B2	187	B12	C15	DQ0T2	DQ0T2	DQ0T2
IO	LVDS47p		B2	VREF0B2	188	C12	D14	DQ0T3	DQ0T3	DQ0T3
VCCIO2			B2	VREF0B2	189					
GND			B2	VREF0B2	190					
VCCINT				VREF0B2	191					
GND				VREF0B2	192					
IO	DPCLK3		B2	VREF0B2	193	E12	B14	DQS0T	DQS0T	DQS0T
IO	VREF0B2		B2	VREF0B2	194	E11	C14			
IO			B2	VREF0B2	195	E9	E13			
IO	LVDS46n		B2	VREF0B2	196	D12	G10			
IO	LVDS46p		B2	VREF0B2	197	D11	F10			
IO	LVDS45n		B2	VREF0B2			B13			
IO	LVDS45p		B2	VREF0B2			A13			

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 13 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
IO	LVDS44n		B2	VREF0B2			D13			DQ0T4
IO	LVDS44p		B2	VREF0B2			C13			DQ0T5
IO	LVDS43n		B2	VREF0B2		C11	D12			DQ0T6
IO	LVDS43p		B2	VREF0B2		B11	C12			DQ0T7
VCCINT				VREF0B2	198					
GND				VREF0B2	199					
IO	LVDS42n		B2	VREF1B2		A11	B12			
IO	LVDS42p		B2	VREF1B2		B10	A12			
VCCIO2			B2	VREF1B2						
GND			B2	VREF1B2						
IO	LVDS41n		B2	VREF1B2	200	C10	C11			
IO	LVDS41p		B2	VREF1B2	201	D10	D11			
IO	LVDS40n		B2	VREF1B2	202	A9	B11			
IO	LVDS40p		B2	VREF1B2	203	B9	A11			DM0T
IO			B2	VREF1B2			E11			
VCCINT				VREF1B2	204					
GND				VREF1B2	205					
IO	LVDS39n		B2	VREF1B2	206	D9	C10	DM0T	DM0T	
IO	LVDS39p		B2	VREF1B2	207	C9	D10			
IO	LVDS38n		B2	VREF1B2			B10			
IO	LVDS38p		B2	VREF1B2			A10			
IO	VREF1B2		B2	VREF1B2	208	E10	E10			

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 14 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
IO	LVDS37n		B2	VREF1B2			G9			
IO	LVDS37p		B2	VREF1B2			F9			
IO	LVDS36n		B2	VREF1B2		C8	D9			DM1T
IO	LVDS36p		B2	VREF1B2		D8	C9			
IO	LVDS35n		B2	VREF1B2			A9			
IO	LVDS35p		B2	VREF1B2			B9			
VCCIO2			B2	VREF1B2	209					
GND			B2	VREF1B2	210					
VCCINT				VREF1B2	211					
GND				VREF1B2	212					
IO	LVDS34n		B2	VREF1B2			D8			
IO	LVDS34p		B2	VREF1B2	213	E8	C8			
IO	LVDS33n		B2	VREF1B2	214	A8	A8			
IO	LVDS33p		B2	VREF1B2	215	B8	B8			
IO	LVDS32n		B2	VREF2B2	216	D7	E8			DQ1T0
IO	LVDS32p		B2	VREF2B2	217	C7	E7			DQ1T1
IO	LVDS31n		B2	VREF2B2	218	B7	A7			DQ1T2
IO	LVDS31p		B2	VREF2B2	219	A6	B7			DQ1T3
VCCINT				VREF2B2	220					
GND				VREF2B2	221					
IO	LVDS30n		B2	VREF2B2			D7			
IO	LVDS30p		B2	VREF2B2	222	E7	C7			

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 15 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
IO	LVDS29n		B2	VREF2B2	223	B6	E6			
IO	LVDS29p		B2	VREF2B2	224	C6	D6			
IO	LVDS28n		B2	VREF2B2	225	D6	B6			
IO	LVDS28p		B2	VREF2B2	226	D5	C6			
IO	VREF2B2		B2	VREF2B2	227	E6	A6			
IO	DPCLK2		B2	VREF2B2	228	E5	B5			DQS1T
VCCINT				VREF2B2	229					
GND				VREF2B2	230					
VCCIO2			B2	VREF2B2	231					
GND			B2	VREF2B2	232					
IO	LVDS27n		B2	VREF2B2	233	C5	C5	DQ0T4	DQ0T4	DQ1T4
IO	LVDS27p		B2	VREF2B2	234	B5	D5	DQ0T5	DQ0T5	DQ1T5
IO	LVDS26n		B2	VREF2B2	235	A4	A4	DQ0T6	DQ0T6	DQ1T6
IO	LVDS26p		B2	VREF2B2	236	B4	B4	DQ0T7	DQ0T7	DQ1T7
IO	LVDS25n		B2	VREF2B2	237	C4	F8			
IO	LVDS25p		B2	VREF2B2	238	B3	G8			
IO	LVDS24n	DEV_OE	B2	VREF2B2	239	A2	B3			
IO	LVDS24p	DEV_CLRn	B2	VREF2B2	240	B2	C4			
VCCINT						A7	A17			
VCCINT						A10	A2			
VCCINT						G8	B1			
VCCINT						G10	B18			

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 16 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
VCCINT						H7	H10			
VCCINT						H9	J9			
VCCINT						J8	K10			
VCCINT						J10	L9			
VCCINT						K7	U1			
VCCINT						K9	U18			
VCCINT						T7	V17			
VCCINT						T10	V2			
VCCIO1						C1				
VCCIO1						G6	E1			
VCCIO1						P1	G7			
VCCIO1							M7			
VCCIO1							P1			
VCCIO4						T3				
VCCIO4						L7	P11			
VCCIO4						L10	P8			
VCCIO4						T14	V14			
VCCIO4							V5			
VCCIO3						P16				
VCCIO3						K11	E18			
VCCIO3						C16	H12			
VCCIO3							M12			

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 17 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
VCCIO3							P18			
VCCIO2						A14				
VCCIO2						F10	A14			
VCCIO2						F7	A5			
VCCIO2						A3	E12			
VCCIO2							E9			
GND						A1	A1			
GND						A16	A16			
GND						A5	A18			
GND						A12	A3			
GND						F6	B17			
GND						F8	B2			
GND						F9	C1			
GND						F11	C18			
GND						G7	H11			
GND						G9	H8			
GND						G11	H9			
GND						H8	J10			
GND						H10	J11			
GND						J7	J8			
GND						J9	K11			
GND						K6	K8			

Table 4–1. Pin List for the Cyclone EP1C12 Device (Part 18 of 18)

Device					Package			DQS for X8 in 240-Pin PQFP	DQS for X8 in 256-Pin FineLine BGA	DQS for X8 in 324-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Num.	VREF Bank	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA			
GND						K8	K9			
GND						K10	L10			
GND						L6	L11			
GND						L8	L8			
GND						L9	T1			
GND						L11	T18			
GND						T1	U17			
GND						T5	U2			
GND						T12	V1			
GND						T16	V16			
GND							V18			
GND							V3			

Pin Definitions

Table 4–2 shows pin definitions for the EP1C12 device.

Table 4–2. Pin Definitions for the EP1C12 Device (Part 1 of 4)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
Supply and Reference Pins		
VCCIO[1..4]	Power	These are I/O supply voltage pins for banks 1 through 4. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, and 3.3-V PCI I/O standards.
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, SSTL2, and SSTL3 I/O standards.
VREF[0..2]B[1..4]	I/O, Inputz	Input reference voltage for banks 1-4. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
VCCA_PLL[1..2]	Power	Analog power for PLLs[1..2]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1..2]	Ground	Analog ground for PLLs[1..2]. The designer can connect this pin to the GND plane on the board.
GNDG_PLL[1..2]	Ground	Guard ring ground for PLLs[1..2]. The designer can connect this pin to the GND plane on the board.
Configuration and JTAG Pins		
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input (PS mode), Output (AS mode)	In passive serial configuration mode, DCLK is a clock input used to clock configuration data from an external source into the Cyclone device. In active serial configuration mode, DCLK is a clock output from the Cyclone device (the Cyclone device acts as master in this mode). This is a dedicated pin used for configuration.
DATA0	Input	Dedicated configuration data input pin.

Table 4–2. Pin Definitions for the EP1C12 Device (Part 2 of 4)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
nCE	Input	Active-low chip enable. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
ASDO	I/O, Output	Active serial data output from the Cyclone device. This output pin is utilized during active serial configuration mode. The Cyclone device controls configuration and drives address and control information out on ASDO. In passive serial configuration, this pin is available as a user I/O pin.
nCSO	I/O, Output	Chip select output that enables/disables a serial configuration device. This output is utilized during active serial configuration mode. The Cyclone device controls configuration and enables the serial configuration device by driving nCSO low. In passive serial configuration, this pin is available as a user I/O pin.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. This pin can be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Dual-purpose pin that can override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the design.
DEV_OE	I/O, Input	Dual-purpose pin that can override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
MSEL[1..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG output pin.
Clock and PLL Pins		
CLK0	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK0 is LVDSCLK1p, which is used for differential input to PLL1.

Table 4–2. Pin Definitions for the EP1C12 Device (Part 3 of 4)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
CLK1	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK1 is LVDSCLK1n, which is used for differential input to PLL1.
CLK2	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK2 is LVDSCLK2p, which is used for differential input to PLL2.
CLK3	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK3 is LVDSCLK2n, which is used for differential input to PLL2.
DPCLK[7..0]	I/O	Dual-purpose clock pins that can connect to the global clock network. These pins can be used for high fan-out control signals, such as clocks, clears, IRDY, TRDY, or DQS signals. These pins are also available as user I/O pins.
PLL1_OUTp	I/O, Output	External clock output from PLL 1. This pin can be used with differential or single ended I/O standards. If clock output from PLL1 is not used, this pin is available as a user I/O pin.
PLL1_OUTn	I/O, Output	Negative terminal for external clock output from PLL1. If the clock output is single ended, this pin is available as a user I/O pin.
PLL2_OUTp	I/O, Output	External clock output from PLL 2. This pin can be used with differential or single ended I/O standards. If clock output from PLL2 is not used, this pin is available as a user I/O pin.
PLL2_OUTn	I/O, Output	Negative terminal for external clock output from PLL2. If the clock output is single ended, this pin is available as a user I/O pin.
Dual-Purpose LVDS & External Memory Interface Pins		
LVDS[0..102]p	I/O, LVDS RX or TX	Dual-purpose LVDS I/O channels 0 to 102. These channels can be used for receiving or transmitting LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for LVDS interfacing, these pins are available as user I/O pins.
LVDS[0..102]n	I/O, LVDS RX or TX	Dual-purpose LVDS I/O channels 0 to 102. These channels can be used for receiving or transmitting LVDS compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for LVDS interfacing, these pins are available as user I/O pins.
LVDSCLK1p	Input, LVDS Input	Dual-purpose LVDS clock input to PLL1. If differential input to PLL1 is not required, this pin is available as the CLK0 input pin.
LVDSCLK1n	Input, LVDS Input	Dual-purpose LVDS clock input to PLL1. If differential input to PLL1 is not required, this pin is available as the CLK1 input pin.

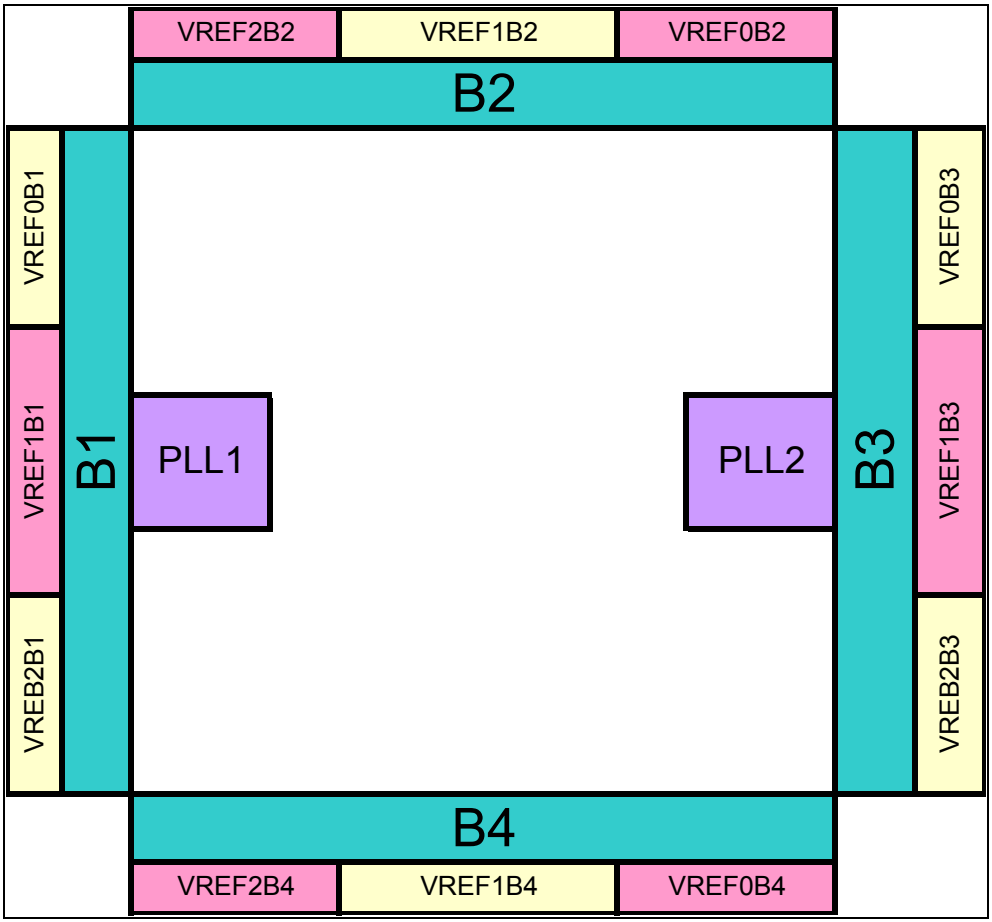
Table 4–2. Pin Definitions for the EP1C12 Device (Part 4 of 4)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
LVDSCLK2p	Input, LVDS Input	Dual-purpose LVDS clock input to PLL2. If differential input to PLL2 is not required, this pin is available as the CLK2 input pin.
LVDSCLK2n	Input, LVDS Input	Dual-purpose LVDS clock input to PLL2. If differential input to PLL2 is not required, this pin is available as the CLK3 input pin.
DQS[0..1][L,R,T,B]	I/O	Optional data strobe signal for use in external memory interfacing. These pins also function as DPCLK pins; therefore, the DQS signals can connect to the global clock network. A programmable delay chain is used to shift the DQS signals by 90 or 72 degrees.
DQ[0..7][L,R,T,B]	I/O	Optional data signal for use in external memory interfacing.
DM[0..1][L,R,T,B]	I/O	Optional data mask output signal for use in external memory interfacing.

PLL & Bank Diagram

Figure 4–1 shows the PLL and bank locations for the EP1C12 device.

Figure 4–1. PLL and Bank Diagram *(1), (2)*



Notes for Figure 4–1:

(1) This is a top view of the silicon die.

(2) This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and the Quartus II software for exact locations.

5. Cyclone EP1C20 Device Pin Information

C52005-1.0

Introduction

The following tables contain pin information for the Cyclone EP1C20 device, organized into the following sections:

Pin List

Table 5–1 shows the complete pin list for the device Cyclone EP1C20 device:

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 1 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
IO	LVDS31p	INIT_DONE	B1	VREF0B1	C3	C3		
IO	LVDS31n		B1	VREF0B1	C2	C2		
IO	LVDS30p	CLKUSR	B1	VREF0B1	D3	D3		
IO	LVDS30n		B1	VREF0B1	D2	D2		
IO	VREF0B1		B1	VREF0B1	D4	D4		
IO			B1	VREF0B1	D1	D1		
IO	LVDS29p		B1	VREF0B1	E3	E4	DQ0L0	DQ0L0
IO	LVDS29n		B1	VREF0B1	E2	E5	DQ0L1	DQ0L1
VCCIO1			B1	VREF0B1				
GND			B1	VREF0B1				
IO	DPCLK1		B1	VREF0B1	F1	F3	DQS0L	DQS0L
IO	LVDS28p		B1	VREF0B1	E4	E3	DQ0L2	DQ0L2
IO	LVDS28n		B1	VREF0B1	E5	E2	DQ0L3	DQ0L3
IO	LVDS27p		B1	VREF0B1	F2	F4		
IO	LVDS27n		B1	VREF0B1	F3	F5		
IO	LVDS26p		B1	VREF0B1	F4	F2		
IO	LVDS26n		B1	VREF0B1	F5	F1		
IO	LVDS25p		B1	VREF0B1	G1	F6		
IO	LVDS25n		B1	VREF0B1	G2	G5		
IO	LVDS24p		B1	VREF0B1	F6	G1		
IO	LVDS24n		B1	VREF0B1	F7	G2		

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 2 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
IO	LVDS23p		B1	VREF0B1	G3	G6		
IO	LVDS23n		B1	VREF0B1	G4	G7	DQ0L4	DQ0L4
IO	LVDS22p		B1	VREF0B1	G5	G3	DQ0L5	DQ0L5
IO	LVDS22n		B1	VREF0B1	G6	G4	DQ0L6	DQ0L6
IO			B1	VREF0B1	H1	H7	DQ0L7	DQ0L7
VCCIO1			B1	VREF0B1				
GND			B1	VREF0B1				
IO	LVDS21p		B1	VREF1B1	H2	H1		
IO	LVDS21n		B1	VREF1B1	H3	H2		
IO	LVDS20p		B1	VREF1B1	H4	H3		
IO	LVDS20n		B1	VREF1B1	H5	H4	DM0L	DM0L
IO	LVDS19p		B1	VREF1B1		J1		
IO	LVDS19n		B1	VREF1B1		J2		
IO	LVDS18p		B1	VREF1B1		H5		
IO	LVDS18n		B1	VREF1B1		H6		
IO	LVDS17p		B1	VREF1B1		J3		
IO	LVDS17n		B1	VREF1B1		J4		
IO	LVDS16p		B1	VREF1B1		J5		
IO	LVDS16n		B1	VREF1B1		J6		
IO			B1	VREF1B1		J7		
IO	VREF1B1		B1	VREF1B1	H6	J8		
VCCIO1			B1	VREF1B1				
IO		nCSO	B1	VREF1B1	J1	K2		

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 3 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
DATA0		DATA0	B1	VREF1B1	H7	K3		
nCONFIG		nCONFIG	B1	VREF1B1	J2	K1		
VCCA_PLL1				VREF1B1	J5	K4		
CLK0	LVDSCLK1p		B1	VREF1B1	J3	K5		
CLK1	LVDSCLK1n		B1	VREF1B1	J4	K6		
GNDA_PLL1				VREF1B1	K1	K7		
GNDG_PLL1				VREF1B1	J6	L7		
nCEO		nCEO	B1	VREF1B1	K2	L2		
nCE		nCE	B1	VREF1B1	J7	L5		
MSEL0		MSEL0	B1	VREF1B1	K3	L1		
MSEL1		MSEL1	B1	VREF1B1	K7	L6		
DCLK		DCLK	B1	VREF1B1	L1	L3		
IO		ASDO	B1	VREF1B1	K6	L4		
GND			B1	VREF1B1				
IO	PLL1_OUTp		B1	VREF1B1	K4	L8		
IO	PLL1_OUTn		B1	VREF1B1	K5	M8		
IO	LVDS15p		B1	VREF1B1		M2		
IO	LVDS15n		B1	VREF1B1		M1		
IO	LVDS14p		B1	VREF1B1		M5		
IO	LVDS14n		B1	VREF1B1		M6		
IO	LVDS13p		B1	VREF1B1		M4		
IO	LVDS13n		B1	VREF1B1		M3		
IO	LVDS12p		B1	VREF1B1	L7	M7	DM1L	DM1L

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 4 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
IO	LVDS12n		B1	VREF1B1	L6	N6		
IO	LVDS11p		B1	VREF1B1	L2	N1		
IO	LVDS11n		B1	VREF1B1	L3	N2		
IO	LVDS10p		B1	VREF1B1	L5	N4		
IO	LVDS10n		B1	VREF1B1	L4	N3		
VCCIO1			B1	VREF2B1				
GND			B1	VREF2B1				
IO			B1	VREF2B1	M1	N5	DQ1L0	DQ1L0
IO	LVDS9p		B1	VREF2B1		N7		
IO	LVDS9n		B1	VREF2B1		P7		
IO	LVDS8p		B1	VREF2B1	M3	P2	DQ1L1	DQ1L1
IO	LVDS8n		B1	VREF2B1	M2	P1	DQ1L2	DQ1L2
IO	LVDS7p		B1	VREF2B1	M5	P6	DQ1L3	DQ1L3
IO	LVDS7n		B1	VREF2B1	M4	P5		
IO	LVDS6p		B1	VREF2B1	N1	P3		
IO	LVDS6n		B1	VREF2B1	N2	P4		
IO	LVDS5p		B1	VREF2B1	M6	R1		
IO	LVDS5n		B1	VREF2B1	N7	R2		
IO	LVDS4p		B1	VREF2B1	N5	R6		
IO	LVDS4n		B1	VREF2B1	N6	R5		
IO	LVDS3p		B1	VREF2B1	N3	R3	DQ1L4	DQ1L4
IO	LVDS3n		B1	VREF2B1	N4	R4	DQ1L5	DQ1L5
IO	DPCLK0		B1	VREF2B1	P5	T4	DQS1L	DQS1L

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 5 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
VCCIO1			B1	VREF2B1				
GND			B1	VREF2B1				
IO	LVDS2p		B1	VREF2B1	P2	T2	DQ1L6	DQ1L6
IO	LVDS2n		B1	VREF2B1	P3	T3	DQ1L7	DQ1L7
IO	VREF2B1		B1	VREF2B1	R1	U1		
IO			B1	VREF2B1	P4	U4		
IO	LVDS1p		B1	VREF2B1	R2	U2		
IO	LVDS1n		B1	VREF2B1	R3	U3		
IO	LVDS0p		B1	VREF2B1	T2	V2		
IO	LVDS0n		B1	VREF2B1	T3	V3		
IO	LVDS128p		B4	VREF2B4	U3	W3		
IO	LVDS128n		B4	VREF2B4	V4	Y4		
IO	LVDS127p		B4	VREF2B4	T4	V4		
IO	LVDS127n		B4	VREF2B4	U4	W4		
IO	LVDS126p		B4	VREF2B4	T5	T5	DQ1B7	DQ1B7
IO	LVDS126n		B4	VREF2B4	U5	U5	DQ1B6	DQ1B6
IO	LVDS125p		B4	VREF2B4		V5		
IO	LVDS125n		B4	VREF2B4		W5		
GND			B4	VREF2B4				
VCCIO4			B4	VREF2B4				
IO	DPCLK7		B4	VREF2B4	R4	T6	DQS1B	DQS1B
IO	VREF2B4		B4	VREF2B4	R5	T7		
IO	LVDS124p		B4	VREF2B4	V6	W6		

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 6 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
IO	LVDS124n		B4	VREF2B4	U6	Y6	DQ1B5	DQ1B5
IO	LVDS123p		B4	VREF2B4	P6	U6	DQ1B4	DQ1B4
IO	LVDS123n		B4	VREF2B4	P7	V6		
IO	LVDS122p		B4	VREF2B4	T6	W7		
IO	LVDS122n		B4	VREF2B4	R6	Y7		
IO	LVDS121p		B4	VREF2B4	U7	R7	DQ1B3	DQ1B3
IO	LVDS121n		B4	VREF2B4	V7	T8	DQ1B2	DQ1B2
IO	LVDS120p		B4	VREF2B4	T7	V7	DQ1B1	DQ1B1
IO	LVDS120n		B4	VREF2B4	R7	U7	DQ1B0	DQ1B0
IO	LVDS119p		B4	VREF1B4	U8	V8		
IO	LVDS119n		B4	VREF1B4	V8	U8		
IO	LVDS118p		B4	VREF1B4	T8	W8		
IO	LVDS118n		B4	VREF1B4	R8	Y8		
GND			B4	VREF1B4				
VCCIO4			B4	VREF1B4				
IO	LVDS117p		B4	VREF1B4	U9	U9		
IO	LVDS117n		B4	VREF1B4	V9	V9		
IO	LVDS116p		B4	VREF1B4	R9	T9	DM1B	DM1B
IO	LVDS116n		B4	VREF1B4	T9	R9		
IO	LVDS115p		B4	VREF1B4		Y9		
IO	LVDS115n		B4	VREF1B4		W9		
IO	LVDS114p		B4	VREF1B4		T10		
IO	LVDS114n		B4	VREF1B4		U10		

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 7 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
IO	VREF1B4		B4	VREF1B4	P9	V10		
IO	LVDS113p		B4	VREF1B4		W10		
IO	LVDS113n		B4	VREF1B4		Y10		
GND			B4	VREF1B4				
VCCIO4			B4	VREF1B4				
IO	LVDS112p		B4	VREF1B4	U10	V11		
IO	LVDS112n		B4	VREF1B4	V10	U11		
IO	LVDS111p		B4	VREF1B4	T10	W11		
IO	LVDS111n		B4	VREF1B4	R10	Y11		
IO			B4	VREF1B4		R11		
IO	LVDS110p		B4	VREF1B4		Y12		
IO	LVDS110n		B4	VREF1B4	P10	W12		
IO	LVDS109p		B4	VREF1B4	R11	T11		
IO	LVDS109n		B4	VREF1B4	T11	T12		
IO	LVDS108p		B4	VREF1B4	U11	U12	DM0B	DM0B
IO	LVDS108n		B4	VREF1B4	V11	V12		
GND			B4	VREF1B4				
VCCIO4			B4	VREF1B4				
IO	LVDS107p		B4	VREF1B4	V12	T13		
IO	LVDS107n		B4	VREF1B4	U12	R13		
IO	LVDS106p		B4	VREF0B4	T12	Y13	DQ0B7	DQ0B7
IO	LVDS106n		B4	VREF0B4	R12	W13	DQ0B6	DQ0B6
IO	LVDS105p		B4	VREF0B4	V13	U13	DQ0B5	DQ0B5

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 8 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
IO	LVDS105n		B4	VREF0B4	U13	V13	DQ0B4	DQ0B4
IO	LVDS104p		B4	VREF0B4	T13	R14		
IO	LVDS104n		B4	VREF0B4	R13	T14		
IO	LVDS103p		B4	VREF0B4		W14		
IO	LVDS103n		B4	VREF0B4		Y14		
IO	LVDS102p		B4	VREF0B4		U14		
IO	LVDS102n		B4	VREF0B4		V14		
IO	LVDS101p		B4	VREF0B4		V15		
IO	LVDS101n		B4	VREF0B4	P12	U15		
IO	VREF0B4		B4	VREF0B4	P13	Y15		
IO	DPCLK6		B4	VREF0B4	U14	W15	DQS0B	DQS0B
GND			B4	VREF0B4				
VCCIO4			B4	VREF0B4				
IO	LVDS100p		B4	VREF0B4		T15		
IO	LVDS100n		B4	VREF0B4		T16		
IO	LVDS99p		B4	VREF0B4	T14	W16	DQ0B3	DQ0B3
IO	LVDS99n		B4	VREF0B4	R14	V16	DQ0B2	DQ0B2
IO	LVDS98p		B4	VREF0B4	V15	V17	DQ0B1	DQ0B1
IO	LVDS98n		B4	VREF0B4	U15	U16	DQ0B0	DQ0B0
IO	LVDS97p		B4	VREF0B4	U16	Y17		
IO	LVDS97n		B4	VREF0B4	T15	W17		
IO	LVDS96n		B3	VREF2B3	T16	W18		
IO	LVDS96p		B3	VREF2B3	T17	V18		

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 9 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
IO	LVDS95n		B3	VREF2B3	R17	V19		
IO	LVDS95p		B3	VREF2B3	R18	U20		
IO	LVDS94n		B3	VREF2B3	R15	U18	DQ1R7	DQ1R7
IO	LVDS94p		B3	VREF2B3	R16	U19		
IO	VREF2B3		B3	VREF2B3	P16	U17		
IO			B3	VREF2B3	P17	T18	DQ1R6	DQ1R6
GND			B3	VREF2B3				
VCCIO3			B3	VREF2B3				
IO	DPCLK5		B3	VREF2B3	P15	T19	DQS1R	DQS1R
IO	LVDS93n		B3	VREF2B3	P14	T17	DQ1R5	DQ1R5
IO	LVDS93p		B3	VREF2B3	N14	R16	DQ1R4	DQ1R4
IO	LVDS92n		B3	VREF2B3	N18	R19		
IO	LVDS92p		B3	VREF2B3	N17	R20		
IO	LVDS91n		B3	VREF2B3	N13	R17		
IO	LVDS91p		B3	VREF2B3	N12	R18		
IO	LVDS90n		B3	VREF2B3	N16	R15		
IO	LVDS90p		B3	VREF2B3	N15	P14		
IO	LVDS89n		B3	VREF2B3	M18	P18		
IO	LVDS89p		B3	VREF2B3	M17	P17	DQ1R3	DQ1R3
IO	LVDS88n		B3	VREF2B3	M14	P16	DQ1R2	DQ1R2
IO	LVDS88p		B3	VREF2B3	M15	P15	DQ1R1	DQ1R1
IO	LVDS87n		B3	VREF2B3		P19		
IO	LVDS87p		B3	VREF2B3		P20		

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 10 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
IO			B3	VREF2B3	M16	N14	DQ1R0	DQ1R0
GND			B3	VREF2B3				
VCCIO3			B3	VREF2B3				
IO	LVDS86n		B3	VREF1B3	L18	N18		
IO	LVDS86p		B3	VREF1B3	L17	N17		
IO	LVDS85n		B3	VREF1B3	M13	N19		
IO	LVDS85p		B3	VREF1B3	L13	N20		
IO	LVDS84n		B3	VREF1B3	L16	N16	DM1R	DM1R
IO	LVDS84p		B3	VREF1B3	L15	N15		
IO	LVDS83n		B3	VREF1B3		M18		
IO	LVDS83p		B3	VREF1B3		M17		
IO	LVDS82n		B3	VREF1B3		M15		
IO	LVDS82p		B3	VREF1B3		M16		
IO	LVDS81n		B3	VREF1B3		M20		
IO	LVDS81p		B3	VREF1B3		M19		
IO			B3	VREF1B3	L14	M14		
IO	PLL2_OUTn		B3	VREF1B3	K16	M13		
IO	PLL2_OUTp		B3	VREF1B3	K15	L13		
CONF_DONE		CONF_DONE	B3	VREF1B3	K17	L18		
nSTATUS		nSTATUS	B3	VREF1B3	L12	L17		
TCK		TCK	B3	VREF1B3	K18	L19		
TMS		TMS	B3	VREF1B3	K14	L16		
TDO		TDO	B3	VREF1B3	K13	L20		

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 11 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
GNDG_PLL2				VREF1B3	J18	L15		
GNDA_PLL2				VREF1B3	K12	K20		
CLK3	LVDSCLK2n		B3	VREF1B3	J16	K14		
CLK2	LVDSCLK2p		B3	VREF1B3	J15	L14		
VCCA_PLL2				VREF1B3	J12	K17		
TDI		TDI	B3	VREF1B3	J17	K18		
VCCIO3			B3	VREF1B3				
IO	VREF1B3		B3	VREF1B3	J14	K19		
IO			B3	VREF1B3		J13		
IO	LVDS80n		B3	VREF1B3		K16		
IO	LVDS80p		B3	VREF1B3		K15		
IO	LVDS79n		B3	VREF1B3		J18		
IO	LVDS79p		B3	VREF1B3		J17		
IO	LVDS78n		B3	VREF1B3		J14		
IO	LVDS78p		B3	VREF1B3		H14		
IO	LVDS77n		B3	VREF1B3		J20		
IO	LVDS77p		B3	VREF1B3		J19		
IO	LVDS76n		B3	VREF1B3	J13	J15		
IO	LVDS76p		B3	VREF1B3	H13	J16	DM0R	DM0R
IO	LVDS75n		B3	VREF1B3	H14	H20		
IO	LVDS75p		B3	VREF1B3	H15	H19		
IO	LVDS74n		B3	VREF1B3	H16	H17		
IO	LVDS74p		B3	VREF1B3	H17	H18		

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 12 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
GND			B3	VREF0B3				
VCCIO3			B3	VREF0B3				
IO			B3	VREF0B3	H18	H16	DQ0R7	DQ0R7
IO	LVDS73n		B3	VREF0B3	G18	G17	DQ0R6	DQ0R6
IO	LVDS73p		B3	VREF0B3	G17	G18	DQ0R5	DQ0R5
IO	LVDS72n		B3	VREF0B3	G13	H15	DQ0R4	DQ0R4
IO	LVDS72p		B3	VREF0B3	G14	G14		
IO	LVDS71n		B3	VREF0B3	G15	G19		
IO	LVDS71p		B3	VREF0B3	G16	G20		
IO	LVDS70n		B3	VREF0B3	G12	G15		
IO	LVDS70p		B3	VREF0B3	F12	G16		
IO	LVDS69n		B3	VREF0B3	F18	F20		
IO	LVDS69p		B3	VREF0B3	F17	F19		
IO	LVDS68n		B3	VREF0B3	F13	F15		
IO	LVDS68p		B3	VREF0B3	F14	F16		
IO	LVDS67n		B3	VREF0B3	F16	E19		
IO	LVDS67p		B3	VREF0B3	F15	E18	DQ0R3	DQ0R3
IO	DPCLK4		B3	VREF0B3	E17	F18	DQS0R	DQS0R
GND			B3	VREF0B3				
VCCIO3			B3	VREF0B3				
IO	LVDS66n		B3	VREF0B3	E16	F17	DQ0R2	DQ0R2
IO	LVDS66p		B3	VREF0B3	E15	E17	DQ0R1	DQ0R1
IO			B3	VREF0B3	D18	D20	DQ0R0	DQ0R0

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 13 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
IO	VREF0B3		B3	VREF0B3	E14	D17		
IO	LVDS65n		B3	VREF0B3	D16	D19		
IO	LVDS65p		B3	VREF0B3	D15	D18		
IO	LVDS64n		B3	VREF0B3	C17	C19		
IO	LVDS64p		B3	VREF0B3	D17	C18		
IO	LVDS63n		B2	VREF0B2	C16	C17		
IO	LVDS63p		B2	VREF0B2	B16	B18		
IO	LVDS62n		B2	VREF0B2	B15	B17	DQ0T0	DQ0T0
IO	LVDS62p		B2	VREF0B2	A15	A17	DQ0T1	DQ0T1
IO	LVDS61n		B2	VREF0B2	C15	C16	DQ0T2	DQ0T2
IO	LVDS61p		B2	VREF0B2	D14	B16	DQ0T3	DQ0T3
IO	LVDS60n		B2	VREF0B2		D16		
IO	LVDS60p		B2	VREF0B2		E16		
VCCIO2			B2	VREF0B2				
GND			B2	VREF0B2				
IO	DPCLK3		B2	VREF0B2	B14	C15	DQS0T	DQS0T
IO	VREF0B2		B2	VREF0B2	C14	D15		
IO	LVDS59n		B2	VREF0B2	E13	B15		
IO	LVDS59p		B2	VREF0B2		A15		
IO	LVDS58n		B2	VREF0B2		E15		
IO	LVDS58p		B2	VREF0B2		F14		
IO	LVDS57n		B2	VREF0B2		A14		
IO	LVDS57p		B2	VREF0B2		B14		

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 14 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
IO	LVDS56n		B2	VREF0B2	B13	E14		
IO	LVDS56p		B2	VREF0B2	A13	E13		
IO	LVDS55n		B2	VREF0B2	D13	C14	DQ0T4	DQ0T4
IO	LVDS55p		B2	VREF0B2	C13	D14	DQ0T5	DQ0T5
IO	LVDS54n		B2	VREF0B2	D12	A13	DQ0T6	DQ0T6
IO	LVDS54p		B2	VREF0B2	C12	B13	DQ0T7	DQ0T7
IO	LVDS53n		B2	VREF1B2	B12	C13		
IO	LVDS53p		B2	VREF1B2	A12	D13		
VCCIO2			B2	VREF1B2				
GND			B2	VREF1B2				
IO	LVDS52n		B2	VREF1B2	C11	E12		
IO	LVDS52p		B2	VREF1B2	D11	F12		
IO	LVDS51n		B2	VREF1B2	B11	A12		
IO	LVDS51p		B2	VREF1B2	A11	B12	DM0T	DM0T
IO	LVDS50n		B2	VREF1B2	E11	D12		
IO	LVDS50p		B2	VREF1B2		C12		
IO			B2	VREF1B2		E11		
IO	LVDS49n		B2	VREF1B2	C10	A11		
IO	LVDS49p		B2	VREF1B2	D10	B11		
IO	LVDS48n		B2	VREF1B2	B10	D11		
IO	LVDS48p		B2	VREF1B2	A10	C11		
VCCIO2			B2	VREF1B2				
GND			B2	VREF1B2				

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 15 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
IO	LVDS47n		B2	VREF1B2		D10		
IO	LVDS47p		B2	VREF1B2		C10		
IO	VREF1B2		B2	VREF1B2	E10	F10		
IO	LVDS46n		B2	VREF1B2		A10		
IO	LVDS46p		B2	VREF1B2		B10		
IO	LVDS45n		B2	VREF1B2		E10		
IO	LVDS45p		B2	VREF1B2		E9		
IO	LVDS44n		B2	VREF1B2	D9	C9	DM1T	DM1T
IO	LVDS44p		B2	VREF1B2	C9	D9		
IO	LVDS43n		B2	VREF1B2	A9	A9		
IO	LVDS43p		B2	VREF1B2	B9	B9		
VCCIO2			B2	VREF1B2				
GND			B2	VREF1B2				
IO	LVDS42n		B2	VREF1B2	D8	C8		
IO	LVDS42p		B2	VREF1B2	C8	D8		
IO	LVDS41n		B2	VREF1B2	A8	A8		
IO	LVDS41p		B2	VREF1B2	B8	B8		
IO	LVDS40n		B2	VREF2B2	E8	E8	DQ1T0	DQ1T0
IO	LVDS40p		B2	VREF2B2	E7	F8	DQ1T1	DQ1T1
IO	LVDS39n		B2	VREF2B2	A7	C7	DQ1T2	DQ1T2
IO	LVDS39p		B2	VREF2B2	B7	D7	DQ1T3	DQ1T3
IO	LVDS38n		B2	VREF2B2	D7	A7		
IO	LVDS38p		B2	VREF2B2	C7	B7		

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 16 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
IO	LVDS37n		B2	VREF2B2	E6	E7		
IO	LVDS37p		B2	VREF2B2	D6	F7		
IO	LVDS36n		B2	VREF2B2	B6	A6		
IO	LVDS36p		B2	VREF2B2	C6	B6		
IO	VREF2B2		B2	VREF2B2	A6	E6		
IO	DPCLK2		B2	VREF2B2	B5	C6	DQS1T	DQS1T
VCCIO2			B2	VREF2B2				
GND			B2	VREF2B2				
IO	LVDS35n		B2	VREF2B2		B5		
IO	LVDS35p		B2	VREF2B2		C5		
IO	LVDS34n		B2	VREF2B2	C5	D6	DQ1T4	DQ1T4
IO	LVDS34p		B2	VREF2B2	D5	D5	DQ1T5	DQ1T5
IO	LVDS33n		B2	VREF2B2	A4	A4	DQ1T6	DQ1T6
IO	LVDS33p		B2	VREF2B2	B4	B4	DQ1T7	DQ1T7
IO	LVDS32n	DEV_OE	B2	VREF2B2	B3	B3		
IO	LVDS32p	DEV_CLRn	B2	VREF2B2	C4	C4		
VCCINT					A17	A19		
VCCINT					A2	A2		
VCCINT					B1	B1		
VCCINT					B18	B20		
VCCINT					F10	H10		
VCCINT					F8	H12		
VCCINT					G11	J11		

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 17 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
VCCINT					G9	J9		
VCCINT					H10	K10		
VCCINT					J9	K12		
VCCINT					K10	L11		
VCCINT					L9	L9		
VCCINT					M10	M10		
VCCINT					M8	M12		
VCCINT					N11	N11		
VCCINT					N9	N9		
VCCINT					U1	W1		
VCCINT					U18	W20		
VCCINT					V17	Y19		
VCCINT					V2	Y2		
VCCIO1						E1		
VCCIO1					E1	H8		
VCCIO1					G7	K8		
VCCIO1					M7	N8		
VCCIO1					P1	T1		
VCCIO4						R10		
VCCIO4					P11	R12		
VCCIO4					P8	R8		
VCCIO4					V14	Y16		
VCCIO4					V5	Y5		

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 18 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
VCCIO3						E20		
VCCIO3					E18	H13		
VCCIO3					H12	K13		
VCCIO3					M12	N13		
VCCIO3					P18	T20		
VCCIO2						A16		
VCCIO2					A14	A5		
VCCIO2					A5	F11		
VCCIO2					E12	F13		
VCCIO2					E9	F9		
GND					A1	A1		
GND					A16	A18		
GND					A18	A20		
GND					A3	A3		
GND					B17	B19		
GND					B2	B2		
GND					C1	C1		
GND					C18	C20		
GND					F11	G10		
GND					F9	G11		
GND					G10	G12		
GND					G8	G13		
GND					H11	G8		

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 19 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
GND					H8	G9		
GND					H9	H11		
GND					J10	H9		
GND					J11	J10		
GND					J8	J12		
GND					K11	K11		
GND					K8	K9		
GND					K9	L10		
GND					L10	L12		
GND					L11	M11		
GND					L8	M9		
GND					M11	N10		
GND					M9	N12		
GND					N10	P10		
GND					N8	P11		
GND					T1	P12		
GND					T18	P13		
GND					U17	P8		
GND					U2	P9		
GND					V1	V1		
GND					V16	V20		
GND					V18	W19		
GND					V3	W2		

Table 5–1. Pin List for the Cyclone EP1C20 Device (Part 20 of 20)

Device					Package		DQS for X8 in 324-Pin FineLine BGA	DQS for X8 in 400-Pin FineLine BGA
Pin Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Bank	324-Pin FineLine BGA	400-Pin FineLine BGA		
GND						Y1		
GND						Y18		
GND						Y20		
GND						Y3		

Pin Definitions

Table 5–2 shows the pin definitions for the EP1C20 device.

Table 5–2. Pin Definitions for the EP1C20 Device (Part 1 of 4)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
Supply and Reference Pins		
VCCIO[1..4]	Power	These are I/O supply voltage pins for banks 1 through 4. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, and 3.3-V PCI I/O standards.
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, SSTL2, and SSTL3 I/O standards.
VREF[0..2]B[1..4]	I/O, Input	Input reference voltage for banks 1-4. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
VCCA_PLL[1..2]	Power	Analog power for PLLs[1..2]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1..2]	Ground	Analog ground for PLLs[1..2]. The designer can connect this pin to the GND plane on the board.
GNDG_PLL[1..2]	Ground	Guard ring ground for PLLs[1..2]. The designer can connect this pin to the GND plane on the board.
Configuration and JTAG Pins		
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input (PS mode), Output (AS mode)	In passive serial configuration mode, DCLK is a clock input used to clock configuration data from an external source into the Cyclone device. In active serial configuration mode, DCLK is a clock output from the Cyclone device (the Cyclone device acts as master in this mode). This is a dedicated pin used for configuration.
DATA0	Input	Dedicated configuration data input pin.

Table 5–2. Pin Definitions for the EP1C20 Device (Part 2 of 4)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
nCE	Input	Active-low chip enable. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
ASDO	I/O, Output	Active serial data output from the Cyclone device. This output pin is utilized during active serial configuration mode. The Cyclone device controls configuration and drives address and control information out on ASDO. In passive serial configuration, this pin is available as a user I/O pin.
nCSO	I/O, Output	Chip select output that enables/disables a serial configuration device. This output is utilized during active serial configuration mode. The Cyclone device controls configuration and enables the serial configuration device by driving nCSO low. In passive serial configuration, this pin is available as a user I/O pin.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. This pin can be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Dual-purpose pin that can override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the design.
DEV_OE	I/O, Input	Dual-purpose pin that can override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
MSEL[1..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG output pin.

Table 5–2. Pin Definitions for the EP1C20 Device (Part 3 of 4)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
Clock and PLL Pins		
CLK0	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK0 is LVDSCLK1p, which is used for differential input to PLL1.
CLK1	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK1 is LVDSCLK1n, which is used for differential input to PLL1.
CLK2	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK2 is LVDSCLK2p, which is used for differential input to PLL2.
CLK3	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK3 is LVDSCLK2n, which is used for differential input to PLL2.
DPCLK[7..0]	I/O	Dual-purpose clock pins that can connect to the global clock network. These pins can be used for high fan-out control signals, such as clocks, clears, IRDY, TRDY, or DQS signals. These pins are also available as user I/O pins.
PLL1_OUTp	I/O, Output	External clock output from PLL 1. This pin can be used with differential or single ended I/O standards. If clock output from PLL1 is not used, this pin is available as a user I/O pin.
PLL1_OUTn	I/O, Output	Negative terminal for external clock output from PLL1. If the clock output is single ended, this pin is available as a user I/O pin.
PLL2_OUTp	I/O, Output	External clock output from PLL 2. This pin can be used with differential or single ended I/O standards. If clock output from PLL2 is not used, this pin is available as a user I/O pin.
PLL2_OUTn	I/O, Output	Negative terminal for external clock output from PLL2. If the clock output is single ended, this pin is available as a user I/O pin.
Dual-Purpose LVDS & External Memory Interface Pins		
LVDS[0..128]p	I/O, LVDS RX or TX	Dual-purpose LVDS I/O channels 0 to 128. These channels can be used for receiving or transmitting LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for LVDS interfacing, these pins are available as user I/O pins.
LVDS[0..128]n	I/O, LVDS RX or TX	Dual-purpose LVDS I/O channels 0 to 128. These channels can be used for receiving or transmitting LVDS compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for LVDS interfacing, these pins are available as user I/O pins.

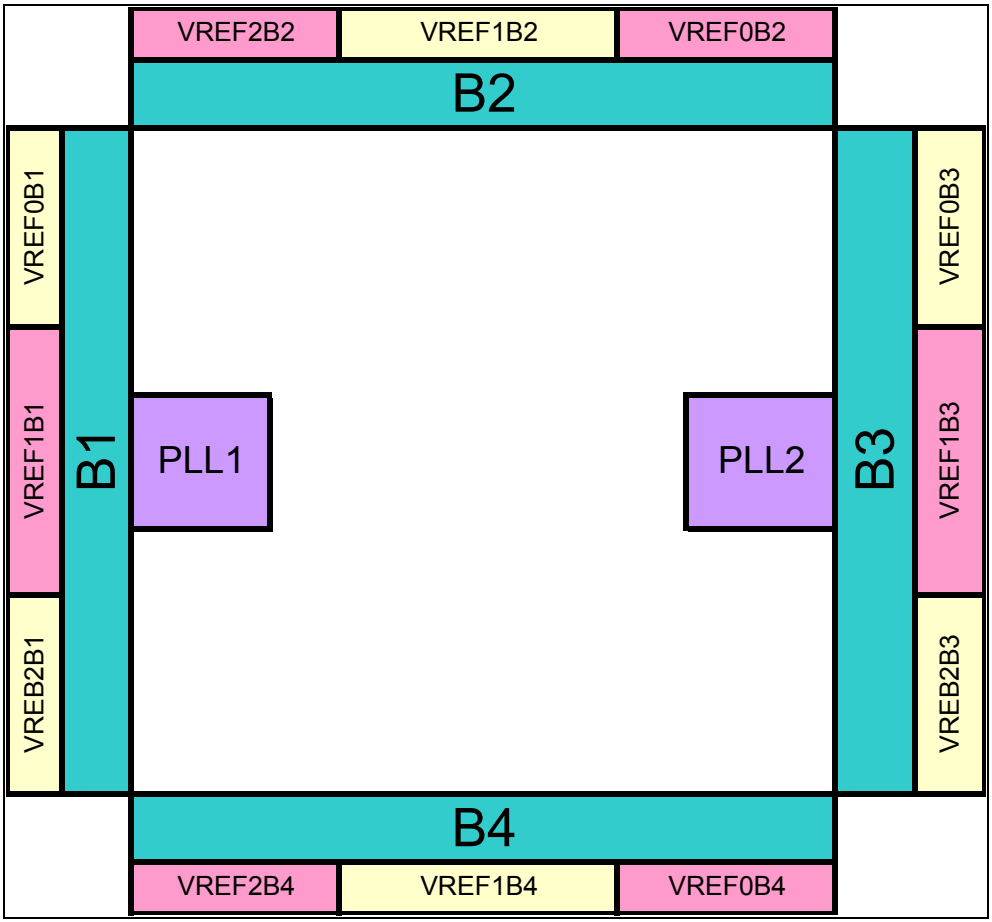
Table 5–2. Pin Definitions for the EP1C20 Device (Part 4 of 4)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
LVDSCLK1p	Input, LVDS Input	Dual-purpose LVDS clock input to PLL1. If differential input to PLL1 is not required, this pin is available as the CLK0 input pin.
LVDSCLK1n	Input, LVDS Input	Dual-purpose LVDS clock input to PLL1. If differential input to PLL1 is not required, this pin is available as the CLK1 input pin.
LVDSCLK2p	Input, LVDS Input	Dual-purpose LVDS clock input to PLL2. If differential input to PLL2 is not required, this pin is available as the CLK2 input pin.
LVDSCLK2n	Input, LVDS Input	Dual-purpose LVDS clock input to PLL2. If differential input to PLL2 is not required, this pin is available as the CLK3 input pin.
DQS[0..1][L,R,T,B]	I/O	Optional data strobe signal for use in external memory interfacing. These pins also function as DPCLK pins; therefore, the DQS signals can connect to the global clock network. A programmable delay chain is used to shift the DQS signals by 90 or 72 degrees.
DQ[0..7][L,R,T,B]	I/O	Optional data signal for use in external memory interfacing.
DM[0..1][L,R,T,B]	I/O	Optional data mask output signal for use in external memory interfacing.

PLL & Bank Diagram

Figure 5–1 shows the PLL and bank locations for the EP1C20 device.

Figure 5–1. PLL and Bank Diagram *(1), (2)*



Notes for Figure 5–1:

(1) This is a top view of the silicon die.

(2) This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and the Quartus II software for exact locations.

6. Package Information for Cyclone Devices

C52006-1.0

Introduction

This data sheet provides package information for Altera® devices. It includes these sections:

In this data sheet, packages are listed in order of ascending pin count.

Device & Package Cross Reference

Table 6–1 shows which Altera Cyclone™ devices are available in FineLine BGA® packages.

Table 6–1. Cyclone Devices in FineLine BGA Packages

Device	Package	Pins
EP1C4	Non-Thermally Enhanced FineLine BGA	324
	Non-Thermally Enhanced FineLine BGA	400
EP1C6	Non-Thermally Enhanced FineLine BGA	256
EP1C12	Non-Thermally Enhanced FineLine BGA	256
	Non-Thermally Enhanced FineLine BGA	324
EP1C20	Non-Thermally Enhanced FineLine BGA	324
	Non-Thermally Enhanced FineLine BGA	400

Thermal Resistance

Table 6–2 provides θ_{JA} (junction-to-ambient thermal resistance) and θ_{JC} (junction-to-case thermal resistance) values for Altera Cyclone devices.

Table 6–2. Thermal Resistance of Cyclone Devices *Notes (1), (2)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EP1C3	100	TQFP	11.0	37.5	35.4	33.4	29.8
	144	TQFP	10.0	31.1	29.4	27.9	25.5
EP1C4	324	FineLine BGA	8.3	28.5	24.4	22.1	20.3
	400	FineLine BGA	7.9	20.7	17.5	15.5	13.9
EP1C6	144	TQFP	9.8	29.4	28.0	26.7	24.7
	240	PQFP	4.3	27.2	24.7	22.1	17.8
	256	FineLine BGA	8.8	28.7	24.5	22.3	20.5
EP1C12	240	PQFP	4.0	26.0	23.4	20.8	17.1
	256	FineLine BGA	6.6	24.3	20.2	18.1	16.4
	324	FineLine BGA	6.1	23.0	19.8	17.7	16.1
EP1C20	324	FineLine BGA	5.0	21.0	17.7	15.6	14.1
	400	FineLine BGA	4.7	20.7	17.5	15.5	13.9

Notes to Table 6–2:
(1) TQFP: thin quad flat pack
(2) PQFP: plastic quad flat pack

Package Outlines

The package outlines on the following pages are listed in order of ascending pin count. Altera package outlines meet the requirements of *JEDEC Publication No. 95*.

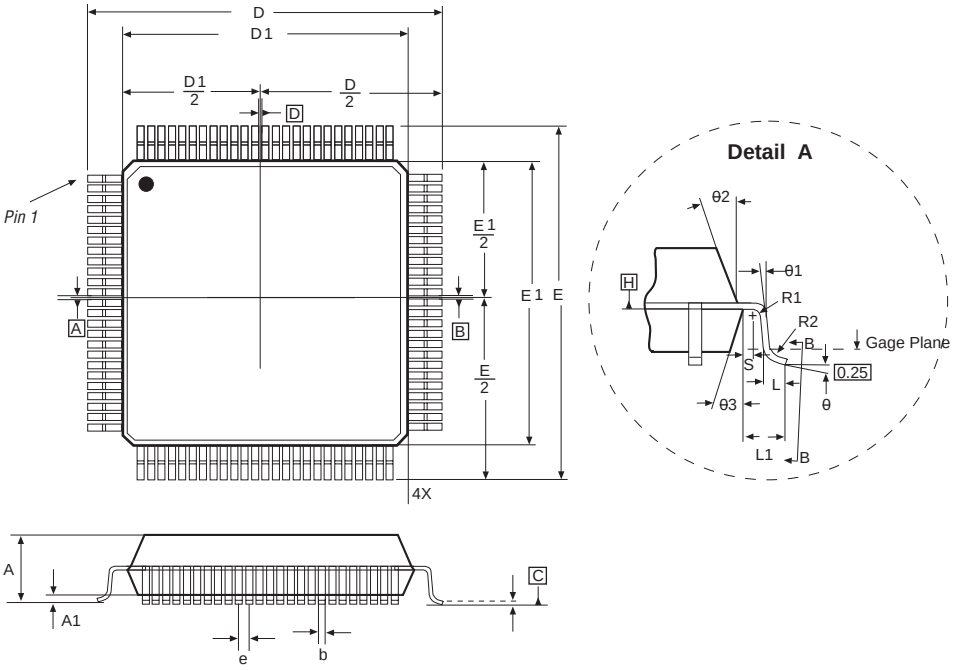
100-Pin Plastic Thin Quad Flat Pack (TQFP)

- All dimensions and tolerances conform to ANSI Y14.5M – 1994.
- Controlling dimension is in millimeters.
- N is the number of leads.

Package Information	
Description	**Specification**
Ordering Code Reference	T
Package Acronym	TQFP
Lead Material	Copper
Lead Finish	Solder plate (85/15 typical)
JEDEC Outline	MS-026
JEDEC Option	BDE
Maximum Lead Coplanarity	0.003 inches (0.08 mm)
Weight	0.5 g
Moisture Sensitivity Level	Printed on moisture barrier bag

Package Outline Figure Reference			
Symbol	**Millimeters**		
	Min.	**Nom.**	**Max.**
A	–	–	1.27
A1	0.05	–	0.15
b	0.17	0.22	0.27
D	15.80	–	16.20
D1	13.50	–	14.50
E	15.80	–	16.20
E1	13.50	–	14.50
q	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°
C	0.09	–	0.20
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
e	0.50 BSC		
N	100		

Package Outline



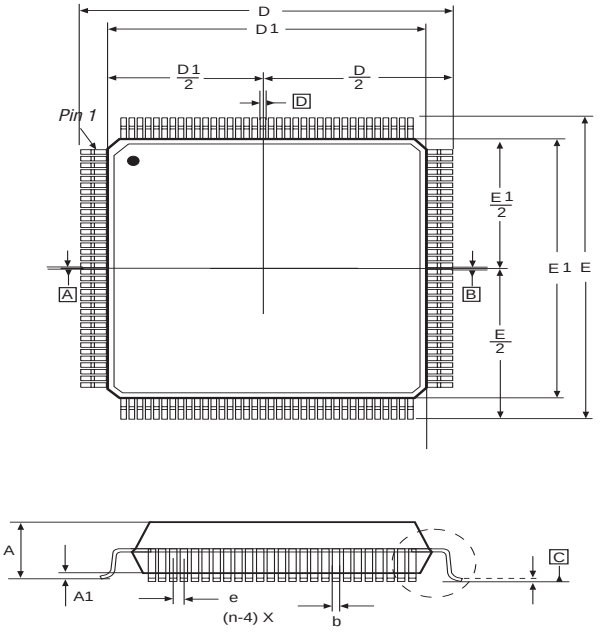
144-Pin Plastic Thin Quad Flat Pack (TQFP)

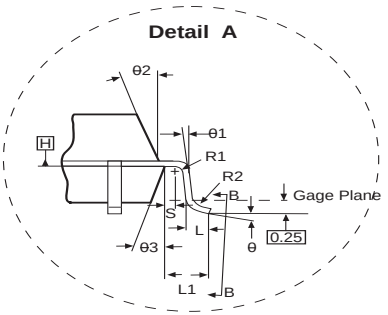
- All dimensions and tolerances conform to ANSI Y14.5M – 1994.
- Controlling dimension is in millimeters.
- N is the number of leads.

Package Information	
Description	**Specification**
Ordering Code Reference	T
Package Acronym	TQFP
Lead Material	Copper
Lead Finish	Solder plate (85/15 typical)
JEDEC Outline	MS-026
JEDEC Option	BFB
Maximum Lead Coplanarity	0.003 inches (0.08 mm)
Weight	1.3 g
Moisture Sensitivity Level	Printed on moisture barrier bag

Package Outline Figure Reference			
Symbol	**Millimeters**		
	Min.	**Nom.**	**Max.**
A	–	–	1.60
A1	0.05	–	0.15
b	0.17	0.22	0.27
D		22.00 BSC	
D1		20.00 BSC	
e		0.50 BSC	
E		22.00 BSC	
E1		20.00 BSC	
q	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°
L	0.45	0.60	0.75
L1		1.00 REF	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
N		144	

Package Outline





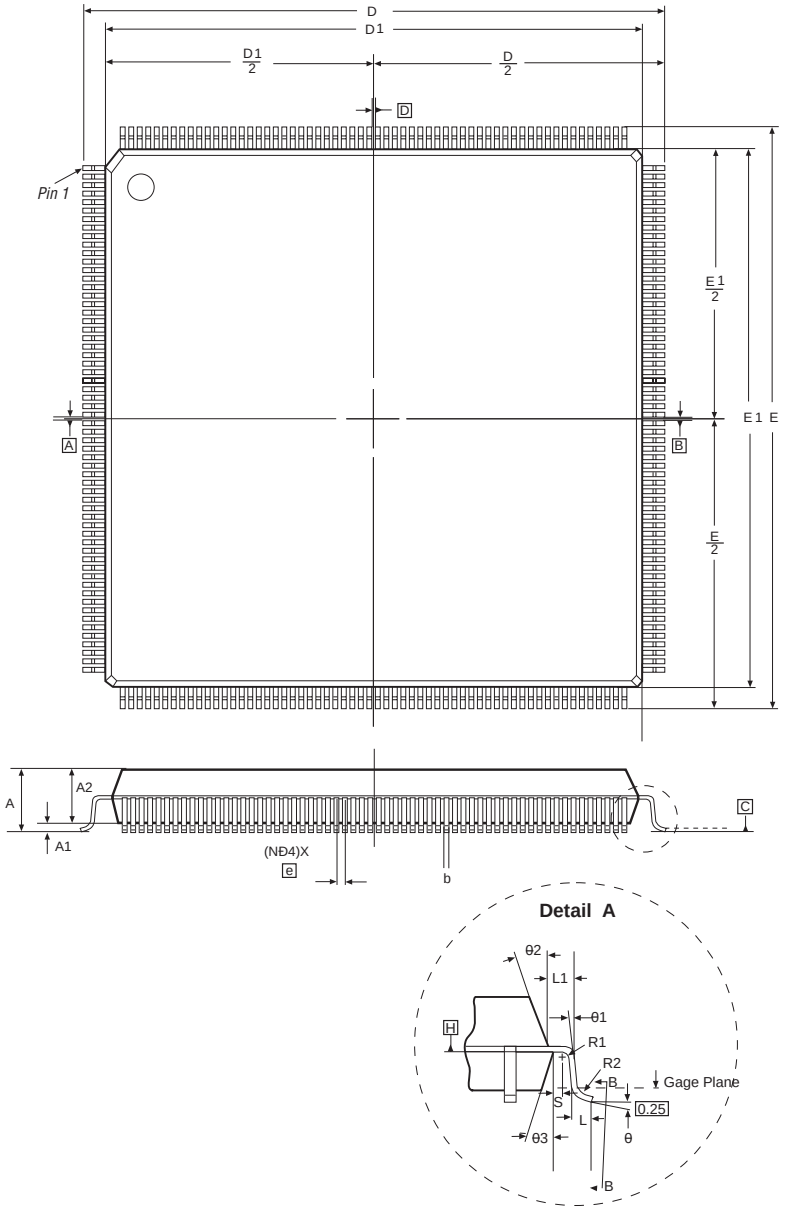
240-Pin Plastic Quad Flat Pack (PQFP)

- All dimensions and tolerances conform to ANSI Y14.5M – 1994.
- Controlling dimension is in millimeters.
- N is the number of leads.

Package Information	
Description	**Specification**
Ordering Code Reference	Q
Package Acronym	PQFP
Lead Material	Copper
Lead Finish	Solder plate (85/15 typical)
JEDEC Outline	MS-029
JEDEC Option	GA
Maximum Lead Coplanarity	0.003 inches (0.08 mm)
Weight	7.0 g
Moisture Sensitivity Level	Printed on moisture barrier bag

Package Outline Figure Reference			
Symbol	**Millimeters**		
	Min.	**Nom.**	**Max.**
A	–	–	4.10
A1	0.25	–	0.50
A2	3.20	3.40	3.60
D	34.35	–	34.85
D1	31.90	–	32.10
E	34.35	–	34.85
E1	31.90	–	32.10
e	0.50 BSC		
b	0.17	–	0.27
R2	0.08	–	0.25
R1	0.08	–	–
q	0°	3.5°	8°
θ1	0°	–	–
θ2	5°	–	16°
θ3	5°	–	16°
L	0.46	–	0.66
L1	0.40	–	–
S	0.20	–	–
N	240		

Package Outline



256-Pin Non-Thermally Enhanced FineLine Ball-Grid Array

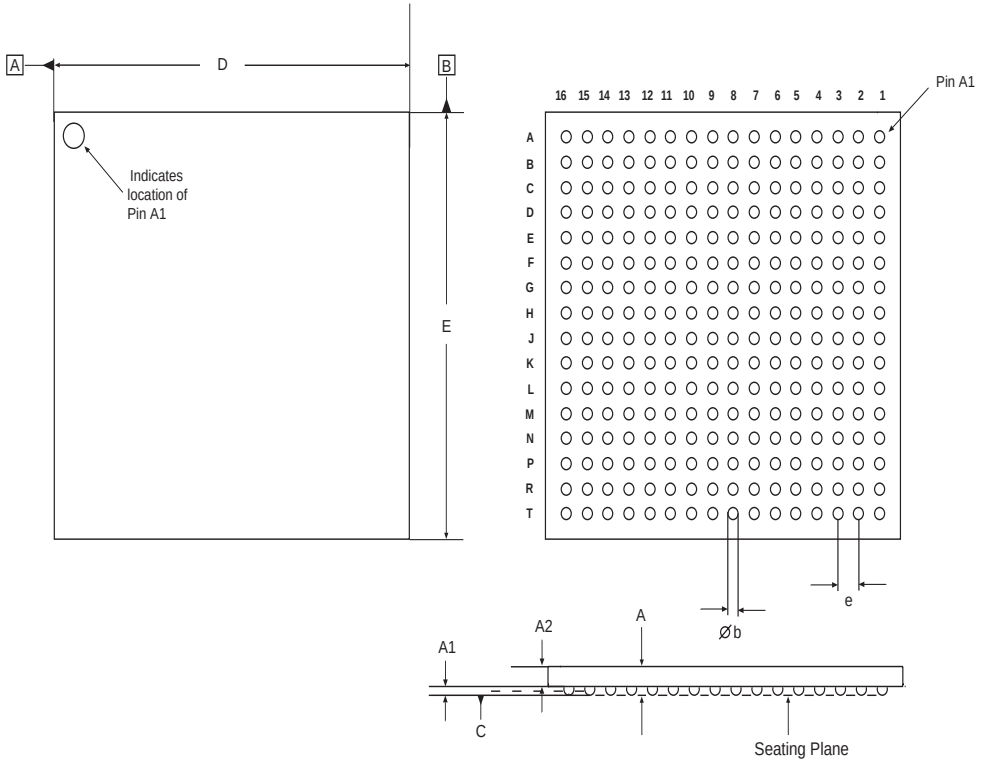
- All dimensions and tolerances conform to ANSI Y14.5M – 1994.
- Controlling dimension is in millimeters.
- M is the maximum solder ball matrix size.

Package Information	
Description	**Specification**
Ordering Code Reference	F
Package Acronym	FBGA
Lead Material	Tin-lead alloy (63/37)
Lead Finish	N/A
JEDEC Outline	MS-034
JEDEC Option	AAF-1
Maximum Lead Coplanarity	0.008 inches (0.20 mm)
Weight	1.2 g
Moisture Sensitivity Level	Printed on moisture barrier bag

Package Outline Figure Reference			
Symbol	**Millimeters**		
	Min.	**Nom.**	**Max.**
A *(3)*	–	–	3.50
A1	0.30	–	–
A2	0.25	–	1.10
A3	–	–	2.50
D/E	17.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		
M	16		

(3) Altera's thickness specification for A is 2.6 mm maximum. The Max item for A in the table reflects the JEDEC specification.

Package Outline



324-Pin Non-Thermally Enhanced FineLine Ball-Grid Array

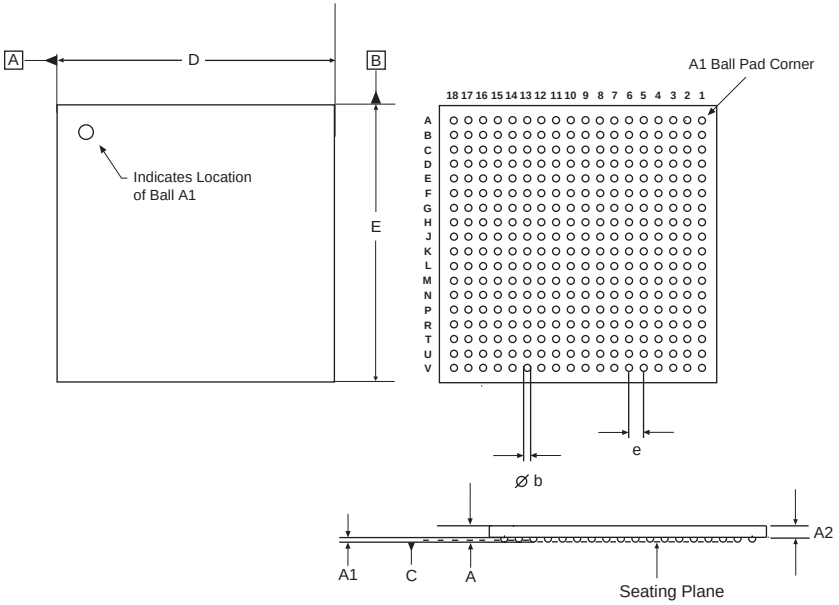
- All dimensions and tolerances conform to ANSI Y14.5M – 1994.
- Controlling dimension is in millimeters.
- M is the maximum solder ball matrix size.

Package Information	
Description	**Specification**
Ordering Code Reference	F
Package Acronym	FBGA
Lead Material	Tin-lead alloy (63/37)
Lead Finish	N/A
JEDEC Outline	MS-034
JEDEC Option	AAG-1
Maximum Lead Coplanarity	0.008 inches (0.20 mm)
Weight	1.5 g
Moisture Sensitivity Level	Printed on moisture barrier bag

Package Outline Figure Reference			
Symbol	**Millimeters**		
	Min.	**Nom.**	**Max.**
A *(4)*	1.20	–	3.50
A1	0.30	–	–
A2	0.25	–	3.00
D/E	19.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		
M	18		

(4) Altera's thickness specification for A is 2.6 mm maximum. The Max item for A in the table reflects the JEDEC specification.

Package Outline



400-Pin Non-Thermally Enhanced FineLine Ball-Grid Array

- All dimensions and tolerances conform to ANSI Y14.5M – 1994.
- Controlling dimension is in millimeters.
- M is the maximum solder ball matrix size.

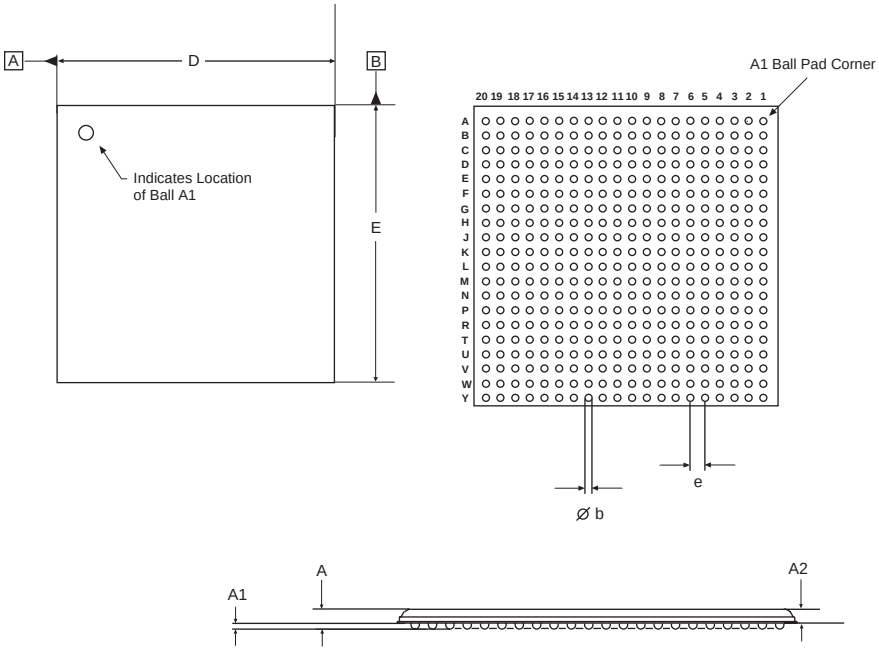
Package Information	
Description	**Specification**
Ordering Code Reference	F
Package Acronym	FBGA
Lead Material	Tin-lead alloy (63/37)
Lead Finish	N/A
JEDEC Outline	MS-034
JEDEC Option	AAJ-1
Maximum Lead Coplanarity	0.008 inches (0.20 mm)
Weight	1.9 g
Moisture Sensitivity Level	Printed on moisture barrier bag

Package Outline Figure Reference			
Symbol	**Millimeters**		
	Min.	**Nom.**	**Max.**
A *(5)*	120	–	3.50
A1	0.30	–	–
A2	0.25	–	3.00
D/E	21.00 BSC		
b *(6)*	0.50	0.60	0.70
e	1.00 BSC		
M	18		

(5) Altera's thickness specification for 'A' is 2.6 mm maximum. The Max. dimension for 'A' in the table reflects the JEDEC specification.

(6) Ball size, parameter 'b', can increase to a maximum of 0.74. Contact Altera Applications for more information.

Package Outline



7. Designing with FineLine BGA Packages

C52007-1.0

Introduction

As programmable logic devices (PLDs) increase in density and I/O pins, the demand for small packages and diverse packaging options continues to grow. Ball-grid array (BGA) packages are an ideal solution because the I/O connections are on the interior of the device, improving the ratio between pin count and board area. Typical BGA packages contain up to twice as many connections as quad flat pack (QFP) packages for the same area. Further, BGA solder balls are considerably stronger than QFP leads, resulting in robust packages that can tolerate rough handling.

Altera has developed a new BGA solution for users of high-density PLDs called the FineLine BGA® package. The new format requires less than half the board space of standard BGA packages. This application note provides guidelines for designing your printed circuit board (PCB) for Altera's FineLine BGA packages and discusses the following topics:

- Overview of BGA packages
- PCB layout terminology
- PCB layout for FineLine BGA packages

Overview of BGA Packages

As PLDs grow to 1 million gates and beyond, designers require more advanced, flexible packages. BGA packages empower designers by offering the technological benefits and flexibility to meet future system requirements.

In BGA packages, the I/O connections are located on the interior of the device. Leads normally placed along the periphery of the package are replaced with solder balls arranged in a matrix across the bottom of the substrate. The final device is soldered directly to the PCB using assembly processes virtually identical to the standard surface mount technology preferred by system designers.

In addition, BGA packages provide the following advantages:

- *Fewer damaged leads*—BGA leads consist of solid solder balls, which are less likely to suffer damage during handling.
- *More leads per unit area*—Lead counts are increased by moving the solder balls closer to the edges of the package and by decreasing the pitch to 1.0 mm.

- *Less expensive surface mount equipment*—BGA packages can tolerate slightly imperfect placement during mounting, requiring less expensive surface mount equipment. The placement can be imperfect because the BGA packages self-align during solder reflow.
- *Smaller footprints*—BGA packages are usually 20% to 50% smaller than QFP packages, making BGA packages more attractive for applications that require high performance and a smaller footprint.
- *Integrated circuit speed advantages*—BGA packages can operate well into the microwave frequency spectrum and can achieve high electrical performance by using ground planes, ground rings, and power rings in the package construction.
- *Improved heat dissipation*—Because the die is located at the center of the FineLine BGA package and most VCC and GND pins are located at the center of the package, the GND and VCC pins are located under the die. As a result, the heat generated in the device can be transferred out through the GND and VCC pins (i.e., the GND and VCC pins act as a heat sink).

PCB Layout Terminology

This section defines common terms used in PCB layout.

Escape Routing

Escape routing is the method used to route each signal from a package to another element on the PCB.

Multi-Layer PCBs

The increased I/O count associated with BGA packages has made multi-layer PCBs the industry-standard method for performing escape routing. Signals can be routed to other elements on the PCB through various numbers of PCB layers.

Vias

Vias, or plated through holes, are used in multi-layer PCBs to transfer signals from one layer to another. Vias are actual holes drilled through a multi-layer PCB and provide electrical connections between various PCB layers. All vias provide layer-to-layer connections only; device leads or other reinforcing material are not inserted into vias.

Table 7–1 describes the terms used to define via dimensions.

Table 7–1. Via Dimension Terms

Term	Definition
Aspect ratio	The aspect ratio is the ratio of a via's length or depth to its pre-plated diameter.
Drilled hole diameter	The drilled hole diameter is the diameter of the actual via hole drilled in the board.
Finished via diameter	The finished via diameter is the diameter of a via hole that has been finished.

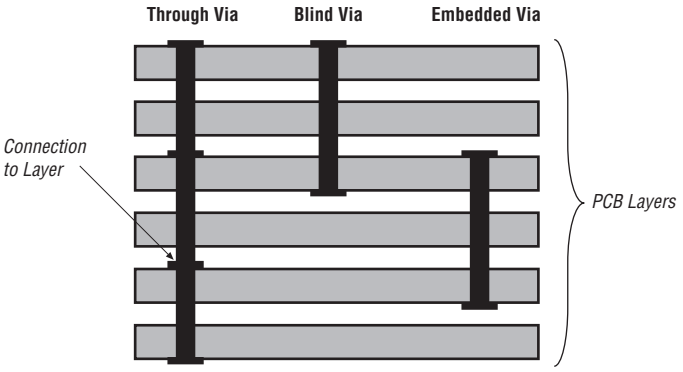
Table 7–2 shows the three via types typically used on PCBs.

Table 7–2. Via Types

Type	Description
Through via	An interconnection between the top and the bottom layer of a PCB. Through vias can also provide interconnections to inner PCB layers.
Blind via	An interconnection from the top or bottom layer to an inner PCB layer.
Embedded via	An interconnection between any number of inner PCB layers.

Figure 7–1 shows all three via types.

Figure 7–1. Types of Vias



Blind vias and through vias are used more frequently than embedded vias. Blind vias can be more expensive than through vias, but overall costs can be reduced because signal traces can be routed under a blind via, requiring fewer PCB layers. Through vias, on the other hand, do not permit signals to be routed through lower layers, which can increase the required number of PCB layers and overall costs.

Via Capture Pad

Vias are connected electrically to PCB layers through via capture pads, which surround each via.

Surface Land Pad

Surface land pads are the areas on the PCB to which the BGA solder balls adhere. The size of these pads affects the space available for vias and escape routing. In general, surface land pads are available in the following two basic designs:

- Non solder mask defined (NSMD), also known as copper defined
- Solder mask defined (SMD)

The main differences between the two surface land pad types are the size of the trace and space, the type of vias you can use, and the shape of the solder balls after solder reflow.

Non Solder Mask Defined Pad

In the non solder mask defined (NSMD) pad, the solder mask opening is larger than the copper pad. Thus, the surface land pad's copper surface is completely exposed, providing greater area to which the BGA solder ball can adhere (see Figure 7–2). Altera recommends that you use a NSMD pad for most applications because it provides more flexibility, fewer stress points, and more line-routing space between pads.

Solder Mask Defined Pad

In the solder mask defined (SMD) pad, the solder mask overlaps the surface land pad's copper surface (see Figure 7–2). This overlapping provides greater adhesion strength between the copper pad and the PCB's epoxy/glass laminate, which can be important under extreme bending and during accelerated thermal cycling tests. However, the solder mask overlap shrinks the amount of copper surface available for the BGA solder ball.

Figure 7–2. Side View of NSMD & SMD Land Pads

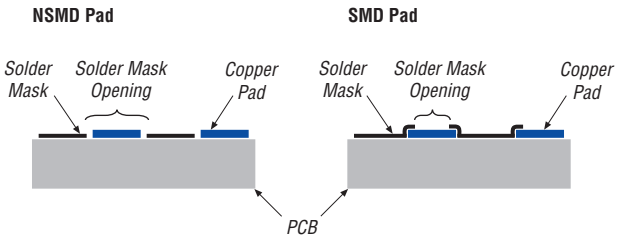
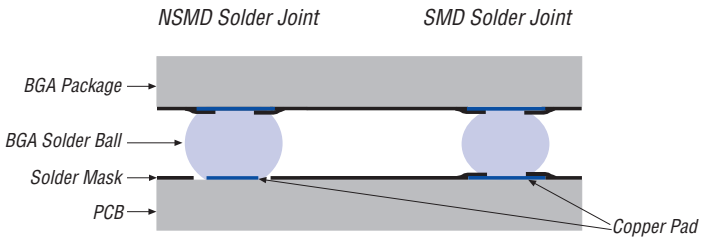


Figure 7–3 shows the side view for an NSMD and SMD solder joint.

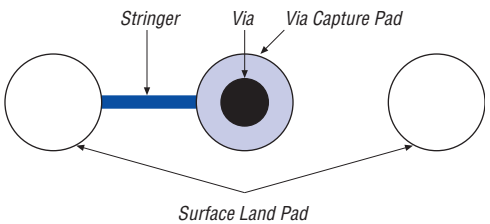
Figure 7–3. Side View of NSMD & SMD Solder Joints



Stringer

Stringers are rectangular or square interconnect segments that electrically connect via capture pads and surface land pads. Figure 7–4 shows the connection between vias, via capture pads, surface land pads, and stringers.

Figure 7–4. Via, Land Pad, Stringer & Via Capture Pad



PCB Layout for FineLine BGA Packages

When designing a PCB for FineLine BGA packages, consider the following factors:

- Surface land pad dimension
- Via capture pad layout and dimension
- Signal line space and trace width
- Number of PCB layers

For all FineLine BGA figures, the controlling dimension is millimeters.

Surface Land Pad Dimension

Surface land pads should be the same size as the BGA pad to provide a balanced stress on solder joints. For this reason, Altera recommends using a 15.75-mil surface land pad, because it is the same size as the BGA pad. Figure 7–5 shows a 15.75-mil BGA pad.

Figure 7–5. 15.75-Mil BGA Pad

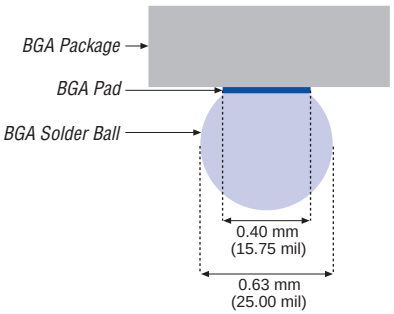
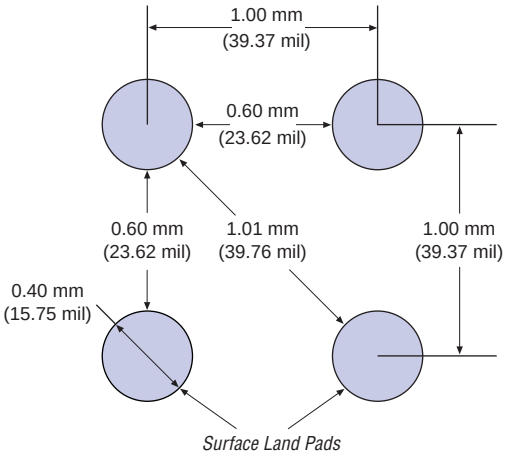


Figure 7–6 shows how much space is available for vias and escape routing when you use 15.75-mil surface land pads.

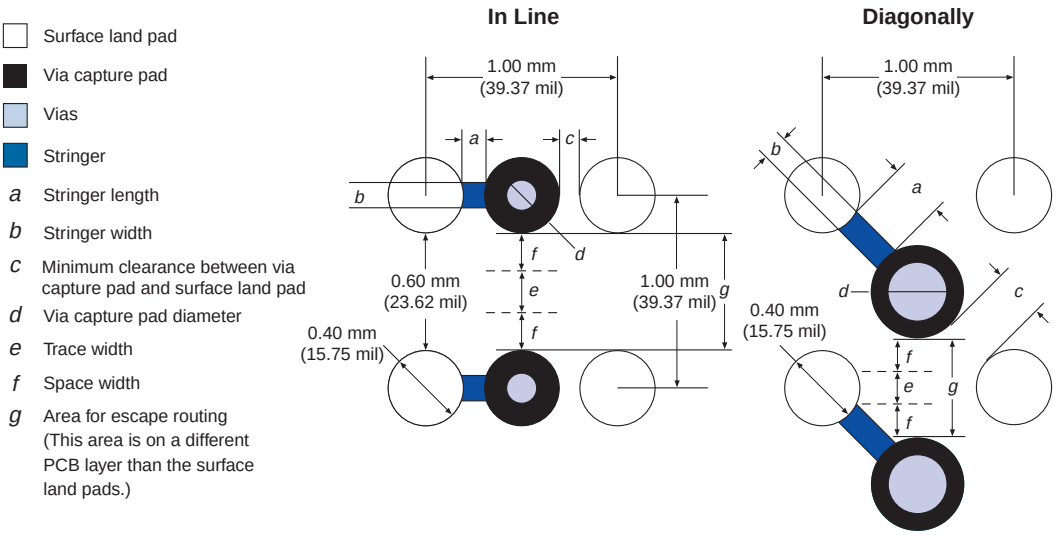
Figure 7–6. Space Available for 15.75-Mil Surface Land Pads



Via Capture Pad Layout & Dimension

The size and layout of via capture pads affect the amount of space available for escape routing. In general, you can layout via capture pads in the following two ways: in-line with the surface land pads or in the diagonal of surface land pads. Figure 7–7 shows both layouts.

Figure 7–7. Placement of Via Capture Pad



The decision to place the via capture pads diagonally or in-line with the surface lands pads is based on the following factors:

- Diameter of the via capture pad
- Stringer length
- Clearance between via capture pad and surface land pad

To decide how to lay out your PCB, use the information shown in Figure 7–7 and Table 7–3. If your PCB design guidelines do not conform to either equation in Table 7–3, contact Altera Applications for further assistance.

Table 7–3. Formula for Via Layouts

Layout	Formula
In-line	*a* + *c* + *d* ð 23.62 mil
Diagonally	*a* + *c* + *d* ð 39.76 mil

Table 7–3 shows that you can place a larger via capture pad diagonally than in-line with the surface land pads.

Via capture pad size also affects how many traces can be routed on a PCB. Figure 7–8 shows sample layouts of typical and premium via capture pads. The typical layout shows a via capture pad size of 27 mil, a via size of 8 mil, and an inner space/trace of 4 mil. With this layout, only one trace can be routed between the vias. If more traces are required, you must reduce the via capture pad size or the space/trace size.

The premium layout shows a via capture pad size of 20 mil, a via size of 5 mil, and an inner space/trace of 3 mil. This layout provides enough space to route two traces between the vias.

Figure 7–8. Typical & Premium Via Capture Pad Sizes

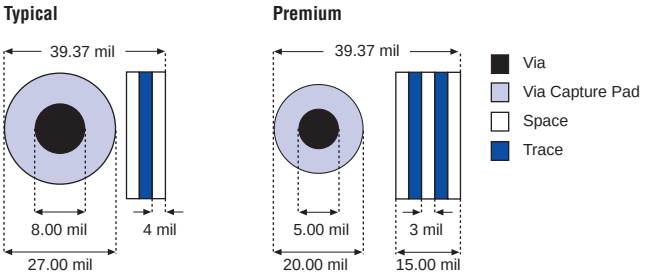


Table 7–4 shows the typical and premium layout specifications used by most PCB vendors.

Table 7–4. Vendor Specifications

Specification	Typical (Mil)	Premium (Mil)
Trace/space width	5/5	3/3
Drilled hole diameter	12	10
Finished via diameter	8	ð 5
Via capture pad	25.5	20
Aspect ratio	7:1	10:1

For detailed information on drill sizes, via sizes, space/trace sizes, or via capture pad sizes, contact your PCB vendor directly.

Signal Line Space & Trace Width

The ability to perform escape routing is defined by the width of the trace and the minimum space required between traces. The minimum area for signal routing is the smallest area that the signal must be routed through (i.e., the distance between two vias, or g in Figure 7–7). This area is calculated by the following formula:

$$g = 39.37 - d$$

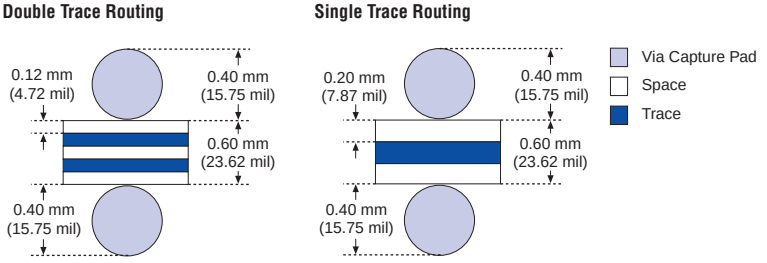
The number of traces that can be routed through this area is based on the permitted line trace and space widths. You can use Table 7–5 to determine the total number of traces that can be routed through g.

Table 7–5. Number of Traces

Number of Traces	Formula
1	$g \geq$ [2 × (space width)] + trace width
2	$g \geq$ [3 × (space width)] + [2 × (trace width)]
3	$g \geq$ [5 × (space width)] + [3 × (trace width)]

Figure 7–9 shows that by reducing the trace and space size, you can route more traces through g. Increasing the number of traces reduces the required number of PCB layers and decreases the overall cost.

Figure 7–9. Escape Routing for Double & Single Traces



Number of PCB Layers

In general, the number of PCB layers required to route signals is inversely proportional to the number of traces between vias (i.e., the greater the number of traces, the fewer the number of PCB layers required). You can estimate the number of layers your PCB requires by first determining:

- Trace and space size
- Number of traces routed between the via capture pads
- Type of vias used

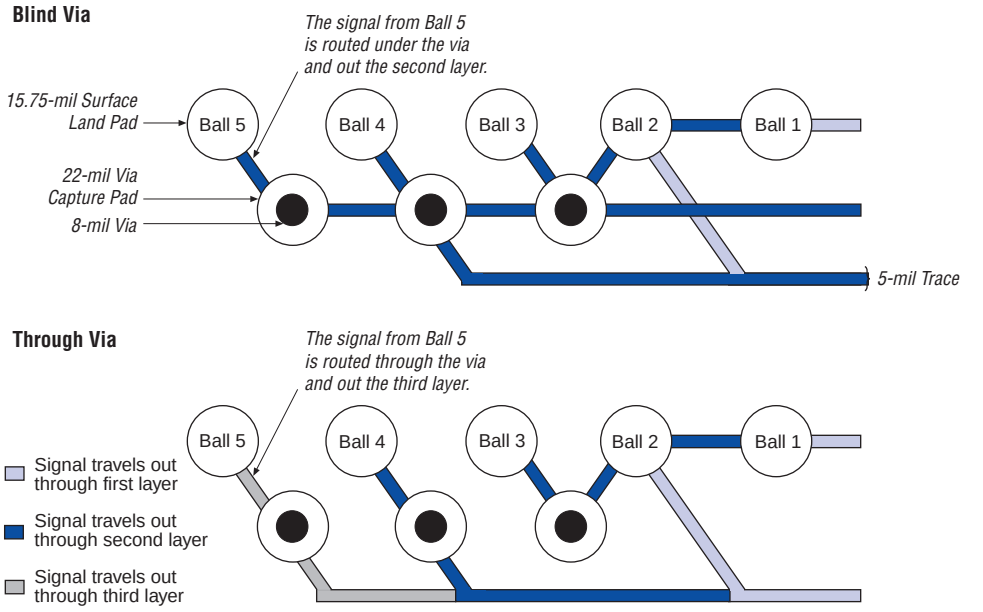
Table 7–6 shows the number of PCB layers required to route signals for various FineLine BGA packages in EPF10K50E devices, assuming the use of a power plane, ground plane, and all I/O pins. This table shows that using double traces and blind vias reduces the required number of layers.

Table 7–6. Minimum Required PCB Layers

FineLine BGA Package (Balls)	Single Trace		Double Trace	
	Blind Vias (Layers)	Through Vias (Layers)	Blind Vias (Layers)	Through Vias (Layers)
100	2	2	1	1
256	2	2	2	2
484	2	3	2	2
672	3	4	2	3

Using fewer I/O pins than the maximum can reduce the required number of layers. Via type can also reduce the number of layers required. To see how the via type can affect the required number of PCB layers, consider the sample layouts shown in Figure 7–10.

Figure 7–10. Sample PCB Layout



The blind via layout in Figure 7–10 requires only two PCB layers. The signals from the first two balls can be routed directly through the first layer. The signals from the third and fourth balls can be routed through a via and out the second layer, and the signal from the fifth ball can be routed under the vias for Ball 4 and Ball 3 and out the second layer. Together, only two PCB layers are required.

In contrast, the through via layout in Figure 7–10 requires three PCB layers, because signals cannot be routed under through vias. The signals from the third and fourth balls can still be routed through a via and out the second layer, but the signal from the fifth ball must be routed through a via and out the third layer. Using blind vias rather than through vias in this example saves one PCB layer.

Conclusion

Altera has taken a leadership position in PLD packaging with the recent introduction of 1.00-mm FineLine BGA packages. These packages use a reduced PCB area while maintaining a very high pin count. By using the information in this application note, you can easily design PCBs to use FineLine BGA packages, and take advantage of the package's reduced size.