Data International Co., Ltd.

DATAVISION

APPROVAL SHEET

Customer	:	
Part Name	:	**LCD MODULE**
Model No.	:	**DG-12864-S2RB**
Drawing No.	:	
Approved by	:	
Date	:	

Approved	Checked	Prepared	Sheet Code:
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CONTENTS

1. SCOPE

This specification covers the engineering requirements for the DG-12864-S2RB liquid crystal module.

2. PRODUCT SPECIFICATIONS

2.1 General

- 128 × 64 dot matrix LCD
- STN (Gray) , Positive mode LCD panel
- Reflective , Normal temperature type
- 6 o'clock
- Multiplexing driving : 1/64duty, 1/9bias

2.2 Mechanical Characteristics

Item	Characteristic
Dot configuration	128 × 64
Dot dimensions(mm)	0.21 × 0.21
Dot spacing (mm)	0.02
Module dimensions (Horizontal × Vertical × Thickness, mm)	93.0 × 70.0 × 9.5max.
Viewing area (Horizontal × Vertical, mm)	71.7 × 39.0
Active area (Horizontal × Vertical, mm)	62.54 × 33.10

2.3 Absolute Maximum Ratings (Without LED back-light)

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit	Note
Operating Voltage	V_{DD}	-0.3~+7.0	V	*1
Supply Voltage	V_{EE}	V_{DD}-19.0~V_{DD}+0.3	V	*4
Driver Supply Voltage	V_B	-0.3~V_{DD}+0.3	V	*1,2
	V_{LCD}	V_{EE}-0.3~V_{DD}+0.3	V	*3,4
Operating Temperature	T_{OPR}	-30~+85	°C	-
Storage Temperature	T_{STG}	-55~+125	°C	-

2.4 Electrical Characteristics (Without LED back-light)

ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD}=+5V ±10%, V_{SS}=0V, |V_{DD}-V_{EE}|=8~17V, T_a= -30 ~ +85°C)

Characteristic		Symbol	condition	Min	Typ	Max	Unit	Note
Input Voltage	High	V_{IH}	-	0.7V_{DD}	-	V_{DD}	V	*1
	Low	V_{IL}		V_{SS}	-	0.3V_{DD}		
Output Voltage	High	V_{OH}	I_{OH}=-0.4 mA	V_{DD}-0.4	-	-	V	*2
	Low	V_{OL}	I_{OL}=0.4 mA	-	-	0.4		
Input Leakage Current		I_{LKG}	V_{IN}=V_{DD}~V_{SS}	-1.0	-	1.0	µA	*1
OSC Frequency		f_{OSC}	Rf=47 kΩ ± 2% Cf=20pf ± 5%	315	450	585	KHz	
On Resistance (Vdiv-Ci)		R_{ON}	V_{DD}-V_{EE} =17V Load current = ±150µA	-	-	1.5	kΩ	
Operating Current		I_{DD1}	Master mode 1/128 Duty	-	-	1.0	mA	*3
		I_{DD2}	Slave mode 1/128 Duty	-	-	200	µA	*4
Supply Current		I_{EE}	Master mode 1/128 Duty	-	-	100		*5
Operating Frequency		f_{op1}	Master mode External clock	50	-	600	KHz	
		f_{op2}	Slave mode	0.5	-	1500		

*1. Applies to input terminals FS, DS1, DS2, CR, SHL, MS and PCLK2 and I/O terminals DIO1, DIO2, M and CL2 in the input state.
*2. Applies to output terminals CLK1, CLK2 and FRM and I/O terminals DIO1, DIO2, M and CL2 in the output state.
*3. This value is specified at about the current flowing through V_{SS}.
Internal oscillation circuit: Rf=47 kΩ, Cf=20 pF
Each terminal of DS1, DS2, FS, SHL and MS is connected to V_{DD} and out is no load.
*4. This value is specified at about the current flowing through V_{SS}.
Each terminal of DS1, DS2, FS, SHL, PCLK2 and CR is connected to V_{DD}, and MS is connected to V_{SS}. CL2, M, DIO1 is external clock.
*5. This value is specified at about the current flowing through V_{EE}.
Don't connect to V_{LCD} (V1~V5).

2.5 Optical Characteristics Absolute maximum ratings

Item	Symbol	Rating	Unit
Applied voltage AC	VAC	15	V
Operating temperature range	Top	0~50	°C
Storage temperature range	Tst	-20~60	°C

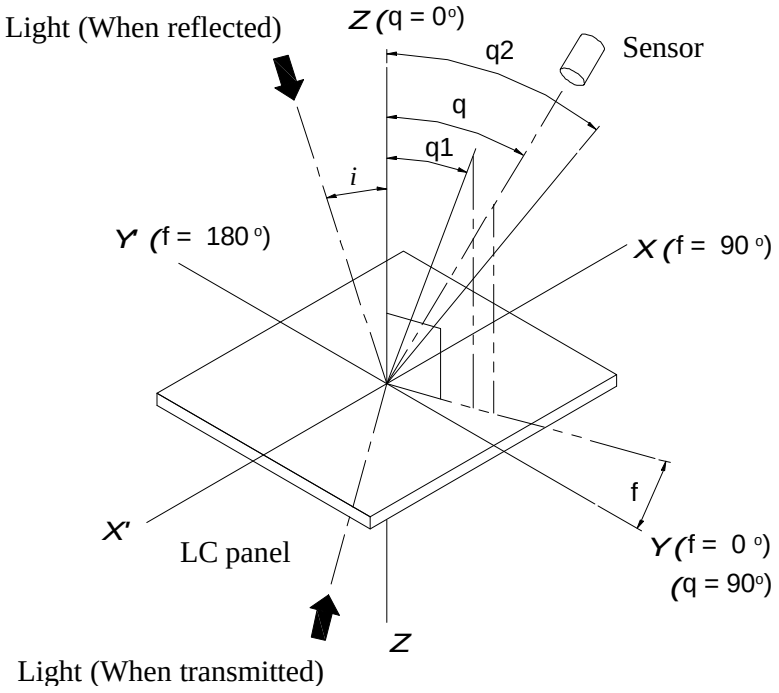
2.6 Optical Characteristics

1/64 duty, 1/9 bias

Item	Symbol	Temp.	Min.	Typ.	Max.	Unit
Driving voltage	Vop	0°C	12.1	12.8	13.5	V
		25°C	11.3	12.0	12.7	
		50°C	10.4	11.1	11.8	
Contrast	K	θ=0° ϕ=0°	2	2.7	--	--
Frame freq.	fF	--	--	70	--	Hz
Viewing angle*	θ_1	25°C	-35	--	40	deg.
	θ_2		-35	--	35	
Response time	t_{on}	25°C	--	140	210	ms
	t_{off}		--	220	330	

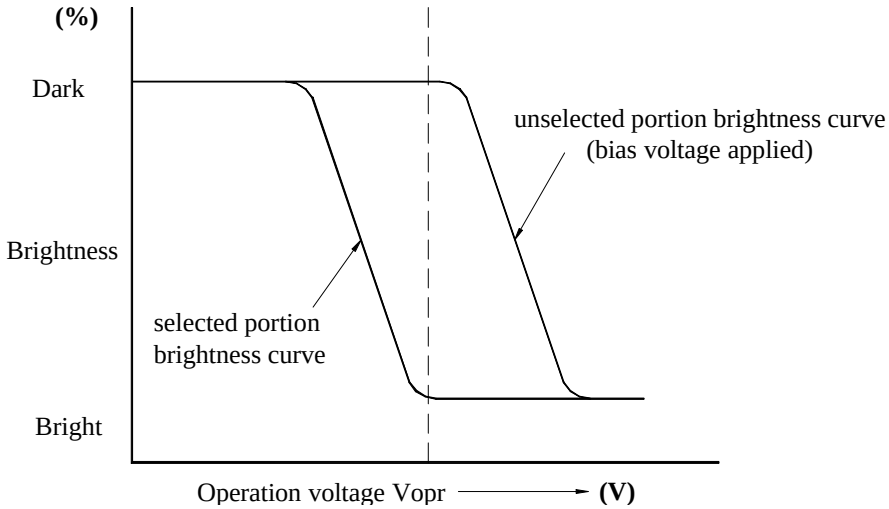
2.6.1 Definition of optical characteristics

* Definition of angles ϕ and θ

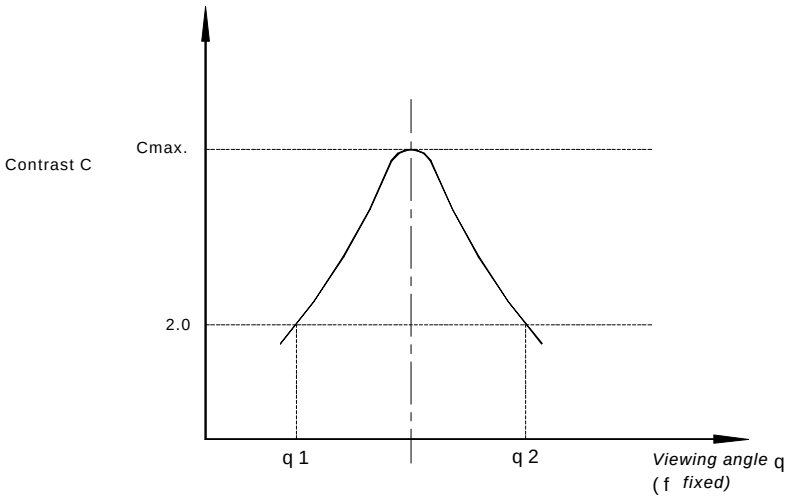


*Definition of contrast C

$$C = \frac{B1}{B2} = \frac{\text{Brightness of selected portion}}{\text{Brightness of unselected portion}}$$

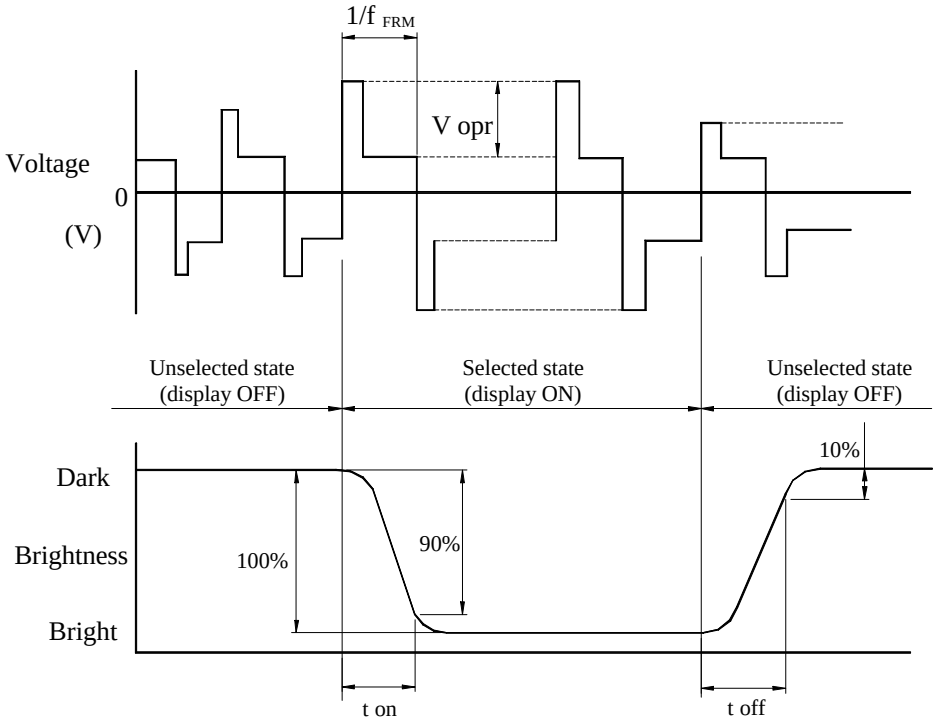


* Definition of viewing angles θ1 and θ2



Note : Optimum vision with the naked eye and viewing angle θ at Cmax above are not always the same.

* Definition of response time



Vopr : Operating voltage (V)
fFRM : Frame frequency (Hz)
ton : Response time (rsie) (ms)
toff : Response time (fall) (ms)

3. RELIABILITY

3.1 Reliability

Test item	Test condition	Evaluation and assessment
Operation at high temperature and humidity	40 °C±2 °C 90%RH for 500hours	No abnormalities in functions* and appearance**
Operation at high temperature	60 °C±2 °C for 500 hours	No abnormalities in functions* and appearance**
Heat shock	-20± ~ +60 °C Left for 1 hour at each temperature, transition time 5 min, repeated 10times	No abnormalities in functions* and appearance**
Low temperature	-20±2 °C for 500 hours	No abnormalities in functions* and appearance**
Vibration	Sweep for 1 min at 10 Hz, 55Hz, 10Hz, amplitude 1.5mm 2 hrs each in the X,Y and Z directions	No abnormalities in functions* and appearance**
Drop shock	Dropped onto a board from a height of 10cm	No abnormalities in functions* and appearance**

* dissipation current, contrast and display functions

** Polarizing filter deterioration, other appearance defects

3.2 Liquid crystal panel service life

100,000 hours minimum at 25 °C±10 °C

3.3 definition of panel service life

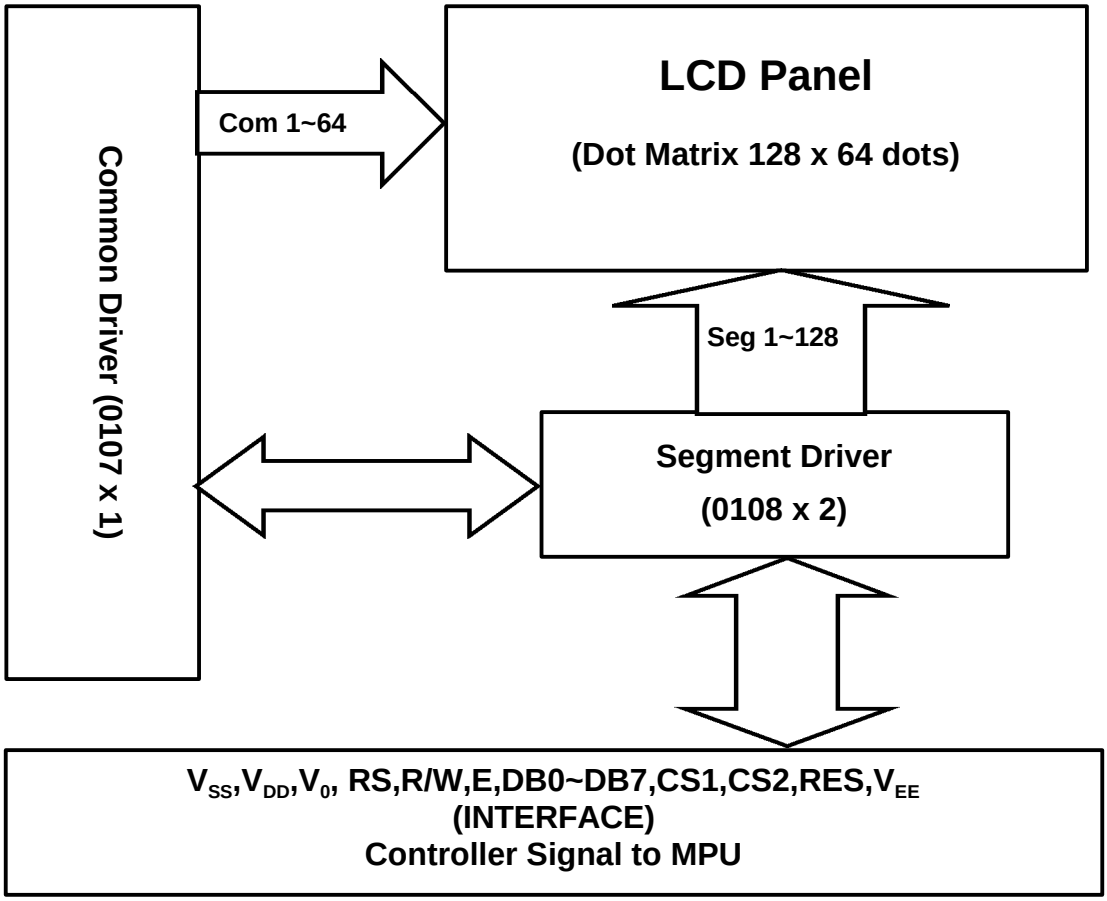
- Contrast becomes 30% of initial value
- Current consumption becomes three times higher than initial value
- Remarkable alignment deterioration occurs in LCK cell layer
- Unusual operation occurs in display functions

4. OPERATING INSTRUCTIONS

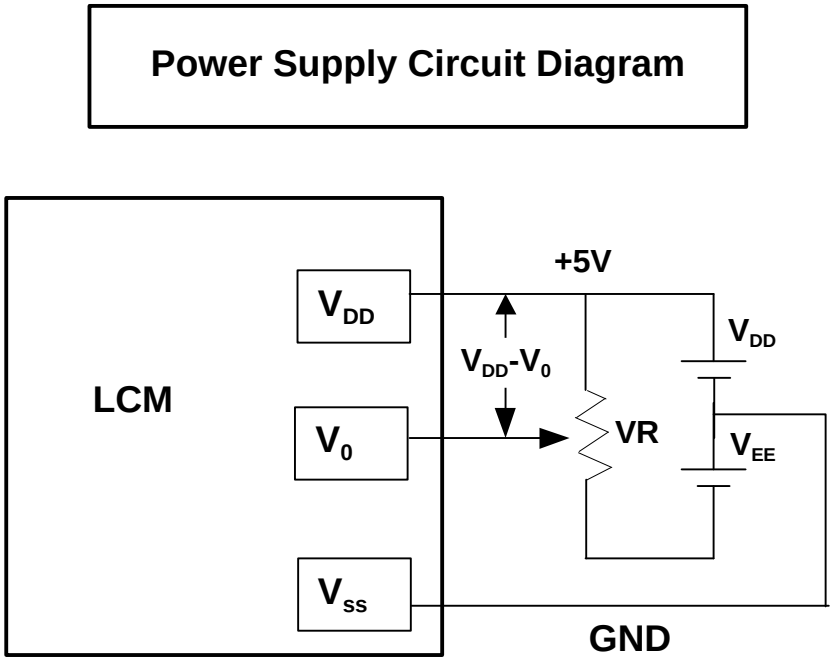
4.1 Input signal Function

NO.	Symbol	Function
1	VSS	Ground (0V)
2	VDD	Power supply for Logic circuit (+)
3	V0	Power supply for LCD
4	RS	H: Instruction L: Data
5	R/W	Read/Write
6	E	Enable Signal
7-14	DB0-DB7	Data Bus Line
15	CS1	Chip Selection For IC1
16	CS2	Chip Selection For IC2
17	/RES	Reset Active “L”
18	VEE	Power supply for LCD (0V)
19	LED 1	Power supply for LED
20	LED 2	Power supply for LED

4.2 Circuit Block Diagram



4.3 Voltage Generator Circuit

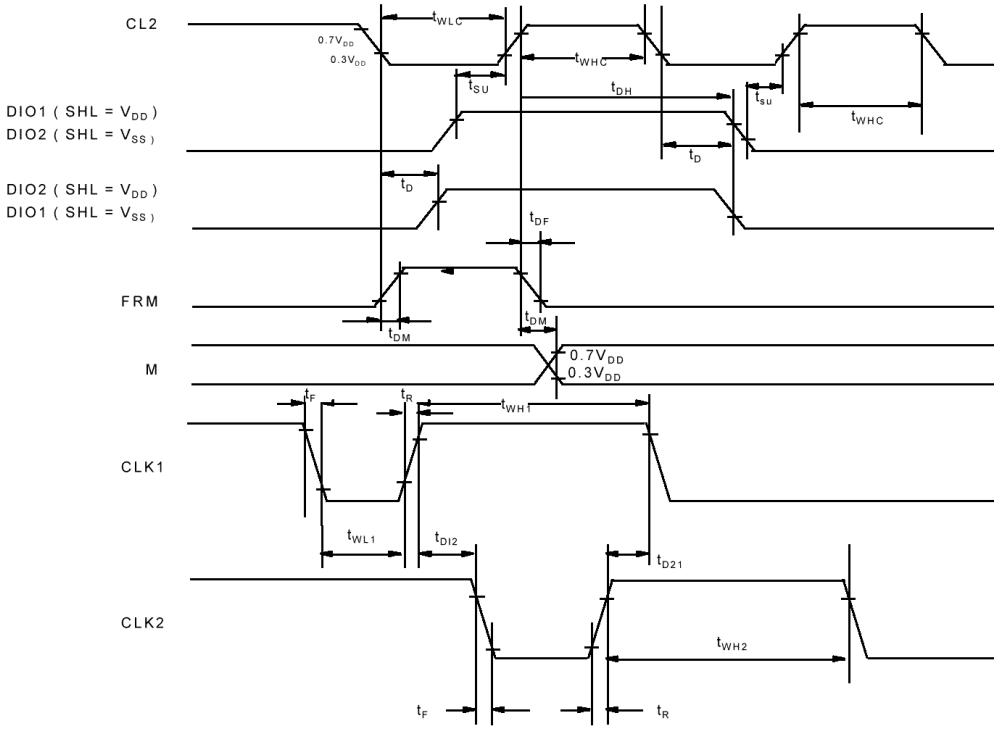


V_{DD} - V_0 : LCD Driving Voltage
VR : 10K~20K

4.4 Timing Characteristics

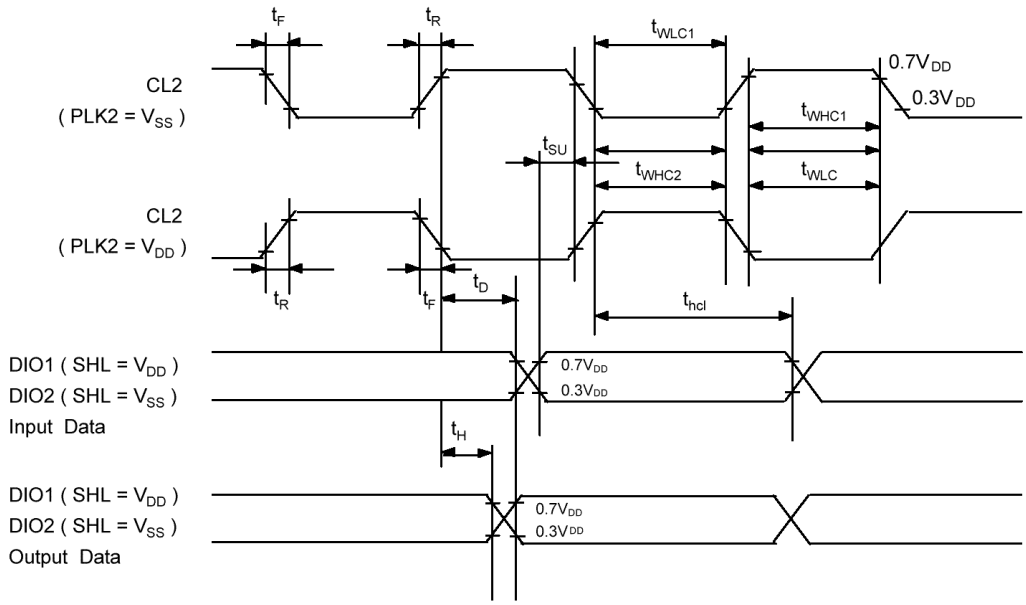
AC Characteristics (VDD=5V ±10%, Ta=-30°C~+85°C)

1. Master mode (MS=V_{DD}, PCLK2=V_{DD}, Cf=20 pF, Rf=47 kΩ)



Characteristic	Symbol	Min	Typ	Max	Unit
Data Setup Time	t_{SU}	20	-	-	µs
Data Hold Time	t_{DH}	40	-	-	
Data Delay Time	t_D	5	-	-	
FRM Delay Time	t_{DF}	-2	-	2	
M Delay Time	t_{DM}	-2	-	2	
CL2 Low Level Width	t_{WLC}	35	-	-	
CL2 High Level Width	t_{WHC}	35	-	-	
CLK1 Low Level Width	t_{WL1}	700	-	-	ns
CLK2 Low Level Width	t_{WL2}	700	-	-	
CLK1 High Level Width	t_{WH1}	2100	-	-	
CLK2 High Level Width	t_{WH2}	2100	-	-	
CLK1-CLK2 Phase Difference	t_{D12}	700	-	-	
CLK2-CLK1 Phase Difference	t_{D21}	700	-	-	
CLK1, CLK2 Rise/Fall Time	t_R/t_F	-	-	150	

2. Slave mode (MS=V_{SS})



Characteristics	Symbol	Min	Typ	Max	Unit	Note
CL2 Low Level Width	t_{WLC1}	450	-	-	ns	PCLK2=V_{SS}
CL2 High Level Width	t_{WHC1}	150	-	-	ns	PCLK2=V_{SS}
CL2 Low Level Width	t_{WLC2}	150	-	-	ns	PCLK2=V_{DD}
CL2 High Level Width	t_{WHL}	450	-	-	ns	PCLK2=V_{DD}
Data Setup Time	t_{SU}	100	-	-	ns	
Data Hold Time	t_{DH}	100	-	-	ns	
Data Delay Time	t_D	-	-	200	ns	*1
Output Data Hold Time	t_H	10	-	-	ns	
CL2 Rise/Fall Time	t_R/t_F	-	-	30	ns	

4.5 Operating Principles & Methods

OPERATING PRINCIPLES & METHODS

1. I/O Buffer

Input buffer controls the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS1B-CS3.

2. Input register

Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display RAM.

When CS1B to CS3 are in the active mode, R/W and RS select the input register. The data from MPU is written into input register. Then Writing it into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

3. Output register

Output register stores the data temporarily from display data RAM when CS1B, CS2B and CS3 are in active mode and R/W a RS=H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W=H, RS=L, status data (busy check) can read out.

To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is, to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

RS	R/W	Function
L	L	Instruction
	H	Status read (busy check)
H	L	Data write (from input register to display data RAM)
	H	Data read (from display data RAM to output register)

4. Reset

The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU When RSTB becomes low, following procedure is occurred.

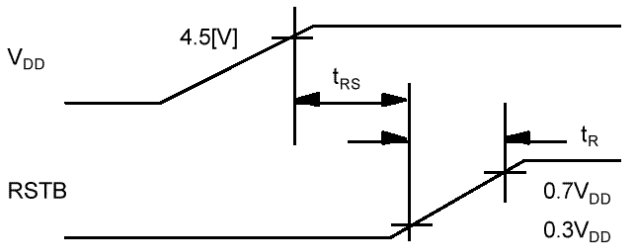
1. Display off
2. Display start line register become set by 0.(Z-address 0)

While RSTB is low, No instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4=0 (clear RSTB) and DB7=0 (ready) by status read instruction.

The Conditions of power supply at initial power up are shown in table 1.

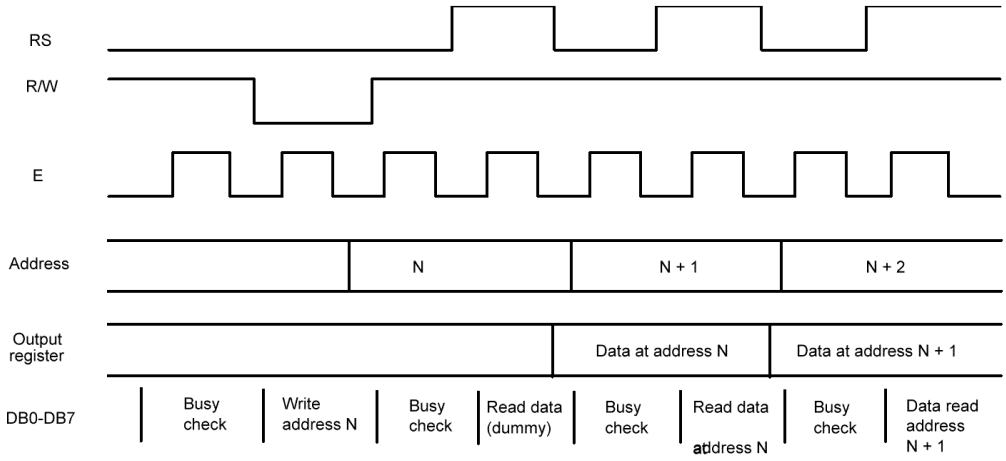
Table 1. Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset Time	t_{RS}	1.0	-	-	us
Rise Time	t_R	-	-	200	ns

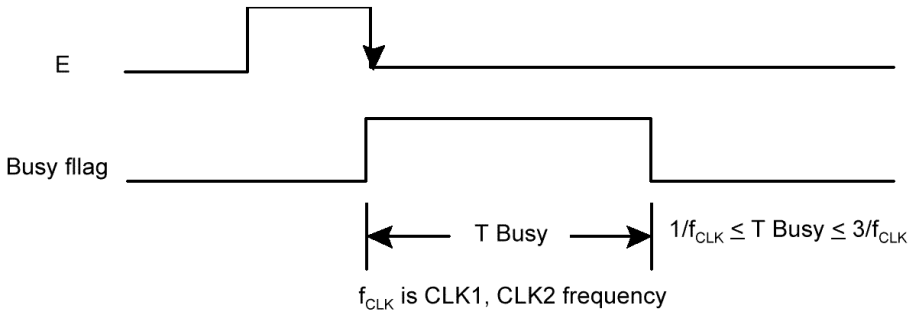


5. Busy flag

Busy flag indicates that KS0108B is operating or no operating. When busy flag is high, KS0108B is in internal operating.
When busy flag is low, KS0108B can accept the data or instruction.
DB7 indicates busy flag of the KS0108B.



Busy Check



Busy Flag

6. Display On/Off Flip - Flop

The display on/off flip-flop makes on/off the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non selective voltage appears on segment output terminals. When flip-flop is set (logic high), non selective voltage appears on segment output terminals regardless of display RAM data.
The display on/off flip-flop can changes status by instruction. The display data at all segment disappear while RSTB is low.
The status of the flip-flop is output to DB5 by status read instruction.
The display on/off flip-flop synchronized by CL signal.

7. X Page Register

X page register designates pages of the internal display data RAM.
Count function is not available. An address is set by instruction.

8. Y address counter

Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by read or write operations of display data.

9. Display Data RAM

Display data RAM stores a display data for liquid crystal display. To indicate on state dot matrix of liquid crystal display, write data 1. The other way, off state, writes 0.
Display data RAM address and segment output can be controlled by ADC signal.
ADC=H⇒ Y-address 0:S1 ~ Y address 63:S64
ADC=L⇒ Y-address 0:S64 ~ Y address 63:S1
ADC terminal connect the V_{DD} or V_{SS}.

10. Display Start Line Register

The display start line register indicates of display data RAM to display top line of liquid crystal display.
Bit data (DB<0:5>) of the display start line set instruction is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter.
It is used for scrolling of the liquid crystal display screen.

4.6 Display control instruction

The display control instructions control the internal state of the KS0108B. Instruction is received from MPU to KS0108B for the display control. The following table shows various instructions.

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Display ON/OFF	L	L	L	L	H	H	H	H	H	L/H	Controls the display on or off. Internal status and display RAM data is not affected. L:OFF, H:ON
Set Address (Y address)	L	L	L	H	Y address (0~63)						Sets the Y address in the Y address counter.
Set Page (X address)	L	L	H	L	H	H	H	Page (0~7)			Sets the X address at the X address register.
Display Start Line (Z address)	L	L	H	H	Display start line (0~63)						Indicates the display data RAM displayed at the top of the screen.
Status Read	L	H	BUSY	L	ON/OFF	RESET	L	L	L	L	Read status. BUSY L: Ready H: In operation ON/OFF L: Display ON H: Display OFF RESET L: Normal H: Reset
Write Display Data	H	L	Write Data								Writes data (DB0:7) into display data RAM. After writing instruction, Y address is increased by 1 automatically.
Read Display Data	H	H	Read Data								Reads data (DB0:7) from display data RAM to the data bus.

1. Display On/Off

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

The display data appears when D is 1 and disappears when D is 0.
Though the data is not on the screen with D=0, it remains in the display data RAM.
Therefore, you can make it appear by changing D=0 into D=1.

2. Set Address (Y Address)

S	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Y address (AC0 ~ AC5) of the display data RAM is set in the Y address counter.
An address is set by instruction and increased by 1 automatically by read or write operations of display data.

3. Set Page (X Address)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	AC2	AC1	AC0

X address(AC0 ~ AC2) of the display data RAM is set in the X address register.
Writing or reading to or from MPU is executed in this specified page until the next page is set.

4. Display Start Line (Z Address)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	AC5	AC4	AC3	AC2	AC1	AC0

Z address (AC0 ~ AC5) of the display data RAM is set in the display start line register and displayed at the top of the screen.
When the display duty cycle is 1/64 or others(1/32 ~ 1/64), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

5. Status Read

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	BUSY	0	ON/OFF	RESET	0	0	0	0

- BUSY
  When BUSY is 1, the Chip is executing internal operation and no instructions are accepted.
  When BUSY is 0, the Chip is ready to accept any instructions.
- ON/OFF
  When ON/OFF is 1, the display is on.
  When ON/OFF is 0, the display is off.
- RESET
  When RESET is 1, the system is being initialized.
  In this condition, no instructions except status read can be accepted.
  When RESET is 0, initializing has finished and the system is in the usual operation condition.

6. Write Display Data

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	D7	D6	D5	D4	D3	D2	D1	D0

Writes data (D0 ~ D7) into the display data RAM.
After writing instruction, Y address is increased by 1 automatically.

7. Read Display Data

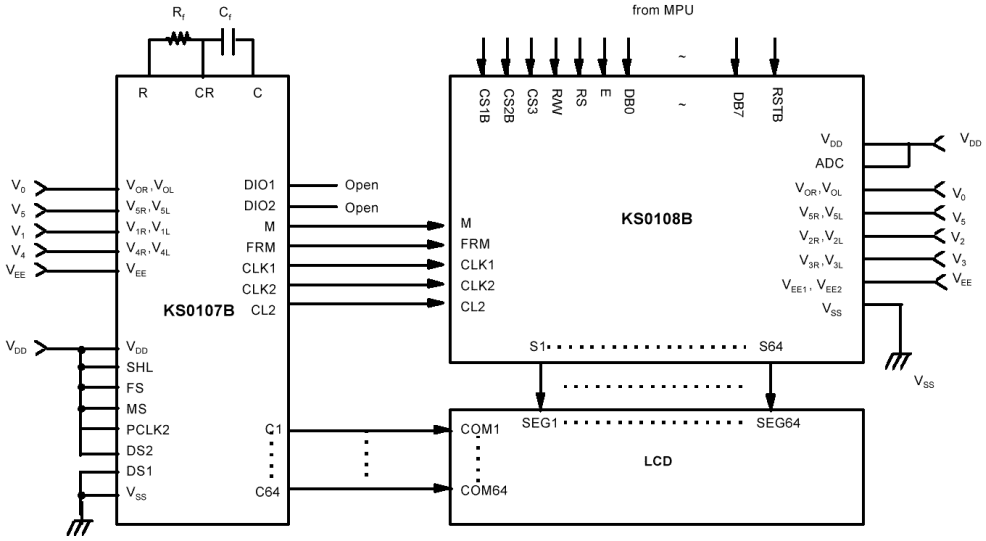
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

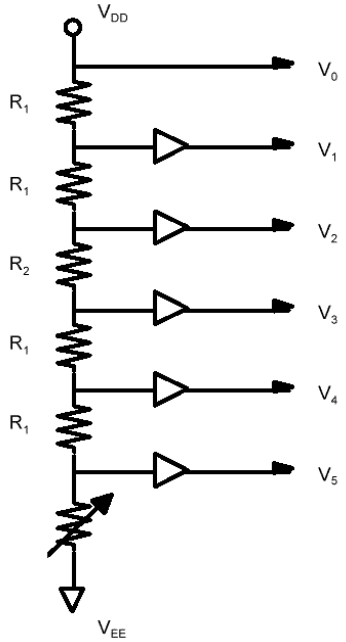
Reads data (D0 ~ D7) from the display data RAM.
After reading instruction, Y address is increased by 1 automatically.

4.7 Application circuit

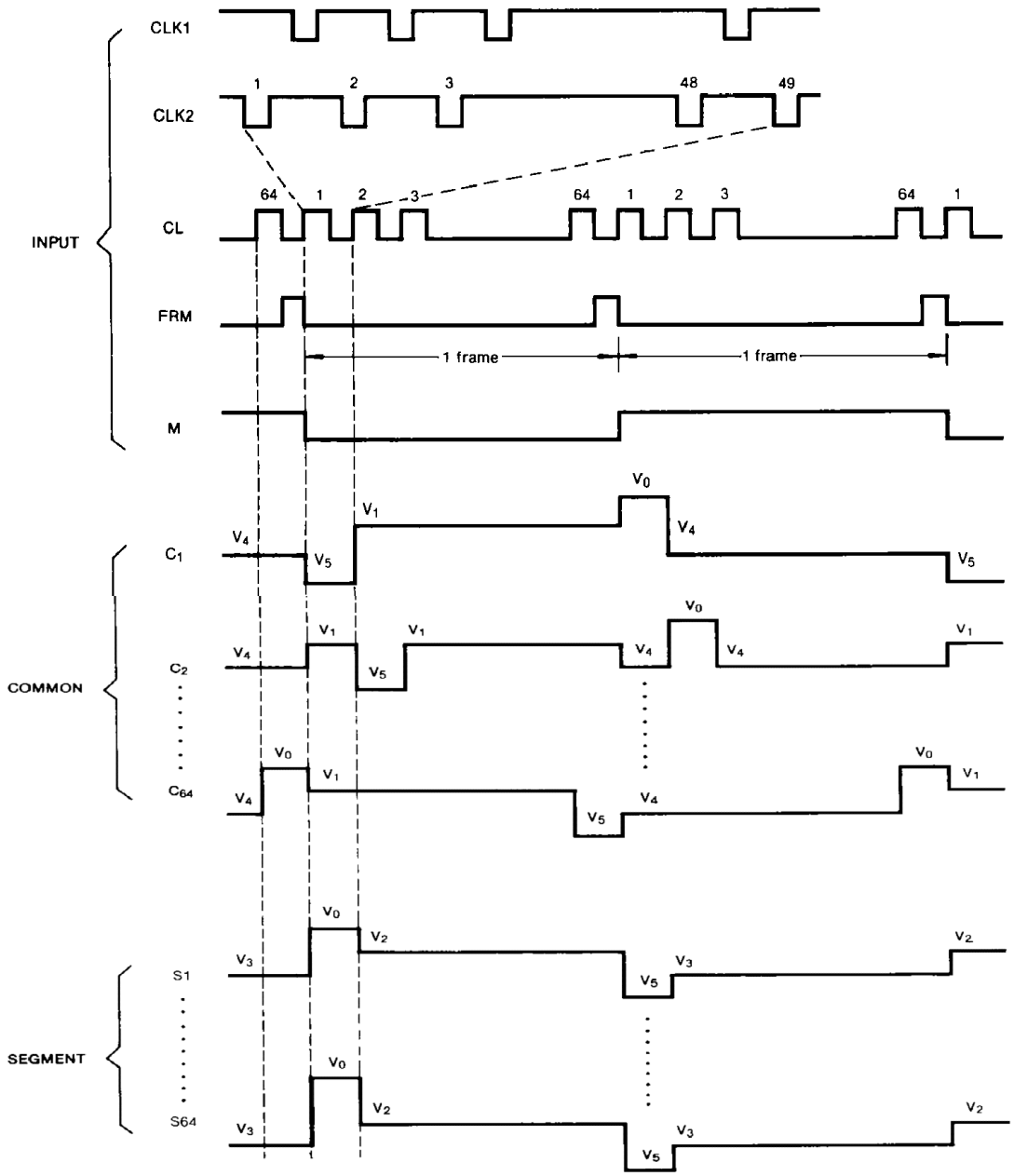
APPLICATION CIRCUIT

1.1/64 duty common driver(KS0107B) interface circuit

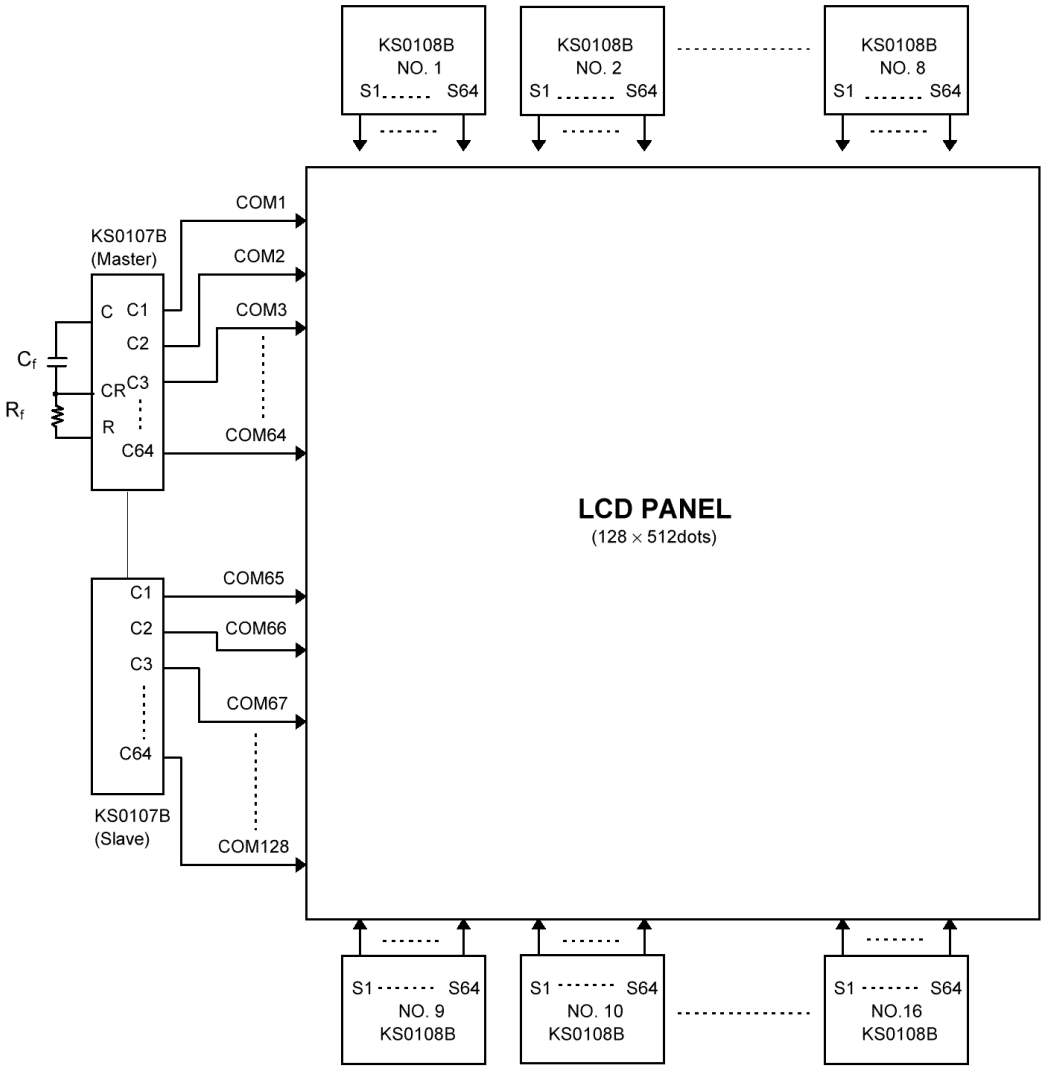




2. Timing diagram (1/64 duty)



3. LCD Panel interface application circuit



5. NOTES

Safety

- If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is plate glass; do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizing plate of the display is very fragile; handle it very carefully

Mounting and Design

- Mount the module by using the specified mounting part and holes.
- To protect the module from external pressure, leave a small gap by placing transparent plates (e.g. acrylic or glass) on the display surface, frame, and polarizing plate
- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Avoid condensation, otherwise the transparent electrodes may break.

Storage

- Store the module in a dark place where the temperature is 25°C±10°C and the humidity below 65% RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module (including accessories).

Cleaning

- Do not wipe the polarizing plate with a dry cloth, as it may scratch the surface.
- Wipe the module gently with soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetoe) or aromatic solvents (toluene and xylene), as they may damage the polarizing plate.

6. OPERATION PRECAUTIONS

Any changes that need to be made in this specification or any problems arising from it will be dealt with quickly by discussion between both companies.

7. LCM Dimension