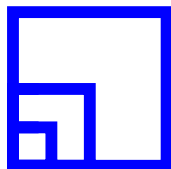


Arca210

Application Design Guide

Revision: 1.0



ARCA Technology Corporation

**Jan. 2003
Beijing, China**

Arca210

Application Design Guide

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Release history

Date	Revision	Change
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Related Documentation From ARCA

Arca Instruction Set Architecture Manual – version 2

Arca210 Hardware Manual

Draco Development Kit for Arca210 Hardware User's Guide

Draco Development Kit for Arca210 Software User's Guide

ARCABoot User's Guide

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1 Introduction

The Arca™ is a Reduced Instruction Set Computer (RISC) architecture which is designed specifically to address the applications requirements and challenges for IA (Information Application) and embedded market. As the second generation of Arca series RISC microprocessor, Arca210 is a high performance system-on-chip (SOC) microprocessor that integrates Arca RISC core, memory controller, PCI controller and other peripheral controllers such as DMA, MAC, USB, AC97, UART, IrDA, SCC, I2C, GPIO and so on.

This document is addressed to present recommendation on schematics and PCB of application design based on Arca210 microprocessor.

1.1 Block Diagram

The system architecture of Arca210 is shown in the following diagram:

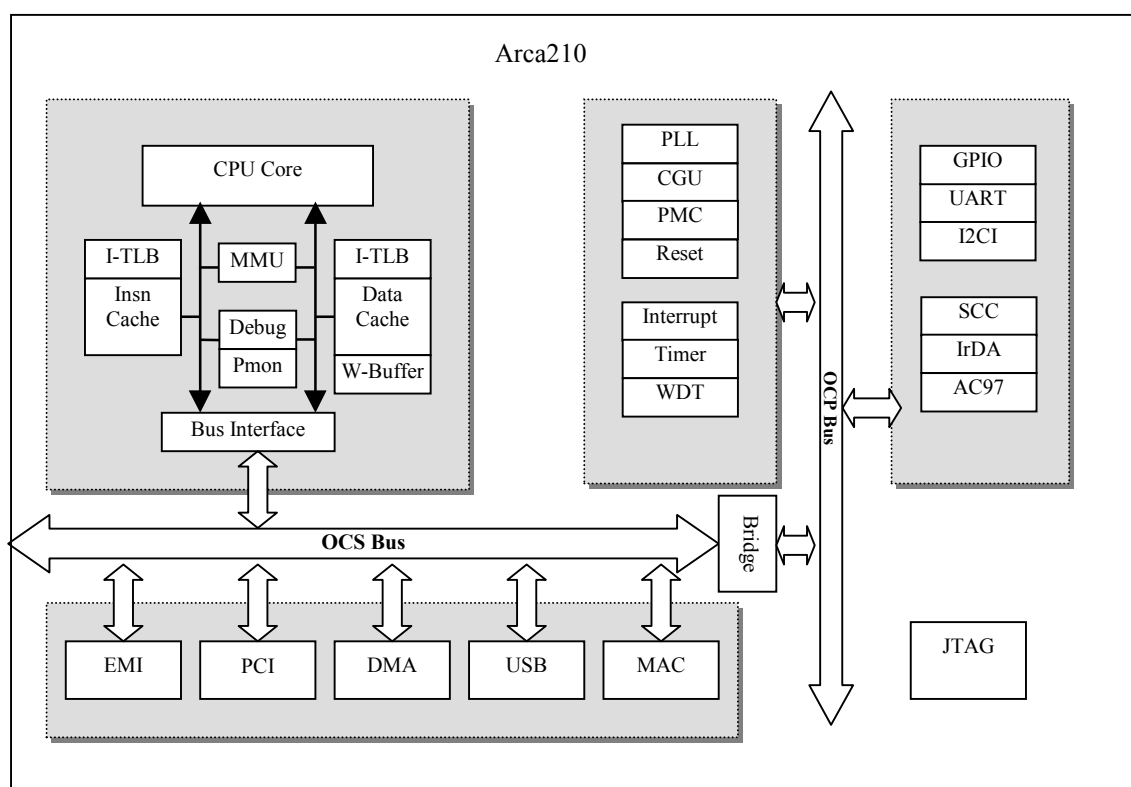


Figure 1-1 Block Diagram of Arca210

Arca210 consists of the following three functional groups:

■ Processor Core

The processor core contains CPU, memory management unit, caches and a bus interface unit. The processor core adopts a Harvard memory architecture that contains 16k byte instruction cache and 16k byte data cache. For data cache, 16 word write back buffer is provided to reduce the performance lost due to bus conflict. Instruction address and data address are translated through separate 128 entry Instruction TLB and 128 entry data TLB.

A debug module with JTAG interface is embedded in the core to assist software, especially kernel code debugging. PMON module is used to monitor CPU-core's performance such as, clock number, instruction executed number, cache miss number and etc.

■ OCS Bus Devices

Devices requiring high performance memory bandwidth or to be in close proximity to the CPU are connected to OCS bus. Arca210 OCS bus devices include memory controller, PCI bus interface controller, DMA controller, USB controller and Ethernet controller. The high speed of the OCS bus guarantees the high bandwidth requirements between CPU and external high speed devices.

■ OCP Bus Devices

Devices that don't need a high bandwidth connection are connected in OCP (On Chip Peripheral) bus. These include clock generation unit, power management unit, interrupt controller, timer, real time clock, watchdog timer, general purpose IO, UART, smart card controller, IrDA, I²C interface and AC97 controller.

1.2 Features

The Arca210 is a highly integrated, low-cost implementation of the Arca RISC architecture, that includes many function units, can be used in a single board design. The features of Arca210 are listed in Table 1-1.

Table 1-1 Arca210 Features

Item	Features
Integer Unit	<ul style="list-style-type: none"> • Arca version 2 architecture, 32-bit Arca instruction set. • 32-bit internal data bus • Thirty-two 32-bit general registers • 5-stage pipeline • Virtual address space: 4 G-Bytes • Space identifier ASID: 8 bits, 256 virtual address space
Memory Manager Unit (MMU)	<ul style="list-style-type: none"> • 4 G-Bytes of address space, 256 address space (8 bits ASID) • Full associative 32-entry instruction TLB (ITLB) and 32-entry data TLB (DTLB), with round robin replacement algorithm • Four different page size: 4KB, 16KB, 1MB and 16MB in any entry • Support entry lock • Translate 32-bit virtual address to 32-bit physical address • Support five address spaces
Data Cache	<ul style="list-style-type: none"> • 16K-Byte, physically-indexed, virtually-tagged • Hardware solve alias issue • 32-way set associative: 8 sets with each set containing 32 ways • Each way contains 32 bytes (one cache line) • Write-back, write-through, round robin algorithm • 4-deep write buffer • Support lock, allocate operations
Instruction Cache	<ul style="list-style-type: none"> • 16K-Byte, physically-indexed, virtually-tagged • 32-way set associative: 8 sets with each set containing 32 ways • Each way contains 32 bytes (one cache line) • Support lock operation
DEBUG	<ul style="list-style-type: none"> • JTAG interface to host machine • ASID match • Two instruction break point or one maskable instruction break

	<ul style="list-style-type: none"> point Two data break point or one maskable data break point Software break Asynchronous break from host machine Asynchronous boot from host machine
Performance Monitor (PMON)	<ul style="list-style-type: none"> One 32-bits internal clock counter Two 32-bits signal counter, each of which can be set to count 1 from 14 signals Count overflow interrupt support
External Memory Interface (EMI)	<ul style="list-style-type: none"> Static memory controller <ul style="list-style-type: none"> Direct interface to ROM, Burst ROM, SRAM, Flash and memory like devices 8, 16 or 32-bit bus width 4 banks up to 256M (64M X 4) Programmable wait and external wait signal Synchronous DRAM controller <ul style="list-style-type: none"> Both DIMM and SODIMM are supported 32-bit bus width Four banks up to 1G (256M x 4) is supported Supports burst operation Page mode supported Has both auto-refresh and self-refresh functions
PCI Controller	<ul style="list-style-type: none"> PCI revision 2.1 32-bit, 33MHz Supports (in host mode) up to 4 external bus masters or slaves Supports (in host mode) bus arbitration between host and 4 external masters Support host and satellite mode Support transaction between Arca210 CPU and PCI slaves Support direct transaction between external master and system device Four 8-deep FIFO for each transaction
Direct Memory Access controller (DMA)	<ul style="list-style-type: none"> Four independent DMA channels with fix or round robin priority Up to 16M transfer count Transfer data unit: byte, half-word, word, 4-word or 8-word Support external DMA request
Ethernet Controller (ETHC)	<ul style="list-style-type: none"> Compliant with IEEE802.3, 802.3u Specification 10/100 Mbps data transfer rates IEEE802.3 compliant MII interface to talk to an external PHY VLAN support Full and half duplex modes Support CSMA/CD protocol in half duplex mode Supports flow-control for full-duplex operation Provides External and internal loop back capability on the MII Interface
USB Host Controller (UHC)	<ul style="list-style-type: none"> Open Host Controller Interface (OHCI)-compatible and USB Revision 1.1-compatible Support low-speed (1.5 Mbps) and full-speed (12 Mbps) USB devices Two downstream ports are provided
Clock Generation Unit (CGU)	<ul style="list-style-type: none"> On-chip phase-locked loop (PLL) with programmable multiple-ratio On-chip oscillator circuit 5 clock modes can be selected by MD0 ~ MD2 The PLL on/off is programmable by software Input clock source can be selected from oscillator or an external

	<p>clock input</p> <ul style="list-style-type: none"> Generates three clocks: internal clock (iclk) for CPU core, peripheral clock (pclk) for peripheral devices, system clock (sclk) for system bus devices Iclk, pclk and sclk frequency can be changed separately for software by setting division ratio
Interrupt controller (INT)	<ul style="list-style-type: none"> Eight external interrupt pins (IRQ0 – IRQ7) On-chip peripheral interrupts
Universal Asynchronous Receiver/Transmitter (UART)	<ul style="list-style-type: none"> Full-duplex communication 16-byte FIFO for transmission/reception DMA can be transferred Modem control functions (RTS and CTS) are provided
Watchdog Timer (WDT)	<ul style="list-style-type: none"> Generates power-on reset or manual reset 16-bit counter
Timer Unit (TMU)	<ul style="list-style-type: none"> 3-channel auto-reload-type 32-bit timer 5 types of counter input clocks can be selected Auto-reload function is provided for each channel
Power/reset Management Controller (PMC)	<ul style="list-style-type: none"> Supports three low-power modes and function: sleep mode, standby mode, module stop function Reset sequence control
I ² C-Bus Interface (I2CI)	<ul style="list-style-type: none"> Supports only single master mode Support of I²C standard-mode and F/S-mode up to 400 kHz Independent, programmable serial clock generator The number of devices that you can connect to the same I²C-bus is limited only by the maximum bus capacitance of 400pF
Smart Card Controller (SCC)	<ul style="list-style-type: none"> Conforms to the ISO/IEC standard 7816-3 Support asynchronous character (T=0) and block (T=1) communication modes Receiver and Transmit mode error signal detection and automatic re-transmission of data (T = 0) Supports both direct convention and inverse convention A straightforward extension of UART: When SCC is disabled, UART can work as a normal UART
Infrared Serial Interface (IrDA)	<ul style="list-style-type: none"> Based on the IrDA 1.0 specification Polarity of transmitted and received signals selectable When transmitting, support normal 3/16 and IrDA low-power mode bit duration When receiving, normal 3/16 and low-power mode bit duration signal will both be received as low-power mode bit duration A straightforward extension of UART2: When IrDA is disabled, UART2 can work as a normal UART
AC97 Controller (AC97)	<ul style="list-style-type: none"> Compliant with AC'97 Component Specification 2.2 Support 16, 18, 20bit sample size Programmable Output channels and Input channels Support Power Down Mode Two Wake-Up mode Support Support DMA transfer mode
General Purpose Input/Output Port (GPIO)	<ul style="list-style-type: none"> 8 bits dedicated ports 39 shared ports

1.3 Pin Description

The pin description of Arca210 is shown as Table 1-1.

Table 1-1 Arca210 Pin Description (total: 304pin)

Pin Name	I/O	Pin Description
1. EMI pins (total 85)		
D[31:0]	IO	Memory data bus
A[25:0]	O	SDRAM memory address For SDRAM, A[16:2] is used as SDRAM address signals /A[20:18]/MD_CLK[2:0]: used as the clock mode configuration when power-up, should be pull-up or pull-down with 4.7-10KΩ resistor for clock mode configuration, it will be latched at the rising-edge of the RESETP_ signal Add[20:18] Core-CLK : OCS_CLK(SDAM Clock CKO[3:0]) 000 1 : 1 001 1 : 2 010 1 : 3 (default, pull-down/pull-up internal) 011 1 : 4 100 Test Mode 101 1 : 6 110 1 : 8 111 No used /A[1]/MD_Endian: used as the Endian configuration when power-up, should be pull-up or pull-down with 4.7-10KΩ resistor for Arca2 Endian configuration, it will be latched at the rising-edge of the RESETP_ signal 0: Big-Endian (default, pull-down internal) 1: Little-Endian
CS0_	O	Static memory bank0 chip select
CS1_	O	Static memory bank1 chip select
CS2_	O	Static memory bank2 chip select
CS3_	O	Static memory bank3 chip select
CS4L_	O	SDRAM bank4 chip select When SDRAM is used, chip select signal to indicate that bank 4 is being accessed
CS4H_	O	SDRAM bank4 upper chip select When SDRAM SODIMM is used, selection signal for D32-D39. When SDRAM DIMM is used, chip select signal to indicate that upper half of bank 4 is being accessed
CS5L_	O	SDRAM bank5 chip select When SDRAM is used, chip select signal to indicate that bank 5 is being accessed
CS5H_	O	SDRAM bank5 upper chip select When SDRAM SODIMM is used, selection signal for D40-D47. When SDRAM DIMM is used, chip select signal to indicate that upper half of bank 5 is being accessed
CS6L_	O	SDRAM bank6 chip select When SDRAM is used, chip select signal to indicate that bank 6 is being accessed

CS6H_	O	SDRAM bank6 upper chip select When SDRAM SODIMM is used, selection signal for D48-D55. When SDRAM DIMM is used, chip select signal to indicate that upper half of bank 6 is being accessed
CS7L_	O	SDRAM bank7 chip select When SDRAM is used, chip select signal to indicate that bank 7 is being accessed
CS7H_	O	SDRAM bank7 upper chip select When SDRAM SODIMM is used, selection signal for D56-D63. When SDRAM DIMM is used, chip select signal to indicate that upper half of bank 7 is being accessed
RAS_	O	SDRAM Row address strobe
CAS_	O	SDRAM Column address strobe
WE0_	O	Byte 0 write enable When static memory is used, selects D7-0 write strobe signal. When SDRAM is used, selection signal for D7-D0
WE1_	O	Byte 1 write enable When static memory is used, selects D15-8 write strobe signal When SDRAM is used, selection signal for D15-D8
WE2_	O	Byte 2 write enable When static memory is used, selects D23-16 write strobe signal When SDRAM is used, selection signal for D23-D16
WE3_	O	Byte 3 write enable When static memory is used, selects D31-24 write strobe signal When SDRAM is used, selection signal for D31-D24
RDWR_	O	Data bus direction designation signal Also used as SDRAM write designation signal 1 – read, 0 – write
RD_	O	When using static memory, RD# signal, indicates a read cycle
WE_	O	When using static memory: WE# signal, indicates a write cycle
CKE	O	Clock enable for SDRAM
CKO0	O	SDRAM Clock0
CKO1	O	SDRAM Clock1
CKO2	O	SDRAM Clock2
CKO3	O	SDRAM Clock3
WAIT_	I	External Wait state request signal for static memory, pull-up internally
2. PCI pins (total 52)		
AD[31..0]	IO	PCI: Address/Data bus
C/BE[3..0]	IO	PCI: Command/Byte enable
PAR	IO	PCI: Even parity across AD[31:0] and C_[3:0]
CLK	I	PCI clock
RST_	IO	PCI reset
FRAME_	IO	PCI frame
TRDY_	IO	Target ready
IRDY_	IO	initiator ready
STOP_	IO	current target request master to stop current transaction
DEVSEL_	IO	device select
LOCK_	I	Lock access to memory
IDSEL_	I	Initialization device select
PERR_	IO	parity error
SERR_	O	system error
INTA_	IO	Interrupt A
INTB_	I	Interrupt B
INTC_	I	Interrupt C
INTD_	I	Interrupt D

REQ_0_	IO	PCIART: bus request 0, used by Arca210
REQ_1_	I	PCIART: bus request 1
REQ_2_	I	PCIART: bus request 2
REQ_3_	I	PCIART: bus request 3
REQ_4_	I	PCIART: bus request 4
GNT_0_	IO	PCIART: bus grant 0, used by Arca210
GNT_1_	O	PCIART: bus grant 1
GNT_2_	O	PCIART: bus grant 2
GNT_3_	O	PCIART: bus grant 3
GNT_4_	O	PCIART: bus grant 4
3. DMA/GPIO D 6~7/GPIO E 0~2 pins (total 8)		
DREQ0_ /GPE0	IO	DMA external request 0 /GPIO E Inout0
DREQ1_ /GPE1	IO	DMA external request 1 /GPIO E Inout1
DREQ2_ /GPE2	IO	DMA external request 2 /GPIO E Inout2
DACK0 /MD_TAP_SEL	IO	DMA external data acknowledge 0 /MD_TAP_SEL : used as the TAP (Test Access Port, JTAG) mode configuration when power-up, should be pull-up or pull-down with 4.7-10K Ω resistor for TAP mode configuration, it will be latched at the rising-edge of the RESETP_ signal 1: debug 0: boundary (default, pull-down internal)
DACK1 /MD_MEM[0]	IO	DMA external data acknowledge 1 /MD_MEM[0]: used as the boot mode configuration when power-up, should be pull-up or pull-down with 4.7-10K Ω resistor for boot mode configuration, it will be latched at the rising-edge of the RESETP_ signal
DACK2 /MD_MEM[1]	IO	DMA external data acknowledge 2 /MD_MEM[1]: used as the boot mode configuration when power-up, should be pull-up or pull-down with 4.7-10K Ω resistor for boot mode configuration, it will be latched at the rising-edge of the RESETP_ signal <div style="margin-left: 40px;"> MD_MEM[1:0] Boot-Mode 00 8-bit (default, pull-down internal) 01 16-bit 10 32-bit 11 Reserved </div>
AEN /GPD6	IO	DMA transaction enable /GPIO D Inout6
EOP /GPD7	IO	DMA transaction complete /GPIO D Inout7
4. UHC pins (total 9)		
UHC_CLK	I	USB 48MHz Clock Input
DPLS0	IO	USB Port 0 Data Plus
DMNS0	IO	USB Port 0 Data Minus
OVC0	I	USB Port 0 Overcurrent to indicate there is a power supply problem with the port
PPWR0	O	USB Port 0 Power Switch used to enable or disable the external voltage supplying power to the port and is de-asserted when a power supply problem is detected at OVC0 pin
DPLS1	IO	USB Port 1 Data Plus
DMNS1	IO	USB Port 1 Data Minus
OVC1	I	USB Port 1 Overcurrent to indicate there is a power supply problem with the port

PPWR1	O	USB Port 1 Power Switch used to enable or disable the external voltage supplying power to the port and is de-asserted when a power supply problem is detected at OVC1 pin
5. ETHC/GPIO E 3~7/GPIO F pins (total 17)		
MII_COL /GPF7	IO	Ethernet Collision MII_COL shall be asserted by the Ethernet PHY Controller chip upon detection of a collision on the medium, and shall remain asserted while the collision condition persists. The transitions on the MII_COL signal are not synchronous to either the MII_TX_CLK or the MII_RX_CLK. The MAC ignores the signal MII_COL during Full Duplex Operation. /GPIO F Inout0
MII_CRS /GPF6	IO	Ethernet Carrier Sense MII_CRS shall be asserted by the Ethernet PHY Controller Chip when either transmit or receive medium is non idle. MII_CRS shall be de-asserted by the PHY when both the TX medium and the RX medium are idle. The PHY shall ensure that MII_CRS remains asserted throughout the duration of a collision condition. The transitions on the MII_CRS signal are not synchronous to either the MII_TX_CLK or the MII_RX_CLK. /GPIO F Inout1
MII_TX_CLK	I	Ethernet Transmit Clock MII_TX_CLK is a continuous clock that provides for the timing reference for the transfer of the MII_TX_EN, MII_TX_ER, and MII_TXD signals from the MAC to the Ethernet PHY Controller. MII_TX_CLK is sourced by the Ethernet PHY Controller chip. The operating frequency of the MII_TX_CLK is 25 MHz when operating at 100-Mb/s and 2.5 MHz when operating at 10-Mb/s.
MII_TXD[3:0] /GPF[5:2]	IO	Ethernet Transmit Data MII_TXD is a bundle of 4 data signals MII_TXD[3:0] that are driven by the MAC. MII_TXD[3:0] will transition synchronously with respect to the MII_TX_CLK. For each MII_TX_CLK period in which MII_TX_EN is asserted, MII_TXD[3:0] will have the data to be accepted by the Ethernet PHY Controller chip. MII_TXD[0] is the least significant bit. While MII_TX_EN is de-asserted the data presented on MII_TXD[3:0] should be ignored. /MII_TXD[3]: GPIO F Inout5 /MII_TXD[2]: GPIO F Inout4 /MII_TXD[1]: GPIO F Inout3 /MII_TXD[0]: GPIO F Inout2
MII_TX_EN /GPF1	IO	Ethernet Transmit Enable MII_TX_EN indicates that the MAC is presenting nibbles on the MII for transmission. It will be asserted by the Mac with the first nibble of the preamble and will remain asserted while all nibbles to be transmitted are presented to the MII. MII_TX_EN will be negated prior to the first MII_TX_CLK following the final nibble of the frame. MII_TX_EN is driven by the MAC and will transition synchronously with respect to the MII_TX_CLK. When asserted the MII_TX_EN will be at logic '1' and it will be at logic '0' while de-asserted. /GPIO F Inout1
MII_RX_CLK	I	MII_RX_CLK is a continuous clock that provides the timing reference for the transfer of the MII_RX_DV, MII_RX_ER, and MII_RXD signals from the Ethernet PHY Controller to the MAC. MII_RX_CLK is sourced by the Ethernet PHY Controller chip. The MII_RX_CLK shall have a frequency equal to 25% of the data rate of the received signal on the Ethernet Cable.
MII_RX_DV /GPF0	IO	MII_RX_DV is driven by the external Ethernet PHY Controller to indicate the MAC that it is presenting the recovered and decoded

		nibbles on the MII_RXD[3:0] bundle and that the data on MII_RXD[3:0] is synchronous to MII_RX_CLK. MII_RX_DV shall transition synchronously with respect to the MII_RX_CLK. MII_RX_DV shall remain asserted continuously from the first recovered nibble of the frame through the final recovered nibble, and shall be negated prior to the first MII_RX_CLK that follows the final nibble. When asserted the MII_RX_DV will be at logic '1' and it will be at logic '0' while de-asserted. /GPIO F Inout0
MIIRXD[3:0] /GPE[7:4]	IO	MIIRXD is a bundle of four data signals MII_RXD [3:0] that transition synchronously with respect to the MII_RX_CLK. RXD[3:0] are driven by the Ethernet PHY Controller chip. For each MII_RX_CLK period in which MII_RX_DV is asserted, MII_RXD [3:0] transfer four bits of recovered data from the PHY to the ETHC. MII_RXD [0] is the least significant bit. While MII_RX_DV is de-asserted, MII_RXD [3:0] will have no effect on the ETHC. MIIRXD[3]: GPIO E Inout7 MIIRXD[2]: GPIO E Inout6 MIIRXD[1]: GPIO E Inout5 MIIRXD[0]: GPIO E Inout4
MIIRX_ER /GPE3	IO	MIIRX_ER is driven by the Ethernet PHY Controller chip. MII_RX_ER shall be asserted for one or more MII_RX_CLK periods to indicate to the MAC that an error (e.g., a coding error, or any error that the PHY is capable of detecting, and that otherwise be undetectable by the MAC) was detected some where in the frame presently being transferred from the PHY to the MAC. MII_RX_ER shall transition synchronously with respect to MII_RX_CLK. While MII_RX_DV is de-asserted, MII_RX_ER will have no effect on the MAC. When asserted the MII_RX_ER will be at logic '1' and it will be at logic '0' while de-asserted. /GPIO E Inout3
MIIMDC	O	Ethernet Management Clock The MAC sources the MII_MDC signal to the Ethernet PHY Controller as the timing reference for transfer of information on the MII_MDIO signal. MII_MDC is an aperiodic signal that has no maximum high or low times. The minimum high and low times for MII_MDC will be 160 ns each, and the minimum period for MII_MDC will be 400 ns, regardless of the nominal period of TXClk and RXClk.
MIIMDIO	IO	Ethernet Management Data Inout When input, MII_MDIO is the data input signal from the Ethernet PHY. The Read Data is driven by the PHY synchronously with respect to the MII_MDC clock during the read cycles. When output, MII_MDIO is the data output signal from the MAC that is used to drive the control information during the Read/Write cycles to the Ethernet PHY. The MAC drives the MII_MDIO signal synchronously with respect to the MII_MDC.
6. AC97/GPIO C 0 ~ 4 pins (total 5)		
SDATA_OUT /GPC0	IO	SDATA_OUT: Serial audio data out, to Codec /GPIO C Inout0
SDATA_IN /GPC1	IO	SDATA_IN : Serial audio data in, from Codec /GPIO C Inout1
SYNC /GPC2	IO	SYNC: Frame Synchronization, 48 kHz fixed rate sample sync /GPIO C Inout2
RESET_ /GPC3	IO	RESET_ : AC97 Master hardware reset, active low /GPIO C Inout3

BIT_CLK	I	12.288MHz Serial Data Clock Input
7. UART/GPIO C 6~7 (total 2)		
TxD /GPC6	IO	TxD: Transmit data output /GPIO C Inout6
RxD/GPC7	IO	RxD: Receive data input /GPIO C Inout7
8. IrDA/UART2/GPIO D 0~3 (total 4)		
RTS_/GPD0	IO	RTS_: Transmission request (Request To Send) /GPIO D Inout0
CTS_/GPD1	IO	CTS_: Transmission enabled (Clear To Send) /GPIO D Inout1
TxD2/GPD2	IO	TxD2: Transmit data output /GPIO D Inout2
RxD2 /GPD3	IO	RxD2: Receive data input /GPIO D Inout3
9. SCC/GPIO D 4~5 (total 2)		
SCC_DATA /GPD4	IO	Transmit/Receive data connects SCC and smart card /GPIO D Inout4
SCC_CLK /GPD5	IO	Serial clock connects SCC and smart card /GPIO D Inout5
10. I2CI pins (total 2)		
SDA	IO	Serial Data Inout
SCL	IO	Serial Clock
11. GPIO A pins (total 8)		
GPA[7:0]	IO	GPIO A Inout[7:0]
12. IRQ/GPIO B pins (total 8)		
IRQ0 /GPB0	IO	Interrupt Request Input 0 /GPIO B Inout0
IRQ1 /GPB1	IO	Interrupt Request Input1 /GPIO B Inout1
IRQ2 /GPB2	IO	Interrupt Request Input2 /GPIO B Inout2
IRQ3 /GPB3	IO	Interrupt Request Input3 /GPIO B Inout3
IRQ4 /GPB4	IO	Interrupt Request Input4 /GPIO B Inout4
IRQ5 /GPB5	IO	Interrupt Request Input5 /GPIO B Inout5
IRQ6 /GPB6	IO	Interrupt Request Input6 /GPIO B Inout6
IRQ7 /GPB7	IO	Interrupt Request Input7 /GPIO B Inout7
13. JTAG pins (total 5)		
TRST_	O	JTAG Reset. Pull-down Internally
TMS	IO	JTAG Mode Select
TDI	I	JTAG Serial Data Input
TCK	O	JTAG Clock, Pull-down Internally
TDO	O	JTAG Serial Data Output
14. SYSTEM pins (total 7)		
EXTAL	I	System Crystal Input
XTAL	O	Crystal Output
RESETOUT_	O	Core Reset output
RESETP_	I	System Power on reset input
RESETM_	I	System Manual reset input, Pull-up- Internally
TEST_SEN	I	scan enable for scan-reg

TEST_MODE	I	Chip test mode
15. Test port / MD pins (total 5)		
TEST_PORT0	IO	Test port 0
TEST_PORT1	IO	Test port 1
TEST_PORT2	IO	Test port 2
TEST_PORT3 /MD_PCI	IO	Test port 3 /MD_PCI: used as the PCI mode configuration when power-up, should be pull-up or pull-down with 4.7-10K Ω resistor for PCI mode configuration, it will be latched at the rising-edge of the RESETP_ signal 0: Satellite 1: Host (default, Pull-up internal)
TEST_PORT4 /MD_PCIARB	IO	Test port 3 /MD_PCIARB: used as the PCI arbiter mode configuration when power-up, should be pull-up or pull-down with 4.7-10K Ω resistor for PCI arbiter mode configuration, it will be latched at the rising-edge of the RESETP_ signal 0: Built-in Arbiter Enable (default pull-down internal) 1: Build-in Arbiter Disable
16. Power pins (total 64)		
VDDIO	POW	Power supply for IO pad(3.3 V) (10pin)
VDDCORE	POW	Power supply for core(1.8 V) (10pin)
VDD(PLL)	POW	PLL Power supply for digital(1.8 V) (2pin)
VSS(PLL)	POW	PLL ground supply for digital (2pin)
VDD (USB)	POW	USB power supply for IO and USB cell (analog 3.3V) (2pin)
VSS (USB)	POW	USB ground supply for IO and USB cell (analog 0 V) (2pin)
VSSIO	POW	Ground supply for IO pad(0 V) (10pin)
VSSCORE	POW	Ground supply for core(0 V) (10pin)
G/T	POW	Ground for thermal radiation (0V) (16pin)
NC	NC	Not Connect Pin

1.4 Package

The Arca210 package is shown below:

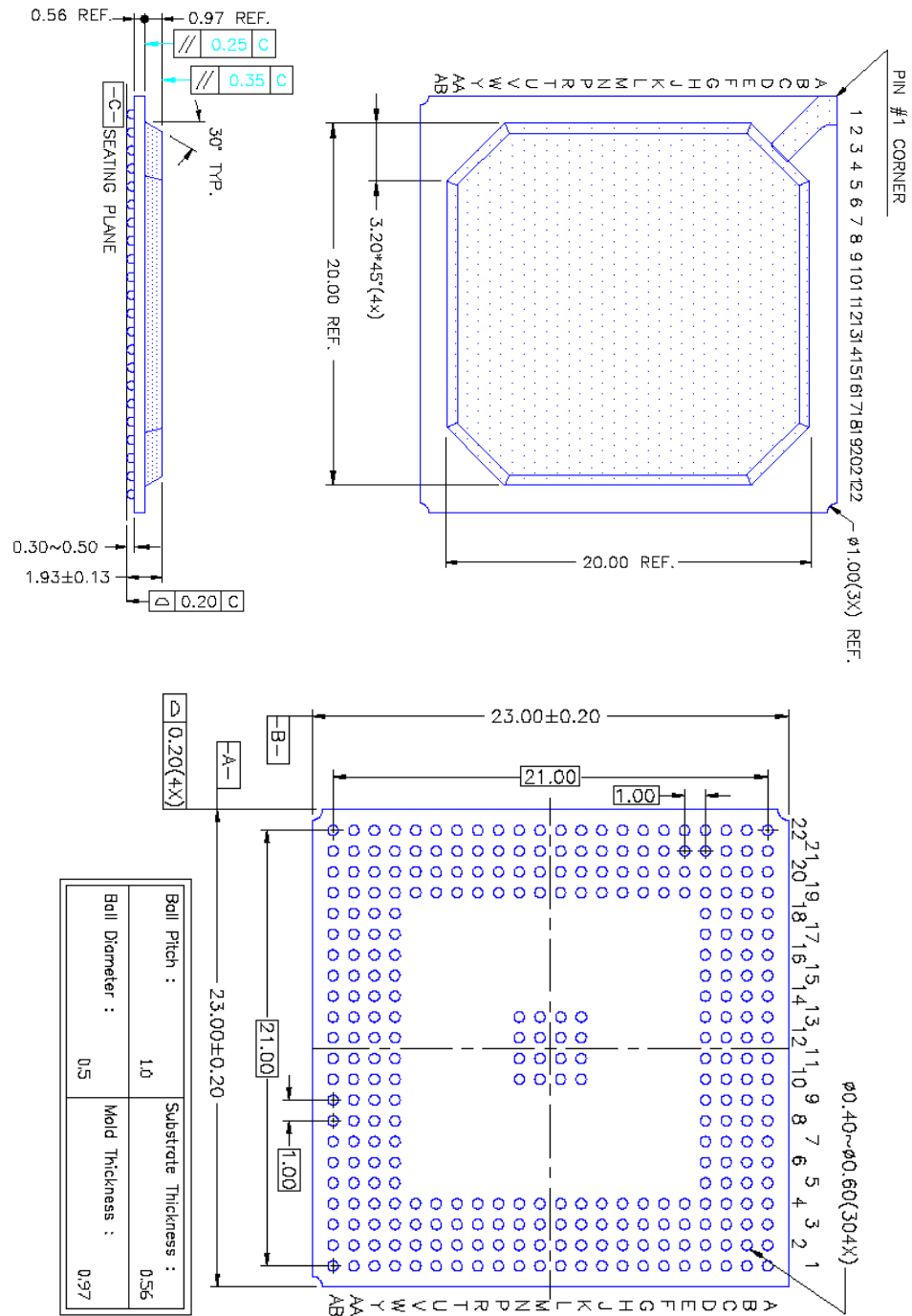


Figure 1-1 Arca210 Package

The Arca210 has a square 22x22 and 4 rows ball assignment (total 304 balls), and a 4x4 (16 balls) Ground/Thermal balls locate the central of the package to enhance the heat dissipation. The ball diameter is 0.4~0.6mm and the pitch is 1.0mm.

1.5 Ball Assignment

The Arca210 ball assignment is shown as Figure 1-1 and Table 1-1:

Arca2 Ball Assignment (BGA304)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	
22	D23	D24	D25	D27	D30	AD1	AD4	AD7	AD8	AD12	AD15	PERR_	TRDY_	FRAME_	AD18	AD21	IDSEL	AD24	AD28	AD31	RST	CLK124	22
21	D21	D22	D26	D28	D31	AD2	AD5	VDDIO	AD9	AD13	C/BE1_	LOCK_	VDDIO	C/BE2_	AD19	AD22	VDDIO	AD25	AD29	REQ0_	GN1_	REQ1_	21
20	D18	D19	D20	D29	AD0	AD3	AD6	C/BE0_	AD10	AD14	PAR	STOP_	IRDY_	AD16	AD20	AD23	C/BE3_	AD26	AD30	GN10_	REQ2_	INTB_	20
19	D16	VDDIO	D17	VSSCORE	NC	NC	VDDCOR	VSSCOR	AD11	VSSIO	SERR_	DEVSEL_	VSSIO	AD17	VDDCOR	VSSIO	VSSCORE	AD27	NC	REQ4_	REQ3_	GN12_	19
18	CS7H_	WE2_	WE3_	VDDCOR														VSSIO	INTC_	VDDIO	GN13_	18	
17	CKO3	CS6H_	CS6L_	CS7L_														TDO	INTA_	INTD_	GN14_	17	
16	CKO2	RAS_	CAS_	VSSIO														VSSIO	TMSI	TCK	TDI	16	
15	A16	A13	CKE	VSSIO														VSSCOR	RESET_	RESETP_	TRST_	15	
14	CKO1	A12	A14	A15														TP4	TEST_SE	TEST_M	RESETM	14	
13	CKO0	A9	A10	A11						G/T	G/T	G/T	G/T					NC	TP1	TP2	TP3	13	
12	A6	VDDIO	A8	VSSCORE						G/T	G/T	G/T	G/T					VSSIO	SDA	SCL	TP0	12	
11	A3	A4	A5	VDDCOR						G/T	G/T	G/T	G/T					GPA3	GPA2	GPA1	GPA0	11	
10	CS6H_	A2	A7	VSSIO						G/T	G/T	G/T	G/T					GPA7	GPA6	GPA5	GPA4	10	
9	CS4L_	CS4H_	CS6L_	VDDCOR															IRQ3	IRQ2	IRQ1	IRQ0	9
8	RDWR_	WE0_	WE1_	VSSCORE															VDDCOR	IRQ6	IRQ5	IRQ4	8
7	D12	D13	D14	D15															VSSCOR	IRQ7	VDDIO	EXTAL	7
6	D10	VDDIO	D11	VSSIO															SDATA_	SDATA_	BIT_CLK	XTAL	6
5	D8	D9	VSSCORE	VDDCOR															VDDCOR	SOC_CLK	RESET_	SYNC	5
4	D5	D6	D7	A2	NC	NC	CS3_	VSSCOR	DACK2_	DACK0_	VDDCOR	MIL_RXD2	NC	MIL_TXEN	VSSCOR	OVCR1	VDDCOR	VSSUSB	CTS_	TXD2	RXD2	SOC_DA	4
3	D3	D4	A24	A20	A17	RD_	CS2_	AEN	DREQ2_	DREQ0	MIL_RXE	MIL_RXD3	MIL_JMDC	MIL_TXD0	MIL_TXD3	PPWR1	VDDUSB	VSSUSB	VSSPLL	VSSPLL	TXD	RXD	3
2	D2	D0	A23	A19	A1	WAIT_	CS1_	VDDIO	DACK1_	MIL_COL	MIL_CRS	MIL_RXD4	MIL_JMDC	MIL_TXD1	VDDIO	PPWR0	DMNS0	VDDUSB	VDDPLL	VDDPLL	NC	RTS_	2
1	D1	A25	A22	A18	A0	WE_	CS0_	EOP	DREQ1_	MIL_RXD	MIL_RXD1	MIL_RXD	MIL_TXD1	MIL_TXD2	OVCR0	UHC_CLK	DP1S0	DMNS1	DP1S1	NC	NC	NC	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	

Top View

EMI: 85 GPA: 8 IRQ: 8 AC97: 5 UART: 8 JTAG: 5 SYSTEM: 7
 PCI: 62 DMA: 8 I2C: 2 MII: 17 USB: 9 TEST: 5 POWER: 64
 Total: BGA304

NC: 11

Figure 1-1 Arca210 Ball Assignment

Table 1-1 Arca210 Ball Assignment

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A1	D1	F21	AD2	U19	VSSCORE
A2	D2	F22	AD1	U20	C/BE3_
A3	D3	G1	CS0_	U21	VDDIO
A4	D5	G2	CS1_	U22	IDSEL
A5	D8	G3	CS2_	V1	DMNS1
A6	D10	G4	CS3_	V2	VDD(USB)
A7	D12	G19	VDDCORE	V3	VSS(USB)
A8	RDWR_	G20	AD6	V4	VSS(USB)
A9	CS4L_	G21	AD5	V19	AD27
A10	CS6H_	G22	AD4	V20	AD26
A11	A3	H1	EOP	V21	AD25
A12	A6	H2	VDDIO	V22	AD24
A13	CKO0	H3	AEN	W1	DPLS1
A14	CKO1	H4	VSSCORE	W2	VDD(PLL)
A15	A16	H19	VSSCORE	W3	VSS(PLL)
A16	CKO2	H20	C/BE0_	W4	CTS_
A17	CKO3	H21	VDDIO	W5	VDDCORE
A18	CS7H_	H22	AD7	W6	SDATA_IN
A19	D16	J1	DREQ1_	W7	VSSCORE
A20	D18	J2	DACK1_	W8	VDDCORE
A21	D21	J3	DREQ2_	W9	IRQ3
A22	D23	J4	DACK2_	W10	GPA7
B1	A25	J19	AD11	W11	GPA3
B2	D0	J20	AD10	W12	VSSIO
B3	D4	J21	AD9	W13	NC
B4	D6	J22	AD8	W14	TP4
B5	D9	K1	MII_RXDV	W15	VSSCORE
B6	VDDIO	K2	MII_COL	W16	VSSIO
B7	D13	K3	DREQ0_	W17	TDO
B8	WE0_	K4	DACK0_	W18	VSSIO
B9	CS4H_	K10	G/T	W19	NC
B10	A2	K11	G/T	W20	AD30
B11	A4	K12	G/T	W21	AD29
B12	VDDIO	K13	G/T	W22	AD28
B13	A9	K19	VSSIO	Y1	NC
B14	A12	K20	AD14	Y2	VDD(PLL)
B15	A13	K21	AD13	Y3	VSS(PLL)
B16	RAS_	K22	AD12	Y4	TXD2
B17	CS5H_	L1	MII_RXCLK	Y5	SCC_CLK
B18	WE2_	L2	MII_CRS	Y6	SDATA_OUT
B19	VDDIO	L3	MII_RXER	Y7	IRQ7
B20	D19	L4	VDDCORE	Y8	IRQ6
B21	D22	L10	G/T	Y9	IRQ2
B22	D24	L11	G/T	Y10	GPA6
C1	A22	L12	G/T	Y11	GPA2
C2	A23	L13	G/T	Y12	SDA
C3	A24	L19	SERR_	Y13	TP1
C4	D7	L20	PAR	Y14	TEST_SEN
C5	VSSCORE	L21	C/BE1_	Y15	RESETOUT_
C6	D11	L22	AD15	Y16	TMS
C7	D14	M1	MII-RXD1	Y17	INTA_
C8	WE1_	M2	MII_RXD0	Y18	INTC_

C9	CS6L_	M3	MII_RXD3	Y19	REQ4_
C10	A7	M4	MII_RXD2	Y20	GNT0_
C11	A5	M10	G/T	Y21	REQ0_
C12	A8	M11	G/T	Y22	AD31
C13	A10	M12	G/T	AA1	NC
C14	A14	M13	G/T	AA2	NC
C15	CKE	M19	DEVSEL_	AA3	TXD
C16	CAS_	M20	STOP_	AA4	RXD2
C17	CS5L_	M21	LOCK_	AA5	RESET_
C18	WE3_	M22	PERR_	AA6	BIT_CLK
C19	D17	N1	MII_TXCLK	AA7	VDDIO
C20	D20	N2	MII_MDC	AA8	IRQ5
C21	D26	N3	MII_MDIO	AA9	IRQ1
C22	D25	N4	NC	AA10	GPA5
D1	A18	N10	G/T	AA11	GPA1
D2	A19	N11	G/T	AA12	SCL
D3	A20	N12	G/T	AA13	TP2
D4	A21	N13	G/T	AA14	TEST_MODE
D5	VDDCORE	N19	VSSIO	AA15	RESETP_
D6	VSSIO	N20	IRDY_	AA16	TCK
D7	D15	N21	VDDIO	AA17	INTD_
D8	VSSCORE	N22	TRDY_	AA18	VDDIO
D9	VDDCORE	P1	MII_TXD2	AA19	REQ3_
D10	VSSIO	P2	MII_TXD1	AA20	REQ2_
D11	VDDCORE	P3	MII_TXD0	AA21	GNT1_
D12	VSSCORE	P4	MII_TXEN	AA22	RST_
D13	A11	P19	AD17	AB1	NC
D14	A15	P20	AD16	AB2	RTS-
D15	VSSIO	P21	C/BE2_	AB3	RXD
D16	VSSIO	P22	FRAME_	AB4	SCC_DATA
D17	CS7L_	R1	OVCR0	AB5	SYNC
D18	VDDCORE	R2	VDDIO	AB6	XTAL
D19	VSSCORE	R3	MII_TXD3	AB7	EXTAL
D20	D29	R4	VSSCORE	AB8	IRQ4
D21	D28	R19	VDDCORE	AB9	IRQ0
D22	D27	R20	AD20	AB10	GPA4
E1	A0	R21	AD19	AB11	GPA0
E2	A1	R22	AD18	AB12	TP0
E3	A17	T1	UHC_CLK	AB13	TP3
E4	NC	T2	PPWR0	AB14	RESETM_
E19	NC	T3	PPWR1	AB15	TRST_
E20	AD0	T4	OVCR1	AB16	TDI
E21	D31	T19	VSSIO	AB17	GNT4_
E22	D30	T20	AD23	AB18	GNT3_
F1	WE_	T21	AD22	AB19	GNT2_
F2	WAIT_	T22	AD21	AB20	INTB_
F3	RD_	U1	DPLS0	AB21	REQ1_
F4	NC	U2	DMNS0	AB22	CLK
F19	NC	U3	VDD(USB)		
F20	AD3	U4	VDDCORE		

2 External Memory Interface

EMI (External Memory Interface) module divides physical address space and output control signals for various types of memory and bus interface specifications. EMI functions enable it to link directly Synchronous DRAM, SRAM, ROM, Burst ROM and Flash without an external circuit.

This section is the design guidelines for the external memory interface.

2.1 Overview

The external memory bus interface for the Arca210 processor supports:

- 133 MHz SDRAM DIMM168
- 133 MHz SDRAM SODIMM144
- 133 MHz SDRAM Chip
- Synchronous and asynchronous Burst mode and Page mode Flash
- Synchronous Mask ROM (SMROM)
- SRAM
- SRAM-like Variable Latency I/O (VLIO)

Use the memory interface configuration registers to program the memory types. Refer to Figure 2-1, “Arca210 EMI Block Diagram” for the block diagram of the Memory Controller configuration. Refer to Figure 1-1, “EMI Physical Address Map” for the Arca210 processor memory map. Refer to Table 2-1, “Physical Memory Address Space Mapping” for the physical address mapping.

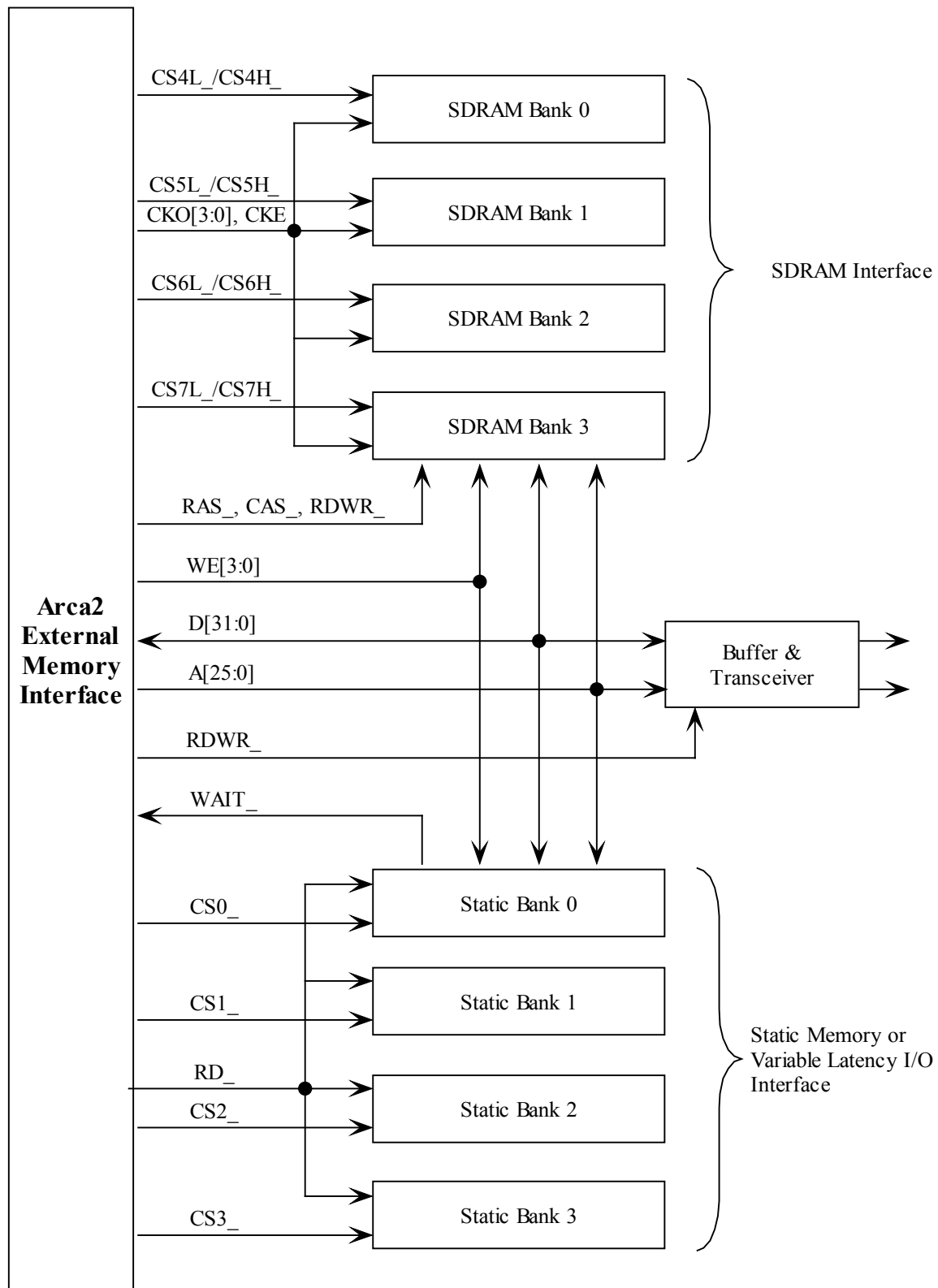


Figure 2-1 Arca210 EMI Block Diagram

2.2 Memory Map

Space Allocation: In the Arca210 architecture, both logical spaces and physical spaces have 32-bit address spaces. The 4Gbyte physical space is divided into several partitions for static memory, SDRAM, PCI and internal I/O. Following table shows the physical space mapping.

Table 2-1 Physical Address Space Mapping

Physical Address	Connectable Memory	Capacity	Chip Select Signals	Access Size
H'0000 0000 to H'03FF FFFF	Static memory bank 0	64 Mbytes	CS0_N	8, 16, 32*
H'0400 0000 to H'07FF FFFF	Static memory bank 1	64 Mbytes	CS1_N	8, 16, 32
H'0800 0000 to H'0BFF FFFF	Static memory bank 2	64 Mbytes	CS2_N	8, 16, 32
H'0C00 0000 to H'0FFF FFFF	Static memory bank 3	64 Mbytes	CS3_N	8, 16, 32
H'1000 0000 to H'1FFF FFFF	SDRAM bank 4	256 Mbytes	CS4H_N, CS4L_N	32
H'2000 0000 to H'2FFF FFFF	SDRAM bank 5	256 Mbytes	CS5H_N, CS5L_N	32
H'3000 0000 to H'3FFF FFFF	SDRAM bank 6	256 Mbytes	CS6H_N, CS6L_N	32
H'4000 0000 to H'4FFF FFFF	SDRAM bank 7	256 Mbytes	CS7H_N, CS7L_N	32
H'5000 0000 to H'6FFF FFFF	PCI space	512 Mbytes		
H'7000 0000 to H'DFFF FFFF	Reserved	1792 Mbytes		
H'E000 0000 to H'FFFF FFFF	Internal I/O	512 Mbytes		

Notes:

- Use external pin to specify static memory bank 0 bus width.
The memory data bus width can be set for bank 0 at power-on reset. The correspondence between the external pin (MD3, MD4) and memory size is listed in the table below.

MD_MEM[1]	MD_MEM[0]	Bank 0 Memory Size
0	0	8 bits
0	1	16 bits
1	0	32 bits
1	1	Reserved

- Do not access the reserved area. If the reserved area is accessed, the correct operation can not be guaranteed.

Following figure shows the physical space map.

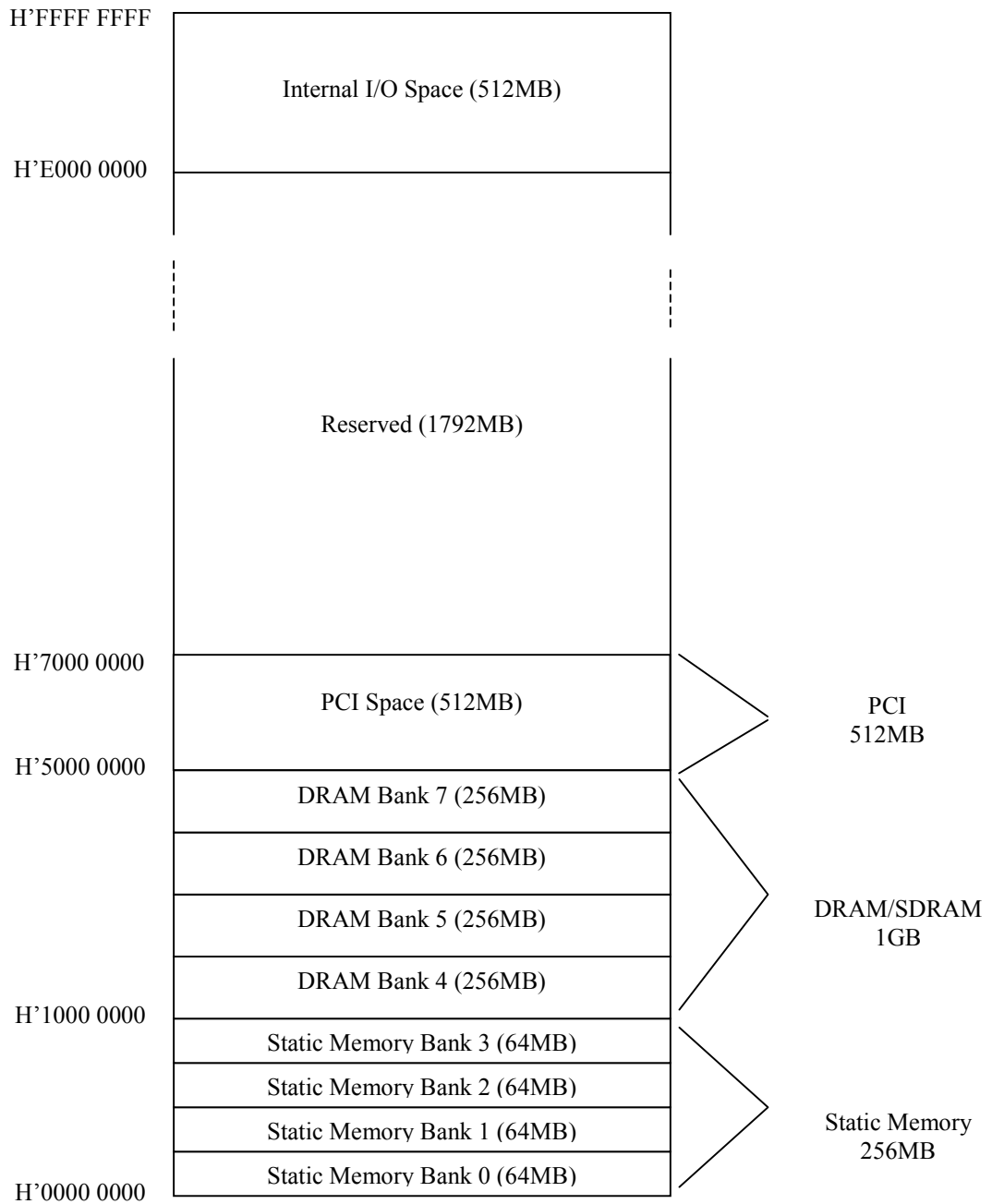


Figure 2-1 EMI Physical Space Map

2.3 Static Memory Interface

The static memory includes ROM, burst ROM, SRAM, Flash or SRAM-like I/O devices. The static memory interface is comprised of CS_n_ (n = 0 to 3), WE_n_, WE_n_ (n = 0 to 3), RD_n_, A[25..0], D[31..0] and WAIT_n_. The data bus width for each chip select region may be programmed to be 8, 16 or 32 bits. RD_n_ is asserted for all reads. WE_n_, WE_n_ (n = 0 to 3) are asserted for SRAM and Flash writes. WE_n_ (n = 0 to 3) are asserted when byte enable is needed. Arca210 supplies 26 bits address for access up to 64M space per chip select. A0 is not used in 16-bit wide bus and A[1..0] are not used in 32-bit wide bus.

The interface examples between Arca210 EMI and static memory are shown as Figure 2-1 to Figure 2-6.

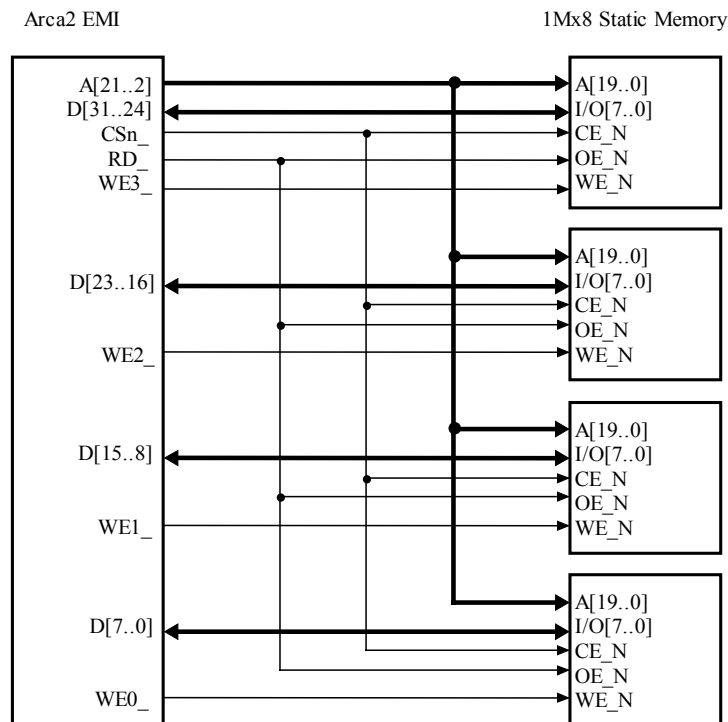


Figure 2-1 Example of 32-Bit Data Width With 8-Bit Width Static Memory

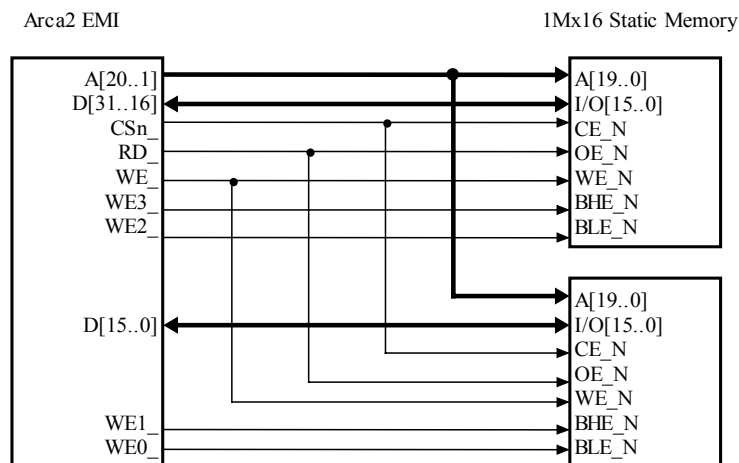


Figure 2-2 Example of 32-Bit Data Width With 16-Bit Width Static Memory

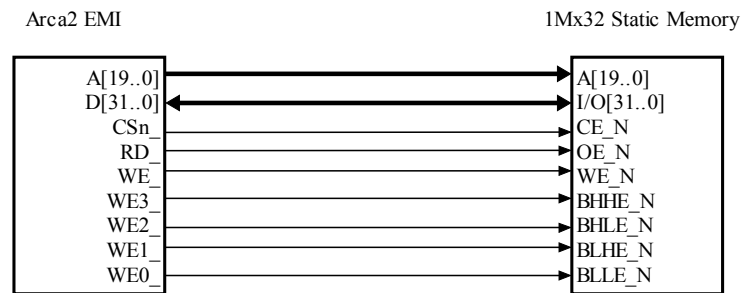


Figure 2-3 Example of 32-Bit Data Width With 32-Bit Width Static Memory

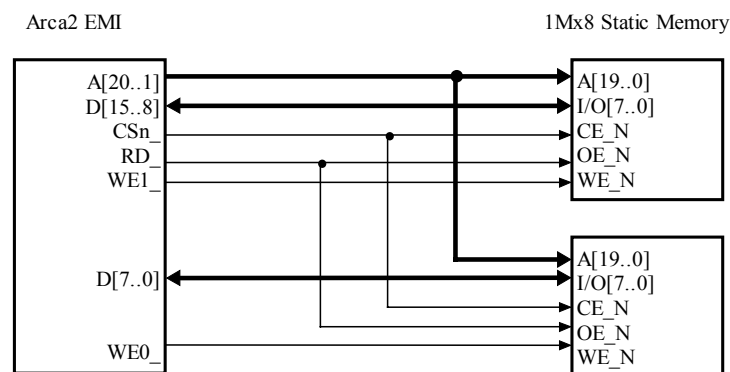


Figure 2-4 Example of 16-Bit Data Width With 8-Bit Width Static Memory

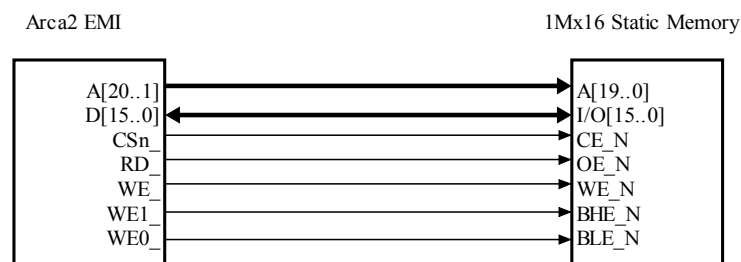


Figure 2-5 Example of 16-Bit Data Width With 16-Bit Width Static Memory

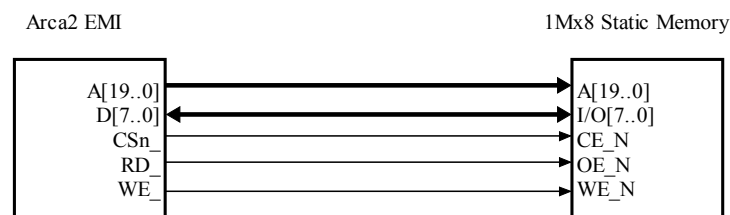


Figure 2-6 Example of 8-Bit Data Width With 8-Bit Width Static Memory

2.4 SDRAM Connection

The SDRAM (synchronous DRAM) includes synchronous DRAM chip, 100/168-pin DIMM and 144-pin SODIMM. The control signals for direction connection of SDRAM are CS4H ~ CS7H_N, CS4L ~ CS7L_N, RAS_, CAS_, RDWR_, DQM0_, DQM1_, DQM2_, DQM3_ and CKE. Both 2-

bank and 4-bank SDRAM are supported. The bank select signals are always output from the A15 pin and A16 pin of Arca210. Byte specification is performed by WE0_/DQM0_, WE1_/DQM1_, WE2_/DQM2_ and WE3_/DQM3_. When SODIMM is used, byte specification is performed by CS4H_ ~ CS7H_ also. A read/write is performed for the byte for which the corresponding DQMn_ is low.

The interface between the Arca210 EMI and SDRAM are shown from Figure 2-1 to Figure 2-5.

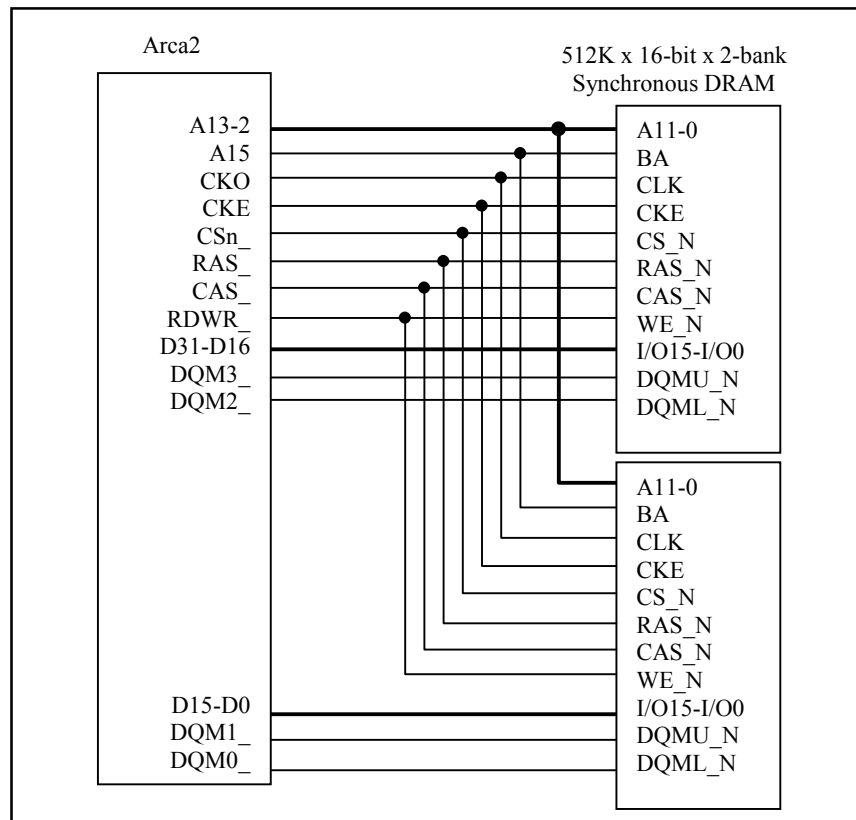


Figure 2-1 Example of Synchronous DRAM Chip Connection (two banks)

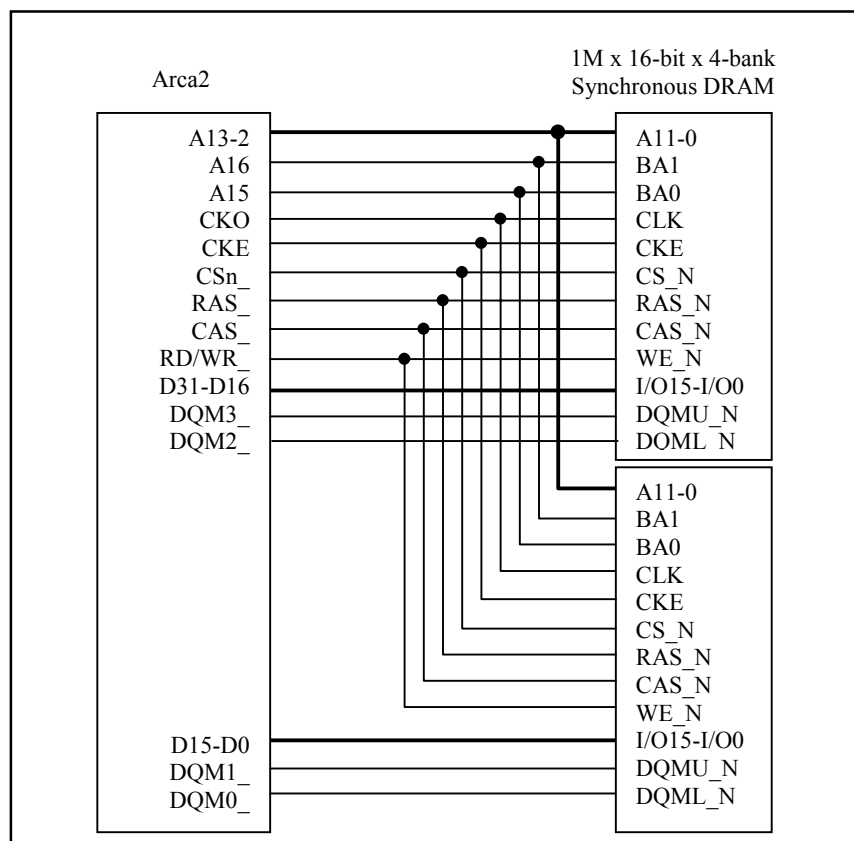


Figure 2-2 Example of Synchronous DRAM Chip Connection (four banks)

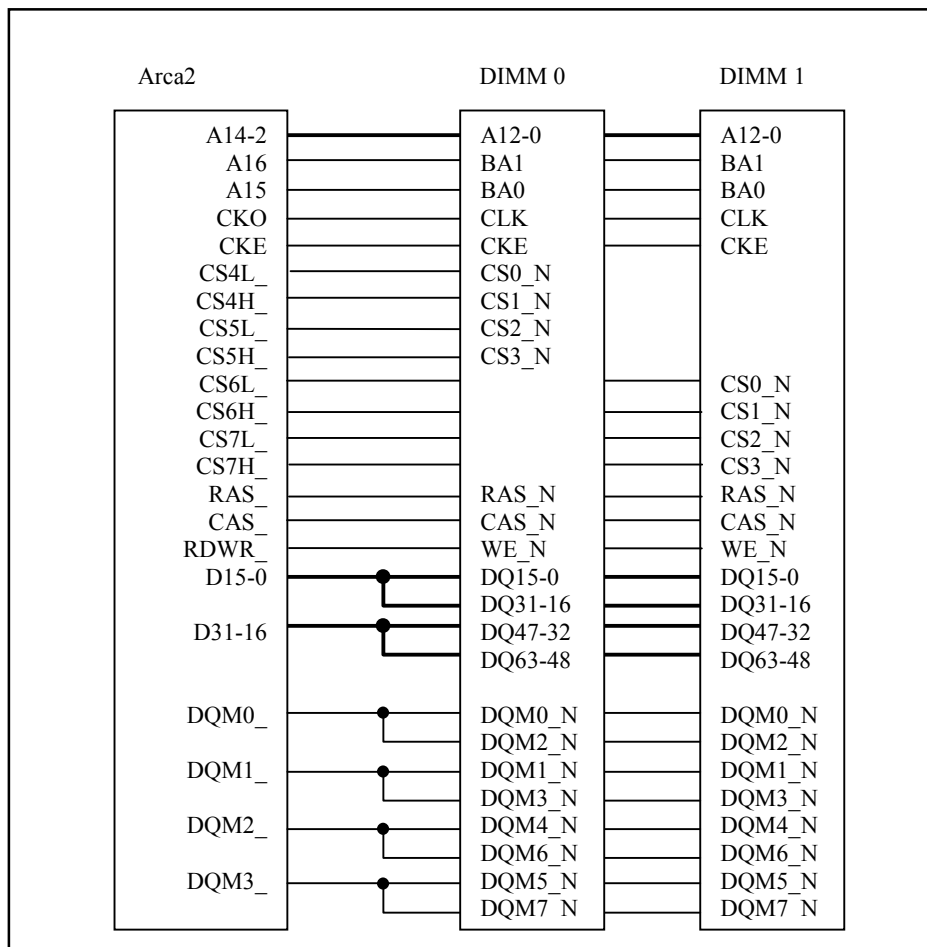


Figure 2-3 Example of Synchronous DRAM 168-pin DIMMs Connection

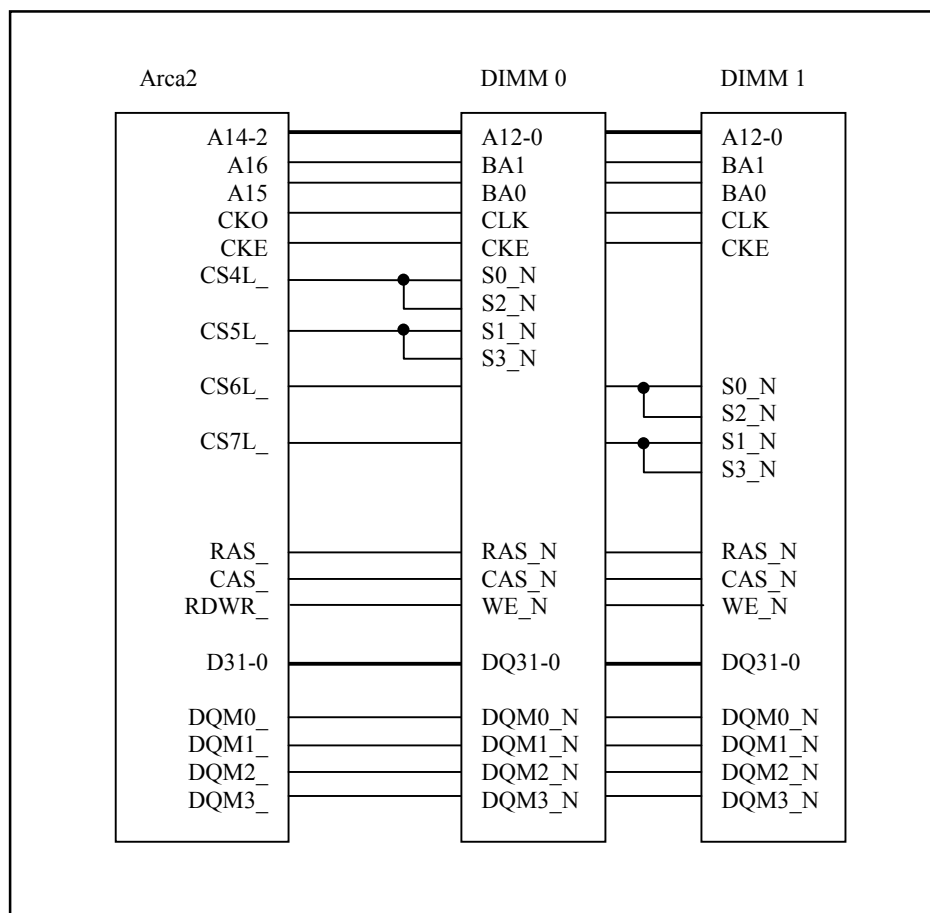


Figure 2-4 Example of Synchronous DRAM 100-pin DIMMs Connection

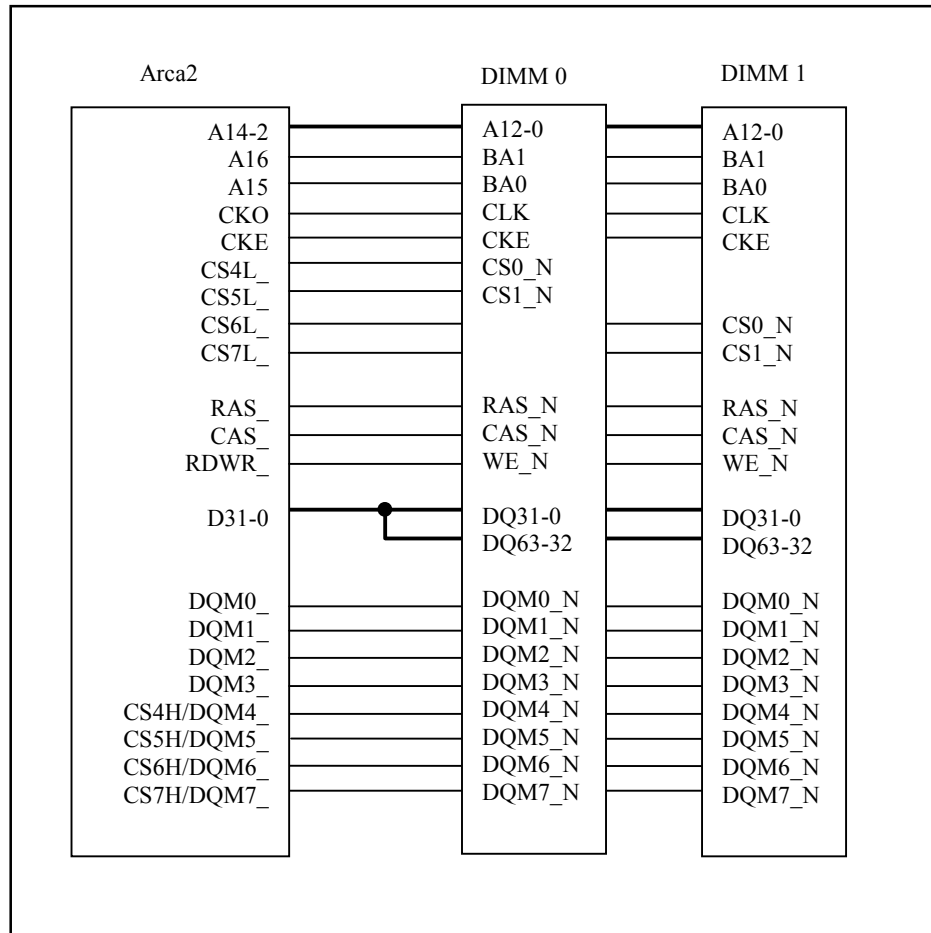


Figure 2-5 Example of Synchronous DRAM 144-pin SODIMMs Connection

2.5 DMA

The DMA controller (DMA) controls data transfers among external memory, external devices with DACKn_, memory-mapped external devices and on-chip modules (TMU, UART, etc) in place of CPU to relieve it of the interrupt overhead in serving those data transfers.

2.5.1 Features

The DMA has the following features:

- Four independent DMA channels, three can be used for external devices (Channel0-3)
- Maximum transfer count: 16M – 1 (16,777,215) transfers
- Transfer data units: 8-bit, 16-bit, 32-bit, 16-byte or 32-byte
- One transfer address type: two-address transfer
- Two transfer modes: single mode or block mode
- Two external DMA request detection modes: low level or falling edge detection
- Transfer objects
 - Between external memory and external device with DACKn_N
 - Between external memory and external memory or memory-mapped devices
 - Between external memory and on-chip modules
- Two types of channel priority ranking: fixed priority or round robin mode.
- Interrupt request can be sent to the CPU on completion of the specified number of transfers or on address e
- rror during transfer.

2.5.2 DMA Interface

The interface between Arca210 and external device shown in Figure 2-1, pull-up resistor (R1, 4.7-10KΩ) is request for proper operation, because the AEN signal is multi-function pin and it is GPIO input when power-up.

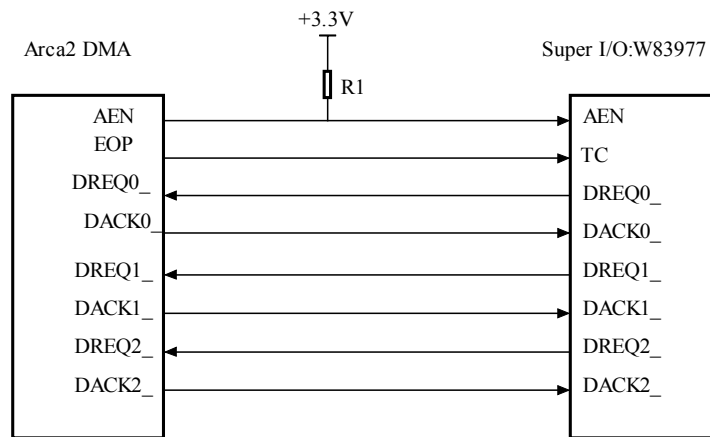


Figure 2-1 Arca210 DMA interface

2.6 EMI layout Guideline

According to related document [3], we can get some design rules about the PCB layout of memory bus:

- The trace length of control, address, data and clock signals should be as short as possible. It's better that the trace length of the clock be less than **3.0 inch** and others be less than **5.0 inch**. The mismatch length of clock should be less than 0.05 inch, and that of others should be less than 0.5 inch.
- The source terminator technology should be adopted for all traces of system memory bus. **33 Ω** resistor is recommended. It's better to add the terminators on the each source end for the data traces.
- The distance between two traces should be as larger as possible, the 5mil wide and 5mil space trace is recommended. In order to decrease the crosstalk, shorter interfering length of traces, lower drive current and fewer times of reflection are recommended.
- In order to let return current strays tightly bunched under the signal trace, the ground plane should be as complete as possible. If the ground plane under a system memory trace is separated, a 0.1uF capacitor is needed to add between the two separated planes near the traces as Figure 2-1. Routing on the ground plane is not recommended.

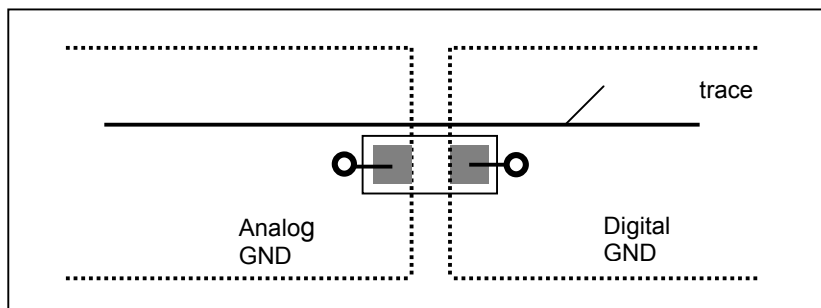


Figure 2-1 Capacitors Between Two Separate Ground Plane

- Avoid parallelism between signals on adjacent if there is no AC reference plane between them. Route adjacent layers orthogonally.

- It's better to route the system memory traces on the layer near the ground layer. If some of traces route on the layer near power layer, a 0.1uF capacitor per three vias should be added between the power layer and the ground layer near the vias as Figure 2-2. And do not route any signals in the field of vias that do not change layers.

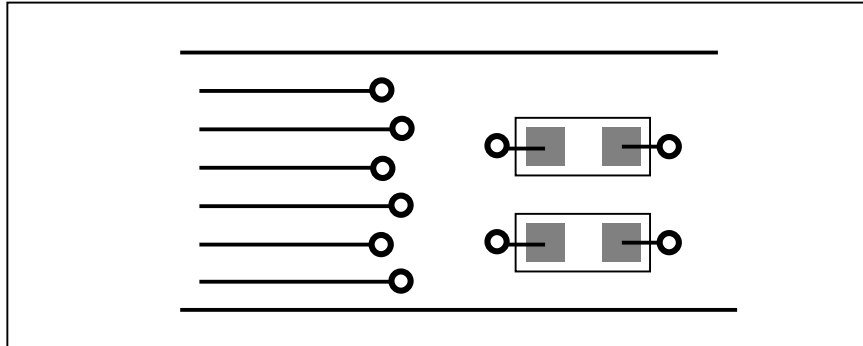


Figure 2-2 Capacitors Near Vias

3 PCI Interface

Arca210 processor has a build-in PCI Controller, which is PCI 2.1 compatible. The main goal of the PCIC is to allow Arca-based systems-on-a-chip to communicate with PCI devices on PCI bus. The PCIC also provides a channel for PCI bus devices to read and write memory attached to the Arca210 EMI.

3.1 Feature

- Complete 33Mhz 32-bit PCI interface
- Support host or satellite operation mode
- Support both PCI master and target operation
- Target(or slave) lock support(master doesn't deliver lock)
- Up to four masters except Arca210 in host mode
- On-chip PCI arbiter (which is disabled in satellite mode and can be selected in host mode) supports total 5 masters

3.2 Configuration

The operation mode is controlled by pin MD_PCI when system reset. Table 3-1 describes the configuration of PCI mode by pin MD_PCI.

Table 3-1 PCI Mode Configuration

MD_PCI	Description
0	Satellite mode. A device in a hosted PCI system. Configured by the host, for example, a PCI card in a PC.
1	Hosts mode. The main processor in a PCI system. Responsible for configuration, and interrupt handling.

Arca210 has an internal PCI-bus arbiter that can be used when Arca210 is in host mode.

Table 3-2 PCI Arbiter Mode Configuration

MD_PCIARB	Description
0	Disable the Arca210 internal PCI arbiter when in PCI host mode.
1	Enable the Arca210 internal PCI arbiter when in PCI host mode.

3.3 Arca210 PCI Interface

The interface example is shown as Figure 3-1. The bus request and grant signals for this PCI device are used the REQ1_ and GNT1_ of the Arca210 built-in PCI arbiter, and the IDSEL of this device is assigned to PCI AD31. The PCI clock signals distributed to Arca210 and PCI device should be taken more careful to minimize the clock jitter and skew for proper operation.

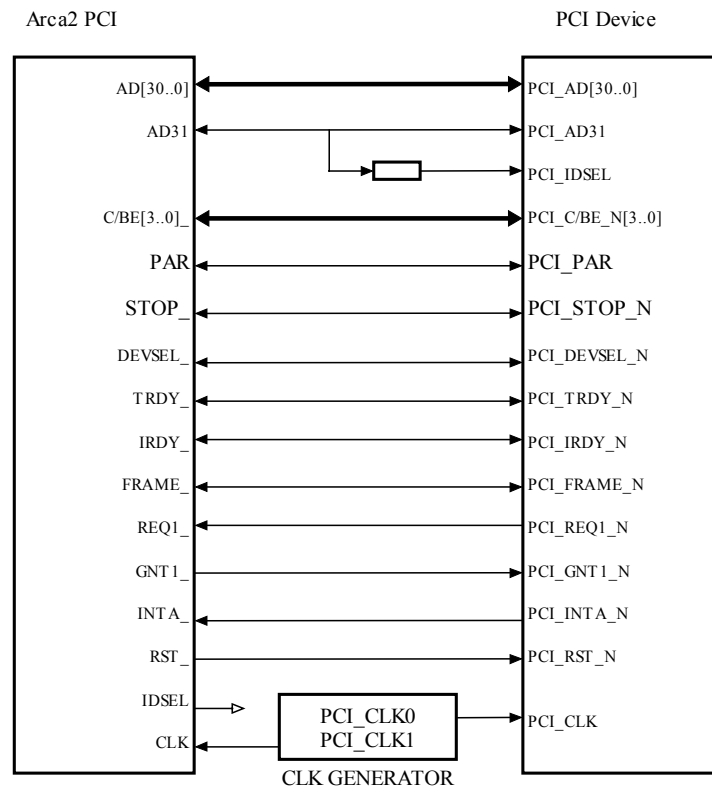


Figure 3-1 Arca210 PCI Interface

3.4 PCI Layout Guideline

The layout of the PCI bus can be referred in "*PCI local bus specification revision 2.1*".

4 Ethernet Interface

Arca210 integrated an Ethernet Controller (ETHC), which provides the interface between the host application and the PHY layer through the Media Independent Interface (MII). The PHY layer devices are external to Arca and selected by the customers.

This section describes the connection between the PHY chip and Arca210 processor.

4.1 Features

The Ethernet Controller operates at either 100 Mbps or 10 Mbps in half-duplex or full-duplex mode. In half-duplex mode, the controller supports the IEEE802.3 Carrier Sense Multiple Access with Collision Detection (CSMA/CD) protocol. In full-duplex mode, it supports the IEEE802.3 MAC Control Layer, including the Pause operation for flow control.

The ETHC has the following features:

- Compliant with IEEE802.3, 802.3u Specification
- 10/100 Mbps data transfer rates
- IEEE802.3 compliant MII interface to talk to an external PHY
- Full and half duplex modes
- Support CSMA/CD protocol in half duplex mode
- Supports flow-control for full-duplex operation
- Collision detection and auto retransmission on collisions in half-duplex mode
- Provides External and internal loop back capability on the MII Interface
- Contains a variety of flexible address filtering modes on the Ethernet side:
 - One 48 bit Perfect address
 - 64 hash-filtered multicast addresses
 - Pass all multicast addresses
 - Promiscuous Mode
 - Pass all incoming packets with a status report
 - Support MII Management
- Tx/Rx buffers (2K bytes/2K bytes)
- DMA engine using burst mode
- Descriptor architecture allows large blocks of data transfer with minimum CPU intervention

4.2 Arca210 Ethernet PHY Connection

The interface example is shown as Figure 4-1, the Ethernet PHY chip is the DAVIDCOM DM9161 (the detail information of the DM9161, please refer the manufacturer's data-sheet). Two source termination resistors (R1, R2) are recommended for MII_TXCLK and MII_RXCLK signals (25MHz at 100M LAN), the value of R1 and R2 maybe 33Ω to compensate for minor the difference between the chip output and PCB trace impedance. R3 is a 4.7-10KΩ pull-up resistor because the signal MII_MDIO of the DM9161 is an open-drain pad. Arca210 RESETOUT_ drive the DM9161 RESET# input to reset the chip when power-up.

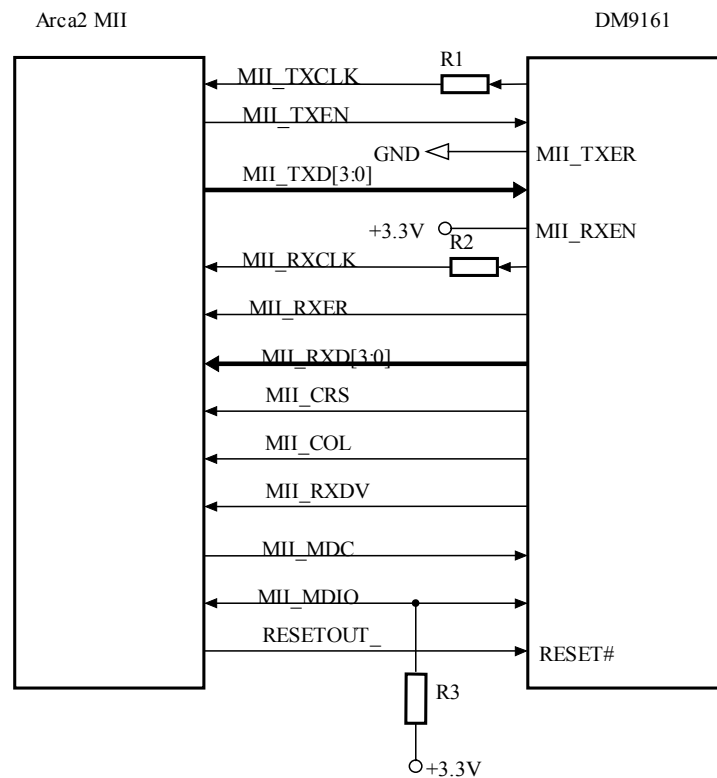


Figure 4-1 Arca210 MII Interface

4.3 MII Layout Guideline

The design rules about the PCB layout of MII bus are listed as follow:

- Control the length of MII bus as short as possible and as same as possible. The mismatch length of MII bus should be less than 0.5 inch.
- The source terminator technology should be adopted for clock signal of MII bus. 33 Ω resistor is recommended, and place the resistor near to the PHY chip as close as possible.
- The 5mil width and 5mil space trace is recommended for MII signals, 8mil width and 12mil space trace is recommended for MII_TXCLK and MII_RXCLK.
- It's better to route the MII traces on the layer near the ground layer.

5 USB Interface

5.1 Overview

The USB Host Controller (UHC) of Arca210 is Open Host Controller Interface (OHCI)-compatible and USB Revision 1.1-compatible. It supports both low-speed (1.5 Mbps) and full-speed (12 Mbps) USB devices. Two downstream ports are provided.

5.2 USB Interface

Figure 5-1 shows the simple and economical USB implementation used Arca210 processor. Two serial termination resistor (R1 and R2, maybe 33Ω) on the different pair (D+, D-) to compensate for minor the impedance difference between the PCB trace and the 90Ω USB cable. Two $15K\Omega$ pull-down resistors (R3, R4) indicate that the host port is full-speed according to the USB specification. A 750mA resettable fuse on the USB +5V power provides the short-circuit and over-current protection when hot-plug or device failure on USB. R5 (510Ω) and R6 ($1.8k\Omega$) are used to detect the power failure on this USB port, when fused, the OVC0 will be pull-down by R6 and interrupt the Arca210-UHC (USB controller). In this case, PPWR0 is not used and can be floated.

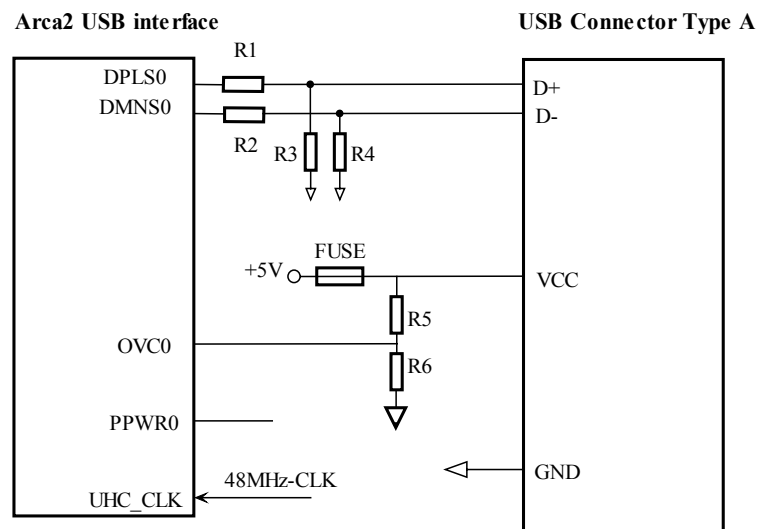


Figure 5-1 Arca210 USB Implementation 1

Figure 5-2 is another USB implementation on the Arca210 processor, an USB power distributor chip is used to provide the much better protection for the USB port. The USB power distributor is Micrel's MIC2026, the chip data-sheet can be download from the manufacturer's web site www.micrel.com.

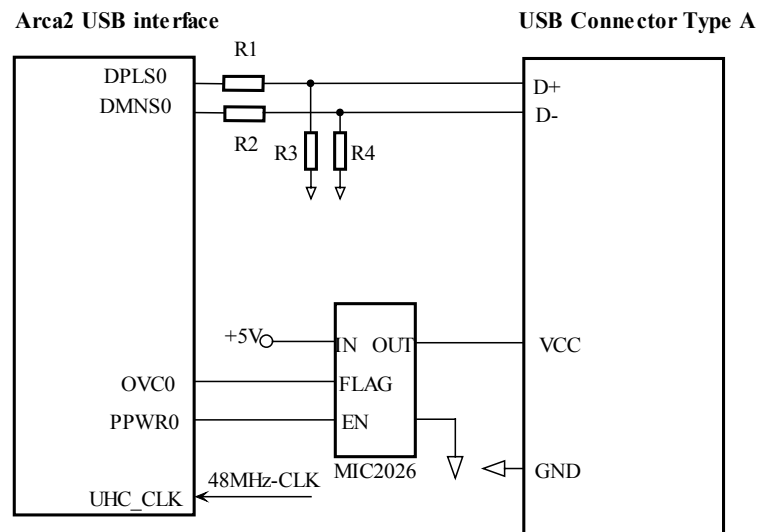


Figure 5-2 Arca210 USB Implementation 2

5.3 Layout of USB Differential Signals

The rules about the layout of USB differential signals are listed as below:

- The length of a differential pair should be as same as possible. The mismatch length should be less than 0.05 inch. In addition, the length of the differential traces should be as short as possible.
- The differential traces of USB should adopt source terminator. The value of source terminator resistor is 33 Ω.
- The distance between center of a differential pair should be 18 mil.
- The differential traces should be routed on the layer near the ground layer and the ground plane under the traces should be complete.
- Don't route any other signals between the differential pair.

6 AC97 Interface

The built-in AC97 controller fully supports AC-Link functions that are compliant with AC'97 Component Specification 2.2. Many popular audio D-2-A converters and codecs use this format and could be support on Arca210 processor simply.

If the AC97 Controller function is disabled, its pins can be used for GPIO functions.

6.1 Feature

Some of the main features are listed as follow:

- Multiple Sample Size (16, 18 and 20 bit) Support
- Programmable Output channels and Input channels Support
- Power Down Mode Support
- Two Wake-Up mode Support
- DMA transfer mode Support
- Programmable Interrupt function Support

6.2 Interface with AC97 CODEC

The AC97 connection is shown in Figure 6-1. The Audio CODEC provides the 12.288MHz clock to the AC97 controller, and source termination resistor (R2, maybe 33Ω) is taken for better clock signal. The pull-up resistor (R1, 4.7-10kΩ) is requested for proper operation, because the RESET_ is a multi-function pin on Arca210 processor, and it is GPIO input function when power-up.

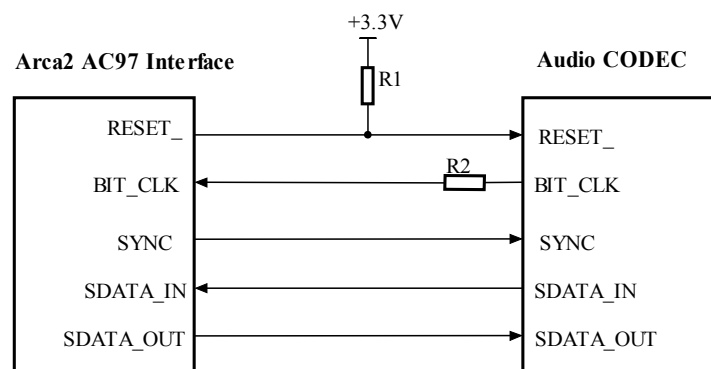


Figure 6-1 AC97 interface

6.3 Layout Guideline of AC97

Because of the analog/digital nature of the codecs, it is important that proper mixed-signal layout procedures be followed. Arca Technology recommends you follow the layout

recommendations given in your Codec datasheet. Some general recommendations are listed as below:

- Use a separate power supply for the analog audio portion of the design.
- Place a digital power/ground plane keep-out underneath the analog portion. Use a separate analog ground plane. You can create an island inside the keep-out. Connect the digital ground pins of the codec to the digital ground. Keep the two ground planes on the same layer, with at least 1/8 of an inch separation between them.
- Connect the two ground planes underneath your codec with a 0 ohm jumper. Do Not Populate 0 ohm jumpers between analog and digital ground at the power supply. Excessive noise on the board may be reduced by installing the 0 ohm resistor.
- Do not to route digital signals underneath the analog portion. Digital traces must go over the digital ground plane, analog traces over the analog plane.
- Buffer any digital signals to or from the codec that go off the board, for example, if your codec is on a daughter card.
- Fill the areas between analog traces with copper tied to the analog ground. Fill the regions between digital traces with copper tied to the digital ground.
- Locate the decoupling capacitors for the analog portion as close to the codec as possible.

7 UART Interface

Universal asynchronous receiver/transmitter (UART) provides asynchronous serial communication with external devices such as modems and other computers.

7.1 Features

Some of the key features are listed as the following:

- Full-duplex operation which enables transmission and reception to be performed simultaneously.
- Asynchronous serial communication executed using an asynchronous system in which synchronization is achieved character by character. 7 or 8 bit operation with optional even or odd parity and one or two stop bits.
- Receive error detection: Parity, frame, overrun, break and timeout errors.
- On-chip baud rate generator allows any bit rate to be selected.
- The DMA controller can be activated to execute a data transfer by issuing a DMA transfer request in the event of a transmit-FIFO-data-empty or receive-FIFO-data-full interrupt.
- Low Power mode by halting the clock supply to UART to reduce power consumption.
- Modem control functions (RTS and CTS) are provided.

7.2 Interface with UART Transceiver

The interface example is shown as Figure 7-1. Arca210 input and output are both LVCMOS level, so the RS232 transceiver provides the level transform between the RS232 and Arca210 processor.

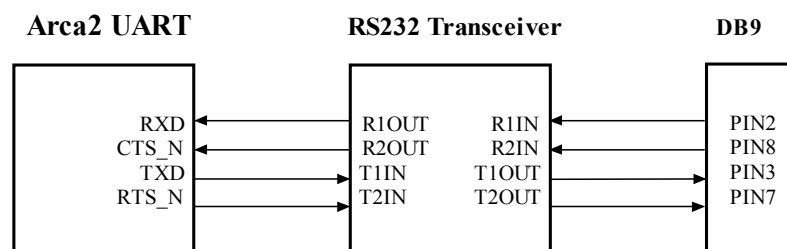


Figure 7-1 Arca210 UART Interface

8 Smart Card Interface

Arca210 integrates a SCC (smart card controller) to support smart card, the SCC is compliant with the ISO/IEC standard 7816-3 for identification of cards. The SCC module is designed to work alternatively with the UART. Register settings are switched between UART and SCC.

8.1 Features

The features of SCC are listed as follow:

- A straightforward extension of UART: When SCC is disabled, UART can work as a normal UART.
- Support asynchronous character (T = 0) communication modes.
 1. Data length: 8 bits
 2. Parity bit generation
 3. Parity error detection and automatic reporting error and re-transmission data on IO line
 4. Supports both direct convention and inverse convention
- Support asynchronous block (T = 1) communication modes.
- SCC clock rate can be selected using on-chip baud rate generator.
- Bit rate can be adjusted according to parameter F/D.
- Support serial clock stop.
- Data communication and error handling are supported by interrupts.

8.2 Interface with Smart Card

The interface example is shown as Figure 8-1. The Linear Technology® LTC1555L provides power conversion and level shifting needed for smart card. The part contains a patented buck/boost charge pump DC/DC converter that delivers a regulated VCC supply voltage to the smart card. Input voltage may range from 2.6V to 6V. The output voltage may be programmed to 1.8V, 3V, 5V or direct connection to the VIN pin. LTC1555L provides >10kV ESD on all smart card pins and short-circuit and over-temperature protected meets all smart card Interface requirements. Please refer to the manufacturer data-sheet for detail information of LTC1555L. The SWA and SWB are used to detect the card insertion, when card insert in the socket, processor will be interrupted.

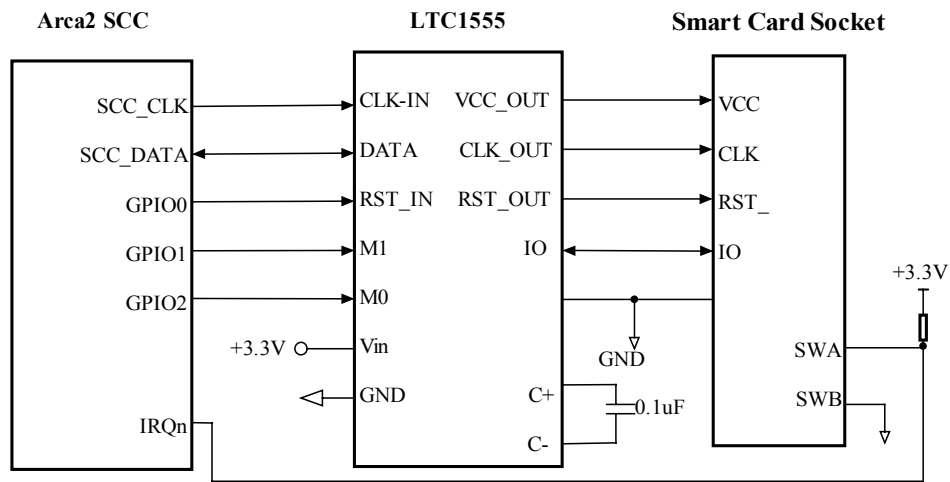


Figure 8-1 Arca210 Smart Card Interface

9 IrDA

Arca210 has an on-chip infrared data association (IrDA) interface that is based on the IrDA 1.0 specification and can perform infrared communication. The IrDA module is designed to work with the UART2. The TxD2 and RxD2 pins are multiplex by IrDA and UART2.

9.1 Features

The features of IrDA are listed as below:

- Based on the IrDA 1.0 specification
- Asynchronous infrared serial communication
 - data length: 8 bits
 - stop bit length: 1 bit
 - parity bit: none
- A straightforward extension of UART2: When IrDA is disabled, UART2 can work as a normal UART.
- Polarity of transmitted and received signals selectable
- When transmitting, support normal 3/16 and IrDA low-power mode bit duration (Here, the “low-power” refers to modulated ‘0’ value bit has a fixed pulse width which is 3/16 of a 115.2Kbps bit duration. This fixed pulse width can lower the power consumption of the optical transceiver out of the chip. So “low-power” in this section has different sense from the “system low power” mode.)
- When receiving, normal 3/16 and low-power mode bit duration signal will both be received as low-power mode bit duration.
- Loopback mode provides a convenient diagnostic method.

9.2 Block Diagram

Figure 9-1 shows the block diagram of the Arca210 IrDA module:

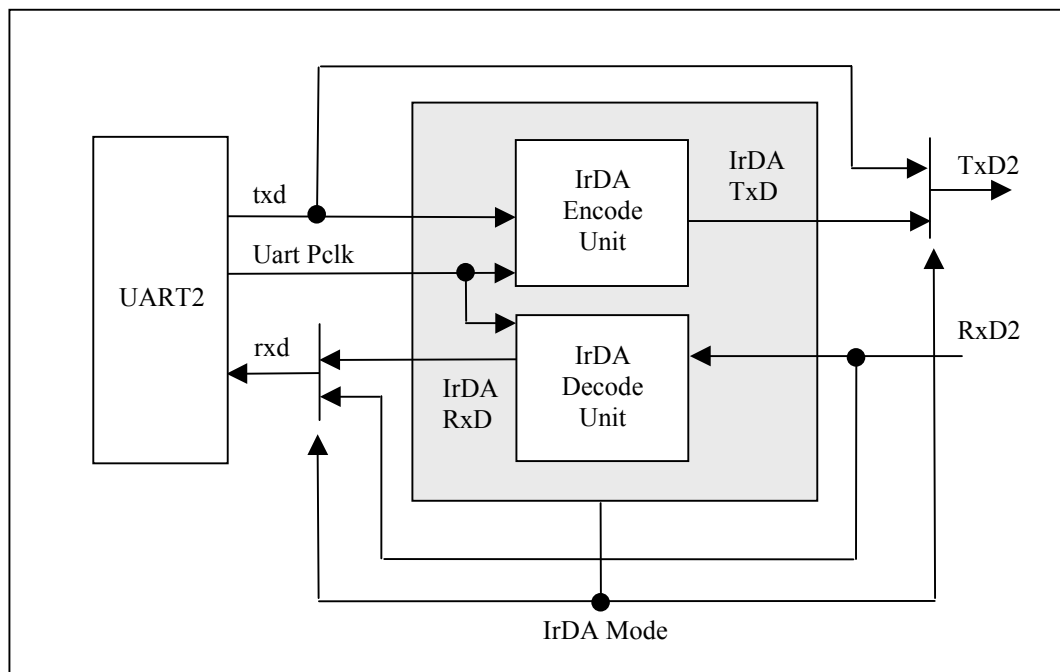


Figure 9-1 IrDA Block Diagram

9.3 Pin Configuration

Table 9-1 IrDA Pins

Name	Full Name	I/O	Function
RxD2	Receive data pin	Input	Receive data input
TxD2	Transmit data pin	Output	Transmit data output

Note: The above pins are disabled for IrDA functions if any of them is used as GPIO.

9.4 Interface with IrDA Device

The interface example is shown as Figure 9-1. Arca Technology recommends you follow the application circuit and layout recommendations given in your IrDA transceiver.

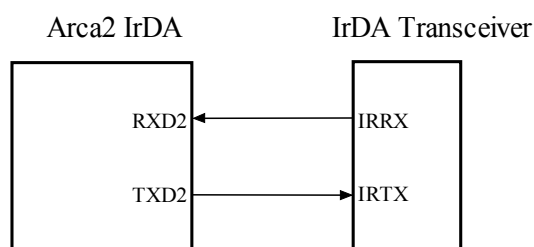


Figure 9-1 Arca210 IrDA Interface

10 I2C

The Inter-Integrated Circuit (I2C) bus interface unit lets the Arca210 processor serve as a master device residing on the I2C bus. The I2C bus is a serial bus developed by Philips Corporation consisting of a two-pin interface. **SDA** is the serial data line and **SCL** is the serial clock line.

Using the I2C bus lets the Arca210 processor interface to other I2C peripherals for system management functions. The serial bus requires a minimum of hardware for an economical system to relay status and reliability information to an external device.

The I2C bus interface unit is a peripheral device that resides on the Arca210 processor internal bus. Data is transmitted to and received from the I2C bus via a buffered interface. Control and status information is relayed through a set of memory-mapped registers. Refer to the I2C Bus Specification for complete details on I2C bus operation.

10.1 Features

The features of Arca210 I2CI are listed as below:

- The I2CI supports only single master mode.
- Support of I²C standard-mode and F/S-mode up to 400 kHz.
- I2CI receiver and transmitter are double-buffered.
- Support burst reading or writing of data.
- Support random writing access of data.
- Support general call address and START byte format after START condition.
- Independent, programmable serial clock generator.
- Support slave coping with fast master during data transfers by holding the SCL line on a bit level.
- The number of devices that you can connect to the same I2C-bus is limited only by the maximum bus capacitance of 400pF.

10.2 Interface with I2C Device

The interface example is shown as Figure 10-1. The I2C bus serial operation uses an open-drain, wired-AND bus structure, so the pull-up device is required on SCL and SDA.

The *I²C Bus Specification*, available from Philips Corporation, states:

The external pull-up devices connected to the bus lines must be adapted to accommodate the shorter maximum permissible rise time for the Fast-mode I²C-bus. For bus loads up to 200 pF, the pull-up device for each bus line can be a resistor; for bus loads between 200 pF and 400 pF, the pull-up device can be a current source (3 mA max.) or a switched resistor circuit.

The design presented in this guide is not intended for loads larger than 200pF, so the pull-up device is a resistor as shown in Figure 10-1.

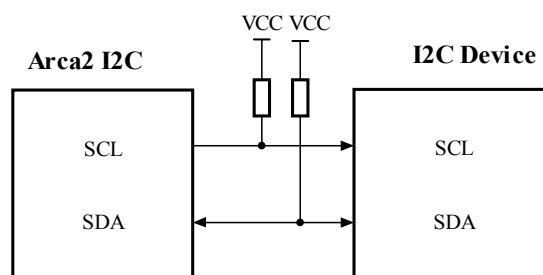


Figure 10-1 Arca210 I2C Interface

11 GPIO

The General Purpose Input/Output (GPIO) ports are used for control and handshake functions between Arca210 and external circuitry by generating output signals and capturing input signals specific for applications. Arca210 supports six GPIO ports – A, B, C, D, E and F. The general-purpose input/output function and alternate internal chip function are configurable. All the pins in port B can be configured as interrupts and sent to INTC. The UART, AC97, SCC, UART2, DMA and ETHC share their pins with GPIO in port C, D, E and F.

11.1 Features

The features of GPIO are listed as below:

- Total pin number is 46 and total port number is 6.
- Each pin can be configured as general purpose input or output.
- Port A is general-purpose I/O port with no alternate functions.
- Signals of Port B have interrupt input alternate function.
- Port C is multiplexed with UART and AC97.
- Port D is multiplexed with SCC, UART2 and DMA.
- Port E is multiplexed with ETHC and DMA.
- Port F is multiplexed with ETHC.
- After power-on reset, all the ports set their pins to input direction and function as general purpose I/O.

12 JTAG/Debug Port

12.1 Description

Arca210 has a built-in JTAG/Debug port, which is essentially several shift registers, with the destination controlled by the TMS pin and data I/O with TDI/TDO. TRST_ provides initialization of the test logic. JTAG is testable via the IEEE 1149.1.

12.2 JTAG Connection

All JTAG pins are directly connected. TCK is driven by external JTAG device, Arca Technology recommends adding a 4.7 k Ω pull-down resistor to TCK. TRST_ must be asserted during power-on. Also, use an external pull-down resistor on TRST_ to prevent spurious state of the JTAG port when disconnected. The circuit in Figure 12-1 shows the connection of the JTAG port.

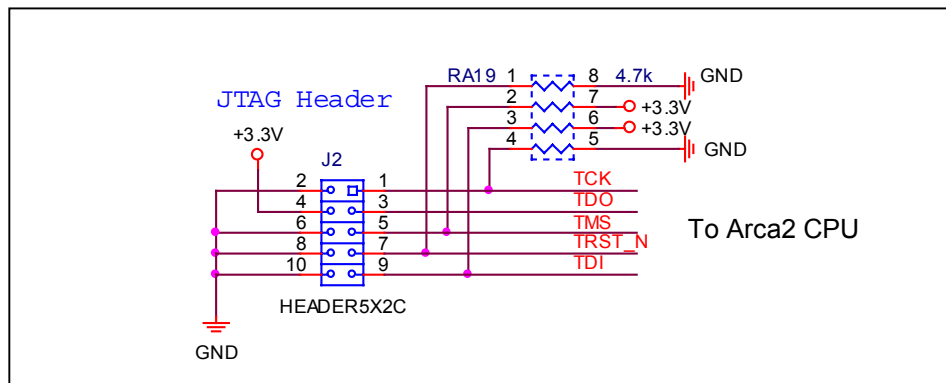


Figure 12-1 JTAG/Debug Header

If you are not utilizing either JTAG or the hardware debug functions, it is highly recommended that you design in a JTAG/debug port on your system anyway. This greatly facilitates board debug, startup, and software development. During final production you would not have to populate the JTAG connector.

13 Power and Clocking

13.1 Operating Conditions

Table 13-1 shows voltage, frequency, and temperature specifications for the Arca210 processor. The frequency range is operation voltage dependent. On a prototype design, the VDDCORE/VDD(PLL) regulator should have a range from 1.5 V to 2.2 V.

Table 13-1 Voltage, Temperature, and Frequency Electrical Specifications

Symbol	Description	Min	Typical	Max
t_A	Ambient Temperature	0°C	-	70°C
VDDCORE	Core Voltage	1.5V	1.8V	2.2V
VDDIO	IO Voltage	3.0V	3.3V	3.6V
VDD(PLL)	PLL Analog Voltage	1.5V	1.8V	2.2V
VDD(USB)	USB Analog Voltage	3.0V	3.3V	3.6V
VSSCORE	Core Power Ground		0V	
VSSIO	IO Power Ground		0V	
VSS(PLL)	PLL Power Ground		0V	
VSS(USB)	USB Power Ground		0V	
Low Voltage Range				
VDDCORE	Core Voltage	1.5V		
VDD(PLL)	PLL Analog Voltage	1.5V		
F_{CORE}	CPU Core Frequency			300MHz
F_{SDARM}	SDRAM Frequency			133MHz
Medium Voltage Range				
VDDCORE	Core Voltage		1.8V	
VDD(PLL)	PLL Analog Voltage		1.8V	
F_{CORE}	CPU Core Frequency			340MHz
F_{SDARM}	SDRAM Frequency			133MHz
High Voltage Range				
VDDCORE	Core Voltage			2.2V
VDD(PLL)	PLL Analog Voltage			2.2V
F_{CORE}	CPU Core Frequency			400MHz
F_{SDARM}	SDRAM Frequency			133MHz

13.2 Electrical Specifications

Table 13-1 provides the Absolute Maximum ratings for the Arca210 processor. These parameters may not be exceeded or the part may be permanently damaged. Operation at Absolute Maximum Ratings is not guaranteed.

Table 13-1 Absolute Maximum Ratings

Symbol	Description	Min	Max
T_s	Storage Temperature	-40°C	125°C
VSS_O	Offset Voltage between any two VSS pins	-0.3V	0.3V
VDD_O	Offset Voltage between any of the following pins: VDDCORE, VDDIO, VDD(PLL), VDD(USB)	-0.3V	0.3V
VDD_HV	Voltage Applied to High Voltage Supplies (VDDIO, VDD(USB))	VSS-0.3 V	VSS+4.0 V
VDD_LV	Voltage Applied to Low Voltage Supplies (VDDCORE, VDD(PLL))	VSS-0.3 V	VSS+2.5 V
V_{IP}	Voltage Applied to non-Supply pins	VSS-0.3 V	max of VDDIO+0.3 V VSS+4.0 V
V_{ESD}	Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000 V

13.3 Power Consumption Specifications

Power consumption on any highly integrated device is extremely dependent on the operating voltage, external switching activity, and external loading (shown in Table 13-1, “Power Consumption Specifications”). Because power consumption on Arca210 processor is optimized, power varies based on which functions are being performed and by the data and frequency requirements of the module.

The maximum power consumption specification is determined by all units running at their maximum: processor speed, voltage, and loading conditions. This method generates a conservative power consumption value; however, power supply and thermal management design requires the highest possible power consumption for robust design. The Arca210 processor’s maximum power consumption is calculated using the following conditions:

- All peripheral units operating at maximum frequency and size configuration
- All I/O loads maximum (50pF for Memory interface, 100pF for peripherals)
- Core operating at worst case power scenario (hit rates adjusted for worst power)
- All voltages at maximum of range

Table 13-1 Power Consumption Specifications

Symbol	Description	Min	Typical	Max
Low Voltage Range				
P_{T_L}	Total Power, Low Range		mW	300 mW
$P_{VDDCORE_VDD(PLL)}$	Power from VDDCORE and VDD(PLL) Supply, Low Range			
$P_{VDDIO_VDD(USB)}$	Power from VDDIO and VDD(USB) Supply, Low Range			
Medium Voltage Range				
P_{T_M}	Total Power, Medium Range			350 mW
$P_{VDDCORE_VDD(PLL)}$	Power from VDDCORE and VDD(PLL) Supply, Medium Range			
$P_{VDDIO_VDD(USB)}$	Power from VDDIO and VDD(USB) Supply, Medium Range			
High Voltage Range				
P_{T_H}	Total Power, High Range			400 mW
$P_{VDDCORE_VDD(PLL)}$	Power from VDDCORE and VDD(PLL) Supply, High Range			
$P_{VDDIO_VDD(USB)}$	Power from VDDIO and VDD(USB) Supply, High Range			

13.4 Oscillator Electrical Specifications

The Arca210 processor contains one oscillators – 14.318 MHz, which need a specific crystal. When choosing a crystal, match the crystal parameters in Table 13-1 as closely as possible.

Table 13-1 14.318 MHz Oscillator Specifications

Symbol	Description	Min	Typical	Max
Crystal - Typical is FOX HC49S				
F_{XP}	Frequency, XTAL/EXTAL	-	14.318 MHz	-
L_{MP}	Motional Inductance, XTAL/EXTAL	-	0.50 H	-
C_{MP}	Motional Capacitance, XTAL/EXTAL	-	3.68 fF	-
R_{MP}	Motional Resistance, XTAL/EXTAL	-	-	40 Ω
C_{OP}	Shunt Capacitance XTAL to EXTAL	-	-	7 pF
C_{LP}	Load Capacitance XTAL/EXTAL	-	16 pF	-

To drive the 14.318 MHz crystal pins from an external source:

- Drive the EXTAL pin with a digital signal that has a low level near 0 V and a high level near VDDIO. The minimum slew rate is 1 V per 10 ns. The maximum current drawn by the external clock source when the clock is at its maximum positive voltage should be about 1 mA.
- Float the XTAL pin.

13.5 Reset and Power AC Timing Specifications

The Arca210 processor asserts the RESETOUT_ pin in one of several modes:

- Power On
- Hardware Reset (RESETP_)
- Manual Reset (RESETM_)
- Watch Dog Reset
- PCI Reset When Satellite Mode

The following sections give the timing and other specifications for the entry and exit of these modes.

13.5.1 Power Supply Connectivity

The Arca210 processor requires two externally-supplied voltage levels. VDDIO/VDD(USB) requires high (3.3V, typical), and VDDCORE and VDD(PLL) require low voltage (1.8V, typical). VDD(PLL) provides power for internal analog PLL and should be separated from other low voltage supplies.

13.5.2 Power On Timing

The External Voltage Regulator and other power-on devices must provide the Arca210 processor with a specific sequence of power and resets to ensure proper operation. This sequence is shown in Figure 13-1, “Power-On Reset Timing” and detailed in Table 13-1, “Power-On Timing Specifications”. It is important that the Arca210 processor power supplies be powered-up in a certain order to avoid high current situations. The required order is:

1. VDDIO & VDD(USB)
2. VDDCORE & VDD(PLL)

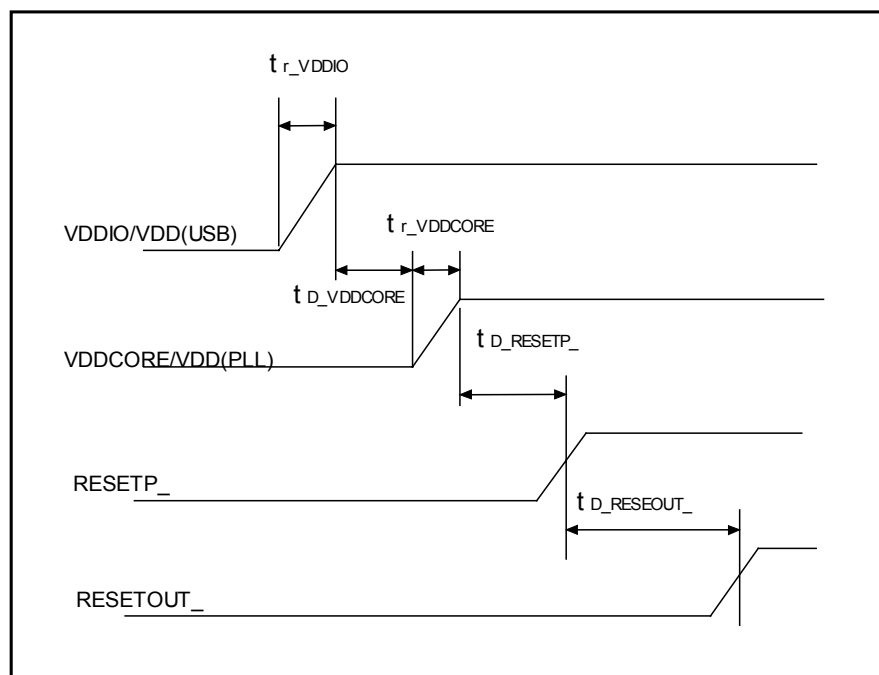


Figure 13-1 Power-On Reset Timing

Table 13-1 Power-On Timing Specifications

Symbol	Description	Min	Typical	Max
t_{r_VDDIO}	VDDIO/VDD(USB) Rise / Stabilization time	0.01 ms	-	100 ms
$t_{D_VDDCORE}$	Delay between VDDIO/VDD(USB) stable and VDDCORE/VDD(PLL) applied	0 ms	-	-
$t_{r_VDDCORE}$	VDDCORE/VDD(PLL) Rise / Stabilization time	0.01 ms	-	100 ms
$t_{D_RESETP_}$	Delay between VDDCORE, VDD(PLL) stable and RESETP_ deasserted	50 ms	-	-
$t_{D_RESETOUT_}$	Delay between RESETP_ deasserted and RESETOUT_ deasserted	-	100 ms	-

13.5.3 Hardware Reset Timing

The timing sequences shown in Figure 13-1 “Hardware Reset Timing” assumes the power supplies are stable at the assertion of RESETP_. If the power supplies are unstable, follow the timings indicated in Section 13.5.2, “Power On Timing”.

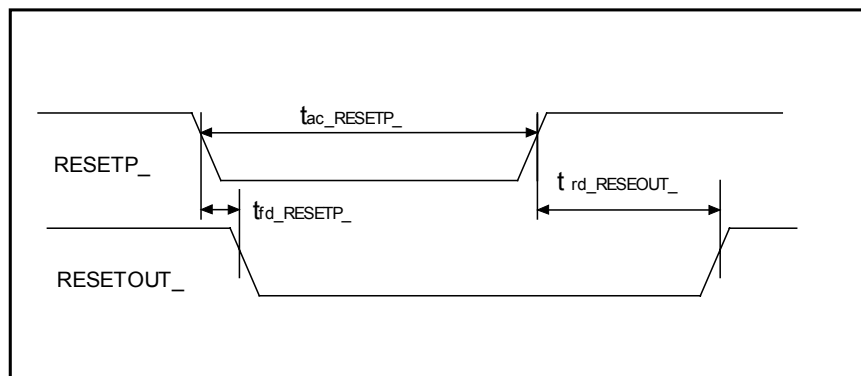


Figure 13-1 Hardware Reset Timing

Table 13-1 Hardware Reset Timing Specifications

Symbol	Description	Min	Typical	Max
$t_{ac_RESETP_}$	Minimum assertion time of RESETP_	1 ms	-	-
$t_{fd_RESETOUT_}$	Delay between RESETP_ Asserted and RESETOUT_ Asserted	0 ms	-	0.01 ms
$t_{rd_RESET_OUT}$	Delay between RESETP_ deasserted and RESETOUT_ deasserted	-	100 ms	-

14 Appendix: Draco Development Platform Schematic