HD66421

(RAM-Provided 160 Channel 4-Level Grey Scale Driver for Dot Matrix Graphics LCD)

Description

The HD66421 drives and controls a dot matrix graphic LCD(Liquid Crystal Display) using a bit-mapped method. It provides a highly flexible display through its on-chip display RAM, in which each two bits of data can be used to turn on or off one dot on LCD panel with four-level grey scale.
A single HD66421 can display a maximum of 160x100 dots using its powerful display control functions. It can display only eight lines out of one hundred lines.

This function realize low power consumption because high voltage for driving LCD is not needed.
An MPU can access HD66421 at any time, because the MPU operations are asynchronous with the HD66421's system clock and display operation.
Its low-voltage operation at 2.2 to 5.5V and standby function provides low power -dissipation, making the HD66421 suitable for small portable device applications.

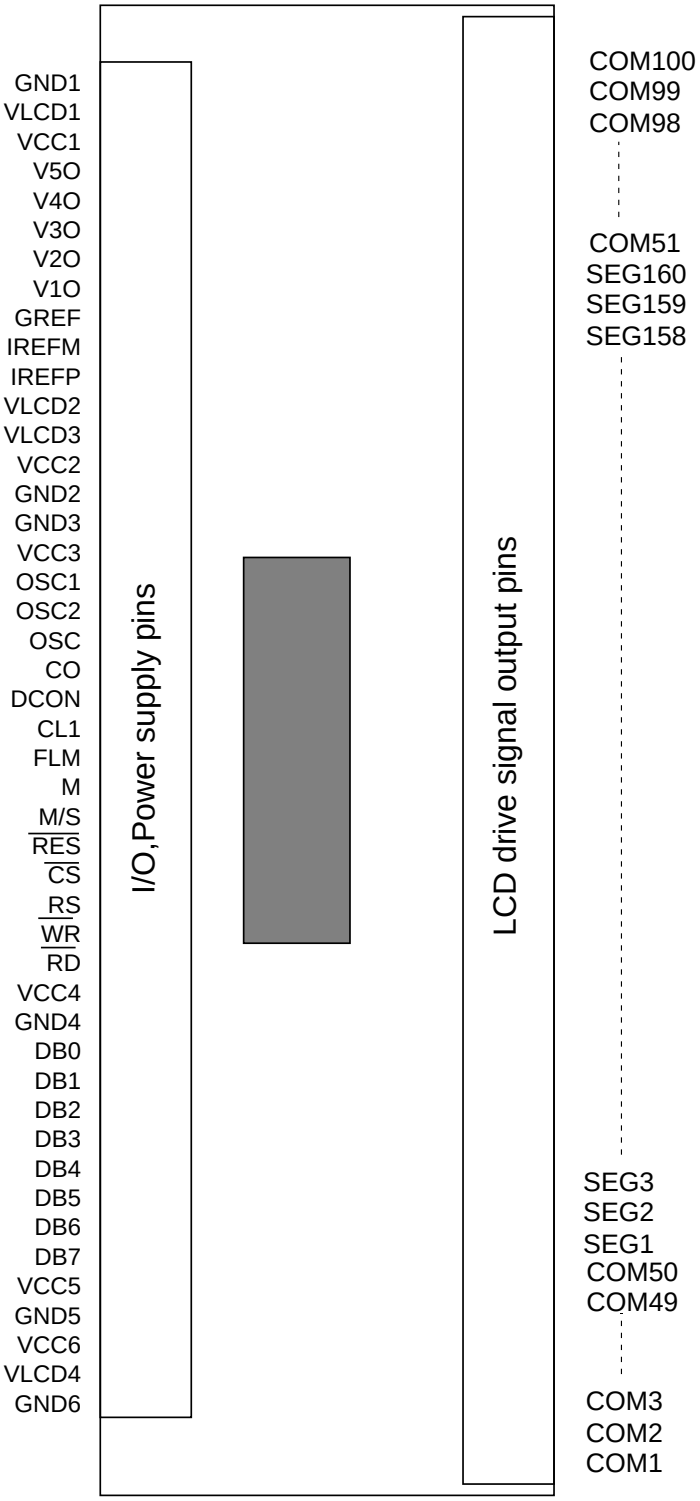
Features

• Built-in bit-mapped display RAM: 30kbits (160 x 100 x 2 bits)
• Grey scale display: PWM four-level grey scale can be selected from 32 levels
• Grey scale memory management: Packed pixel
• Monochrome display: two planes can be selected. One plane is displayed while the other plane is being written.
• Partial display: Eight-lines data can be displayed in any place
• An 80-system MPU interface
• Power supply voltage for operation : 2.2V to 5.5V
• Power supply voltage for LCD : 18 V max.
• Selectable multiplex duty ratio: 1/8, 1/64, 1/80, 1/100
• LCD driving alternating cycle: 7, 11, 13 lines or flame
• Built-in oscillator: external resister
• Low power consumption:
• Circuits for generating LCD driving voltage : Contrast control, Operational amplifier, and Resistive dividers
• Internal resistive divider: programmable bias rate
• 32-level programmable contrast control
• Wide range of instructions
reversible display, display on/off, vertical display scroll, blink, reversible address, read-modify-write mode
• Package: TCP

Ordering Information

Type No.	Package
HD66421TB0	TCP
HCD66421BP	Die with gold bump

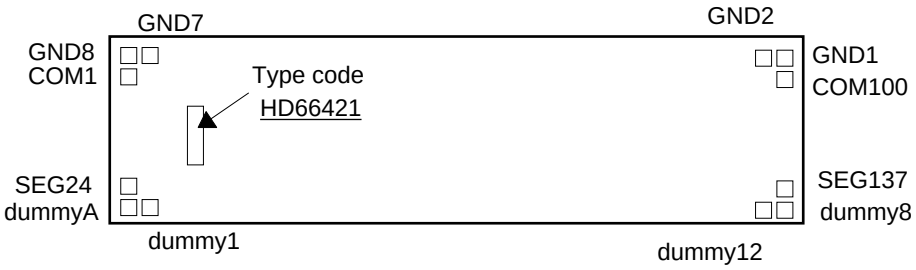
Pin Arrangement



Note: This figure is not drawn to a scale

Pad Arrangement

Chip size : 8.99 x 4.72 mm
Coordinate : Pad center
Origin : Chip Center
Bump size : GND1, GND8, dummy A, dummy B 70 x 70 µm
Power, I/O (Pad No. 276 to 321) 50 x 70 µm
COM1 - 100, SEG1 - 160, dummy1 -12 35 x 50 µm



Pad Location Coordinate

No.	PAD NAME	X	Y	No.	PAD NAME	X	Y	No.	PAD NAME	X	Y
1	COM1	-4217	1731	31	COM31	-4217	230	61	SEG11	-4217	-1299
2	COM2	-4217	1681	32	COM32	-4217	179	62	SEG12	-4217	-1349
3	COM3	-4217	1631	33	COM33	-4217	129	63	SEG13	-4217	-1399
4	COM4	-4217	1581	34	COM34	-4217	79	64	SEG14	-4217	-1449
5	COM5	-4217	1531	35	COM35	-4217	29	65	SEG15	-4217	-1499
6	COM6	-4217	1481	36	COM36	-4217	-21	66	SEG16	-4217	-1549
7	COM7	-4217	1430	37	COM37	-4217	-71	67	SEG17	-4217	-1599
8	COM8	-4217	1380	38	COM38	-4217	-121	68	SEG18	-4217	-1649
9	COM9	-4217	1330	39	COM39	-4217	-171	69	SEG19	-4217	-1699
10	COM10	-4217	1280	40	COM40	-4217	-221	70	SEG20	-4217	-1749
11	COM11	-4217	1230	41	COM41	-4217	-271	71	SEG21	-4217	-1799
12	COM12	-4217	1180	42	COM42	-4217	-321	72	SEG22	-4217	-1849
13	COM13	-4217	1130	43	COM43	-4217	-371	73	SEG23	-4217	-1899
14	COM14	-4217	1080	44	COM44	-4217	-421	74	SEG24	-4217	-1949
15	COM15	-4217	1030	45	COM45	-4217	-471	75	dummy A	-4217	-2082
16	COM16	-4217	980	46	COM46	-4217	-521	76	dummy 1	-4029	-2082
17	COM17	-4217	930	47	COM47	-4217	-571	77	dummy 2	-3907	-2082
18	COM18	-4217	880	48	COM48	-4217	-621	78	dummy 3	-3827	-2082
19	COM19	-4217	830	49	COM49	-4217	-671	79	dummy 4	-3619	-2082
20	COM20	-4217	780	50	COM50	-4217	-721	80	dummy 5	-3497	-2075
21	COM21	-4217	730	51	SEG1	-4217	-798	81	dummy 6	-3419	-2075
22	COM22	-4217	680	52	SEG2	-4217	-848	82	SEG25	-2822	-2082
23	COM23	-4217	630	53	SEG3	-4217	-898	83	SEG26	-2772	-2082
24	COM24	-4217	580	54	SEG4	-4217	-948	84	SEG27	-2722	-2082
25	COM25	-4217	530	55	SEG5	-4217	-998	85	SEG28	-2672	-2082
26	COM26	-4217	480	56	SEG6	-4217	-1049	86	SEG29	-2622	-2082
27	COM27	-4217	430	57	SEG7	-4217	-1099	87	SEG30	-2572	-2082
28	COM28	-4217	380	58	SEG8	-4217	-1149	88	SEG31	-2522	-2082
29	COM29	-4217	330	59	SEG9	-4217	-1199	89	SEG32	-2472	-2082
30	COM30	-4217	280	60	SEG10	-4217	-1249	90	SEG33	-2422	-2082

No.	PAD NAME	X	Y	No.	PAD NAME	X	Y	No.	PAD NAME	X	Y
91	SEG34	-2372	-2082	141	SEG84	220	-2082	191	SEG134	2722	-2082
92	SEG35	-2322	-2082	142	SEG85	270	-2082	192	SEG135	2772	-2082
93	SEG36	-2272	-2082	143	SEG86	320	-2082	193	SEG136	2822	-2082
94	SEG37	-2222	-2082	144	SEG87	370	-2082	194	dummy 7	3419	-2075
95	SEG38	-2172	-2082	145	SEG88	420	-2082	195	dummy 8	3497	-2075
96	SEG39	-2121	-2082	146	SEG89	470	-2082	196	dummy 9	3619	-2082
97	SEG40	-2071	-2082	147	SEG90	520	-2082	197	dummy 10	3827	-2082
98	SEG41	-2021	-2082	148	SEG91	570	-2082	198	dummy 11	3907	-2082
99	SEG42	-1971	-2082	149	SEG92	620	-2082	199	dummy 12	4029	-2082
100	SEG43	-1921	-2082	150	SEG93	670	-2082	200	dummy B	4217	-2082
101	SEG44	-1871	-2082	151	SEG94	720	-2082	201	SEG137	4217	-1949
102	SEG45	-1821	-2082	152	SEG95	770	-2082	202	SEG138	4217	-1899
103	SEG46	-1771	-2082	153	SEG96	820	-2082	203	SEG139	4217	-1849
104	SEG47	-1721	-2082	154	SEG97	870	-2082	204	SEG140	4217	-1799
105	SEG48	-1671	-2082	155	SEG98	921	-2082	205	SEG141	4217	-1749
106	SEG49	-1621	-2082	156	SEG99	971	-2082	206	SEG142	4217	-1699
107	SEG50	-1571	-2082	157	SEG100	1021	-2082	207	SEG143	4217	-1649
108	SEG51	-1521	-2082	158	SEG101	1071	-2082	208	SEG144	4217	-1599
109	SEG52	-1471	-2082	159	SEG102	1121	-2082	209	SEG145	4217	-1549
110	SEG53	-1421	-2082	160	SEG103	1171	-2082	210	SEG146	4217	-1499
111	SEG54	-1371	-2082	161	SEG104	1221	-2082	211	SEG147	4217	-1449
112	SEG55	-1321	-2082	162	SEG105	1271	-2082	212	SEG148	4217	-1399
113	SEG56	-1271	-2082	163	SEG106	1321	-2082	213	SEG149	4217	-1349
114	SEG57	-1221	-2082	164	SEG107	1371	-2082	214	SEG150	4217	-1299
115	SEG58	-1171	-2082	165	SEG108	1421	-2082	215	SEG151	4217	-1249
116	SEG59	-1121	-2082	166	SEG109	1471	-2082	216	SEG152	4217	-1199
117	SEG60	-1071	-2082	167	SEG110	1521	-2082	217	SEG153	4217	-1149
118	SEG61	-1021	-2082	168	SEG111	1571	-2082	218	SEG154	4217	-1099
119	SEG62	-971	-2082	169	SEG112	1621	-2082	219	SEG155	4217	-1049
120	SEG63	-921	-2082	170	SEG113	1671	-2082	220	SEG156	4217	-998
121	SEG64	-870	-2082	171	SEG114	1721	-2082	221	SEG157	4217	-948
122	SEG65	-820	-2082	172	SEG115	1771	-2082	222	SEG158	4217	-898
123	SEG66	-770	-2082	173	SEG116	1821	-2082	223	SEG159	4217	-848
124	SEG67	-720	-2082	174	SEG117	1871	-2082	224	SEG160	4217	-798
125	SEG68	-670	-2082	175	SEG118	1921	-2082	225	COM51	4217	-721
126	SEG69	-620	-2082	176	SEG119	1971	-2082	226	COM52	4217	-671
127	SEG70	-570	-2082	177	SEG120	2021	-2082	227	COM53	4217	-621
128	SEG71	-520	-2082	178	SEG121	2071	-2082	228	COM54	4217	-571
129	SEG72	-470	-2082	179	SEG122	2121	-2082	229	COM55	4217	-521
130	SEG73	-420	-2082	180	SEG123	2172	-2082	230	COM56	4217	-471
131	SEG74	-370	-2082	181	SEG124	2222	-2082	231	COM57	4217	-421
132	SEG75	-320	-2082	182	SEG125	2272	-2082	232	COM58	4217	-371
133	SEG76	-270	-2082	183	SEG126	2322	-2082	233	COM59	4217	-321
134	SEG77	-220	-2082	184	SEG127	2372	-2082	234	COM60	4217	-271
135	SEG78	-170	-2082	185	SEG128	2422	-2082	235	COM61	4217	-221
136	SEG79	-120	-2082	186	SEG129	2472	-2082	236	COM62	4217	-171
137	SEG80	-70	-2082	187	SEG130	2522	-2082	237	COM63	4217	-121
138	SEG81	70	-2082	188	SEG131	2572	-2082	238	COM64	4217	-71
139	SEG82	120	-2082	189	SEG132	2622	-2082	239	COM65	4217	-21
140	SEG83	170	-2082	190	SEG133	2672	-2082	240	COM66	4217	29

No.	PAD NAME	X	Y
241	COM67	4217	79
242	COM68	4217	129
243	COM69	4217	179
244	COM70	4217	230
245	COM71	4217	280
246	COM72	4217	330
247	COM73	4217	380
248	COM74	4217	430
249	COM75	4217	480
250	COM76	4217	530
251	COM77	4217	580
252	COM78	4217	630
253	COM79	4217	680
254	COM80	4217	730
255	COM81	4217	780
256	COM82	4217	830
257	COM83	4217	880
258	COM84	4217	930
259	COM85	4217	980
260	COM86	4217	1030
261	COM87	4217	1080
262	COM88	4217	1130
263	COM89	4217	1180
264	COM90	4217	1230
265	COM91	4217	1280
266	COM92	4217	1330
267	COM93	4217	1380
268	COM94	4217	1430
269	COM95	4217	1481
270	COM96	4217	1531
271	COM97	4217	1581
272	COM98	4217	1631
273	COM99	4217	1681
274	COM100	4217	1731
275	GND1	4217	2195
276	GND2	4091	2195
277	VLCD1	3992	2195
		3912	2195
278	Vcc1	3809	2195
		3729	2195
279	V5O	3628	2195
		3548	2195
280	V4O	3447	2195
		3367	2195
281	V3O	3266	2195
		3186	2195
282	V2O	3084	2195
		3004	2195
283	V1O	2903	2195
		2823	2195
284	GREF	2722	2195
		2642	2195
285	IREFM	2541	2195
		2461	2195
286	IREFP	2360	2195
		2280	2195
287	VLCD2	2179	2195
		2099	2195
288	VLCD3	2009	2195
		1929	2195
289	Vcc2	1830	2195
		1750	2195
290	GND3	1647	2195
		1567	2195
291	GND4	1494	2195
		1414	2195
292	Vcc3	1316	2195
		1236	2195
293	OSC1	947	2195
		867	2195
294	OSC2	766	2195
		686	2195
295	OSC	585	2195
		505	2195
296	CO	404	2195
		324	2195
297	DCON	223	2195
		143	2195
298	CL1	41	2195
		-39	2195
299	FLM	-140	2195
		-220	2195
300	M	-321	2195
		-401	2195
301	M/S	-502	2195
		-582	2195
302	RES	-683	2195
		-763	2195
303	CS	-864	2195
		-944	2195
304	RS	-1045	2195
		-1125	2195
305	WR	-1226	2195
		-1306	2195
306	RD	-1407	2195
		-1487	2195
307	Vcc4	-1587	2195
		-1667	2195
308	GND5	-1770	2195
		-1850	2195
309	DB0	-1948	2195
		-2028	2195
310	DB1	-2131	2195
		-2211	2195
311	DB2	-2310	2195
		-2390	2195
312	DB3	-2494	2195
		-2574	2195
313	DB4	-2672	2195
		-2752	2195
314	DB5	-2856	2195
		-2936	2195
315	DB6	-3034	2195
		-3114	2195
316	DB7	-3218	2195
		-3298	2195
317	Vcc5	-3398	2195
		-3478	2195
318	GND6	-3581	2195
		-3661	2195
319	Vcc6	-3739	2195
		-3819	2195
320	VLCD4	-3910	2195
		-3990	2195
321	GND7	-4091	2195
322	GND8	-4217	2195

Pin Description

Pin Name	Number of Pins	I/O	Connected to	Description
Vcc1-6, GND1-6	12	-	Power supply	Vcc: +2.2V to +5.5V, GND: 0V
VLCD1-4	4	-	Power supply	Power supply to LCD driving circuit
V1O, V2O, V3O,V4O, V5O	5	-	V1 to V5 of HD66421	Several levels of power to the LCD driving outputs. Master HD66421 outputs these levels to the slave HD66421.
OSC	1	I,	Oscillator resister or external clock	Must be connected to external resister when using R-C oscillation. When using an external clock, it must be input to the OSC terminal.
OSC1,OSC2	2	I/O		
CO	1	O	OSC of Slave HD66421	Clock output
DCON	1	O	External DC/DC convertor	Controls on/off switch of external DC/DC convertor
CL1	1	I/O	CL1 of HD66421	Line clock
FLM	1	I/O	FLM of HD66421	Frame signal
M	1	I/O	M of HD66421	Converts LCD driving outputs to AC
M/S	1	I	Vcc or GND	Specifies master/slave mode.
$\overline{RES}$	1	I	-	Reset the LSI internally when drive low.
$\overline{CS}$	1	I	MPU	Select the LSI, specifically internal registers (index and data registers) when driven low.
RS	1	I	MPU	Select one of the internal registers; select the index register when driven low and data registers when driven low.
$\overline{WR}$	1	I	MPU	Inputs write strobe; allows a write access when driven low.
$\overline{RD}$	1	I	MPU	Inputs read strobe; allows a read access when driven low.
DB7 to DB0	8	I/O	MPU	8-bits three-state bidirectional data bus; transfer data between the HD66420 and MPU through this bus.
SEG1 to SEG160	160	O	LCD	Output column drive signals
COM1 to COM100	100	O	LCD	Output row drive signals
IREFP	1	-	VCC	Power supply for internal operation amplifier
IREFM	1	-	External resistor	Bias current for internal operational amplifier
GREF	1	-	GND	Power supply for internal operation amplifier

Register List

CS	RS	Index Reg. Bits						Register Name	R/W	Data bits							
		4	3	2	1	0				7	6	5	4	3	2	1	0
1	-	-	-	-	-	-			-								
0	0	-	-	-	-	-	IR	Index register	W				IR4	IR3	IR2	IR1	IR0
0	1	0	0	0	0	0	R0	Control register 1	W	RMW	DISP	STBY	PWR	AMP	REV	HOLT	ADC
0	1	0	0	0	0	1	R1	Control register 2	W	BIS1	BIS0	WLS	GRAY	DTY1	DTY0	INC	BLK
0	1	0	0	0	1	0	R2	X address register	W			XA5	XA4	XA3	XA2	XA1	XA0
0	1	0	0	0	1	1	R3	Y address register	W		YA6	YA5	YA4	YA3	YA2	YA1	YA0
0	1	0	0	1	0	0	R4	Display RAM access register	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	1	R5	Display start line register	W		ST6	ST5	ST4	ST3	ST2	ST1	ST0
0	1	0	0	1	1	0	R6	Blink start line register	W		BSL6	BSL5	BSL4	BSL3	BSL2	BSL1	BSL0
0	1	0	0	1	1	1	R7	Blink end line register	W		BEL6	BEL5	BEL4	BEL3	BEL2	BEL1	BEL0
0	1	0	1	0	0	0	R8	Blink register 1	W	BK0	BK1	BK2	BK3	BK4	BK5	BK6	BK7
0	1	0	1	0	0	1	R9	Blink register 2	W	BK8	BK9	BK10	BK11	BK12	BK13	BK14	BK15
0	1	0	1	0	1	0	R10	Blink register 3	W					BK16	BK17	BK18	BK19
0	1	0	1	0	1	1	R11	Partial display block register	W				CLE	PB3	PB2	PB1	PB0
0	1	0	1	1	0	0	R12	Gray scale palette 1 (0,0)	W				GP14	GP13	GP12	GP11	GP10
0	1	0	1	1	0	1	R13	Gray scale palette 2 (0,1)	W				GP24	GP23	GP22	GP21	GP20
0	1	0	1	1	1	0	R14	Gray scale palette 3 (1,0)	W				GP34	GP33	GP32	GP31	GP30
0	1	0	1	1	1	1	R15	Gray scale palette 4 (1,1)	W				GP44	GP43	GP42	GP41	GP40
0	1	1	0	0	0	0	R16	Contrast control register	W		CM1	CM0	CC4	CC3	CC2	CC1	CC0
0	1	1	0	0	0	1	R17	Plane selection register	W						MON	DSEL	PSEL
0	1	1	0	0	1	0	R18	Reserved	-								
0	1	1	0	0	1	1	R19	Reserved	-								
0	1	1	0	1	0	0	R20	Reserved	-								
0	1	1	0	1	0	1	R21	Reserved	-								
0	1	1	0	1	1	0	R22	Reserved	-								
0	1	1	0	1	1	1	R23	Reserved	-								
0	1	1	1	0	0	0	R24	Reserved	-								
0	1	1	1	0	0	1	R25	Reserved	-								
0	1	1	1	0	1	0	R26	Reserved	-								
0	1	1	1	0	1	1	R27	Reserved	-								
0	1	1	1	1	0	0	R28	Reserved	-								
0	1	1	1	1	0	1	R29	Reserved	-								
0	1	1	1	1	1	0	R30	Reserved	-								
0	1	1	1	1	1	1	R31	Reserved	-								

RMW

RMW = 1: Read-modify-write mode; Address is incremented only after write access
RMW = 0: Address is incremented after both write and read access

DISP

DISP = 1: Display on
DISP = 0: Display off

STBY

STBY = 1:Internal operation and power circuit halt; display off
STBY = 0: Normal operation

PWR

PWR = 1: Output 'High' from DCON
PWR = 0: Output 'Low' from DCON

AMP

AMP = 1: OP amp enable
AMP = 0: OP amp disable

REV

REV = 1: Reverse display
REV = 0: Normal display

HOLT

HOLT = 1: Internal operation stops, Oscillator works
HOLT = 0: Internal operation starts

ADC

ADC = 1: Data in X address H'0 is output from SEG160
ADC = 0: Data in X address H'0 is output from SEG1

BIS1, 0

BIS1, 0 = (1,1): 1/8 LCD drive levels bias ratio
BIS1, 0 = (1,0): 1/9 LCD drive levels bias ratio
BIS1, 0 = (0,1): 1/10 LCD drive levels bias ratio
BIS1, 0 = (0,0): 1/11 LCD drive levels bias ratio

WLS

WLS = 1: 6-bit data is valid
WLS = 0: 8-bit data is valid

GRAY

GRAY = 1: Grayscale palette is available(gray scales can be selected from 32-levels)
GRAY = 0: Grayscale palette is not available(4-gray scales fixed)

DTY1, 0

DTY1, 0 = (1,1): 1/8 display duty cycle - Partial display
DTY1, 0 = (1,0): 1/64 display duty cycle
DTY1, 0 = (0,1): 1/80 display duty cycle
DTY1, 0 = (0,0): 1/100 display duty cycle

INC

INC = 1: X address is incremented for each access
INC = 0: Y address is incremented for each access

BLK

BLK = 1: Blink function is used
BLK = 0: Blink function is not used

CM1, 0

CM1, 0 = (1,1): Alternative cycle is 13 lines.
CM1, 0 = (1,0): Alternative cycle is 11lines.
CM1, 0 = (0,1): Alternative cycle is 7 lines.
CM1, 0 = (0,0): Alternative cycle is 1 frame.

MON

MON = 1: Monochrome display
MON = 0: Four levels gray scale display

DSEL

DSEL = 1: Plane 1 is displayed
DSEL = 0: Plane 0 is displayed

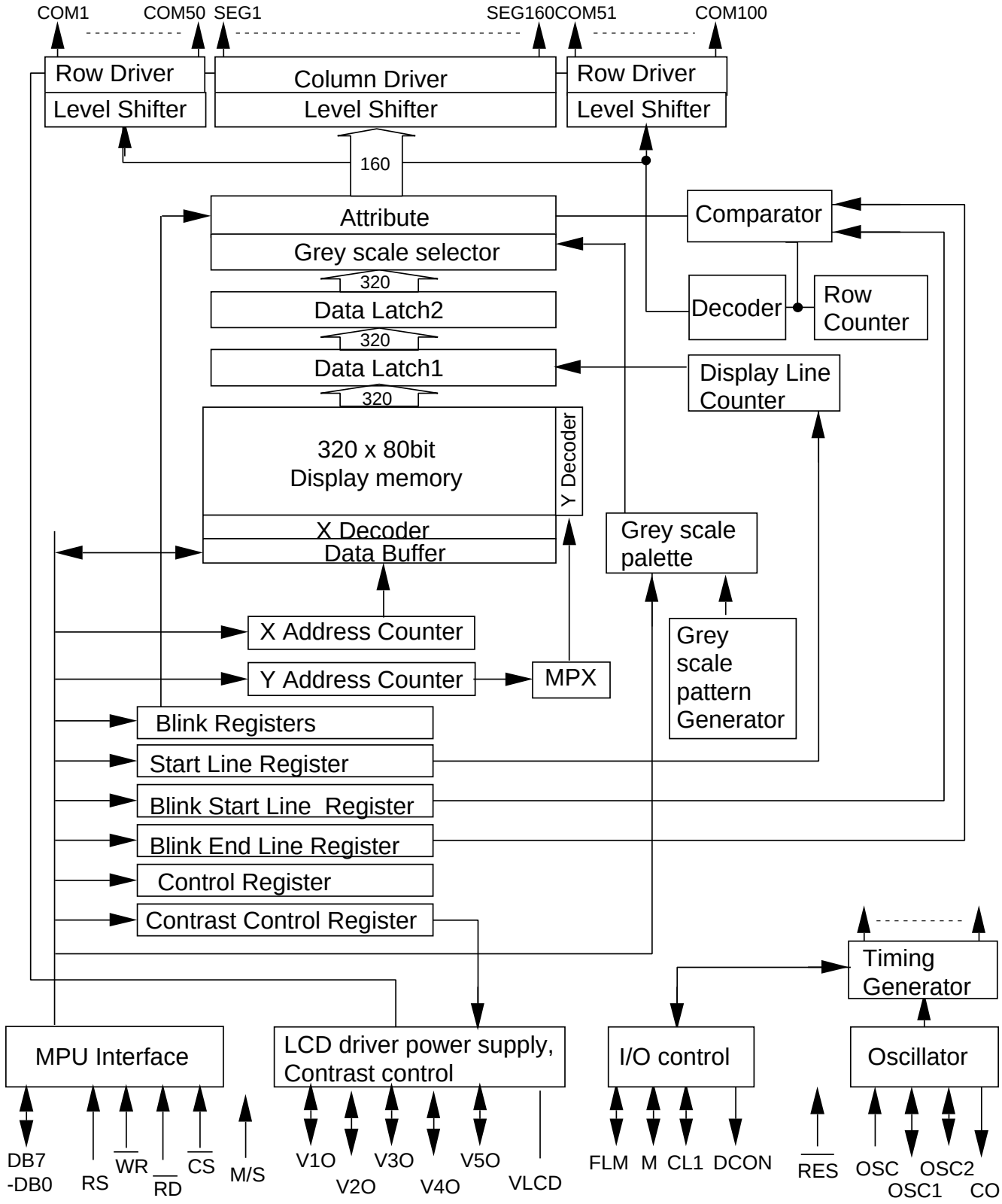
PSEL

PSEL = 1: Plane 1 is read/written from the MPU
PSEL = 0: Plane 0 is read/written from the MPU

CLE

CLE = 1: CO,CL1,FLM,M stop in master mode. They are high-Z.
CLE = 0: CO,CL1,FLM,M are operating in master mode. Normal operation.

Block Diagram



System Description

The HD66421 can display a maximum of 160 x 100 dots (ten 16x16-dot characters x 6 lines) four-level gray scale or four colour LCD panel. Four levels of gray scale can be selected from 32-levels, so the appropriate 4-level gray scale can be displayed. And Monochrome display can be selected from two planes. One plane is displayed while the other plane is being written. The HD66421 can reduce power dissipation without affecting display because data is retained in the display RAM even during standby modes. An LCD system can be configured simply by attaching external power supply, capacitors and resistors (figure 1) since the HD66421 incorporates power circuits.

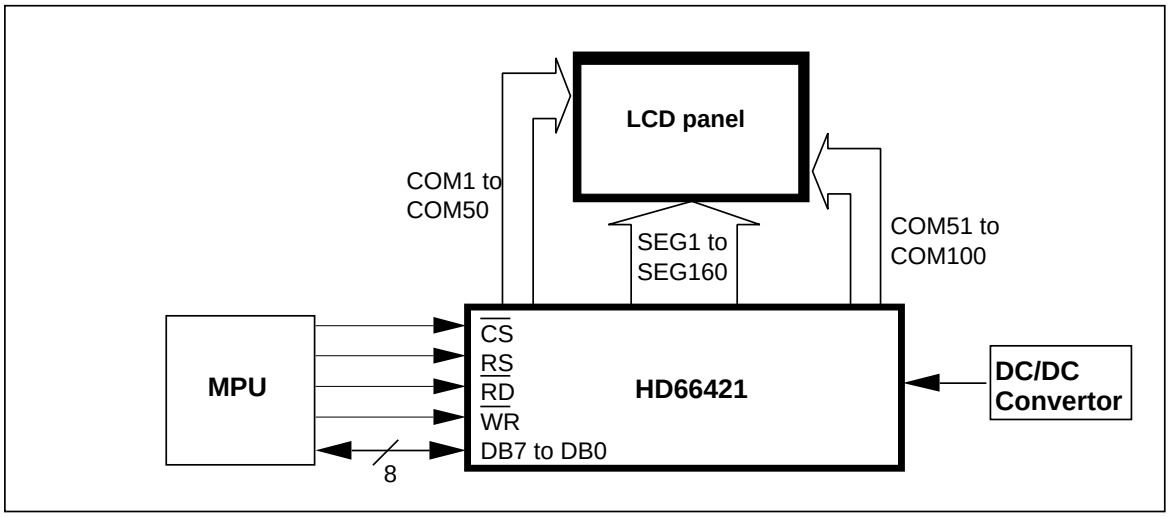
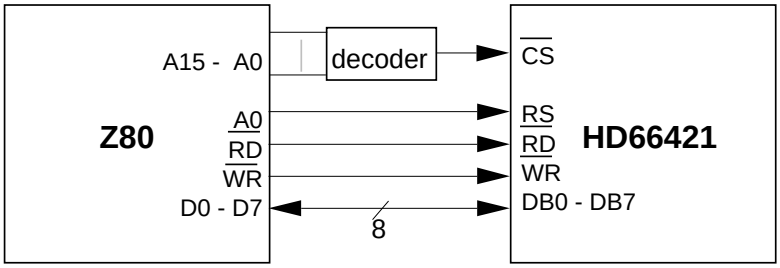


Figure 1 System Block Diagram

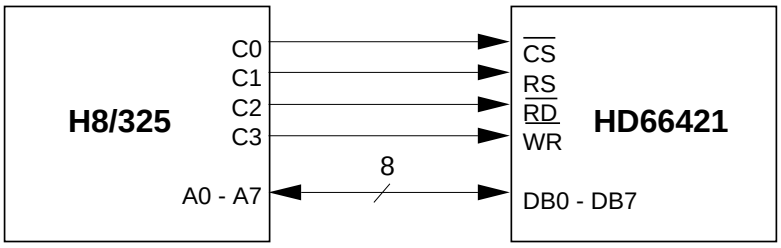
MPU Interface

The HD66421 can interface directly to an MPU through an 8-bit data bus or through an I/O port (figure 2). The MPU can access the HD66421 internal registers independently of internal clock timing.

The index register can be directly accessed but the other registers (data registers) cannot. Before accessing a data register, its register number must be written to the index register. Once written, the register number is held until it is rewritten, enabling the same register to be consecutively accessed without having to rewrite to the register number for each access. An example of a register access sequence is shown in figure 3.



a) Interface through Bus



b) Interface through I/O Port

Figure 2 8-Bit MPU Interface Examples

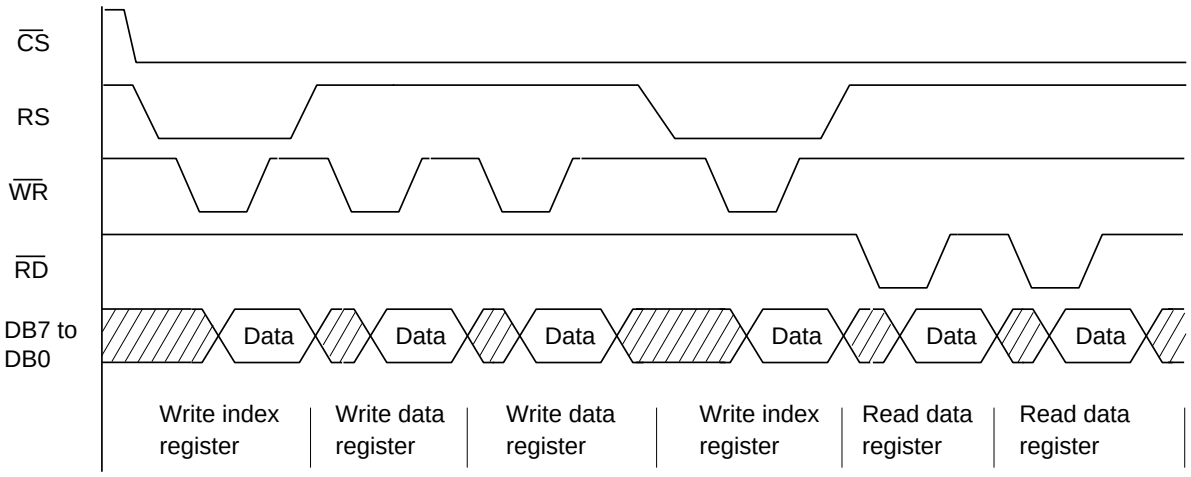


Figure 3 8-Bit Data Transfer Sequence

LCD Driver Configuration

Row and column outputs: The HD66421's row outputs is only both sides. In any case, each output's function is fixed; COM1 to COM100 output row signals and SEG1 to SEG160 output column signals.

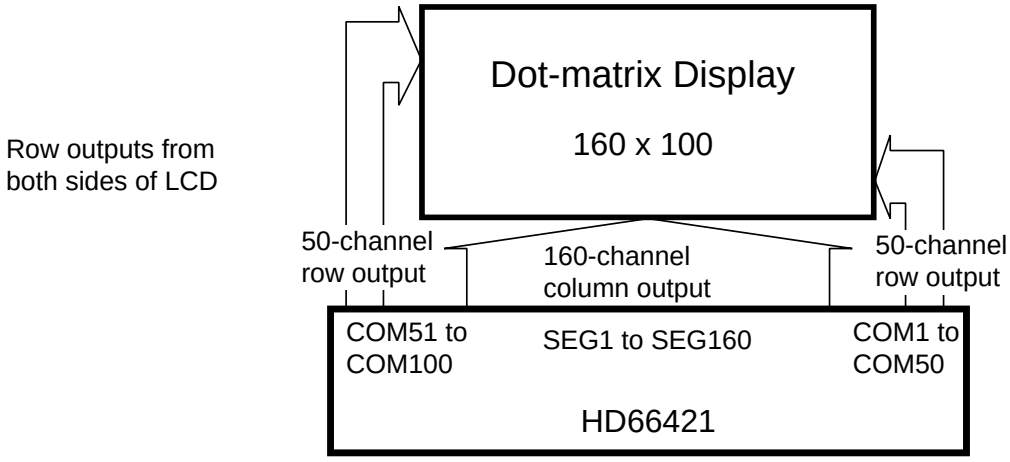


Figure 4 Common outputs from both sides

Column Address Inversion According to LCD Driver Layout: The HD66421 can always display data in address H'0 on the top left of an LCD panel regardless of where it is positioned with respect to the panel. This is because the HD66421 can invert the positional relationship between display RAM addresses and LCD driver output pins by inverting RAM addresses. Specifically, the HD66421 outputs data in address H'0 from SEG1 when the ADC bit in control register 1 is 0, and from SEG160 otherwise. Here. the scan direction of row output is also inverted according to the situation. as shown in figure 6. Note that addresses and scan direction are inverted when data is written to the display RAM, and thus changing the ADC bit after data has been written has no effect. Therefore. hardware control bits such as ADC must be set immediately after reset is canceled, and must not be set while data is being displayed.

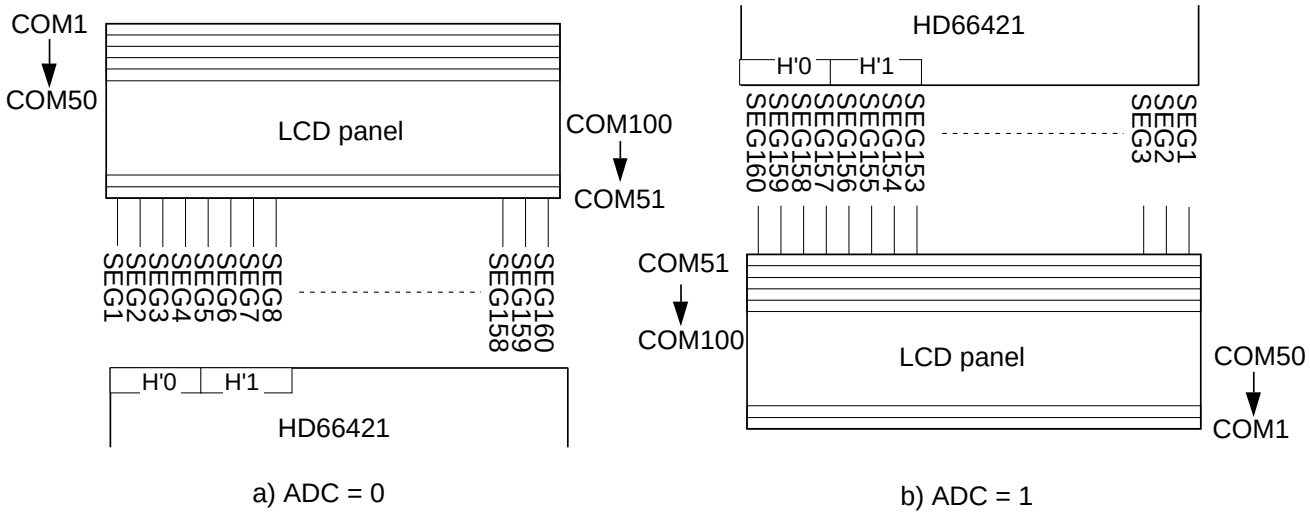


Figure 5 LCD Driver Layout and RAM addresses : 1/100 Duty cycle

Table 1 Scanning Direction and RAM Address

DTY1	DTY0	ADC	COMMON	SEGMENT
0	0	0	COM1 –> COM50, COM100 –> COM51	H'00 –> SEG1
		1	COM51 –> COM100, COM50 –> COM1	H'00 –> SEG160
0	1	0	COM1 –> COM40, COM100 –> COM61	H'00 –> SEG1
		1	COM61 –> COM100, COM40 –> COM1	H'00 –> SEG160
1	0	0	COM1 –> COM32, COM100 –> COM69	H'00 –> SEG1
		1	COM69–> COM100, COM32 –> COM1	H'00 –> SEG160
1	1	0	8 COM depend on R11	H'00 –> SEG1
		1	8 COM depend on R11	H'00 –> SEG160

Multi-LSI Operation

Using multiple HD66421s provides the means for extending the number of display dots. Note the following items when using the multi-LSI operation.

(1) The master LSI and the slave LSI must be determined; the M/S pin of the master LSI must be set high and the M/S pin of the slave LSI must be set low.
2) The master LSI supplies the FLM, M, CL1 and clock signals to the slave LSI via the corresponding pins, which synchronizes the slave LSI with the master LSI.
(3) All control bits of slave LSI must be set with the same data with that of the master LSI.
(4) All LSIs must be set to LCD off in order to turn off the display.
(5) The standby function of slave LSI must be started up first, and that of the master LSI must be terminated first.
(6) The power supply circuit of slave LSI stop working, so V1 to V5 levels are supplied from the master LSI. If the internal power supply circuit can not drive two LSIs, use an external power supply circuit.

Figure 6 shows the configuration using two HD66421s and table 2 lists the differences between master and slave modes.

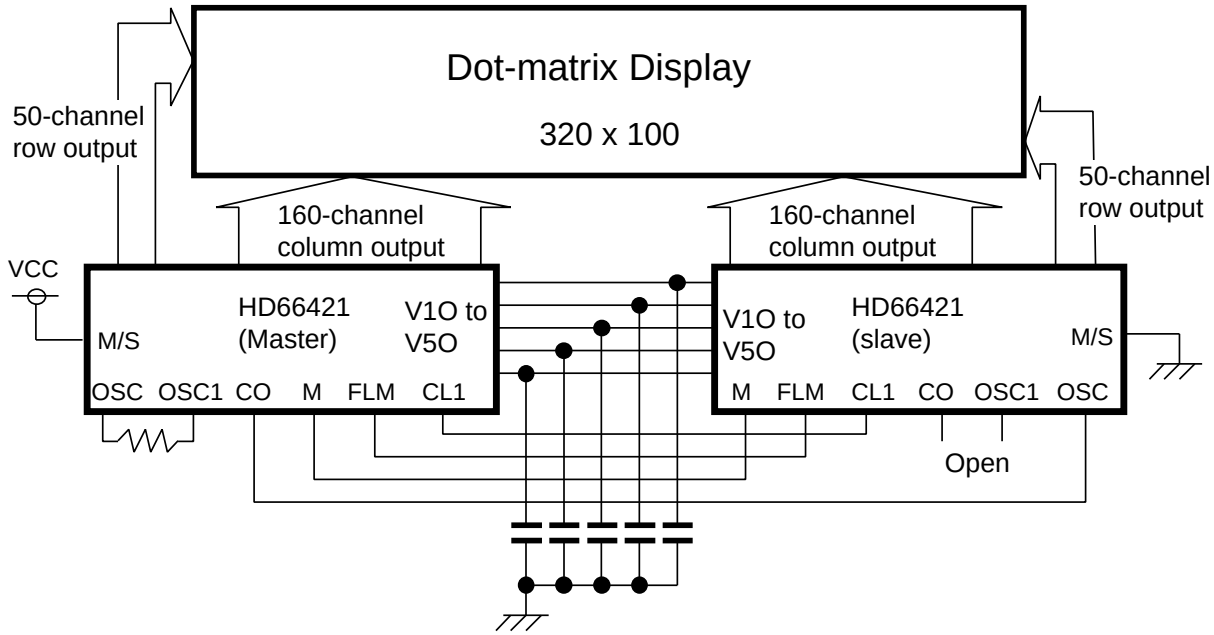


Figure 6 Configuration Using Two HD66421s

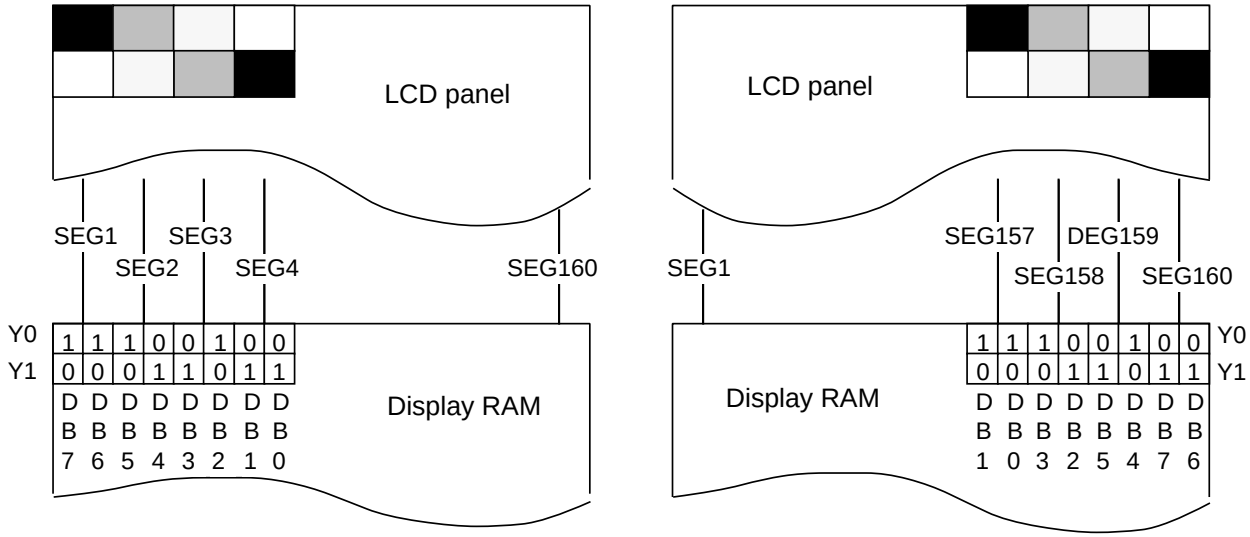
Table 2 Comparison between Master and Slave Modes

Item		Master Mode	Slave Mode
Pin	M/S	Must be set high	Must be set low
	OSC	Oscillation is active	Oscillation is active
	CO	Output	High-Z
	FLM, M, CL1	Output signals	Input signals
Registers	R0, R2 to R15,R17	Valid	Valid
	R1:BIS1, 0	Valid	Invalid
	R1:other	Valid	Valid
	R16	Valid	Invalid
Power supply circuit		Valid	Invalid

Display RAM Configuration and Display

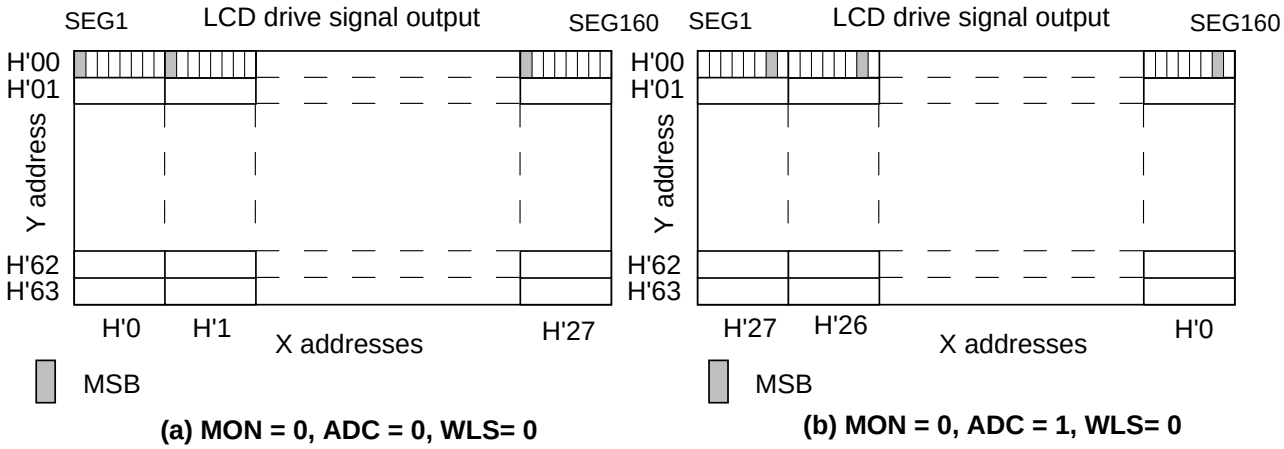
The HD66421 incorporates a bit-mapped display RAM. It has 320 bits in the X direction and 100 bits in the Y direction. The 320 bits are divided into forty 8-bit groups. As shown in figure 7, data written by the MPU is stored horizontally with the MSB at the far left and the LSB at the far right. The consecutive two bits control one pixel of LCD in 4-level gray scale mode, this means that one 8-bits data contains data which controls four pixels. One bit of memory designates one dot of display in the monochrome display mode.

The ADC bit of control register 1 can control the positional relationship between X addresses of the RAM and LCD driver output (figure 8). Specifically. the data in address H'0 is output from SEG1 when the ADC bit in control register 1 is 0, and from SEG160 otherwise. Here. data in each 8-bit group is also inverted. Because of this function, the data in X address H'0 can be always displayed on the top left of an LCD panel with the MSB at the far left regardless of the LSI is positioned with respect to the panel. In this case, DB7, DB5, DB3 and DB1 are more significant bit in consecutive two bits.



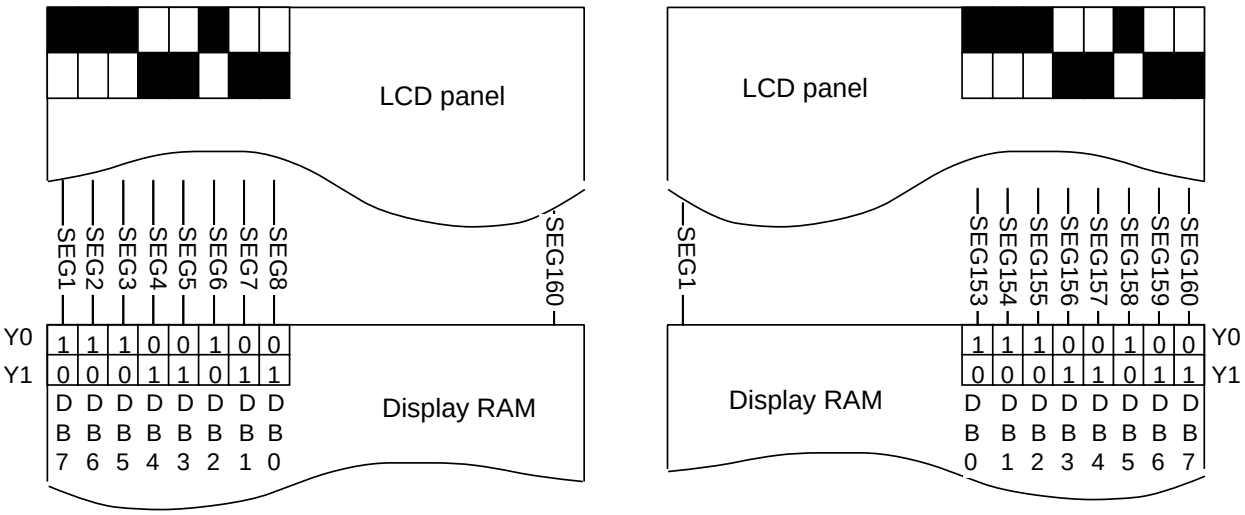
(a) MON = 0, ADC = 0, WLS= 0 **(b) MON = 0, ADC = 1 , WLS= 0**

Figure 7 Display RAM Data and Display in Gray Scale Mode



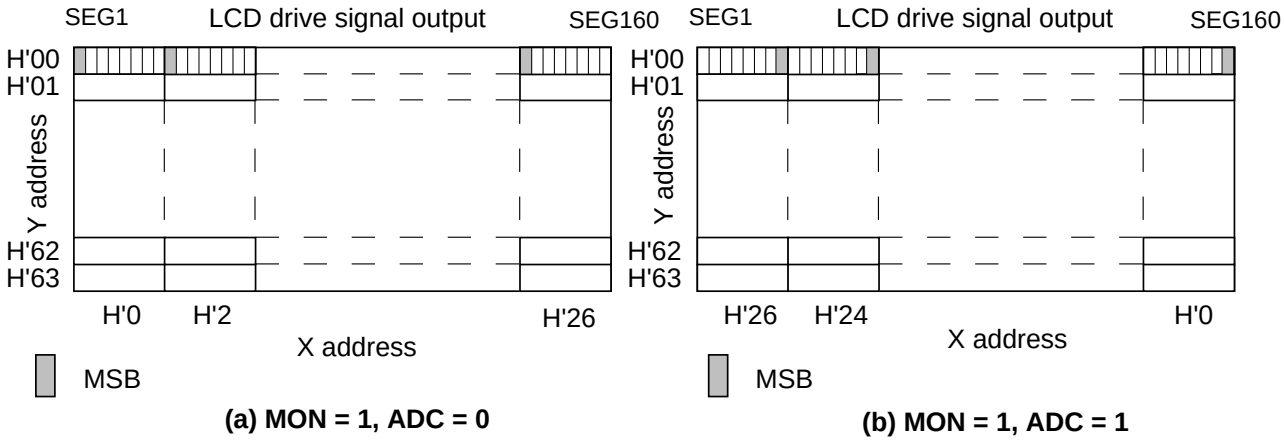
(a) MON = 0, ADC = 0, WLS= 0 **(b) MON = 0, ADC = 1, WLS= 0**

Figure 8 Display RAM Configuration in Gray Scale Mode



(a) MON = 1, ADC = 0, WLS= 0 **(b) MON = 1, ADC = 1, WLS= 0**

Figure 9 Display RAM Data and Display in Monochrome Mode



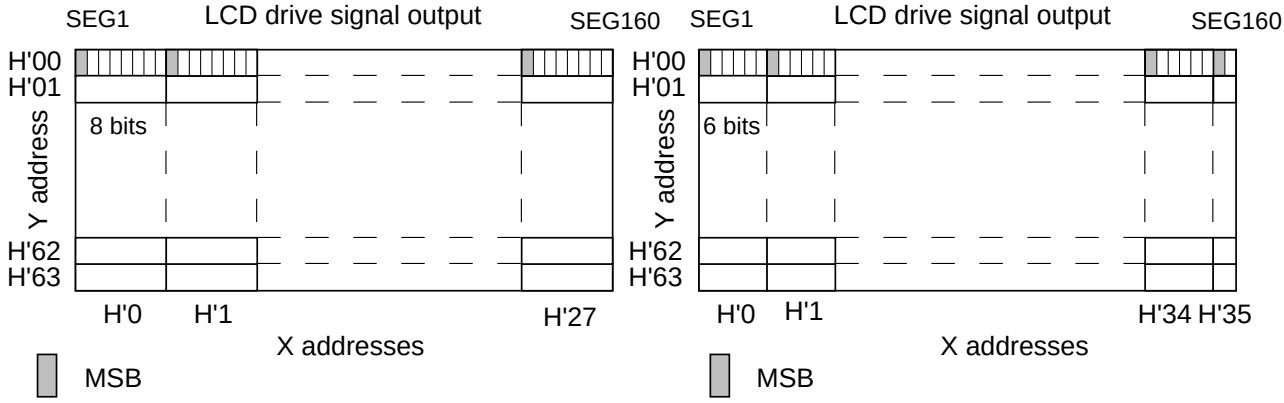
(a) MON = 1, ADC = 0 **(b) MON = 1, ADC = 1**

Figure 10 Display RAM Configuration in Monochrome Mode

Word Length

The HD66421 can handle either 8- or 6-bits as a word. In the display memory, one X address is assigned to each word of 8- or 6-bits long in X direction.

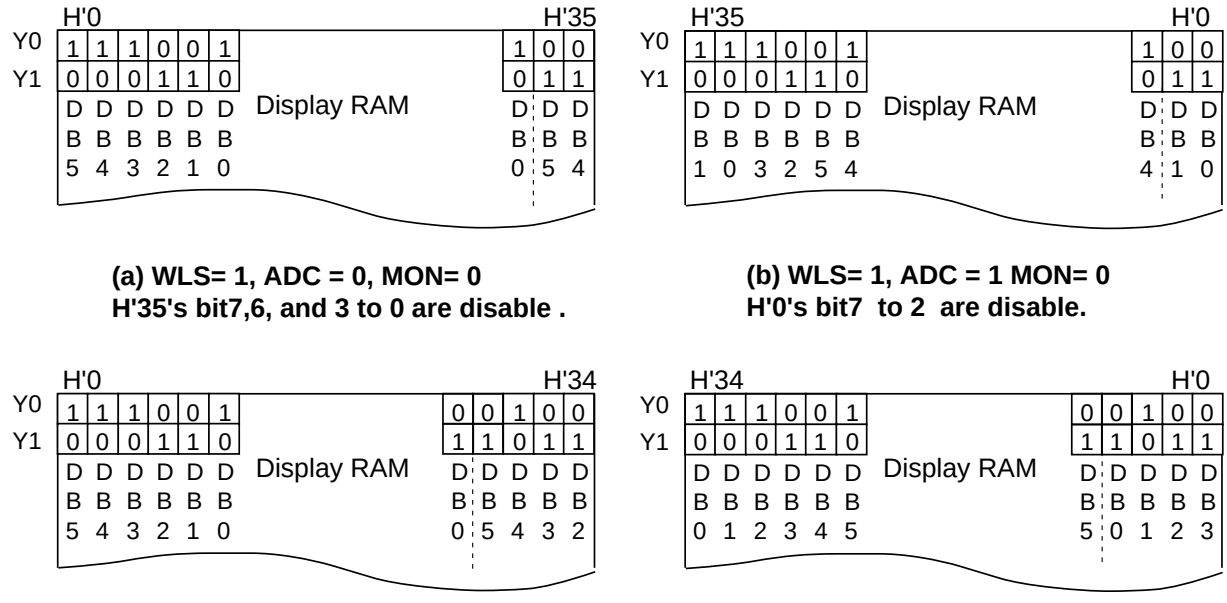
When the 6-bits mode is selected, only data on DB5 to DB0 are used and data on DB7 and DB6 are discarded. This word length is only applied to data to internal RAM. The word length of internal register is always 8-bits



(a) Address assignment when one word is 8 bits long (MON=0)

(b) Address assignment when one word is 6 bits long (MON=0)

Figure 11 Display RAM Addresses in Gray Scale Mode



(a) WLS= 1, ADC = 0, MON= 0
H'35's bit7,6, and 3 to 0 are disable .

(b) WLS= 1, ADC = 1 MON= 0
H'0's bit7 to 2 are disable.

(c) WLS= 1, ADC = 0, MON= 1
H'34's bit7,6, and 1,0 are disable .

(d) WLS= 1, ADC = 1, MON= 1
H'0's bit7 to 4 are disable.

Figure 12 Display RAM Bits Map at 6-bits Mode

Monochrome Display Mode

The HD66421 can control monochrome display. This mode is set when MON is set to 1. Two plane of display can be selected in this mode using two bits data for gray scale. One plane can be selected with PSEL bit for access from the CPU and with DSEL bit for display. Theses two operations are independent to each other, thus oneplane can be rewritten while the other plane is displayed. This means no flicker during being rewritten. The address area is mapped to even address from H'0 to H'26 in monochrome mode and this address area is the same for both planes. The plane 0 is accessed when PSEL is cleared to 0 and the plane 1 is selected when PSEL is set to 1. The plane 0 is displayed when DSEL is cleared to 0 and the plane 1 is displayed when DSEL is set to 1.

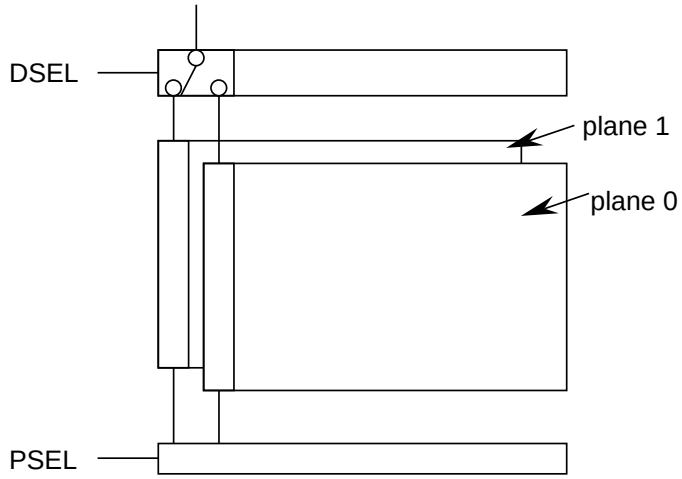


Figure 13 Memory Planes in Monochrome Display Mode

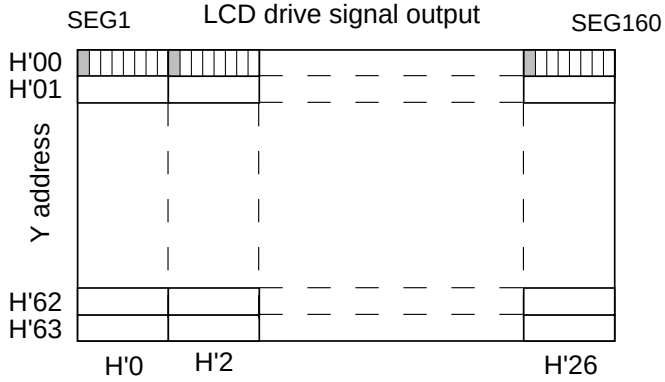


Figure 14 Memory Addresses in Monochrome Display Mode

Configuration of Display Data Bit

Packed Pixel Method

For grey scale display and super reflective colour display, multiple bits are needed for one pixel. In the HD66421, two bits are assigned to one pixel, enabling a four-level grey scale display and four colour display.
One address, eight bits, specifies four pixels, and pixel bits 0 and 1 for gray scale are managed as consecutive bits in one byte.

When grey scale display data is manipulated in bit units, one memory access is sufficient, which enables smooth high-speed data rewriting.

The bit data to input to pin DB7, DB5, DB3 and DB1 become MSB and the bit data to input via pin DB6, DB4, DB2 and DB0 are LSB.

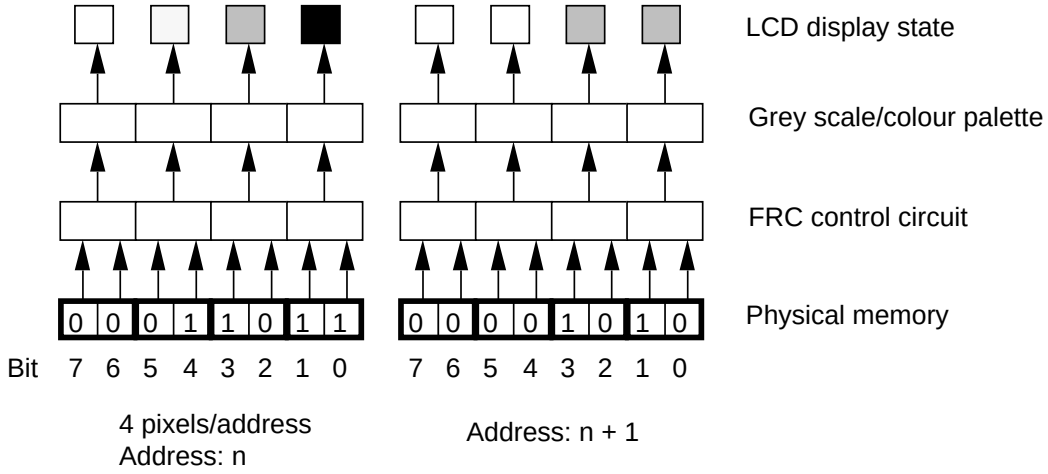


Figure 15 Packed Pixel Method

Gray scale/Colour palette

The HD66421 uses PWM, Pulse Width Modulation, technique for gray scale display. A period of one line is divided into thirty-one or four and HD66421 outputs turn-on levels for one period and turn-off levels for rest of these period. This technique changes gray scale on monochrome display and colour on super reflective colour panel. The characteristics of these panel vary with different panel. To allow for this, the HD66421 designed to generate 32-levels gray scale levels and provides palette registers that assign desired levels to certain of the four colours, GRAY = 0, or generate dedicated 4-level grayscale , GRAY = 1. Using the palette registers to select any 4 out of 32 levels of applied voltages enables an optimal grayscale/colour display. Because of this grayscale technique using 32-levels gray scale needs higher clock rate. If 32-levels gray scale is not needed, lower clock rate can be used. Table 3 shows default value of palette registers and Table 4 and 5 show relationship between value of a palette register and grayscale level.

Table 3 Default Value of Palette Registers

DB7, 5, 3, 1	DB6, 4, 2, 0	Register Name	Default Value
0	0	Grayscale Palette 1	0 0 0 0 0
0	1	Grayscale Palette 2	0 1 0 1 1
1	0	Grayscale Palette 3	1 0 1 1 1
1	1	Grayscale Palette 4	1 1 1 1 1

Table 4 Value of a Palette Register and Grayscale Levels (GRAY= 0)

Value					Grayscale Level	
0	0	0	0	0	0	default R12
0	0	0	0	1	1/31	
0	0	0	1	0	2/31	
0	0	0	1	1	3/31	
0	0	1	0	0	4/31	
0	0	1	0	1	5/31	
0	0	1	1	0	6/31	
0	0	1	1	1	7/31	
0	1	0	0	0	8/31	
0	1	0	0	1	9/31	
0	1	0	1	0	10/31	
0	1	0	1	1	11/31	default R13
0	1	1	0	0	12/31	
0	1	1	0	1	13/31	
0	1	1	1	0	14/31	
0	1	1	1	1	15/31	
1	0	0	0	0	16/31	
1	0	0	0	1	17/31	
1	0	0	1	0	18/31	
1	0	0	1	1	19/31	
1	0	1	0	0	20/31	
1	0	1	0	1	21/31	
1	0	1	1	0	22/31	
1	0	1	1	1	23/31	default R14
1	1	0	0	0	24/31	
1	1	0	0	1	25/31	
1	1	0	1	0	26/31	
1	1	0	1	1	27/31	
1	1	1	0	0	28/31	
1	1	1	0	1	29/31	
1	1	1	1	0	30/31	
1	1	1	1	1	1	default R15

Table 5 Grayscale Levels (GRAY= 1)

DB7,5,3,1	DB6,4,2,0	Grayscale Level
0	0	0
0	1	1/3
1	0	2/3
1	1	1

Access to Internal Registers and Display RAM

Access to Internal Registers by the MPU: The internal registers includes the index register and data registers. The index register can be accessed by driving both the CS and RS signals low. To access a data register, first write its register number ID to the index register with RS set to 0, and then access the data register with RS set to 1 . Once written, the register number is held until it is rewritten, enabling the same register to be consecutively accessed without having to rewrite to the register number for each access. Some data registers contain unused bits; they should be set to 0. Note that all data registers except the display memory access register can only be written to.

Access to Display RAM by the MPU: To access the display RAM, first write the RAM address desired to the X address register (R2) and the Y address register (R3). Then read/write the display memory access register (R4). Memory access by the MPU is independent of memory read by the HD66421 and is also asynchronous with the HD66421's clock, thus enabling an interface independent of HD66421's internal operations. However, when reading. data is temporarily latched into a H66421's buffer and then output next time, a read is performed in a subsequent cycle. This means that a dummy read is necessary after setting X and Y addresses. The memory read sequence is shown in figure 16.

X and Y addresses are automatically incremented after each memory access according to the INC bit value in control register 2; therefore, it is not necessary to update the addresses for each access. Figure 16 shows two cases of incrementing display RAM address. When the INC bit is 0, the Y address will be incremented up to H'7F with the X address unchanged. However, actual memory is valid only within H'00 to H'4F; accessing an invalid address is ignored. When the INC bit is 1 , the X address will be incremented up to H'27 or H'35 according to WLS bit with the Y address unchanged. After address H'27 or H'35, the X address will be returned to H'00; accessing more than forty bytes causes rewriting to the same address.

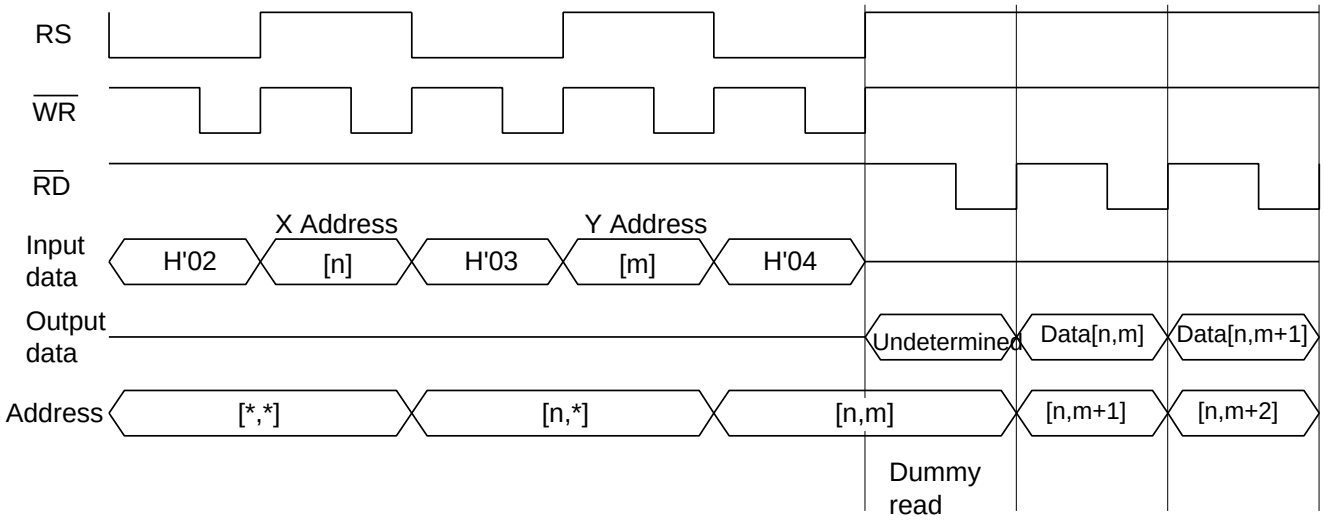
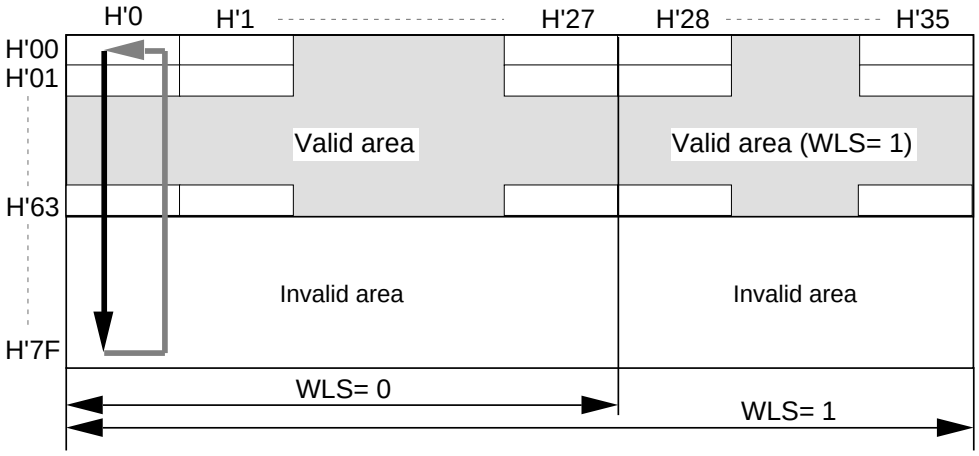


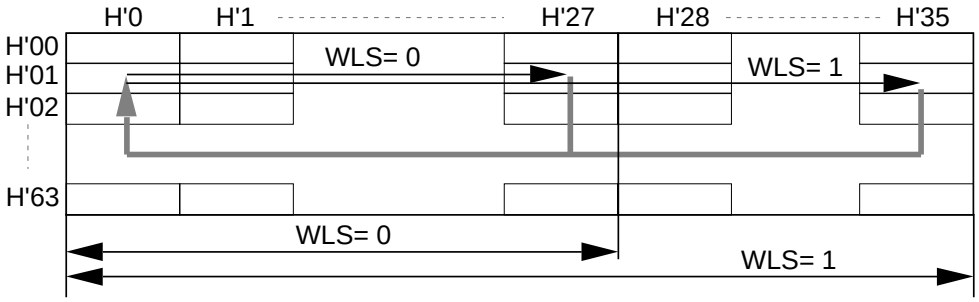
Figure 16 Display RAM read sequence

Display RAM Reading by LCD Controller:

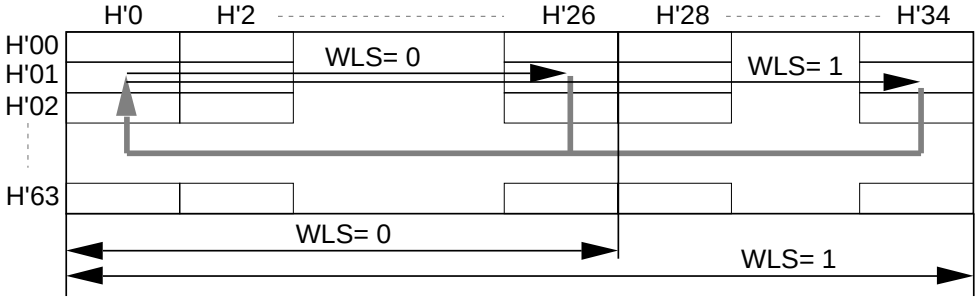
Data is read by the HD66421 to be displayed asynchronously with accesses by the MPU. However, because simultaneous access could damaging data in the display RAM, the HD66421 internally arbitrates access timing; access by the MPU usually has priority and so access by the HD66421 is placed between accesses by the MPU. Accordingly, an appropriate time must be secured (see the given electrical characteristics between two accesses by the MPU).



(a) INC = 0



(b) INC = 1, MON= 0



(c) INC = 1, MON= 1

Figure 17 Display Address Increment

Read-Modify-Write: X- or Y-address is incremented after reading form or writing data to the display RAM at normal mode. However, X- or Y-address is not incremented after reading data from the display RAM at read-modify-write mode. The data which is read from the display RAM may be modified and written to the same address without re-setting the address. Data is temporarily latched into a HD66421's buffer and then output next time a read is performed in a subsequent cycle. This means that the dummy read is necessary after every cycle. This sequence is shown in figure 18.

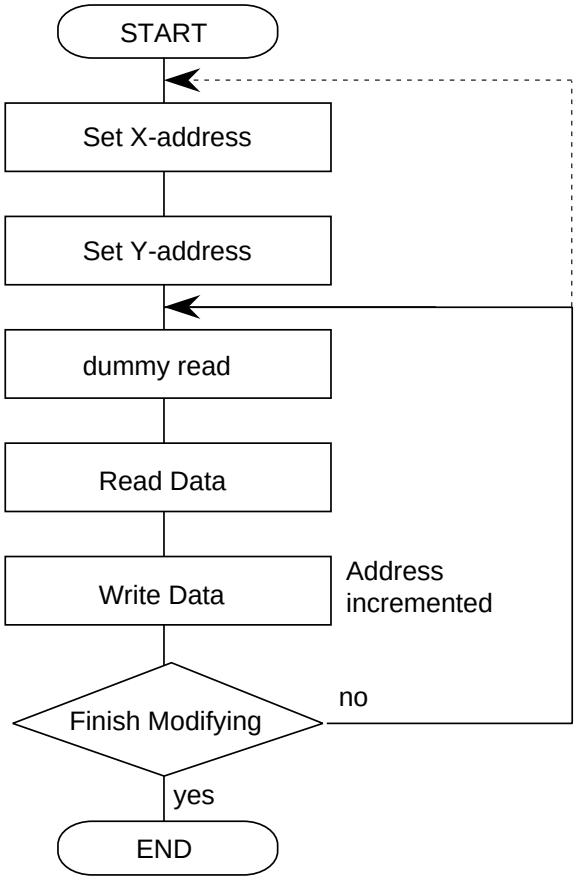


Figure 18 The Flow Chart for Read-Modify-Write

Arbitration Control

The HD66421 controls the arbitration between draw access and display access. The draw access read and write display data of display memory incorporated in the HD66421. The display access outputs display data to the liquid crystal panel. The draw access has the priority over display access, so continuous access is enabled without having the system to wait. For arbitration control, draw access is recognized as valid when $\overline{CS}$ and $\overline{WR}$/$\overline{RD}$ are low.

When draw and display access occur at the same time, draw access is executed prior to display access. Display access is executed between two draw access during display access period. If a period of one draw access is longer than that of display access, display access will not be executed properly. If this condition happens frequently, flicker will be seen on the display. The low level width of $\overline{WR}$ and $\overline{RD}$ must be less than the period of display access - 450ns.

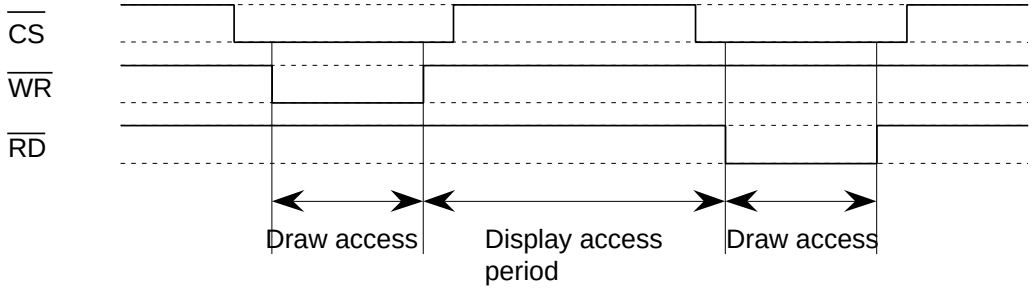


Figure 19 Definition of Draw Access

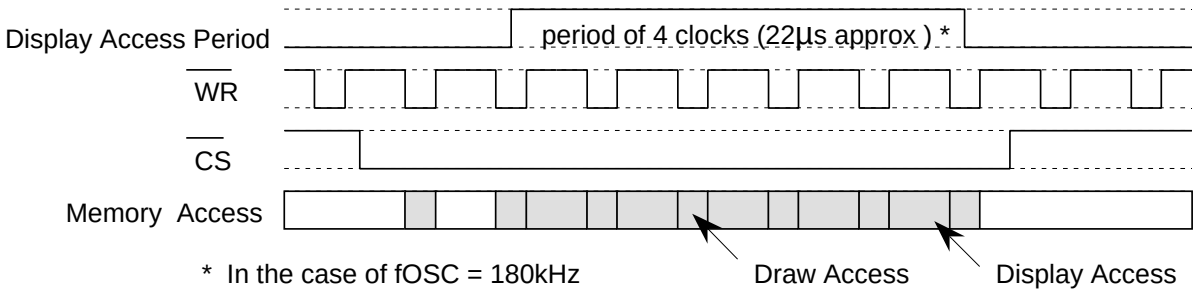


Figure 20 Memory Access when Display and Draw Access Occur at The Same Time

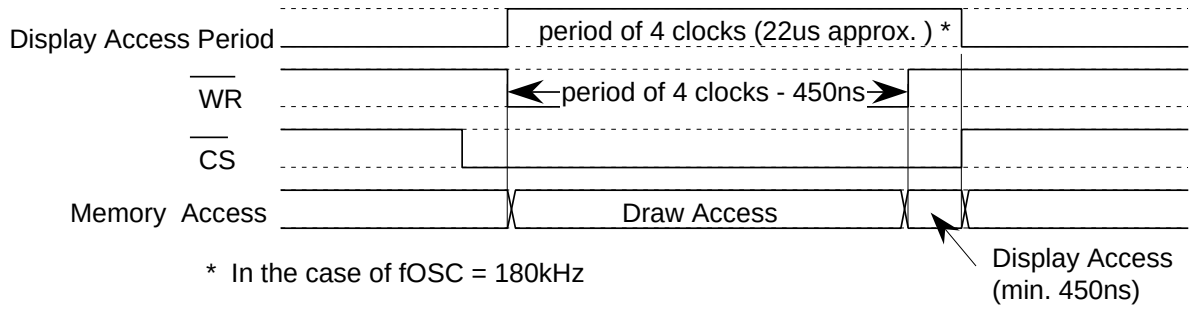


Figure 21 $\overline{WR}$ Low Level Width

Vertical Scroll Function

The HD66421 can vertically scroll a display by varying the top raster to be displayed. which is specified by the display start raster register. Figure 22 and 23 show vertical scroll examples. As shown, when the top raster to be displayed is set to l, data in Y address H'0 is displayed on the 100th raster. To display another frame on the 100th raster, therefore, data in Y address H'0 must be modified after setting the top raster. When display duty is less than 100, for example 1/80, data of address H'50 is displayed after address H'4F.

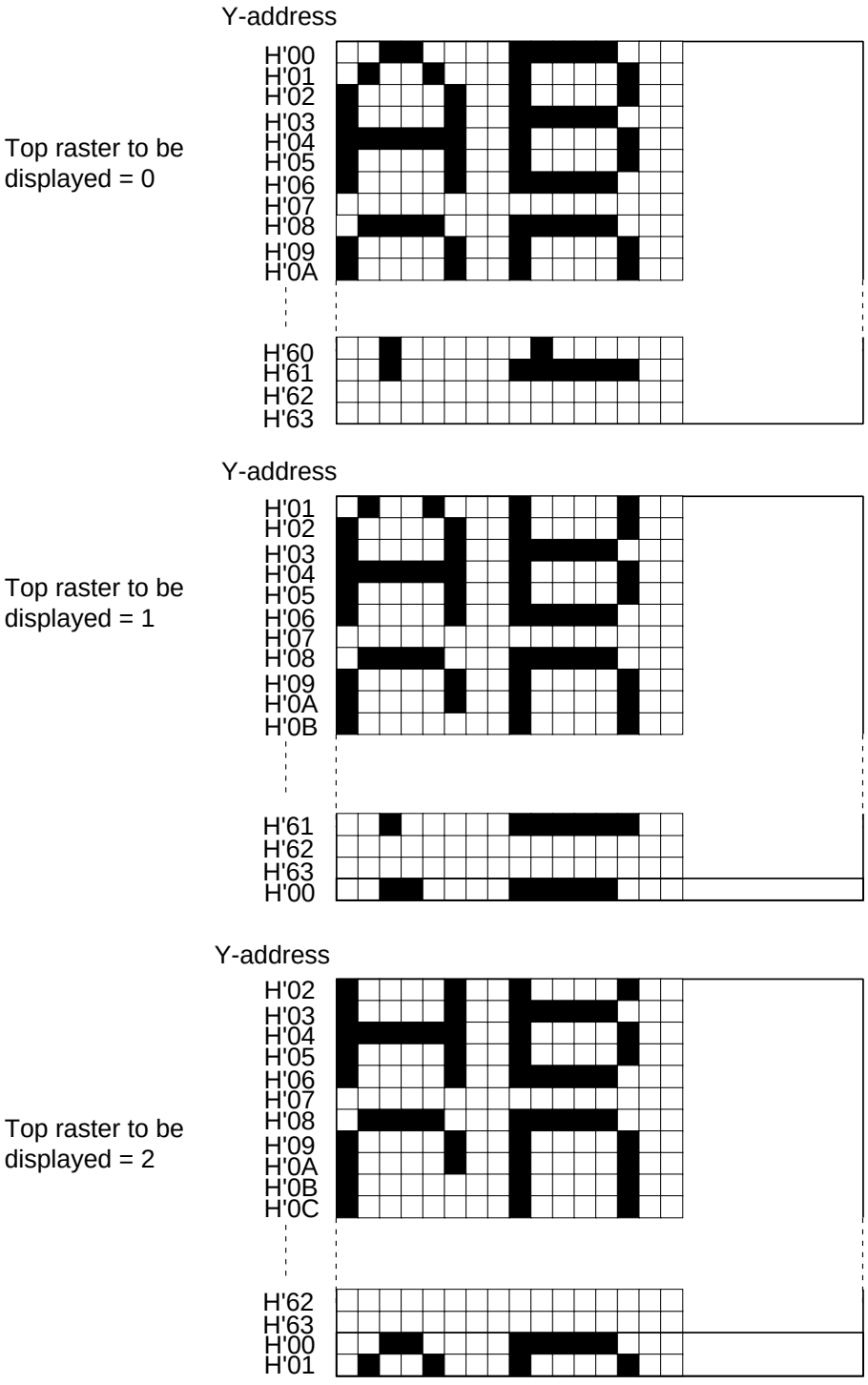


Figure 22 Vertical Scroll : 1/100Duty Cycle

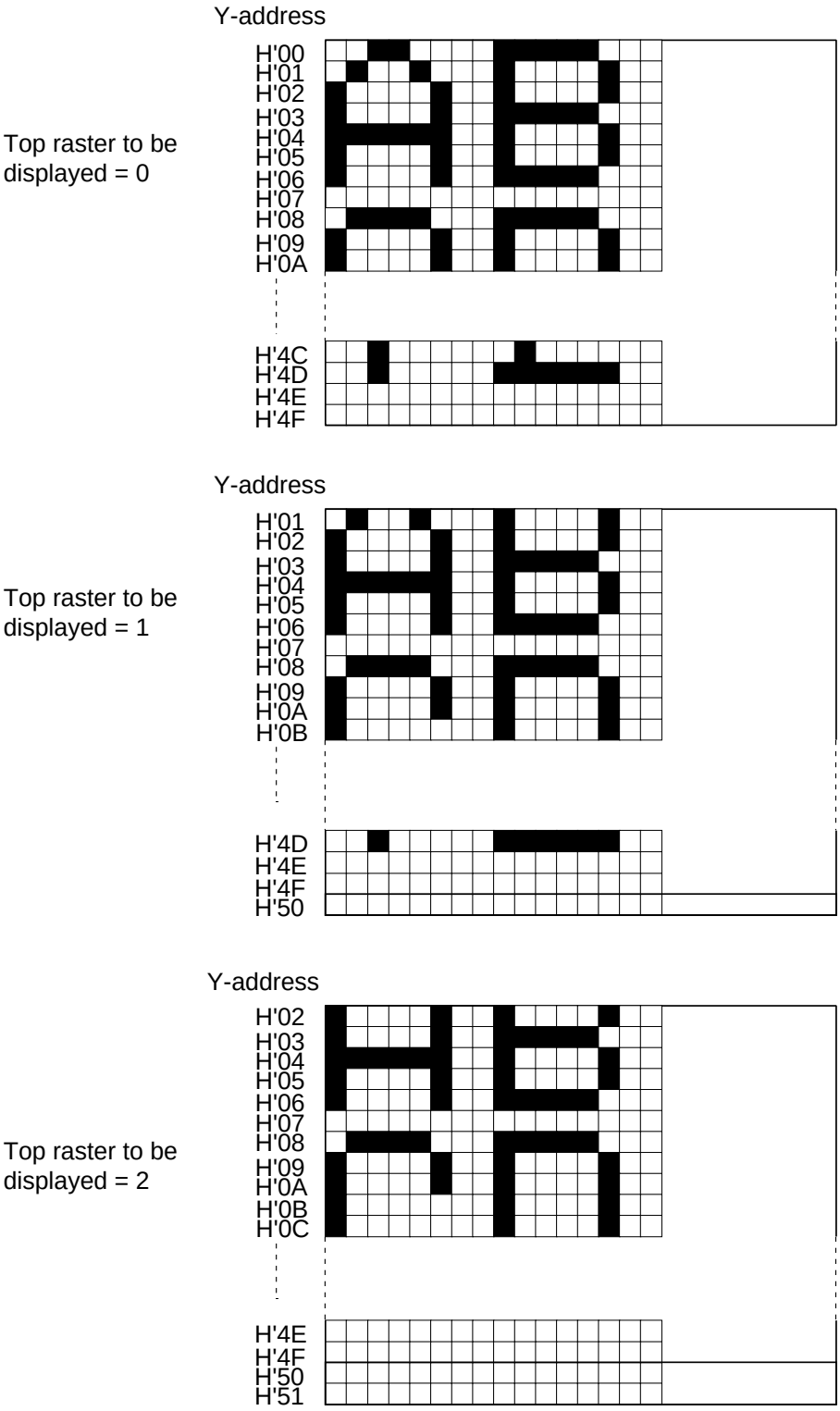


Figure 23 Vertical Scroll : 1/80Duty Cycle

Partial Display Function

The HD66421 can display only a part of a full display. The duty ratio of this partial display is 1/8 and rest of display is scanned with unselected levels. The position of this partial display can be located at any position with using partial display position register. To launch this mode, following processes are needed:
(1) supplied voltage to VLCD must be cut off, PWR bit can be used if external voltage supplier is controlled with DCON output (R0)
(2) set DTY bits (R1)
(3) set display position (R11)
(4) set contrast level (R16)

The clock frequency may be 220kHz at normal display mode. When a partial display is driven, oscillation frequency will be 18kHz, 1/12.5 of that of normal display mode. This function is useful for lower power dissipation. To change clock frequency, follow the process which is showed in Figure 28.

Warning:
VLCD must be cut off when partial display mode is launched. Vcc is supplied to LCD driving circuit instead of VLCD. So if VLCD is supplied externally during partial display mode, Vcc short-circuit to VLCD.

Table 6 Partial Display Block

R11	ADC= 0	ADC= 1
H'00	COM1 –> COM8	COM8 –> COM1
H'01	COM9 –> COM16	COM16 –> COM9
H'02	COM17 –> COM24	COM24 –> COM17
H'03	COM25 –> COM32	COM32 –> COM25
H'04	COM33 –> COM40	COM40 –> COM33
H'05	COM41 –> COM48	COM48 –> COM41
H'06	COM100–> COM93	COM93 –> COM100
H'07	COM92 –> COM85	COM85 –> COM92
H'08	COM84 –> COM77	COM77 –> COM84
H'09	COM76 –> COM69	COM69 –> COM76
H'0A	COM68 –> COM61	COM61 –> COM68
H'0B	COM60 –> COM53	COM53 –> COM60

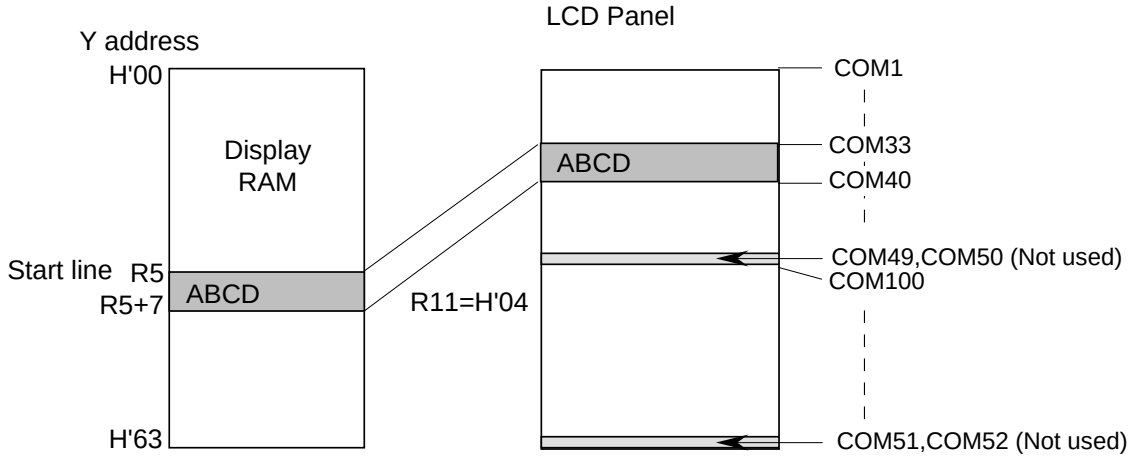


Figure 24 Partial Display

Blink Function

The HD66421 can blink a specified area on the dot-matrix display. Blinking is achieved by repeatedly turning on and off the specified area at a frequency of one sixty-fourth the frame frequency. For example, when the frame frequency is 80 Hz. the area is turned on and off every 0.8 seconds.

The area to be blinked can be designated by specifying vertical and horizontal positions of the area. The vertical position. or the rasters to be blinked, are specified by the blink start raster register (R6) and blink end raster register (R7).

The horizontal position, or the dots to be blinked in the specified rasters, are specified by the blink registers R8, R9 and R10 in an 8-dot group; each data bit in the blink registers controls its corresponding 8-dots group. The relationship between the registers and blink area is shown in figure 25. Setting the BLK bit to 1 in control register 2 after setting the above registers starts blinking the designated area. Note that since the area to be blinked is designated absolutely with respect to the display RAM, it will move along with a scrolling display (figure 26).

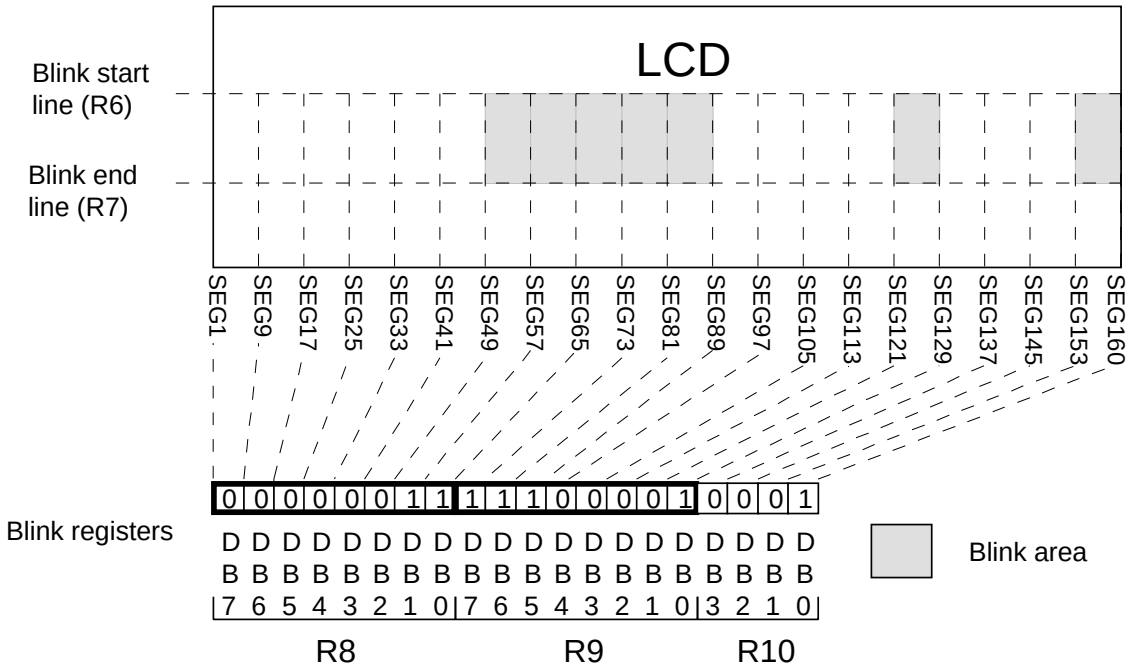


Figure 25 Blink Area Designation by Blink Control Registers

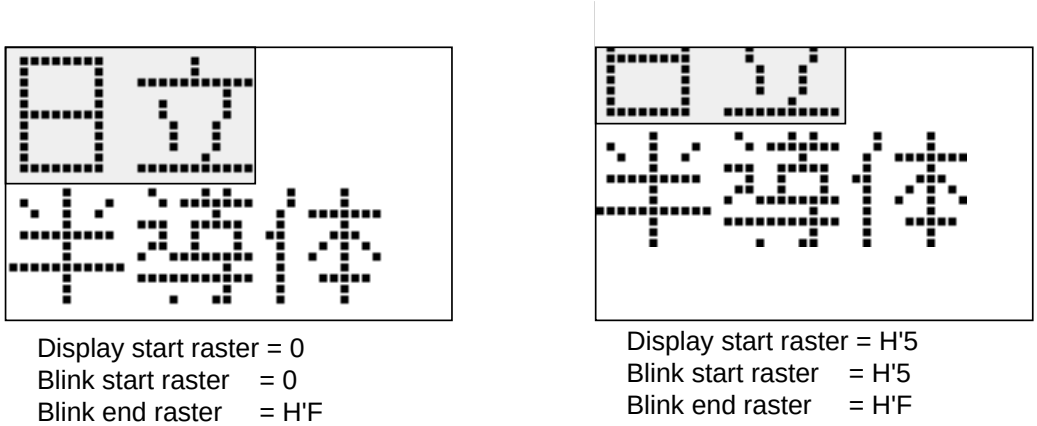


Figure 26 Scrolling Blink Area

Power Down Modes

The HD66421 has a standby function providing low power-dissipation, which is initiated by internal register settings. During standby mode, all the HD66421 functions are inactive and data in the display RAM and internal registers except the DISP bit are retained. However, only control registers can be accessed during standby mode. HD66421 has an another power down mode: partial display. In this mode only a part of display is active. However, this duty ratio is 1/8 so the external power supply for LCD drive will be inactive. The oscillator does not halt, thus dissipating more power than standby mode. Table 6 lists the LCD driver output pin status during standby mode. Figure 27 shows the procedure for initiating and canceling a standby mode and figure 28 shows the procedure for changing oscillator. Note that these procedure must be strictly followed to protect data in the display RAM.

Table 7 Output Pin Status during Power Down modes

Signal Name	STBY	Status
COM1-COM100	1	Output VLCD (display off)
	0	Output common signals (VLCD - GND)
SEG1-SEG160	1	Output VLCD (display off)
	0	Output segment signals (VLCD - GND)

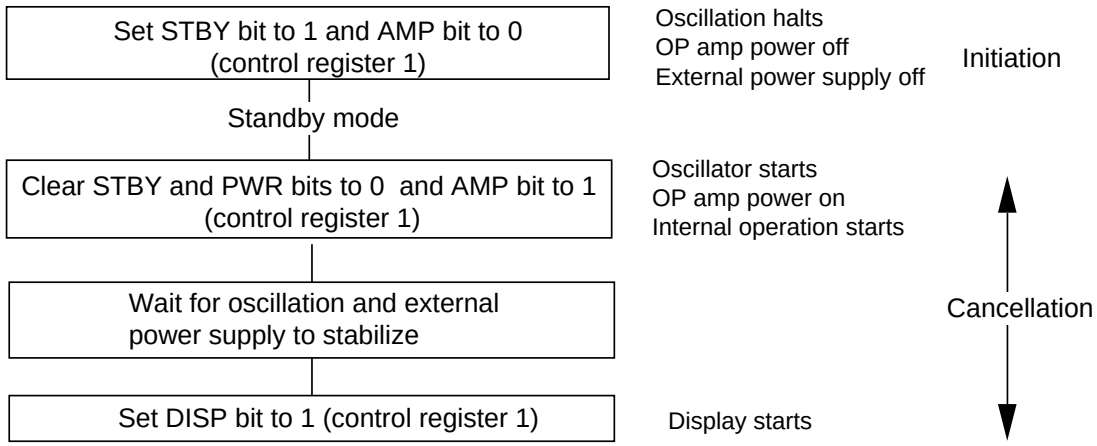


Figure 27 Procedure for Initiation and Canceling a Standby Mode

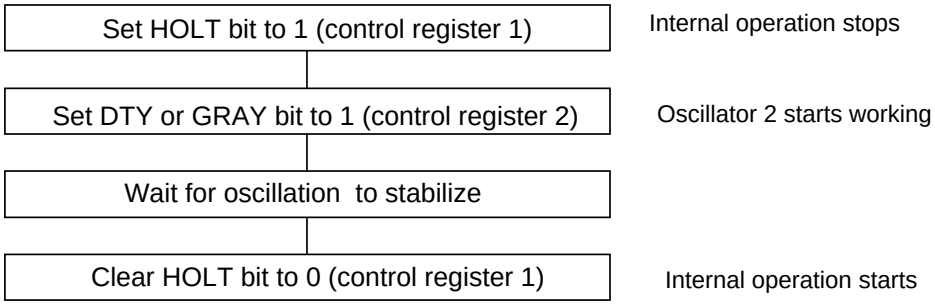


Figure 28 Procedure for Changing Oscillator

Power On/Off Procedure

Figure 29 shows the procedure for turning the power supply on and off. This procedure must be strictly followed to prevent incorrect display because the HD66421 incorporates a power supply circuit.

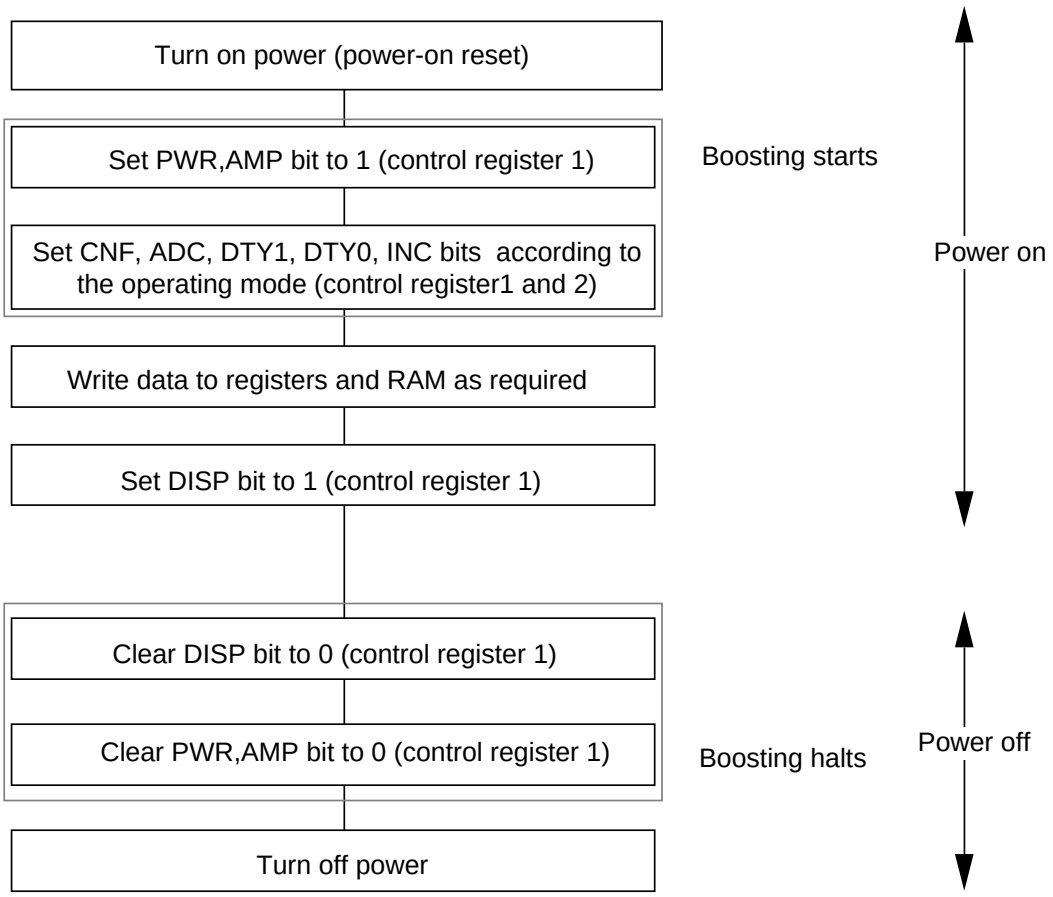


Figure 29 Procedure for Turning Power Supply On/Off

Oscillator

The HD66421 incorporates two sets of R-C oscillator for two display modes: OSC-OSC1 oscillator is used for 32-levels gray scale display mode and OSC-OSC2 oscillator for 4-levels gray scale display mode. If the internal oscillator is not used, an appropriate clock signal must be externally input through the OSC pin. In this case, the OSC1 and OSC2 pins must be left unconnected. Oscillation resister must be placed near LSI, because if capacitance exists between OSC and OSC1 oscillator may not work properly. Figure 30 shows oscillator connections.

Changing Oscillator

Two oscillators are alternated automatically depending on modes. An external clock must be input from OSC terminal at any modes.

Clock and Frame Frequency

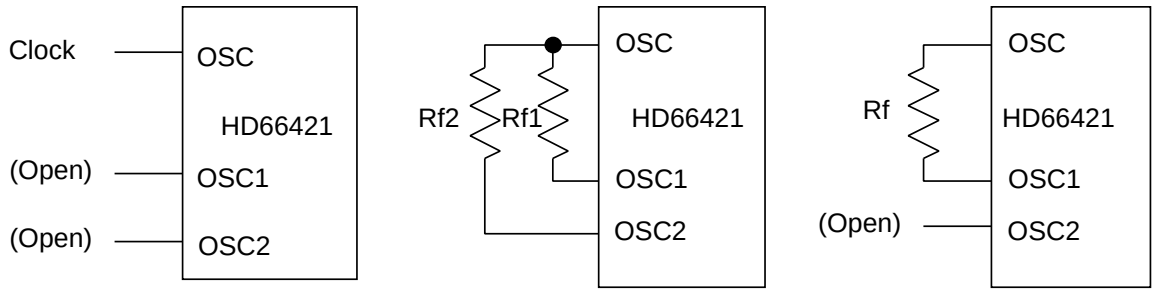
The HD66421 generates the frame frequency by dividing the input clock. Clock frequency is determined with following equation:

fOSC = N * (Duty ratio) * (Frame frequency)
N: 31 for 32-level gray scale display mode
3 for 4-level gray scale display mode

The frame frequency is usually 70 to 90 Hz; when the frame frequency is 70 Hz, for example, the input clock frequency will be 220 kHz for 32-level gray scale display mode, and 18kHz for 4-level gray scale.

LCD Driving Alternating Cycle

AC voltage needs to be applied to liquid crystals to prevent deterioration due to DC voltage. This alternated cycle is determied by setting Alernating cycle register (R16); 7, 11, 13lines or flame.



a) External clock b) Dual oscillator c)Single oscillator

Figure 30 Oscillator Connections

Table 8 LCD alternative drive cycle

CM1	CM0	Alternative Cycle
0	0	Frame
0	0	7 lines
0	0	11 lines
0	0	13 lines

Power Supply Circuits

HD66421 has following circuits for power supply circuit: operational amplifiers, resistive dividers, bias control circuit and contrast control circuit. LCD driving voltage, VLCD, must be generated externally.

LCD Drive Voltage Power Supply Levels: To drive the LCD, a 6-level power supply are necessary. These levels are generated internally or supplied from outside. When an internal voltage levels generator is chosen, external capacitors are needed to stabilize these levels. AS the HD66421 incorporates operational amplifiers to these levels, this circuit gives better quality of display with less power consumption. This divided ratio is programmable.
Bias current of internal operational amplifier is determined with a resister which is inserted between IREFM and GND. This resister value is between 1MΩ and 5MΩ. Larger resister value make less power consumption at internal operational amplifier. However, too large value loose operational margin of amplifiers.
Keep following relationship among voltage levels;

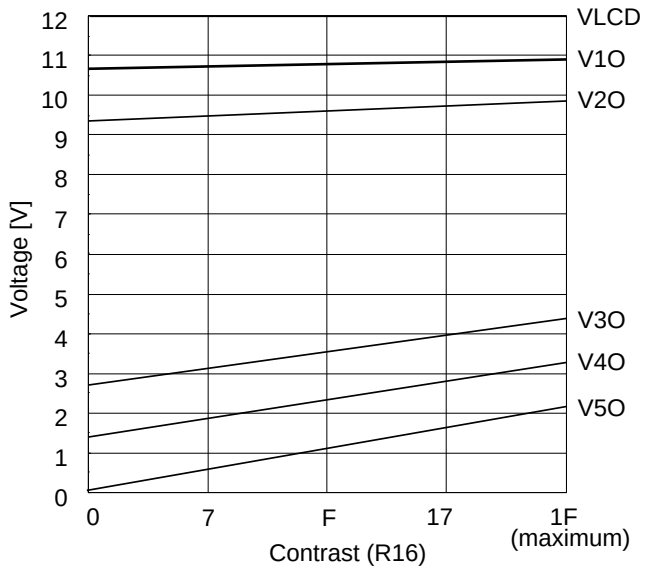
Vcc ≥ IREFMP > IREFM ≥ GND
VLCD > Vcc > GREF ≥ GND
VLCD ≥ V1O ≥ V2O ≥ V3O ≥ V4O ≥ V5O ≥ GREF≥ GND
VLCD-Vcc ≥ 1.0V
IREFP-IREFM ≥ 1.0V
Vcc-GREF ≥ 1.0V

Contrast Control: Internal contrast control circuit can change the output voltage level of VLCD by setting data to contrast control register, R16. VLCD adjustable range are showed below;

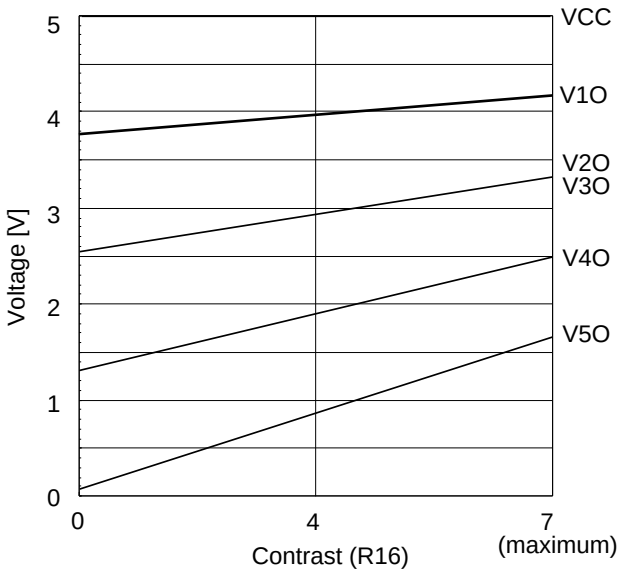
- 1/8 bias
  0.73 * (VLCD-GND) ≤ VLCD ≤ 0.988 * (VLCD-GND)
- 1/9 bias
  0.82 * (VLCD-GND) ≤ VLCD ≤ 0.993 * (VLCD-GND)
  (Example 1.)
- 1/11 bias
  0.79 * (VLCD-GND) ≤ VLCD ≤ 0.992 * (VLCD-GND)
- Partial Display
  0.82 * (Vcc-GND) ≤ VCC ≤ 0.997 * (VCC-GND)
  (Example 2.)

Partail display function uses 1/4 bias ratio from VCC to GND. 8 levels of contrast can be selected with data bit 2 to 0 of R16.

Example.1 LCD bias level
1/80 duty Display(1/9 bias, VLCD=12V,GND=0V)



Example 2. LCD bias level
Partial Display(1/4 bias,VCC=5V,GND=0V)



LCD drive levels bias ratio: LCD driving levels bias ratio can be selected from 1/8, 1/9, 1/10 or 1/11.

Power Supply: The HD66421 needs the external power supply for LCD driving circuit. If this power circuit has on/off control, the HD66421 controls the external power supply circuit by setting PWR bit.

External Power Supply Circuit: When the internal operational amplifier cannot fully drive the LCD panel used, V1O to V5O voltages can be supplied from external power supply circuit. Here, the AMP bit must be set to 1 to turn off the internal power supply circuit.

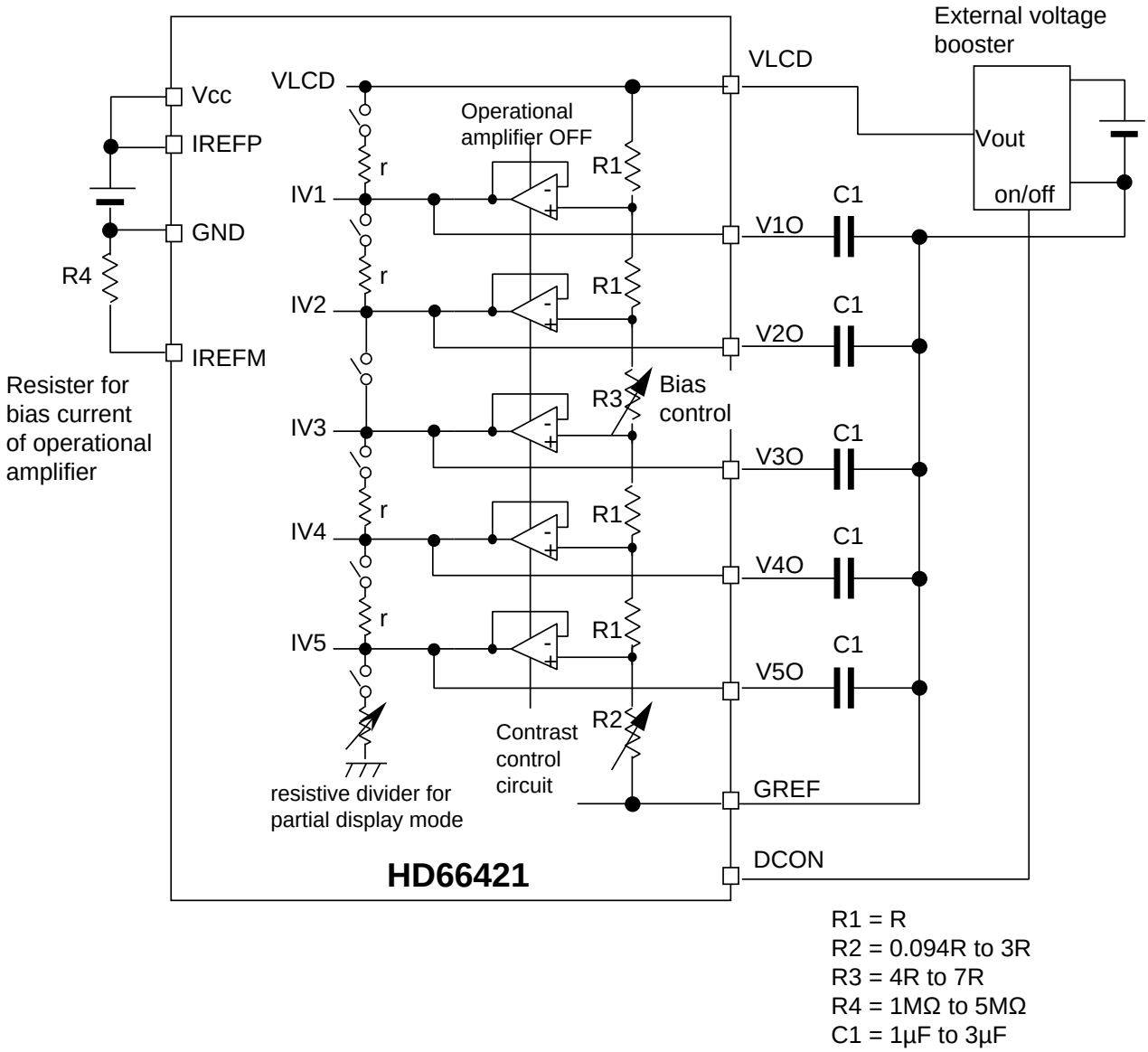


Figure 31 Power Supply Circuit

Reset

The low $\overline{RES}$ signal initializes the HD66421, clearing all the bits in the internal registers. During reset. the internal registers cannot be accessed.

Note that if the reset conditions specified in the Electric Characteristics section are not satisfied, the HD66421 will not be correctly initialized. In this case, the internal registers of the HD66421 must be initialized by software.

Initial Setting of Internal Registers: All the internal register bits are cleared to 0. Details are listed below.

- Normal operation
- Oscillator is active; OSC-OSC1 is used
- Display is off
- Y address of display RAM is incremented
- 1/100 duty cycle
- X and Y addresses are 0
- Data in address H'0 is output from the SEGl pin
- Blink function is inactive
- Operational amplifier is disabled

Initial Setting of Pins:

Bus interface pins

During reset, the bus interface pins do not accept signals to access internal registers; data is undefined when read.

LCD driver output pins

During reset. all the LCD driver output pins (SEG1 to SEGl61, COM1 to COM100) output Vcc-level voltage, regardless of data value in the display RAM, turning off the LCD. Here, the output voltage is not alternated. Note that the same voltage (VLCD) is applied to both column and row output pins to prevent liquid crystals from degrading.

Internal Registers

The HD66421 has one index register and 18 data registers, all of which can be accessed asynchronously with the internal clock. All the registers except the display memory access register are write-only. Accessing unused bits or addresses affects nothing; unused bits should be set to 0 when written to.

Index Register (IR): The index register (figure 32) selects one of 18 data registers. The index register itself is selected when both the $\overline{CS}$ and RS signals are low. Data bits 7 to 5 are unused; they should be set to 0 when written to.

Control Register 1 (R0): Control register 1 (figure 33) controls general operations of the HD66421. Each bit has its own function as described below.

RMW bit
RMW = l: Read-modify-write mode
Address is incremented only after write access
RMW = 0: Address is incremented after both write and read accesses

DISP bit
DISP = 1: Display on
DISP = 0: Display off (all LCD driver output pins output VLCD level)

STBY bit
STBY = l: Internal operation and oscillation halt; display off
STBY = 0: Normal operation

PWR bit
PWR = l: Output high level from DCON terminal
PWR = 0: Output low level from DCON terminal
This bit controls the external power supply for LCD driving outputs.

AMP bit
AMP = 1: OP amp enable
AMP = 0: OP amp disable

REV bit
REV = 1: Reverse display
REV = 0: Normal display

HOLT bit
HOLT = l : Internal operation stops
HOLT = 0: Internal operation starts

ADC bit
ADC = l: Data in X address H'0 is output from SEG160; row signals depend on duty.
ADC = 0: Data in X address H'0 is output from SEG1; row signals are scanned from COM1.

Data bit	7	6	5	4	3	2	1	0
Set value				Register number				

Figure 32 Index Register (IR)

Data bit	7	6	5	4	3	2	1	0
Set value	RMW	DISP	STBY	PWR	AMP	REV	HOLT	ADC

Figure 33 Control Register 1 (R0)

Control Register 2 (R1): Control register 2 (figure 34) controls general operations of the HD66421. Each bit has its own function as described below.

BIS1, BIS0 bits
BIS1, 0 = (1, 1): 1/8 LCD drive levels bias ratio
BIS1, 0 = (1, 0): 1/9 LCD drive levels bias ratio
BIS1, 0 = (0, 1): 1/10 LCD drive levels bias ratio
BIS1, 0 = (0, 0): 1/11 LCD drive levels bias ratio

WLS bit
WLS = l: A word length is 6-bits
WLS = 0: A word length is 8-bits

GRAY bit
GRAY = l : 4-levels of gray scale are fixed
GRAY = 0: 4-levels of gray scale are selected from 32-levels

DTY1,DTY0 bits
DTY1, 0 = (1, 1): 1/8 display duty cycle; partial display mode
DTY1, 0 = (1, 0): 1/64 display duty cycle
DTY1, 0 = (0, 1): 1/80 display duty cycle
DTY1, 0 = (0, 0): 1/100 display duty cycle

INC bit
I NC = l: X address is incremented for each access
INC = 0: Y address is incremented for each access

BLK bit
BLK = 1: Blink function is used
BLK = 0: Blink function is not used

The blink counter is reset when the BLK bit is set to 0. It starts counting and at the same time initiates blinking when the BLK bit is set to l.

X Address Register (R2): The X address register (figure 35) designates the X address of the display RAM to be accessed by the MPU. The set value must range from H'00 to H'27 in the case of 8-bit a word or range from H'00 to H'35 in the case of 6-bit a word; setting a greater value is ignored. The set address is automatically incremented each time the display RAM is accessed; it is not necessary to update the address each time. Data bits 7 and 6 are unused; they should be set to 0 when written to. When you use monochrome display, the set value must range the even number from H'00 to H'26 in the case of 8-bit a word or range from H'00 to H'34 in the case of 6-bit a word.

Y Address Register (R3): The Y address register (figure 36) designates the Y address of the display RAM to be accessed by the MPU. The set value must range from H'00 to H'40; setting a greater value is ignored. The set address is automatically incremented each time the display RAM is accessed; it is not necessary to update the address each time. Data bit 7 is unused; it should be set to 0 when written to.

Data bit	7	6	5	4	3	2	1	0
Set value	BIS1	BIS0	WLS	GRAY	DTY1	DTY0	INC	BLK

Figure 34 Control Register 2 (R1)

Data bit	7	6	5	4	3	2	1	0
Set value			XA5	XA4	XA3	XA2	XA1	XA0

Figure 35 X address Register (R2)

Data bit	7	6	5	4	3	2	1	0
Set value		YA6	YA5	YA4	YA3	YA2	YA1	YA0

Figure 36 Y address Register (R3)

Display Memory Access Register (R4): The display memory access register (figure 37) is used to access the display RAM. If this register is write-accessed, data is directly written to the display RAM. If this register is read-accessed, data is first latched to this register from the display RAM and sent out to the data bus on the next read; therefore, a dummy read access is necessary after setting the display RAM address.

Display Start Raster Register (R5): The display start raster register (figure 38) designates the raster to be displayed at the top of the LCD panel. Varying the set value scrolls the display vertically. The set value must be one less than the actual top raster and less than the duty ratio. If the value is set outside these ranges, data may not be displayed correctly. Data bits 7 is unused; they should be set to 0 when written to.

Blink Start Raster Register (R6): The blink start raster register (figure 39) designates the top raster in the area to be blinked. The set value must be one less than the actual top raster and less than the duty ratio. If the value is set outside these ranges, operations may not be correct. Data bits 7 is unused; they should be set to 0 when written to.

Blink End Raster Register (R7): The blink end register (figure 40) designates the bottom raster in the area to be blinked. The area to be blinked is designated by the blink registers, blink start raster register, and blink end raster register. The set value must be one less than the actual bottom raster and less than the duty ratio. It must also be greater than the value set in the blink start raster register. If an inappropriate value is set, operations may not be correct. Data bits 7 is unused; they should be set to 0 when written to.

Data bit	7	6	5	4	3	2	1	0
Set value	D7	D6	D5	D4	D3	D2	D1	D0

Figure 37 Display Memory Access Register (R4)

Data bit	7	6	5	4	3	2	1	0
Set value		ST6	ST5	ST4	ST3	ST2	ST1	ST0

Figure 38 Display Start Raster register (R5)

Data bit	7	6	5	4	3	2	1	0
Set value		BSL6	BSL5	BSL4	BSL3	BSL2	BSL1	BSL0

Figure 39 Blink Start Raster register (R6)

Data bit	7	6	5	4	3	2	1	0
Set value		BEL6	BEL5	BEL4	BEL3	BEL2	BEL1	BEL0

Figure 40 Blink End Raster register (R7)

Blink Registers (R8 to R10): The blink bit registers (figure 41) designate the 8-bit groups to be blinked. Setting a bit to 1 blinks the corresponding 8-bit group. Any number of groups can be blinked; setting all the bits to 1 will blink the entire LCD panel. These bits are valid only when the BLK bit of control register 2 is 1. R10's data bits 7 to 4 are unused; they should be set to 0 when written to.

Partial Display Block Register (R11): The Partial display block register (figure 42) designates the block of partial display. It use from bit 3 to bit 0.

Bit 4 is clock-enable bit. This bit sets to 1, the signal CO,CL1,FLM and M stop in master mode. They are high-Z. Data bits 7 and 5 are unused; they should be set to 0 when written to.

Gray Scale Palette Registers (R12 to R15): The gray scale palette registers (figure 43) designate the grayscale level or colour. Use these registers to enable an optimal grayscale or colour display. If GRAY bit is 1, these registers are inactive. Data bits 7 to 5 are unused; they should be set to 0 when written to.

	Data bit	7	6	5	4	3	2	1	0
R8	Set value	BK0	BK1	BK2	BK3	BK4	BK5	BK6	BK7
R9	Set value	BK8	BK9	BK10	BK11	BK12	BK13	BK14	BK15
R10	Set value					BK16	BK17	BK18	BK19

Figure 41 Blink Registers (R8, R9, R10)

Data bit	7	6	5	4	3	2	1	0
Set value				CLE	PB3	PB2	PB1	PB0

Set value	Row no.
H'00	COM1 to COM8
H'01	COM9 to COM16
H'02	COM17 to COM24
H'03	COM25 to COM32
H'04	COM33 to COM40
H'05	COM41 to COM48

Set value	Row no.
H'06	COM100 to COM93
H'07	COM92 to COM85
H'08	COM84 to COM77
H'09	COM76 to COM69
H'0A	COM68 to COM61
H'0B	COM60 to COM53

(ADC= "0". If "1" , reverse direction)

Figure 42 Partial Display Start Raster Register (R11)

	Data bit	7	6	5	4	3	2	1	0
R12	Set value				GP14	GP13	GP12	GP11	GP10
R13	Set value				GP24	GP23	GP22	GP21	GP20
R14	Set value				GP34	GP33	GP32	GP31	GP30
R15	Set value				GP44	GP43	GP42	GP41	GP40

Figure 43 Grayscale Palette Registers (R12 to R15)

Contrast Control and LCD Alternative Drive Cycle Register (R16): The contrast control register (figure 44) designates the contrast level of LCD display. These bits change the voltage which is supplied to LCD drivers.

The LCD alternative drive cycle register designates the number of lines that LCD drive outputs are alternated.

Data bits 7 is unused; they should be set to 0 when written to.

Table 9 Grayscale Levels

GP14 GP24 GP34 GP44	GP13 GP23 GP33 GP43	GP12 GP22 GP32 GP42	GP11 GP21 GP31 GP41	GP10 GP20 GP30 GP40	Gray scale Level	GP14 GP24 GP34 GP44	GP13 GP23 GP33 GP43	GP12 GP22 GP32 GP42	GP11 GP21 GP31 GP41	GP10 GP20 GP30 GP40	Gray scale Level
0	0	0	0	0	0	1	0	0	0	0	16/31
0	0	0	0	1	1/31	1	0	0	0	1	17/31
0	0	0	1	0	2/31	1	0	0	1	0	18/31
0	0	0	1	1	3/31	1	0	0	1	1	19/31
0	0	1	0	0	4/31	1	0	1	0	0	20/31
0	0	1	0	1	5/31	1	0	1	0	1	21/31
0	0	1	1	0	6/31	1	0	1	1	0	22/31
0	0	1	1	1	7/31	1	0	1	1	1	23/31
0	1	0	0	0	8/31	1	1	0	0	0	24/31
0	1	0	0	1	9/31	1	1	0	0	1	25/31
0	1	0	1	0	10/31	1	1	0	1	0	26/31
0	1	0	1	1	11/31	1	1	0	1	1	27/31
0	1	1	0	0	12/31	1	1	1	0	0	28/31
0	1	1	0	1	13/31	1	1	1	0	1	29/31
0	1	1	1	0	14/31	1	1	1	1	0	30/31
0	1	1	1	1	15/31	1	1	1	1	1	1

Table 10 LCD alternative drive cycle

CM1	CM0	Alternative Cycle
0	0	Frame
0	0	7 lines
0	0	11 lines
0	0	13 lines

Data bit	7	6	5	4	3	2	1	0
Set value		CM1	CM0	CC4	CC3	CC2	CC1	CC0

Figure 44 Contrast Control register (R16)

Figure 45 shows characteristics of the LCD effective value against grayscale. This value is almost linear at all grayscale range without LCD panel. This linearity will be lost if LCD panel is connected. In this case, the four appropriate levels must be selected from grayscale No.1 to 31.

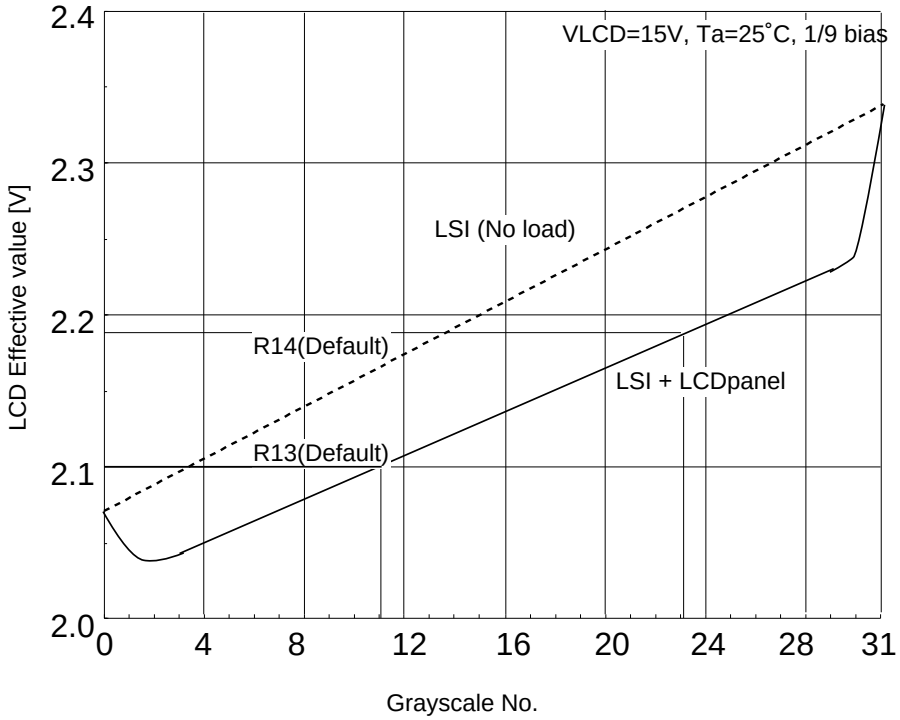


Figure 45 LCD Effective Value

Plane Selection Register (R17): The plane selection register (figure 46) controls general operations of the HD66421. Each bit has its own function as described below.

MON bit
MON = l: Monochrome display
MON = 0: 4-level gray scale display

DSEL bit
DESL = 1: Plane 1 is displayed
DESL = 0: Plane 0 is displayed

PSEL bit
PESL = 1: Access to plane 1 from CPU
PESL = 0: Access to plane 0 from CPU

Data bit	7	6	5	4	3	2	1	0
Set value						MON	DSEL	PSEL

Figure 46 Plane Selection Register (R17)

Note

When you use the monochrome display, you have to initialize the x-address to even number before access to display RAM. And you alway have to use even number.

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Notes
Power supply	Logic circuit	Vcc	-0.3 to +7.0	V	1
voltage	LCD drive circuit	VLCD	-0.3 to +20.0	V	
Input voltage 1		VT1	-0.3 to Vcc+0.3	V	1, 2
Input voltage 2		VT2	-0.3 to VLCD+0.3	V	1, 3
Operating temperature		Topr	-40 to +85	°C	
Storage temperature		Tstg	-55 to +110	°C	

Notes: 1 .Measured relative to GND
2 Applies to pins M/$\overline{S}$, OSC, OSC1, OSC2, DB7 to DB0, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, RS, $\overline{RES}$, CL1, M, FLM
3 Applies to pins V1O, V2O, V3O, V4O and V5O
4 If the LSI is used beyond its absolute maximum rating, it may be permanently damaged. It should always be used within the limits of its electrical characteristics to prevent malfunction or unreliability.

Electrical Characteristics

DC Characteristics (Vcc=2.2 to 5.5V, GND=0V, VLCD=6 to 18V, Ta=-40 to +85°C Note 9)

Item	Symbol	Applicable Pins	min.	Typ	Max	Unit	Measurement Condition	Notes
I/O leakage current	IIOL		-1	-	1	µA	Vin=Vcc to GND	1
V-pins leakage current	IVL		-10	-	10	µA	Vin=GND to VLCD	2
Driver on resistance	Ron	SEG1 to SEG160 COM1 to COM100			20	kΩ	Ion = 100µA VLCD = 6V	3
Input high voltage	VIH1		0.8xVcc	-	Vcc	V		1
Input low voltage	VIL1		0	-	0.2xVcc	V		1
Output high voltage	VOH	DB7 to DB0	0.8xVcc	-	Vcc	V	IoH=-50µA	4
Output low voltage	VOL	DB7 to DB0	0	-	0.2xVcc	V	IoL=50µA	4
Current consumption during display	Idisp	Vcc	-		T.B.D	µA	Vcc = 3.0V Rf = 180kΩ	5, 6
Current consumption during standby	Istb	Vcc	-	1	5	µA		5, 7
Current consumption in LCD drive part	Ilcd	VLCD	-		T.B.D	µA		5, 8

Notes: 1 Applies to pins: M/S, $\overline{CS}$, RS, $\overline{WR}$, $\overline{RD}$, $\overline{RES}$, OSC, DB7 to DB0, CL1, M and FLM

2 Applies to pins: V0O, V1O, V2O, V3O, V4O and V5O

3 Indicates the resistance between one pin from SEG1 to SEG160,COM1 to COM100 from V1O to V5O V1O and V2O should be near VLCD level, and V3O to V5O should be near GND level. All voltage must be within ΔV.ΔV is the range within which Ron is stable. V1 to V4 levels should keep following condition:VLCD≥V1O≥V2O≥V3O≥V4O≥V5O≥GND

4 Applies to pins: DB7-DB0, CO, CL1, M and FLM

5 Input and output current are excluded. When a CMOS input is floating, excess current flows from power supply to the input circuit. To avoid this, ViH and ViL must be held to Vcc and GND levels, respectively. The current which flows at resistive divider and LCD are excluded.
Where the unmolded side of LSI is exposed to light , excess current flows. Use under sealed condition.

6 Specified under following conditions:
Internal oscillator is used; Rf = 180kΩ
32-levels gray scale mode; GRAY = 0
CO,CL1,FLM,M stop; CLE = 1
Vcc = 3.0V
Checker board is displayed
No access fro CPU

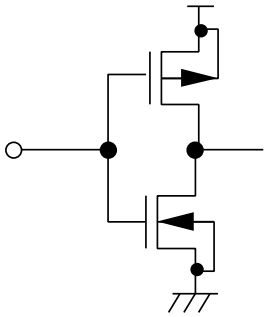
7 Measured during stand-by mode.
Vcc = 3.0V

8 Specified under following conditions:
Internal power supply circuit is used.
Resister value is 5MΩ which is connected between IREFM and GND
Vcc = 3.0V, VLCD = 15V, IREFP = Vcc, GREF = GND

9. All electrical characteristic are guaranteed at +85°C for die products.

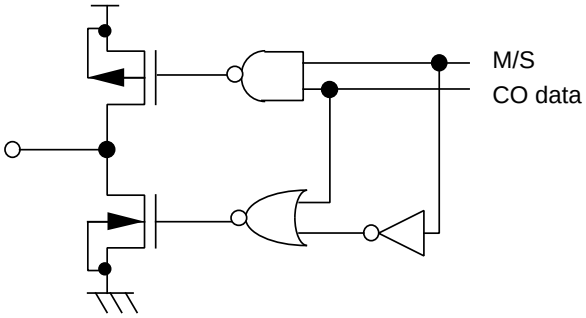
Input Terminal

Pins: $\overline{CS}$, RS, $\overline{WR}$, $\overline{RD}$, $\overline{RES}$, M/S



Output Terminal

Pins: CO



I/O Terminal Pins: DB7 to DB0, FLM, M, CL1

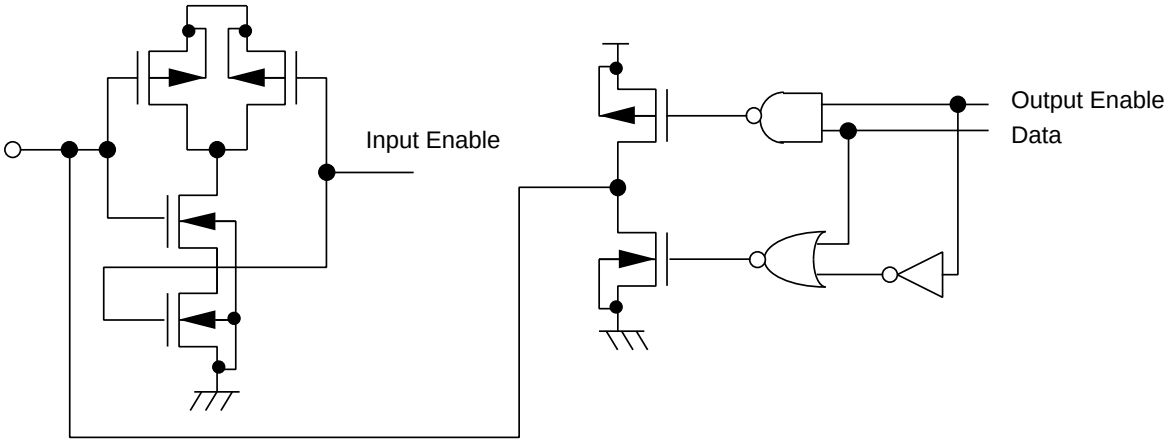


Figure 47 Terminal Configuration

AC Characteristics (Vcc = 2.2 to 5.5V, GND = 0V, Ta = -40 to +85°C Note 1)

Clock Characteristics

Item	Symbol	Min	Typ	Max	Unit	Notes
Oscillation frequency	fOSC	160	220	280	kHz	Rf = 180kΩ, Vcc = 3.0V
External clock frequency	fCP	50	–	400	kHz	
External clock duty cycle	Duty	45	50	55	%	
External clock fall time	tr	–	–	0.2	µs	
External clock rise time	tf	–	–	0.2	µs	

MPU Interface

Item	Symbol	Min	Typ	Max	Unit	Notes
RD low-level width	tWRDL	250	–	4tOSC - 450	ns	Vcc = 2.2V to 3.0V, 2
		190	–	4tOSC - 450	ns	Vcc = 3.0V to 5.5V, 2
RD high-level width	tWRDH	450	–	–	ns	
WR low-level width	tWWRL	250	–	4tOSC - 450	ns	Vcc = 2.2V to 3.0V, 2
		190	–	4tOSC - 450	ns	Vcc = 3.0V to 5.5V, 2
WR high-level width	tWWRH	450	–	–	ns	
Address setup time	tAS	20	–	–	ns	
Address hold time	tAH	20	–	–	ns	
Data delay time	tDDR	–	–	180	ns	Vcc = 2.2V to 3.0V
		–	–	150	ns	Vcc = 3.0V to 5.5V
Data output hold time	tDHR	20	–	–	ns	
Data setup time	tDSW	150	–	–	ns	Vcc = 2.2V to 3.0V
		100	–	–	ns	Vcc = 3.0V to 5.5V
Data hold time	tDHW	10	–	–	ns	

Reset Timing

Item	Symbol	Min	Typ	Max	Unit	Notes
RES low-level width	tRES	1	–	–	ms	

Note 1 All electrical characteristic are guaranteed at +85°C for die products.
Note 2 tOSC = 1 / fOSC

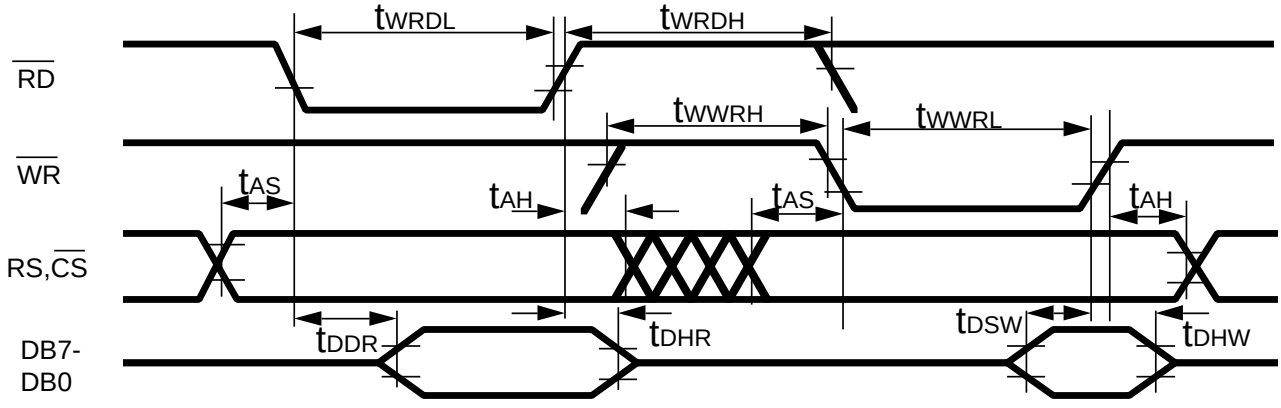


Figure 44 MPU Interface

Notes. The following load circuit is connected for specification.
VOH and VOL of the timing specification is 1/2 VCC level.