MDT2051A

1. General Description

This EPROM-Based 8-bit micro-controller uses a fully static CMOS design technology combines higher speeds and smaller size with the low power and high noise immunity of CMOS.
On chip memory system includes 1.0 K bytes of ROM, and 68 bytes of static RAM.

2. Features

The followings are some of the features on the hardware and software :

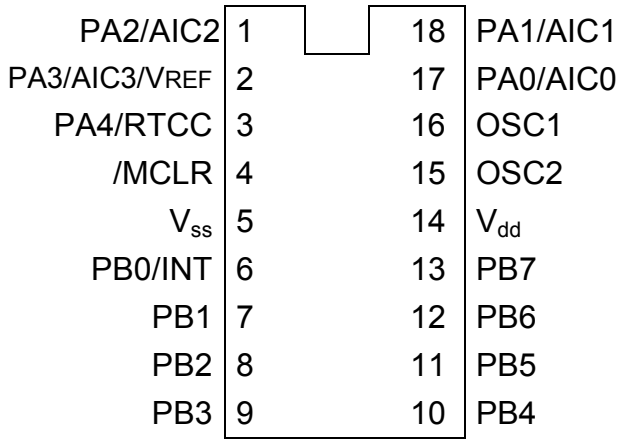
- Fully CMOS static design
- 8-bit data bus
- On chip ROM size : 1 K words
- Internal RAM size : 84 bytes
  (68 general purpose registers, 16 special registers)
- 37 single word instructions
- 14-bit instructions
- 8-level stacks
- Operation voltage : 2.3 V ~ 6.3 V
- Operation frequency : 0 ~ 20 MHz
- The most fast execution time is 200 ns under 20 MHz in all single cycle instructions except the branch instruction
- Addressing modes include direct, indirect and relative addressing modes
- Power-on Reset
- Power edge-detector Reset
- Power range-detector Reset
- Sleep Mode for power saving
- Four interrupt sources : -External INT pin
  -TMR0 timer
  -A/D conversion completion
  -PortB<7:4> interrupt on change
- A/D converter module : - Four analog inputs multiplexed into one A/D converter
  - 8-bit resolution
- 8-bit real time clock/counter(RTCC) with 8-bit programmable prescaler

- 4 types of oscillator can be selected by code options :
  RC－Low cost RC oscillator
  LFXT－Low frequency crystal oscillator
  XTAL－Standard crystal oscillator
  HFXT－High frequency crystal oscillator
- On-chip RC oscillator based Watchdog Timer(WDT) can be operated freely
- 13 I/O pins with their own independent direction control

3. Applications

The application areas of this MDT2051A range from appliance motor control and high speed automotive to low power remote transmitters/receivers, pointing devices, and telecommunications processors, such as Remote controller, small instruments, chargers, toy, automobile and PC peripheral … etc.

4. Pin Assignment



5. Pin Function Description

Pin Name	I/O	Function Description
PA0~PA3	I/O	Port A, TTL input level / Analog input channel
PB0~PB7	I/O	Port B, TTL input level / PB0 : External interrupt input
RTCC/PA4	I/O	Real Time Clock/Counter, Schmitt Trigger input levels Open-drain output / input pin
/MCLR	I	Master Clear, Schmitt Trigger input levels
OSC1	I	Oscillator Input
OSC2	O	Oscillator Output
V_{dd}		Power supply
V_{ss}		Ground

6. Memory Map

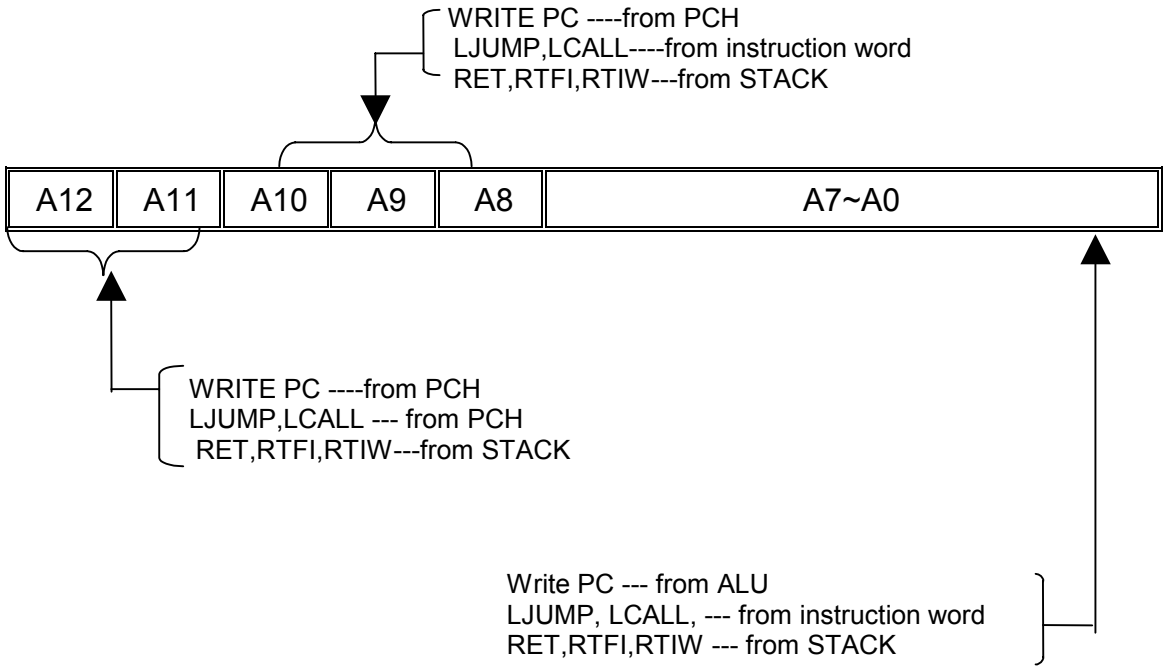
(A) Register Map

Address	Description
PAGE0	
00	Indirect Addressing Register
01	RTCC
02	PCL
03	STATUS
04	MSR
05	Port A
06	Port B
08	ADS0
09	ADRES
0A	PCH
0B	INTS
0C~4F	Internal RAM, General Purpose Register
PAGE1	
01	TMR
05	CPIO A
06	CPIO B
07	PSTA
08	ADS1

(1) IAR (Indirect Address Register) : R0

(2) RTCC (Real Time Counter/Counter Register) : R1

(3) PC (Program Counter) : R2,R0A



(4) STATUS (Status register) : R3

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	PF	Power loss Flag bit
4	TF	Time overflow Flag bit
5	RB0	Bank select bit : 0 : 00H --- 7FH 1 : 80H --- FFH
6—7	——	General purpose bit

(5) MSR (Memory Select Register) : R4

(6) PORT A : R5

PA4~PA0, I/O Register

(7) PORT B : R6

PB7~PB0, I/O Register

(8) TMR (Time Mode Register) : R81

Bit	Symbol	Function		
		Prescaler Value	RTCC rate	WDT rate
2—0	PS2—0	0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assignment bit : 0 — RTCC 1 — Watchdog Timer		
4	TCE	RTCC signal Edge : 0 — Increment on low-to-high transition on RTCC pin 1 — Increment on high-to-low transition on RTCC pin		
5	TCS	RTCC signal set : 0 — Internal instruction cycle clock 1 — Transition on RTCC pin		
6	IES	Interrupt edge select 0 — Interrupt on falling edge on PB0 1 — Interrupt on rising edge on PB0		
7	PBPH	PORTB pull-Hi Enable 0 — PORTB pull-hi are enable 1 — PORTB pull-hi are disable		

(9) CPIO A, CPIO B (Control Port I/O Mode Register)

The CPIO register is “write-only”
＝“0”, I/O pin in output mode;
＝“1”, I/O pin in input mode.

(10) EPROM Option by Writer Programming：

Oscillator Type
RC Oscillator
LFXT Oscillator
XTAL Oscillator
HFXT Oscillator

Power-up Time

Oms
75 ms

Watchdog Timer control
Watchdog timer disable all the time
Watchdog timer enable all the time

Power-range control
Power-range disable
Power-range enable

Power-edge control
Power-edge disable
Power-edge enable

Security bit
Security weak Disable
Security Disable
Security Enable

(11) ADS0 (A/D Status Register) : R8

Bit	Symbol	Function
0	ADRUN	0 : A/D converter module is shut off and consumes no operating current 1 : A/D converter module is operating
1	ADIF	A/D conversion complete interrupt flag bit Set when conversion is completed. Reset in software.
2	GO/DONEB	GO/DONEB must be set to begin a conversion . It is automatically reset in hardware when the conversion is complete
4,3	CHS1-0	00 : AIC0 01 : AIC1 10 : AIC2 11 : AIC3
5	Reserved	Can be used as a general purpose r/w bit
7,6	ASCS1-0	00 : fosc/2 01: fosc/8 10 : fosc/32 11 : f RC

(12) ADRES (A/D result register) : R9

(13) INTS (Interrupt Status Register) : RB

Bit	Symbol	Function
0	RBIF	PORT B change interrupt flag. Set when PB <7:4> inputs change
1	INTF	Set when INT interrupt occurs. INT interrupt flag.
2	TIF	Set when TMR overflows.
3	RBIE	0 : disable PB change interrupt 1 : enable PB change interrupt
4	INTS	0 : disable INT interrupt 1 : enable INT interrupt
5	TIS	0 : disable TMR interrupt 1 : enable TMR interrupt
6	ADIS	0 : disable A/D interrupt 1 : enable A/D interrupt
7	GIS	0 : disable global interrupt 1 : enable global interrupt

(14) ADS1 (A/D Status Register) : R88

Bit	Symbol	Function
1,0	PAVM1-0	00 : PA0 - 3 = analog input . V_{REF} = VDD 01 : PA0 - 2 = analog input . PA3 =ref input, V_{REF} =PA3 10 : PA0 - 1 = analog input. PA2-3 = digital I/O ,V_{REF} = VDD 11 : PA0 - 3 = digital I/O , V_{REF} = VDD

(15) PSTA : R87

Bit	Symbol	Function
0	PRDB	0:Power range-detector Reset occurred 1:No Power range-detector Reset Occurred
1	PORB	0:Power on Reset occurred 1:No Power on Reset occurred

(B) Program Memory

Address	Description
000-3FF	Program memory
000	The starting address of the power on, external reset or WDT time out
004	Interrupt Vector

7. Reset Condition for all Registers

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
IAR	00h	—	—	—
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PC	0Ah,02h	0 0000 0000 0000	0 0000 0000 0000	0 0000 0000 0100
STATUS	03h	0001 1xxx	000# #uuu	000# #uuu
MSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT A	05h	- - -x 0000	- - -u uuuu	- - -u uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADS0	08h	00-0 0000	00-0 0000	uu-u uuuu
ADRES	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu
INTS	0Bh	0000 000X	0000 000u	uuuu uuuu
TMR	81h	1111 1111	1111 1111	uuuu uuuu
CPIOA	85h	- - - 1 1111	- - - 1 1111	- - -u uuuu
CPIOB	86h	1111 1111	1111 1111	uuuu uuuu
PSTA	87h	- - - - - - 0u	- - - - - - uu	- - - - - - uu
ADS1	88h	- - - - - - 00	- - - - - -00	- - - - - - uu

Note : u＝unchanged, x＝unknown, - ＝unimplemented, read as “0”
#＝value depends on the condition of the following table

Condition	Status: bit 4	Status: bit 3
/MCLR reset (not during SLEEP)	u	u
/MCLR reset during SLEEP	1	0
WDT reset (not during SLEEP)	0	1
WDT reset during SLEEP	0	0

8. Instruction Set

Instruction Code	Mnemonic Operands	Function	Operation	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMODE register	W→TMODE	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO r	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiiiii	LDWI I	Load immediate to W	I→W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3) ↔ R(4~7)]→t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R – W→t (R+/W+1→t)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	R – 1→t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R – 1→t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
110100 iiiiiiii	ANDWI i	AND W and immediate	i ∩ W→W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
110101 iiiiiiii	IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
110110 iiiiiiii	XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
011111 trrrrrrr	COMR R, t	Complement register	/R→t	Z
010110 trrrrrrr	RRR R, t	Rotate right register	R(n) →R(n-1), C→R(7), R(0)→C	C
010101 trrrrrrr	RLR R, t	Rotate left register	R(n)→r(n+1), C→R(0), R(7)→C	C
010000 1xxxxxxx	CLRW	Clear working register	0→W	Z
010001 0rrrrrrr	CLRR R	Clear register	0→R	Z
0000bb brrrrrrr	BCR R, b	Bit clear	0→R(b)	None

Instruction Code	Mnemonic Operands	Function	Operation	Status
0010bb brrrrrrr	BSR R, b	Bit set	1→R(b)	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
1000nn nnnnnnnn	LCALL n	Long CALL subroutine	n→PC, PC+1→Stack	None
1010nn nnnnnnnn	LJUMP n	Long JUMP to address	n→PC	None
110001 iiiiiiii	RTIW i	Return, place immediate to W	Stack→PC, i→W	None
110111 iiiiiiii	ADDWI	Add immediate to W	PC+1→PC, W+i→W	C,HC,Z
111000 iiiiiiii	SUBWI	Subtract W from immediate	i-W→W	C,HC,Z
01 0000 0000 1001	RTFI	Return from interrupt	Stack→PC, 1→GIS	None
01 0000 0000 0100	RET	Return from subroutine	Stack→PC	None

Note :

W	:	Working register	b	:	Bit position
WT	:	Watchdog timer	t	:	Target
TMODE	:	TMODE mode register	0	:	Working register
CPIO	:	Control I/O port register	1	:	General register
TF	:	Timer overflow flag	R	:	General register address
PF	:	Power loss flag	C	:	Carry flag
PC	:	Program Counter	HC	:	Half carry
OSC	:	Oscillator	Z	:	Zero flag
Inclu.	:	Inclusive ‘∪’	/	:	Complement
Exclu.	:	Exclusive ‘⊕’	x	:	Don’t care
AND	:	Logic AND ‘∩’	i	:	Immediate data (8 bits)
			n	:	Immediate address

9. Electrical Characteristics

(A) Operation Voltage & Frequency

V_{dd} ： 2.3 V ~ 6.3 V

Frequency： 0 Hz ~ 20 MHz

(B) Input Voltage

@ V_{dd}＝5.0 V, Temperature＝25 ℃

	Port	Min.	Max.
V_{il}	PA, PB	V_{ss}	1.0 V
	RTCC, /MCLR	V_{ss}	1.0 V
V_{ih}	PA, PB	2.0 V	V_{dd}
	RTCC, /MCLR	3.5 V	V_{dd}

∗Threshold Voltage :

Port A, Port B V_{th}＝1.5 V

RTCC, /MCLR V_{il}＝1.8V, V_{ih}＝3.4 V　(Schmitt Trigger)

(C) Output Voltage：

@ V_{dd}＝5.0 V, Temperature＝25 ℃, the typical value as followings :

PA, PB Port	
I_{oh}＝－20.0 mA	V_{oh}＝4.0 V
I_{ol}＝20.0 mA	V_{ol}＝0.5 V
I_{oh}＝－5.0 mA	V_{oh}＝4.5 V
I_{ol}＝5.0 mA	V_{ol}＝0.2 V

(D) Leakage Current

@ V_{dd}＝5.0 V, Temperature＝25 ℃, the typical value as followings :

I_{il}	－ 1.0 μA (Max.)
I_{ih}	＋ 1.0 μA (Max.)

(E) Sleep Current

@PRD－Disable,

@WDT－Enable, Temperature＝25 ℃, the typical value as followings :

V_{dd}＝2.3 V	I_{dd}＜1 μA
V_{dd}＝3.0 V	I_{dd}＝2 μA
V_{dd}＝4.0 V	I_{dd}＝8 μA
V_{dd}＝5.0 V	I_{dd}＝16 μA
V_{dd}＝6.4 V	I_{dd}＝32 μA

@PRD－Disable,

@WDT－Disable, Temperature＝25 ℃, the typical value as followings :

V_{dd}＝2.3 V~6.4 V, I_{dd}＜1.0 μA

(F) Operation Current

Temperature＝25 ℃, the typical value as followings :

(i) OSC Type＝RC ; WDT－Enable ; PRD－Disable ; @ V_{dd}＝5.0 V

Cext. (F)	Rext. (Ohm)	Frequency (Hz)	Current (A)
3P	4.7 K	13.5 M	2.5 m
	10.0 K	6.9 M	1.4 m
	47.0 K	1.7 M	530 μ
	100.0 K	796 K	400 μ
	300.0 K	269 K	300 μ
	470.0 K	173 K	280 μ
20P	4.7 K	6.5 M	1.3 m
	10.0 K	3.3 M	800 u
	47.0 K	772 K	400 μ
	100.0 K	364 K	300 μ
	300.0 K	122 K	280 μ
	470.0 K	78 K	250 μ
100P	4.7 K	1.9 M	570 u
	10.0 K	957 K	420 μ
	47.0 K	216 K	310 μ
	100.0 K	103 K	290 μ
	300.0 K	35 K	260 μ
	470.0 K	22 K	250 μ
300P	4.7 K	732 K	400 u
	10.0 K	369 K	330 μ
	47.0 K	82 K	290 μ
	100.0 K	39 K	280 μ
	300.0 K	13 K	270 μ
	470.0 K	8.3 K	260 μ

(ii) OSC Type＝LF (C=20 p);　WDT－Disable　;　PRD－Disable

Voltage/Frequency	32 K	455 K	1 M	Sleep
2.3 V	36 uA	X	X	< 1 μA
3.0 V	80 μA	120 μA	173 μA	< 1 μA
4.0 V	140 μA	200 μA	257 μA	2 μA
5.0 V	204 μA	287 μA	362 μA	6 μA
6.4 V	342 μA	433 μA	542 μA	10 μA

(iii) OSC Type＝XT (C=10 p);　WDT－Enable　;　PRD－Disable

Voltage/Frequency	1 M	4 M	10 M	Sleep
2.1 V	137 μA	320 μA	674 μA	< 1 μA
3.0 V	224 μA	507 μA	1.0 mA	2 μA
4.0 V	360 μA	763 μA	1.5 mA	8 μA
5.0 V	540 μA	1.1 mA	2.1 mA	16 μA
6.4 V	890 uA	1.6 mA	2.9 mA	32 μA

(iv) OSC Type＝HF (C=10 p);　WDT－Enable　;　PRD－Disable

Voltage/Frequency	4 M	10 M	20 M	Sleep
2.1 V	345 μA	700 μA	@2.4V 1.5mA	< 1 μA
3.0 V	545 μA	1.1 mA	2.1 mA	2 μA
4.0 V	848 μA	1.7 mA	2.9 mA	8 μA
5.0 V	1.2 mA	2.3 mA	3.9 mA	16 μA
6.4 V	1.8 mA	3.3 mA	5.5 mA	32 μA

(G) Power Edge-detector Reset Voltage (Not in Sleep Mode), @ V_{dd}＝5.0 V

$V_{pr} \leqq 1.3$ V　　V_{pr} ： V_{dd} (Power Supply)

(H) The basic WDT time-out cycle time

Temperature＝25 ℃, the typical value as followings :

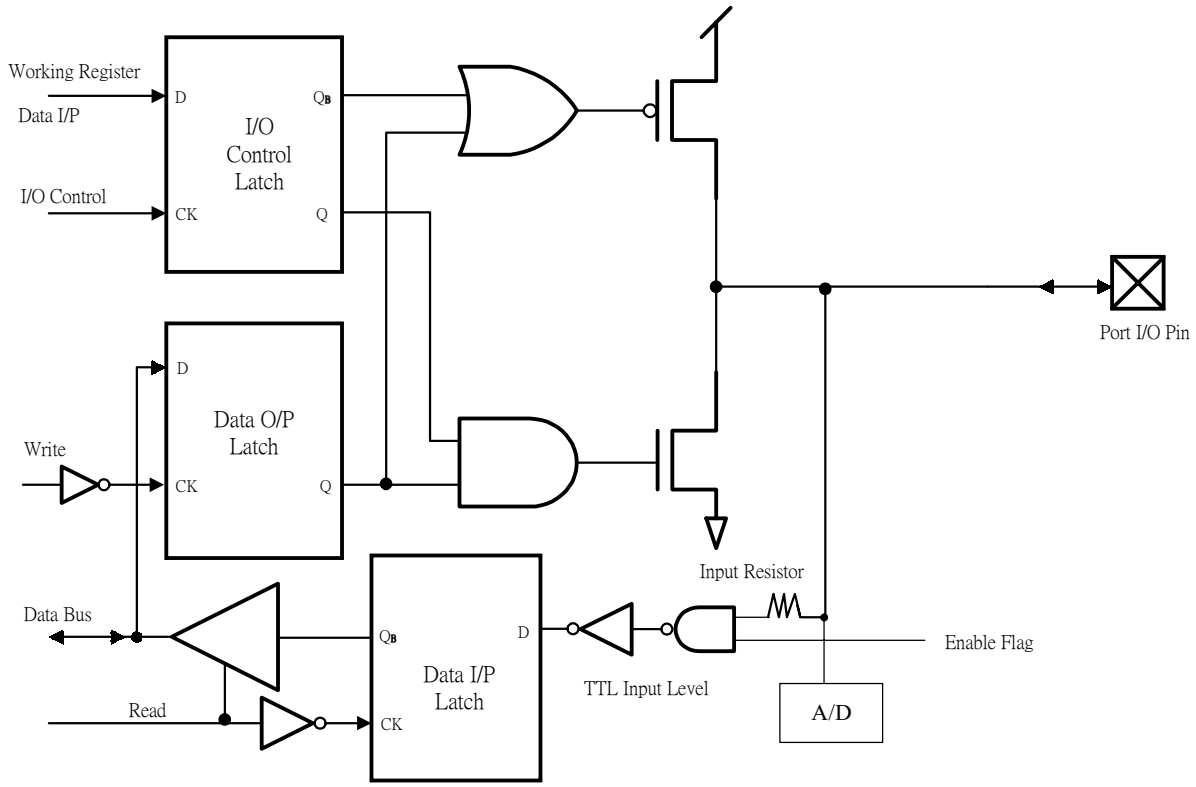
Voltage (V)	Basic WDT time-out cycle time (ms)
2.3	26.2
3.0	23.6
4.0	20.8
5.0	19.1
6.3	17.6

(I) PRD Enable:

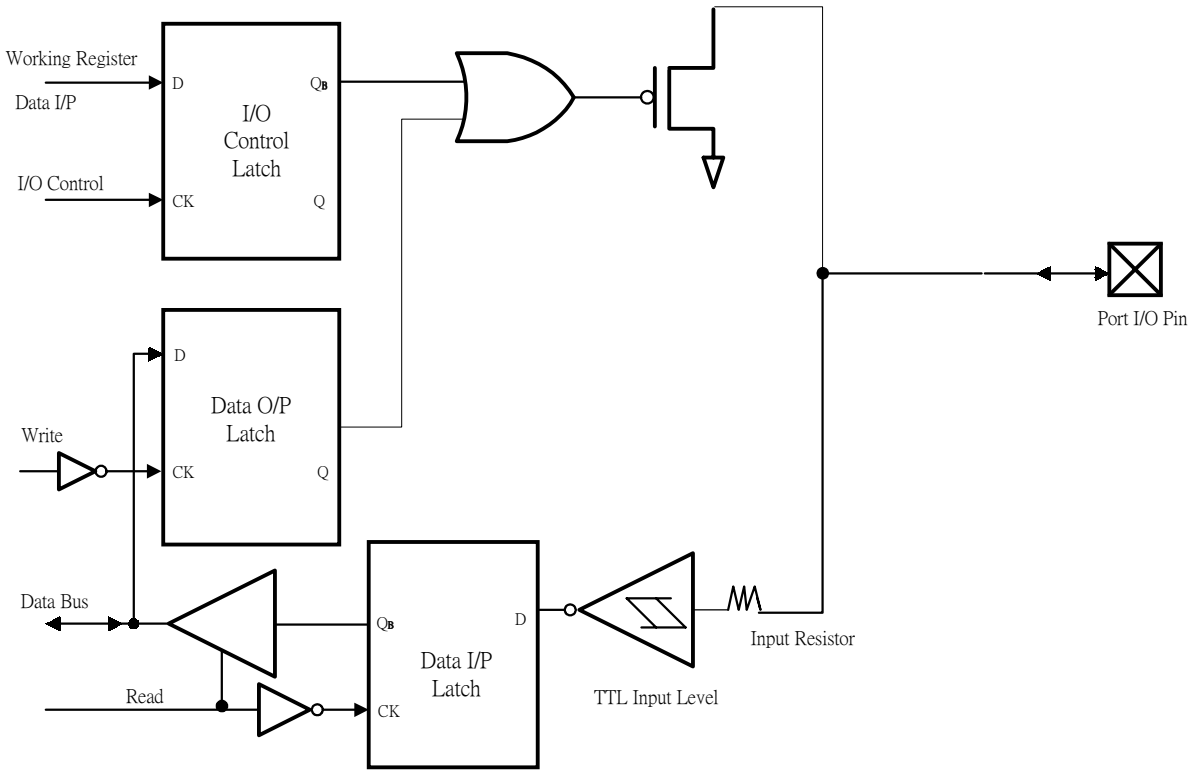
PRD Reset Voltage :3.8V~4.2V
PRD Reset Current :400uA~600uA

10. Port A and Port B Equivalent Circuit

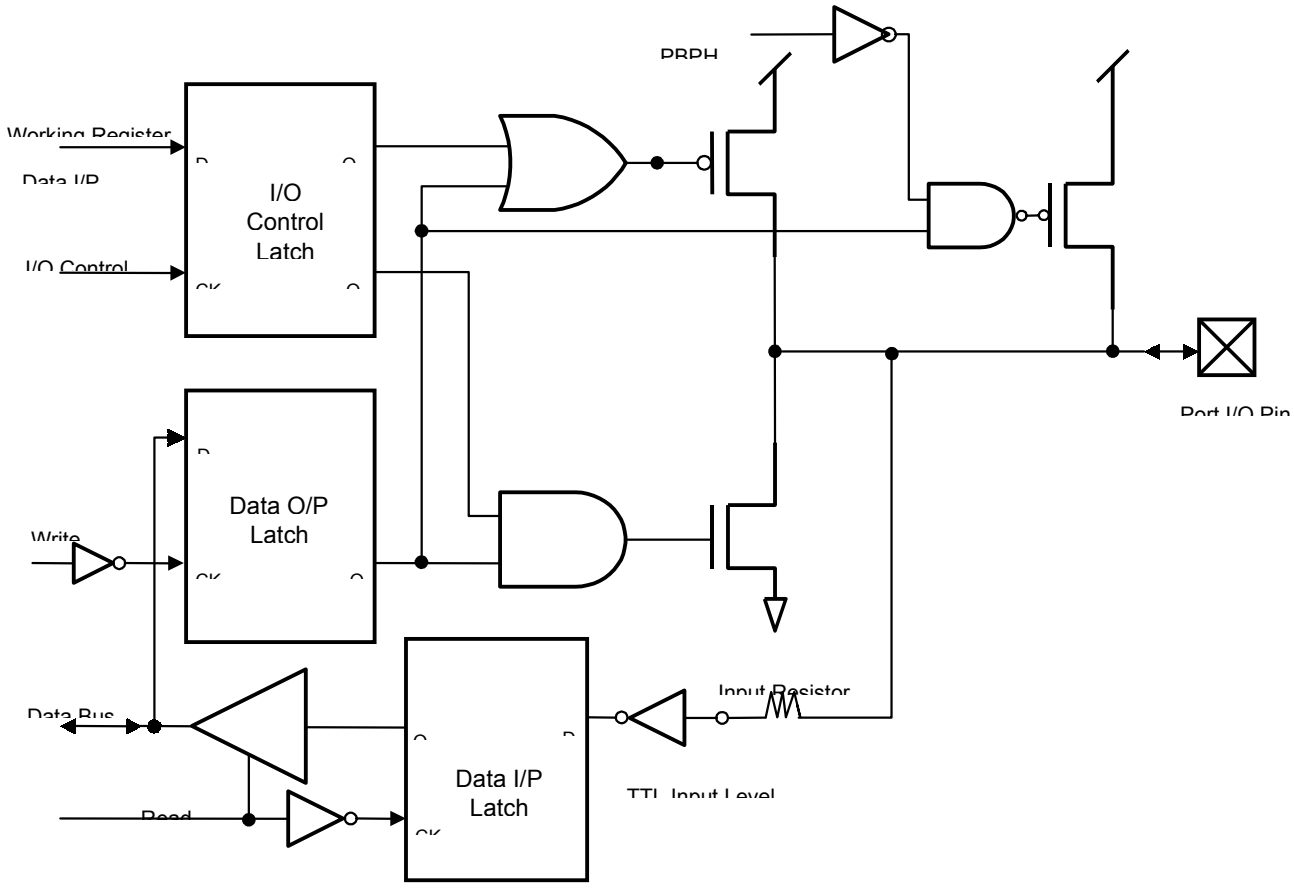
PA0~PA3



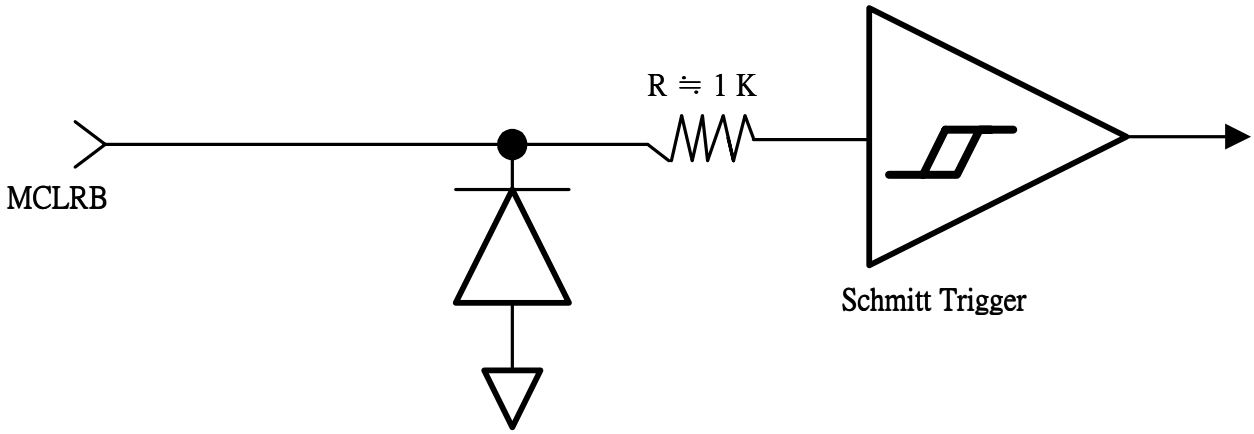
PA4

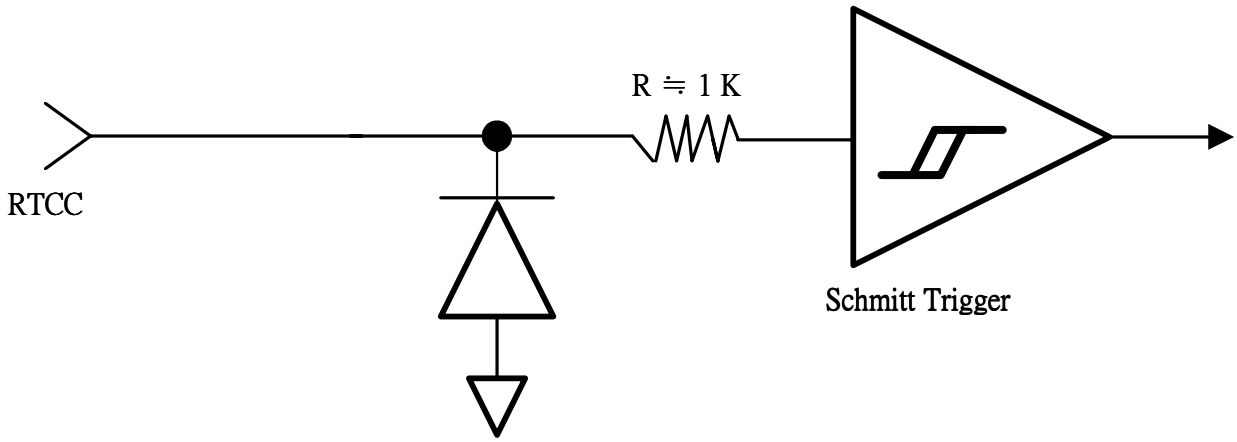


PB0~PB7

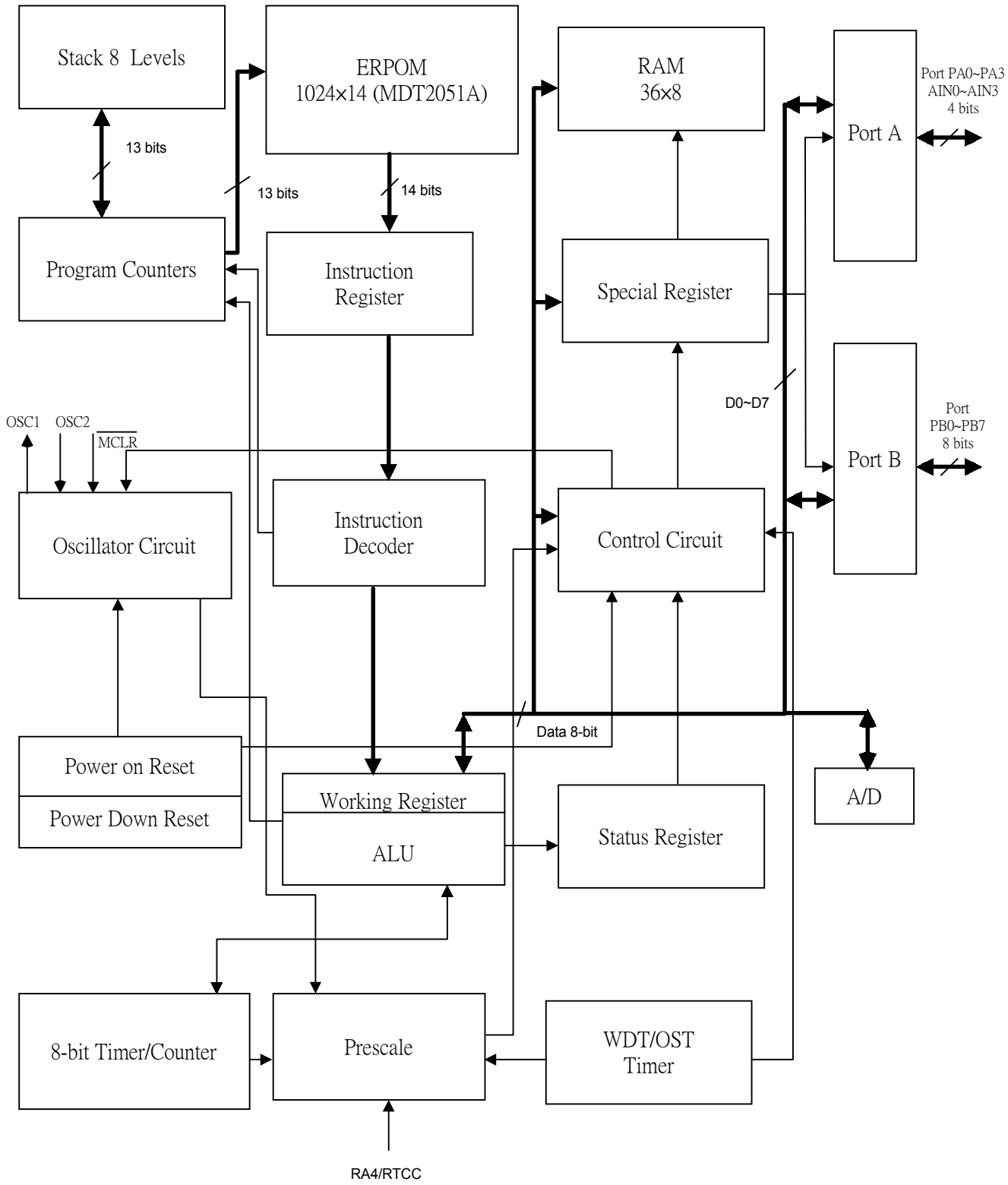

PRPH
Working Register
Data I/P
I/O
Control
Latch
I/O Control
Port I/O Pin
Data O/P
Latch
Write
Input Resistor
Data Bus
Data I/P
Latch
TTL Input Level
Read

11. MCLRB and RTCC Input Equivalent Circuit





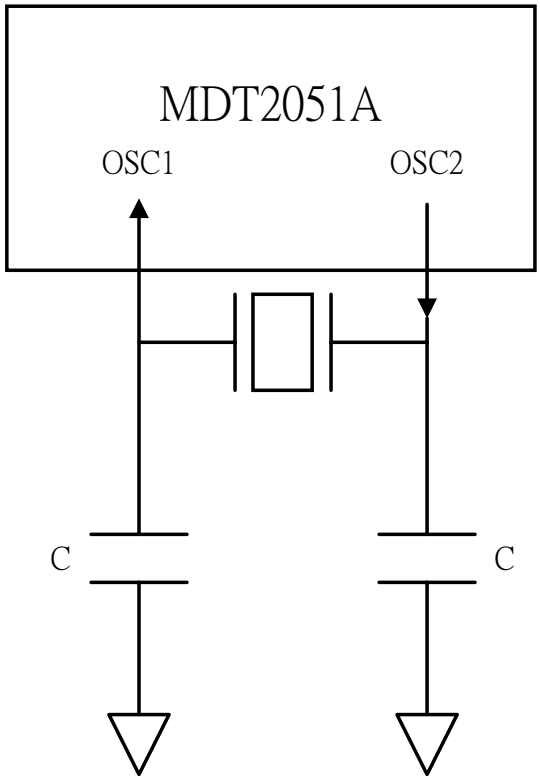
12. Block Diagram



13. External Capacitor Selection For Crystal Oscillator

@ V_{dd} = 5.0 V

Osc. Type	Resonator Freq.	Capacitor Range
HF	20 MHz	20 pF~30 pF
	10 MHz	3 pF ~10 pF
	4 MHz	3 pF ~10 pF
XT	10 MHz	3 pF ~10 pF
	4 MHz	3 pF ~10 pF
	1 MHz	10 pF ~30 pF
LF	1 MHz	3 pF ~10 pF
	455 K	30 pF ~100 pF
	32 K	20 pF ~50 pF



To increase the stability of oscillator and the ability of anti-noise, the above values of the external capacitor range can be recommended for reference, but the higher capacitance also increases the start-up time.