FEATURES

- Control
  - Controller and integrated bus interface total solution for IEEE 802.3, 10BASE5, 10BASE2 and 10BASE-T
  - Software-compatible with industry standard Ethernet adapters:
    * Novell®'s NE 2000
    * Western Digital/SMC's (8003E, 8003EBT, 8013EBT)
  - Selectable buffer memory size
  - No external bus logic or drivers
  - Integrated controller, MCC and transceiver
  - Full IEEE 802.3 AUI interface
  - Single 5V supply
  - Software-compatible with DP8390, DP83901 and DP83902
  - Efficient buffer management implementation
- MCC module (Manchester Code Converter, also called ENDEC)
  - 10 Mbit/s Manchester encoding/decoding
  - Squelch on receive and collision pairs
- TPI module (10BASE-T) transceiver
  - Transmitter and receiver functions
  - Collision detect, heartbeat and jabber
  - Selectable link integrity test or link disable
  - Polarity detection/correction
- Provides more powerful functions than NS DP83905
  - Supports 15 I/O bases instead of 7
  - Direct ID PROM access through I/O port instead of through remote DMA
  - Auto configuration function-supported makes jumperless more powerful
  - Solution for multiple LAN cards I/O bases conflict problem to make manufacture more efficient.
  - Supports "write ID back to EEPROM" function instead of just writing configuration back to EEPROM to make manufacture more efficient.
  - Modify current configurations without turning off power
  - Variety of EEPROM supported

GENERAL DESCRIPTION

The MX98905 is designed for easy implementation of CSMA/CD local area networks, which include Ethernet® (10BASE5), Thin Ethernet (10BASE2), and Twisted-pair Ethernet (10BASE-T). The Media Access Control (MAC) and Encode-Decode (ENDEC) are provided with an AUI interface. The 10BASE-T transceiver functions according to the IEEE 802.3 standards, and the MX98905 10BASE-T transceiver operations in compliance with the IEEE standard.

The functional block of the MX98905 consists of the integration of the entire bus interface for PC-AT® (Industry Standard Architecture, ISA) bus-based systems, receiver, transmitter, collision, heartbeat, loopback, jabber, and link integrity blocks. When combined with equalization resistors, the transceiver transmits or receives filters, and pulse transformers provide physical interface from the ENDEC module of the MX98905 and the twisted-pair medium.

When software and hardware are properly configured, the MX98905 can be set to be compatible with either the NE2000 or EtherCard PLUS16™. All bus drivers and control logic are integrated inside the chip to reduce LAN card cost and area.

Manchester encoding and decoding is made possible through the integrated ENDEC by means of a differential transceiver and phase lock loop decoder at 10 Mbit/sec. Collision detect translator and diagnostic loopback capability are included in this process. Interfacing directly with the transceiver module, the ENDEC module also provides a fully IEEE-compliant AUI (Attachment Unit Interface) to connect with other media transceivers.

The Media Access Control function, provided by the Ethernet Network Control (ENC) module, effects an efficient packet transmission and reception control through unique dual DMA channels and an internal FIFO. To lessen board cost and area overheads, bus arbitration and memory control logic are integrated.

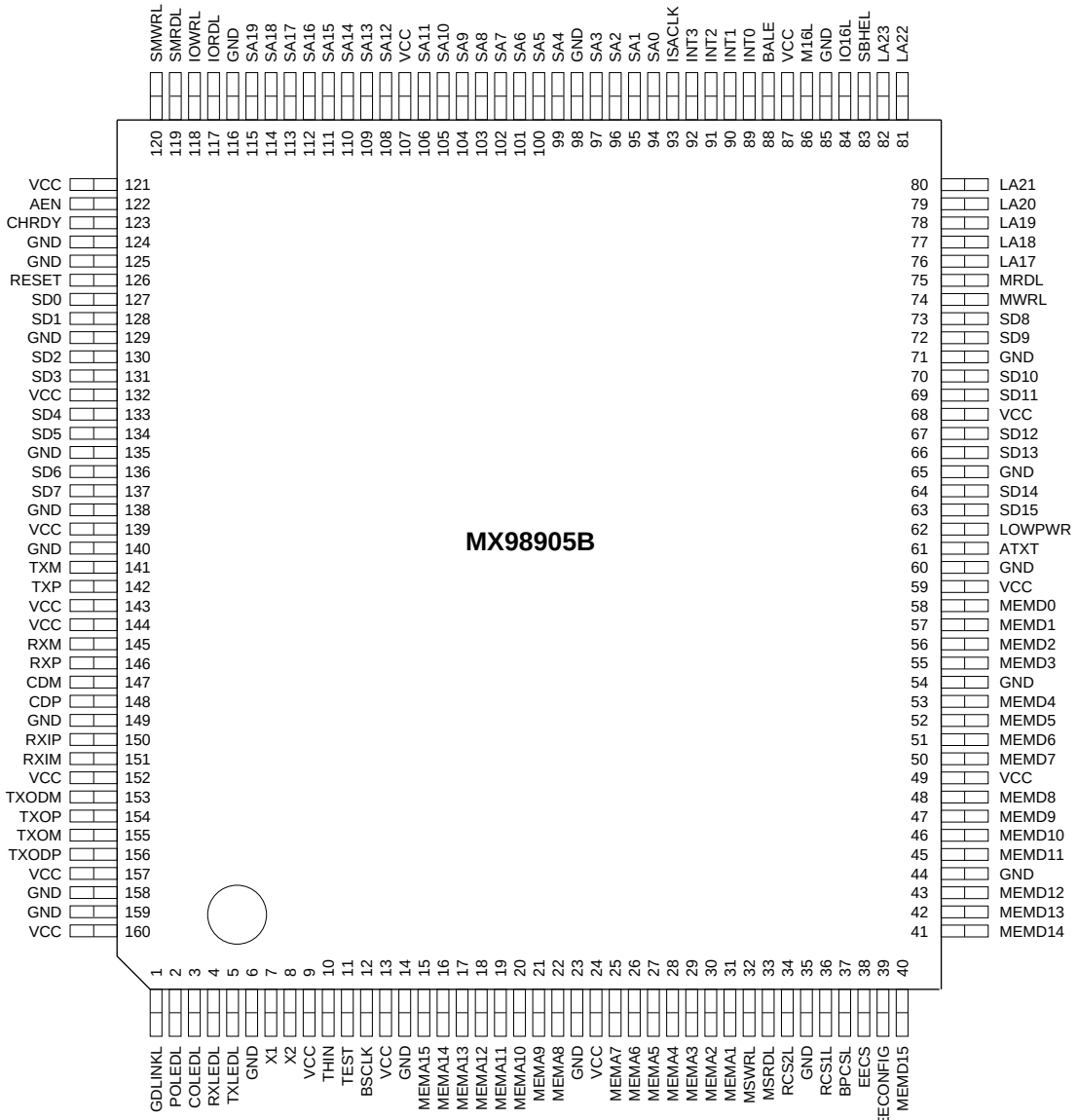
Designed for easy interface with other transceivers by means of the AUI interface, the MX98905 provides a thorough single chip solution for 10BASE-T IEEE 802.3 network.

Constraints of CMOS processing require that isolation, whether capacitive or inductive, be used at the AUI differential signal interface for 10BASE5 and 10BASE2 applications.

Note:

TRI-STATE® is a registered trademark of National Semiconductor.
PC-AT® is a register trademark of International Business Machines Corp.
Novell® is a registered trademark of Novell Inc.
EtherCard PLUS™ and EtherCard PLUS 16™ are trademarks of standard Microsystems Corp.
Ethernet® is a registered trademark of Xerox Corp.

PIN CONFIGURATION



PIN DESCRIPTIONS

A. ISA BUS INTERFACE

SYMBOL	PIN TYPE	PIN NUMBER	DESCRIPTION
SA0-SA19	I	94-97, 99-106, 108-115	LATCHED ADDRESS BUS: Low-order bits of the system's 24-bit address bus. These lines are enabled onto the bus when BALE is high and latched when BALE is deasserted. The MX98905 uses these bits to decode the boot PROM address and internal registers. In shared memory mode, they are used to decode accesses to memory of the MX98905.
LA17-LA23	I	76-82	UNLATCHED ADDRESS BUS: High-order 7 bits of the 24-bit system address bus. These lines are valid on the falling edge of BALE. The MX98905 uses these bits to decode shared memory address in shared memory mode. The validity of M16L depends on these signals only.
SD0-SD15	I/O	127, 128, 130, 131, 133, 134, 136, 137, 73, 72 70, 69, 67, 66, 64, 63	SYSTEM DATA BUS: 16-bit system data bus. Used to transfer data between the system and the MX98905.
BALE	I	88	BUS ADDRESS LATCH ENABLE: Active-high signal. Used to latch valid addresses from the current Bus Master on the falling edge of BALE.
SBHEL	I	83	SYSTEM BUS HIGH ENABLE: Active-low. Indicates that the system expects a transfer on the address on the bus is 16 bits wide.
IO16L	O	84	16-BIT I/O TRANSFER: Active-low. In I/O mode this signal indicates that the MX98905 is responding to a 16-bit I/O access by driving 16 bits of data on SD0-SD15.
M16L	O	86	16-BIT MEMORY TRANSFER: Active-low.
MWRL	I	74	MEMORY WRITE STROBE: Active-low. System uses this signal to write to the memory map of the MX98905.
MRDL	I	75	MEMORY READ STROBE: Active-low. System uses this signal to read from the memory map of the MX98905.
SMRDL, SMWRL	I	119, 120	LOW MEMORY STROBES: Active-low. The MX98905 uses MRDL and MWRL in 16-bit memory mode and will use SMRDL and SMRL in memory mode when ATXT is low (8-bit mode). Note that SMRDL and SMWRL are also used to access the BOOT PROM.
IOWRL	I	118	I/O WRITE STROBE: Active-low. Strobe from system to write to the I/O Map of the MX98905.
IORDL	I	117	I/O READ STROBE: Active-low. Strobe from system to read from the I/O Map of the MX98905.

A. ISA BUS INTERFACE *(Continued)*

SYMBOL	PIN TYPE	PIN NUMBER	DESCRIPTION
RESET	I	126	RESET : Active high. Used to reset all devices on the bus. The MX98905 will recognize this signal only when the duration of this signal is larger than 400 ns.
CHRDY	O	123	CHANNEL READY: Used to insert wait states into system accesses.
AEN	I	122	DMA ACTIVE: Indicates that the address lines are driven by a DMA controller.
INT0-INT3	O	89-92	INTERRUPT REQUEST: Activation or not of these 4 signals is determined by Configuration Registers A and C. They can be used to either directly drive the interrupt lines or used as a 3-bit code with strobe to generate up to 8 interrupts.
ATXT	I	61	8/16 BIT SLOT SELECT: Indicates that the MX98905 is in 8- or 16-bit ISA bus. It is in 16-bit mode when ATXT is high ATXT has internal pulldown register; if left unconnected, 8-bit mode is the default mode.
ISACLK	I	93	ISA CLOCK: Clock from ISA bus.

B. NETWORK INTERFACE

SYMBOL	PIN TYPE	PIN NUMBER	DESCRIPTION
POLEDL	O	2	POLARITY LED: Active-low signal. When the MX98905 detects seven consecutive link pulses or three consecutive received packets with reversed polarity, POLEDL is asserted.
TXLEDL	O	5	TRANSMIT LED: Active-low signal. It is asserted for approximately 50ms whenever the MX98905 transmits data in either AUI or TPI modes.
RXLEDL	O	4	RECEIVE LED: Active-low signal. An open-drain output. It is asserted for approximately 50ms whenever valid received data is detected while in AUI or TPI modes.
COLEDL	O	3	COLLISION LED: An open-drain active-low signal. It is asserted for approximately 50ms whenever collision is detected while in AUI or TPI modes.
GDLINKL	O	1	GOOD LINK LED: An open-drain active-low signal. Used to display link integrity status. OFF (when high): A. MX98905 is in AUI mode B. MX9805E is in TPI mode, link testing is enabled and link integrity is bad. ON (when low): A. Link testing is disabled B. Link testing is enabled and link integrity is good.
X1	I	7	Crystal or external oscillator input.
X2	O	8	CRYSTEL FEEDBACK OUTPUT: Used in crystal connection only. Should be left completely unconnected when using an oscillator module.
THIN	O	10	THIN CABLE: Active-high signal. It is high when the MX98905 is configured for thin cable (program PHY1 and PHY0 of Configuration B). This signal can be used to turn on the DC-DC converter required by thin Ethernet.
TXODP, TXOM, TXOP, TXODM	O	156-153	TWISTED-PAIR TRANSMIT OUTPUTS: These high-drive CMOS level outputs are resistively combined external to the chip to produce a differential output signal with equalization to compensate for inter-symbol interference (ISI) on the twisted-pair medium.

B. NETWORK INTERFACE *(Continued)*

SYMBOL	PIN TYPE	PIN NUMBER	DESCRIPTION
RXIP, RXIM	I	150-151	TWISTED-PAIR RECEIVE INPUTS: These inputs feed a differential amplifier which passes valid data to the MCC module.
TXM, TXP	O	141-142	AUI TRANSMIT OUTPUT: Differential driver which sends the encoded data to the transceiver. The outputs are source follower which requires 270 W pulldown resistors.
RXM, RXP	I	145-146	AUI RECEIVE INPUTS: Differential receive input pair from the transceiver.
CDM, CDP	I	147-148	AUI COLLISION INPUTS: Differential collision pair input from the transceiver cable.

C. EXTERNAL MEMORY SUPPORT

SYMBOL	PIN TYPE	PIN NUMBER	DESCRIPTION
MEMD0-7 CA0-7 DO, DI, SK	I/O	58-55	MEMORY SUPPORT DATA BUS; CONFIGURATION REGISTER A INPUT; EEPROM SIGNALS. MEMD0-7 : These pins can be used to access external memory (RAM) and boot PROM while RESET is inactive. CA0-7: When RESET is active more than 400 ms, Configuration Register A is loaded with the value on these pins on the falling edge of RESET signal. These 8 bits have internal pulldown resistors, hence if the pin is left unconnected the corresponding register bit is 0. DO, DI, SK: When RESET goes from an active to an inactive level, the MX98905 will read the contents of an EEPROM. At this moment, DO = MEMD0, DI = MEMD1 and SK = MEMD2. The value read from EEPROM will be stored in Configuration Registers and PROM space.
MEMD8-15	I/O	48-45	MEMORY SUPPORT DATA BUS; CONFIGURATION REGISTER B INPUT. MEMD8-15 : These pins can be used to access external memory when RESET is inactive. CB0-7 : When RESET is active more than 400 ms, Configuration Register B is loaded with the value on these pins on the falling edge of RESET signal. These 8 bits have internal pulldown registers, hence if the pin is left unconnected the corresponding register bit is 0.
MEMA1-8	I/O	31-25, 22	MEMORY SUPPORT ADDRESS BUS; CONFIGURATION REGISTER C INPUT. MEMA1-8 : These pins can be used to drive external memory address bus when RESET is inactive. CC0-7 : When RESET is active more than 400 ms, Configuration Register C is loaded with the value on these pins on the falling edge of RESET signal. For application without EEPROM (i.e. EECONFIG is low) and try to load configuration data to CC from these eight pins, external resistor is necessary.
MEMA9-15	O	21-15	MEMORY SUPPORT ADDRESS: These pins can be used to drive external memory address bus when RESET is inactive. When the memory is only 8 bits wide (single RAM) and the MX98905 is in compatible mode, A0 will appear on A13; and on A15 in non-compatible mode.
MSRDL	O	33	MEMORY SUPPORT BUS READ: Strobes data from the external RAM into the MX98905 through the memory support data bus.
MSWRL	O	32	MEMORY SUPPORT BUS WRITE: Strobes data from the MX98905 into the external RAM via the memory support data bus.
BPCSL	O	37	BOOT PROM CHIP SELECT: Active-low signal for selecting the Boot PROM.

C. EXTERNAL MEMORY SUPPORT *(Continued)*

SYMBOL	PIN TYPE	PIN NUMBER	DESCRIPTION
RCS1L	O	36	RAM CHIP SELECT 1 : Active-low signal to drive the CS signal of the external RAM on the lower half of the memory-supported data bus.
RCS2L	O	34	RAM CHIP SELECT 2: Active-low signal to drive the CS signal of external RAM on the upper half of the memory-supported data bus.
EECS	O	38	EEPROM CHIP SELECT: Active-high signal to drive the CS signal of the external EEPROM.
EECONFIG	I	39	CONFIGURE FROM EEPROM: The MX98905 will NOT load configurations from EEPROM if this pin is low during power-on reset.
BSCLK	I	12	INTERNAL BUS CLOCK: This pin controls the speed of the controller DMA function. When CLKSEL of configuration C is set low, this pin should be tied to ground.

D. LOW POWER SUPPORT

SYMBOL	PIN TYPE	PIN NUMBER	DESCRIPTION
LOWPWR	I	62	LOW POWER: When it is high, the MX98905 enters its low-power mode. This pin should be tied to ground for normal operation.

E. TEST SUPPORT

SYMBOL	PIN TYPE	PIN NUMBER	DESCRIPTION
TEST	I	11	TEST: This pin is only used for industry test. It should be left unconnected in normal operation (because it has internal pulldown resistor).

F. POWER SUPPLY PINS

SYMBOL	PIN TYPE	PIN NUMBER	DESCRIPTION
VCC	I	160, 157, 152, 144, 143, 9, 59, 49, 24, 13, 132, 121, 107, 87, 68,139	5V POWER SUPPLY PIN.
GND	I	159, 158, 149, 140, 138, 6, 60, 54, 44, 35, 23, 14, 135, 129, 125, 124, 116, 98, 85, 71, 65	GND SUPPLY PIN.

FUNCTIONAL DESCRIPTION

1. I/O BASES DETERMINATION

The I/O bases are determined by 6 bits in the MX98905. They are: IOAD2-0 in Configuration A (CA); PAGE and IOBEN in Hidden Configuration Register (HCFR) and HCFRE in Hidden Command Register (HCMR). For details about HCMR and HCFR (Registers provided by the MX98905 only) see Register Description. User can directly modify the value of PAGE and IOAD2-0 to change I/O base or use AUTO configuration feature provided by the MX98905. See Enhanced mode description for details about AUTO configuration.

The following are the I/O bases mapping:

TABLE 1. I/O BASES MAPPING

HCMR HCFRE	HCFR IOBEN	HCFR PAGE	IOAD2	CA IOAD1	IOAD0	I/O BASE
0	X	X	0	0	0	300H
1	X	X	0	0	1	Not supported
0	X	X	0	1	0	240H
0	X	X	0	1	1	280H
0	X	X	1	0	0	2C0H
0	X	X	1	0	1	320H
0	X	X	1	1	0	340H
0	X	X	1	1	1	360H
1	0	X	0	0	0	300H
1	0	X	0	0	1	Not supported
1	0	X	0	1	0	240H
1	0	X	0	1	1	280H
1	0	X	1	0	0	2C0H
1	0	X	1	0	1	320H
1	0	X	1	1	0	340H
1	0	X	1	1	1	360H
1	1	0	0	0	0	300H
1	1	0	0	0	1	Not supported
1	1	0	0	1	0	240H
1	1	0	0	1	1	280H
1	1	0	1	0	0	2C0H
1	1	0	1	0	1	320H
1	1	0	1	1	0	340H
1	1	0	1	1	1	360H

HCMR HCFRE	HCFR IOBEN	PAGE	IOAD2	CA IOAD1	IOAD0	I/O BASE
1	1	1	0	0	0	380H
1	1	1	0	0	1	3A0H
1	1	1	0	1	0	3C0H
1	1	1	0	1	1	3E0H
1	1	1	1	0	0	200H
1	1	1	1	0	1	220H
1	1	1	1	1	0	2A0H
1	1	1	1	1	1	2E0H

HCFRE, IOBEN and PAGE are powered on low if software driver doesn't alter the value of these bits. The I/O bases of the MX98905 are fully compatible with DP83905.

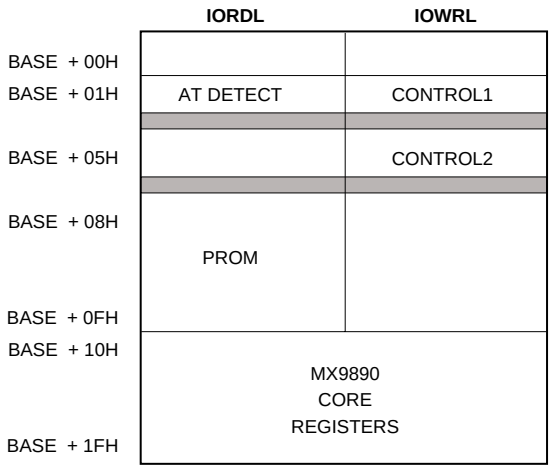
2. SHARED MEMORY COMPATIBLE MODE

This mode is compatible with the EtherCARD PLUS16. I/O address mapping and Memory mapping will be described subsequently.

After I/O Base is determined, the following structure appears:

2.1 I/O Address Mapping

FIGURE 2. SHARED MEMORY MODE REGISTER MAPPING



The AT Detect register indicates whether the MX98905 is in an 8- or 16-bit slot. The MX98905 uses the falling edge of RESET to latch the value shown on ATXT to determine the value of ATDET.

Address 08H to 0FH are specified as PROM space. The contents of PROM are loaded from EEPROM during power-on reset. User should program the EEPROM to contain these value. In enhanced mode of the MX98905, the contents of PROM can be written back to EEPROM. See enhanced mode description for details.

2.2 Memory Address Mapping

FIGURE3. SHARED MEMORY MODE ENC CORE MEMORY MAP

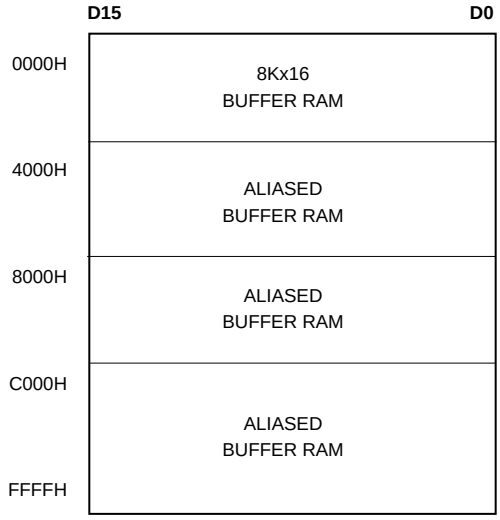


FIGURE 4. SHARED MEMORY MODE HOST MEMORY MAP FOR 8 KBYTES BUFFER RAM

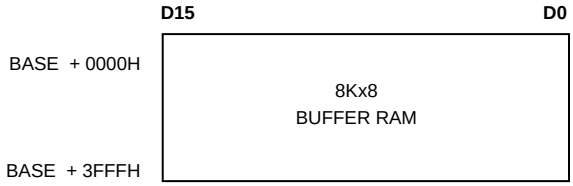
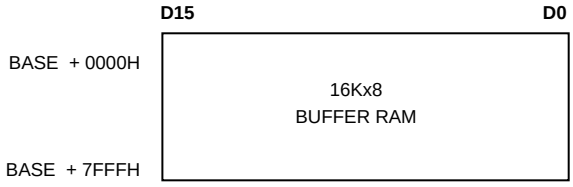


FIGURE 5. SHARED MEMORY MODE HOST MEMORY MAP FOR 16 KBYTES BUFFER RAM



The 8 kwords of memory can be accessed directly by the host system in the same manner as any other memory. Typically the programmer can remove data from this buffer using a "MOV" or "MOVSW" instruction.

In compatible mode, data located at address 4000h-7FFFH, 8000H-BFFFH and C000H-FFFFH is just the mirror of contents located at 0000H-3FFFH.

2.3 Configuration vs. Operation

MEMW	COMP	SIZE	ATDET	MX98905 ACCESS MODE	HOST ACCESS MODE
0	0	8K	0	Byte	Byte
0	0	8K	1	Byte	Byte
1	0	16K	0	Byte/Word	Byte
1	0	16K	1	Byte/Word	Byte/Word
0	1	32K	0	Byte	Byte
0	1	32K	1	Byte	Byte
1	1	64K	0	Byte/Word	Byte
1	1	64K	1	Byte/Word	Byte/Word

2.4 SRAM Size vs. MEMA[15:1]

SRAMSIZE	MEMA15	MEMA14	MEMA13	RCS1L	RCS2L
8K	0	1	A0	Even/Odd	X
16K	0	1	A13	Even	Odd
32K	A0	A14	A13	Even/Odd	X
64K	A15	A14	A13	Even	Odd

3. SHARED MEMORY NON-COMPATIBLE MODE

The difference between compatible and non-compatible mode is that the non-compatible mode maps a full 64 kbytes of RAM into the PC's memory address space instead of 8 kbytes. The I/O map for both modes is the same.

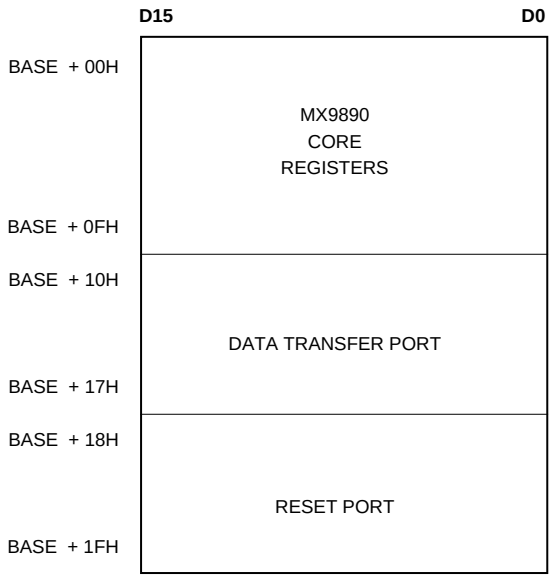
4. 16-BIT I/O PORT COMPATIBLE MODE

This mode is compatible with the Novel NE2000. I/O address mapping and Memory mapping will be shown in the following subsection.

After I/O base is determined, the following structure appears:

4.1 I/O Address Mapping

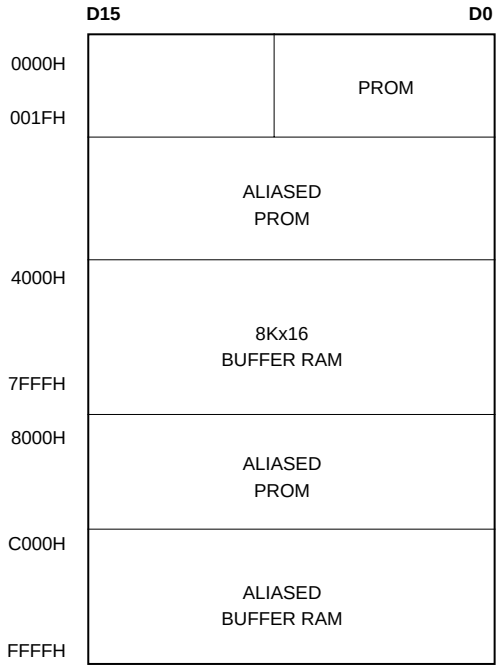
FIGURE 6. I/O MODE I/O PORT MAP



The registers within this area are 8 bits wide, but the data transfer port is 16 bits wide. By programming the ENC's internal registers, the user can issue Remote DMA to transfer data between the data port and the external memory.

4.2 Memory Address Mapping

FIGURE 7. I/O MODE MEMORY MAP



The MX98905 Controller has a 64K address range, but only does partial decoding on these devices. The PROM data is mirrored at all decodes up to 4000H and the entire map is repeated at 8000H. In order to access either the PROM or the RAM, the user must initiate a Remote DMA transfer between the I/O port (see I/O map) and the memory.

Address 00H to 1FH are specified as the PROM space to make the MX98905 compatible with NE2000. Similar to shared memory map, this is actually an array of 8-bit registers which are loaded from EEPROM during power-on reset. User should prepare data in the EEPROM as show in the format.

For user's convenience, the MX98905 provides an enhanced mode to facilitate software to access the contents of ID PROM -- Read ID PROM through I/O port. User can refer to Enhanced mode description for details.

4.3 PROM Map

TABLE 2.

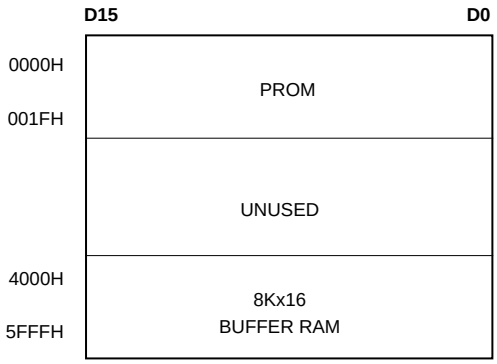
PROM LOCATION	LOCATION CONTENTS
00H	EtherNet Address 0 (MSB)
01H	EtherNet Address 1
02H	EtherNet Address 2
03H	EtherNet Address 3
04H	EtherNet Address 4
05H	EtherNet Address 5
06H-0DH	00H
0E-0FH	57H
10-15H	EtherNet Address 0 thru 5
16-1DH	Reserved
1E-1FH	42H

The upper two addresses of the PROM store contain bytes that identify whether the MX98905 Controller is in 8- or 16-bit mode. For 16-bit mode the values of these bytes are 57H; for 8-bit mode they both contain 42H. Software driver can read these two bytes to determine whether the Controller is in 8- or 16-bit mode.

5. 8-BIT I/O PORT COMPATIBLE MODE

In 8-bit I/O port compatible mode, the I/O mapping is the same as in 16-bit mode. The memory map for 8-bit I/O port compatible mode is shown below:

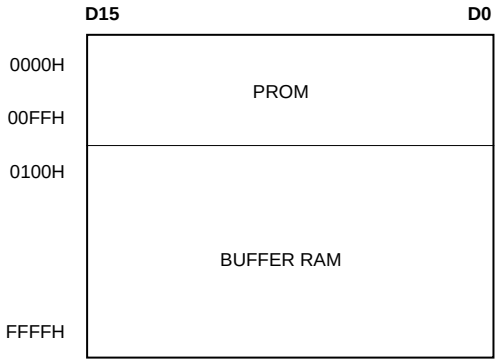
FIGURE 8. I/O MODE 8-BIT MEMORY MAP



6. I/O PORT NON-COMPATIBLE MODE

Although this mode is similar to Novell's NE2000, it also allows the user to use the full 64 kbytes of address space except for an initial page for the PROM. I/O map is the same as compatible mode. Memory map is shown below:

FIGURE 9. I/O MODE NON-COMPATIBLE MODE MEMORY MAP



Although the PROM occupies 256 bytes, it is only 16 bytes long. There is a partial decode inside the MX98905 so the PROM is mirrored at 16 addresses in this region.

7. POWER-ON RESET OPERATION

When the duration of RESET signal is longer than 400ns, the MX98905 will read configurations from EEPROM depending on the value shown on EECONFIG pin. User should prepare all the data the MX98905 needs in the EEPROM before switching on the PC. The following table shows the format of EEPROM:

TABLE 3. EEPROM DATA MAPPING

	D15	D0
0FH	NOT USED	CONFIG. C
0EH	CONFIG. B	CONFIG. A
	•	•
	•	•
	•	•
08H	42H	42H
07H	57H	57H
	•	•
	•	•
	•	•
03H	RESERVED	RESERVED
	(CHECKSUM)	(BOARD TYPE)
02H	ETEHR ADD 5	ETHER ADD 4
01H	ETHER ADD 3	ETEHR ADD 2
00H	ETEHR ADD 1	ETEHR ADD 0

values shown on parentheses are for Shared memory map only. For the shared memory mode, the two's complement of these eight bytes (00-03H) should be equal to FFH.

High byte of 0FH is not used in NS DP83905 compatible mode, but the value will be loaded into Hidden ConFiguration Register (HCFR) inside the MX98905 in enhanced mode. See Enhanced mode description for details.

7.1 Valid Power-On Reset

The MX98905 is equipped with a filter to screen out RESET signal whenever its duration is less than 400ns. The default value of each Configuration Register is:

Configuration Register A : 39H
Configuration Register B : 00H
Configuration Register C : 00H

When RESET is active more than 400ns, the MX98905 will recognize such action and begin its power-on reset algorithm. At this moment, all I/O will be disabled except the RESET signal. On the falling edge of RESET signal, the MX98905 will load data shown on MEMD0-7, MEMD8-15 and MEMA1-8 into Configuration Register A, B and C, respectively. The value loaded from jumper will overwrite the default value.

Figure 10 shows the example for jumper configuration.

After loading jumper value into relative Configuration Registers, the MX98905 will execute EEPROM operation, which depends on the value of EECONFIG. If EECONFIG is high, then both the configuration and ID PROM data will be loaded into the MX98905; otherwise, only ID PROM data is loaded.

7.2 EEPROM Operation

During EEPROM operation, all internal registers are inaccessible. If EECONFIG is high, then the configurations loaded from EEPROM will overwrite the value loaded from jumper selection. Configurations loaded from EEPROM will be stored in Configuration Registers and Ether ID will be stored in PROM space inside the MX98905 (refer to PROM MAP for details).

7.2.1 Load Configurations from EEPROM
When EECONFIG is set to high, configurations stored in EPPROM will be loaded into MX98905. After loading configurations fom EEPROM, following sequence depends on the value of ATXT:
ATXT= 1 : 00H-07H
ATXT= 0 : 00H-06H, 08H
EECONFIG = 1 : OEH (Configuration A, B), OFH
DWID = 1 (Configuration C),00H - 02H (Ether Address 0 theu 5) and 03H - 07H

EECONFIG = 1 : OEH (Configuration A, B), OFH
DWID = 0 (Configuration C),00H - 02H (Ether Address 0 true 5)and 03H - 06H and 08H (data 42H)

7.2.2 Without loading configurations from EEPROM

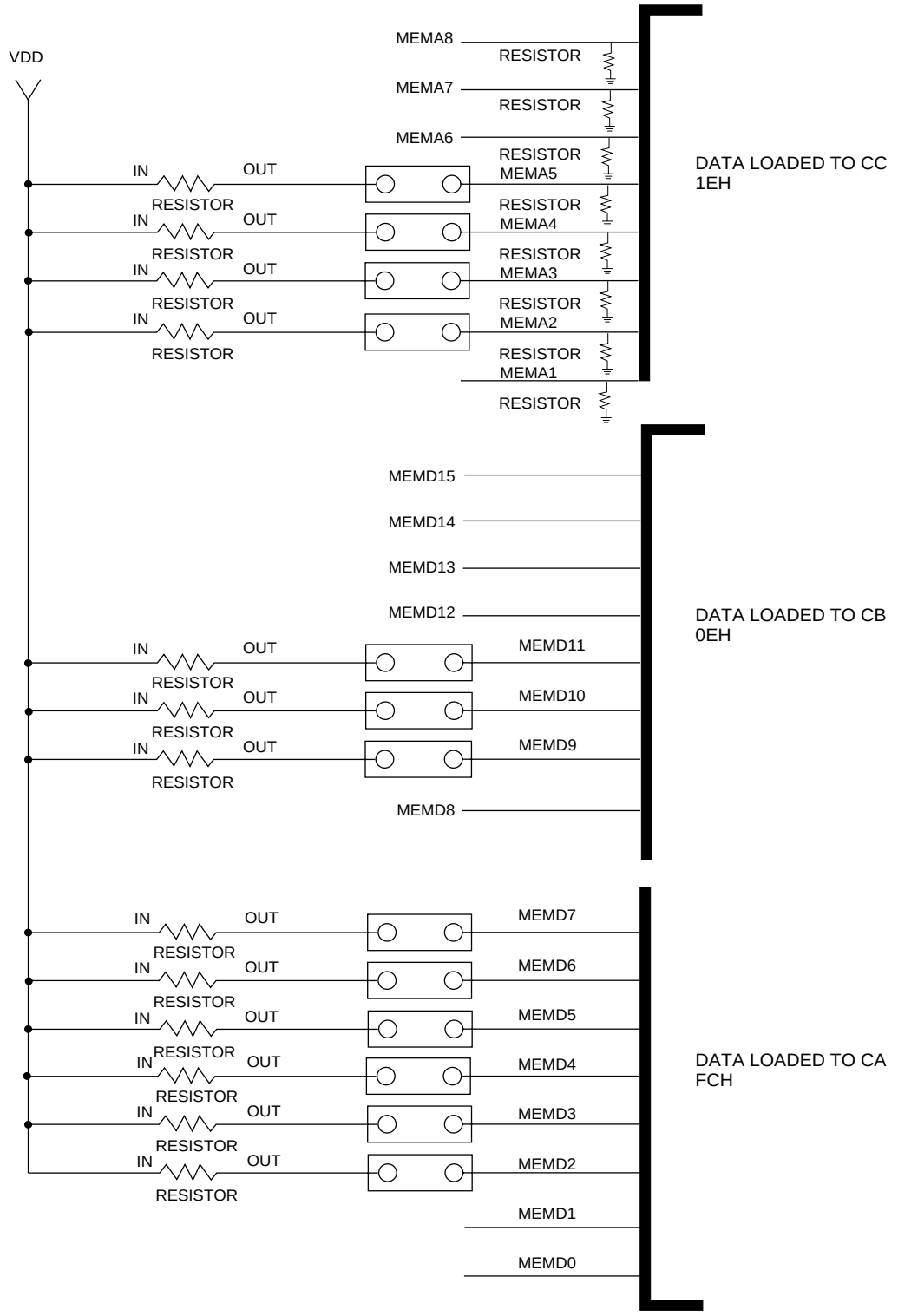
When EECONFIG is set to low, configrations stored in EEPROM will NOT be loaded into the MX98905 depends on
the value of ATXT:
ATXT = 1 : 00H-07H
ATXT = 0 : 00H-06H,08H

8. STORING CONFIGURATION BACK TO EEPROM

To write configuration into the EEPROM, user must follow the procedure specified below:

```
EEPROM_STORE ( )  {
      Disable_All_Interrupts ( ) ;
      value = READ (CB) ;
      value = value & GDLINK ;
      value = value Í EESTORE ;
      write (CB, value) ;              / / Issue EESTORE
      / / EESTORE algorithm starts
      Read (CB) ;
         write (CB, value_for_CA) ;      / / write new
                                              /  /into  CA
                                  through CB
      write (CB, value_for_CB) ;  / / write CB
      write (CB, value_for_CC) ;  / / write new value
                                    into CC through CB
      while (value & EESTORE)  {
           value = Read(CB) ;
           wait ( ) ;
      }
      Enable_All_Interrupts ( ) ;
```

FIGURE 10. EXAMPLE OF JUMPER CONFIGURATION



Note:Pull down resistors(4.7Ký~10Ký) are required to be connected to MEMA8~MEMA1.

After EEPROM_STORE is executed, the current configuration will NOT be changed. If user wants to use the new configuration, he should turn the power off and then turn it on to load new configuration into the MX98905 through valid power-on reset.

For user's convenience, the MX98905 provides the feature for software programmer to update the current configuration after EEPROM_STORE is executed, i.e., you don't have to switch the power to update the configuration. See Enhanced Description for details.

9. ENHANCED FEATURE FUNCTIONAL DESCRIPTION

There are two registers, HCMR and HCFR which control the main fuctions of MX98905's enhaned mode. HCMR is the abbreviation of Hidden Command Register and HCFR for Hidden Configuration Register. Bit assignment and function of each bit of HCMR and HCFR will be fully descibed in REGISTER DESCRIPTIONS. For your quick reference, bit assignments of HCMR and HCFR are shown below before we present the enhanced features of MX98905. The following shows the bit assignment for HCMR:

RESVD	MULTI	ALLWR	IDECMD	AUTO	NPGEN	PGSEL	HCFRE

Following shows the bit assignment for HCFR

RESVD	RESVD	RESVD	RESVD	LOCKE	NEWCF	PAGE	IOBEN

9.1 Load HCFR From EEPROM

The high-byte value of address 0FH of EEPROM will be loaded into Hidden ConFiguration Register (HCFR) if a valid power-on reset is detected by the MX98905. HCFR is only active when HCFRE bit of HCMR (Hidden CoMmand Register, supported by the MX98905) is set high. If software doesn't alter the value of HCFRE, the value in HCFR has no effect. In the same way, when EEPROM_STORE algorithm is executed, contents of HCFR will be stored back to EEPROM at the location from where they come.

9.2 16 Bytes IDPROM write back function

To write configuration into the EEPROM in either MX98905 or MX98905A, user must follow the procedure described in section 8.

In MX98905, a "1" value in ALLWR bit will cause the controller to write CA, CB, CC and ID to EEPROM. While in MX98905A, a "1" value in ALLWR bit will write CA, CB, CC, ID, and the rest of 8 bytes from IDPROM registers. i.e. the entire 16 bytes of IDPROM registers can be written back to EEPROM. The other EEPROM write back command is IDWCMD command whose function remains the same as old version.

When loading data from EEPROM during power-on reset, values in IDPROM register byte 15th and 16th are never written back to EEPROM but initialized to correct value according to slot's data width during power-on reset. these two bytes can be modified through software programming.

9.3 Update Current Configuration After EEPROM_STORE is Finished

When NEWCF bit of HCFR is set, the contents of CA, CB and CC will be updated to the value in EEPROM_STORE algorithm after EEPROM_STORE algorithm is finished. USER DOESN'T HAVE TO SWITCH THE POWER TO USE THE NEW CONFIGURATION.

9.4 Access ID PROM Through I/O Port IN NE2000 Compatible

When NPGEN is high and PGSEL is low (both in HCMR), the MX98905 is programmed to New Page 0. Contents of ID PROM can be directly accessed through I/O port. Table 4 and Table 5 show the address mapping.

9.5 Auto Configuration

The MX98905 provides a powerful feature for programmer to program the LAN card in order to avoid the "IO base is conflict with other add_ on cards" program. When bit 3 (AUTO) of HCMR is set to 1, the MX98905 will change the internal IO base automatically. When software writes to AUTO the first time, the IO base will change to 300H no matter the current IO base is. Susbsequent writing to AUTO bit will make the MX98905 jump to the "next" IO base as described in next paragraph. After AUTO is issued, user can use the information provided below to read the AutoStatus

Register (ASR) to determine whether the IO base is conflict with other add_ on card(s) or not. When 15 IO base is not enabled (see HCMR register description for more detail), internal state machine will only support 7 IO bases when AUTO is written; if IOBEN of HCFR is set to high (see HCFR register description for more detail), the internal state machine will alter the value of PAGE of HCFR automatically when further IO base is necessary during auto configuration.

The following I/O bases are supported by MX98905. (*) represents that the IO bases are not supported by MX98905 when 15 IO base is not enabled. 200H (*), 220H (*), 240H, 280H,2A0H (*), 2C0H, 2E0H (*), 300H, 320H, 340H, 360H, 380H (*), 3A0H (*), 3C0H (*) , and 3E0H (*)

The following IO base and its relative ASR value (shown in parenthses) will be followed after software write an "1" to AUTO bit of HCMR.

TABLE 4. NEW PAGE 0 ADDERSS ASSIGNMENT FOR I/O MAP

SA00..3	READ	WRITE
00H	PROM BYTE #0 (PB0)	PROM BYTE #0 (PB0)
01H	PROM BYTE #1 (PB1)	PROM BYTE #1 (PB1)
02H	PROM BYTE #2 (PB2)	PROM BYTE #2 (PB2)
03H	PROM BYTE #3 (PB3)	PROM BYTE #3 (PB3)
04H	PROM BYTE #4 (PB4)	PROM BYTE #4 (PB4)
05H	PROM BYTE #5 (PB5)	PROM BYTE #5 (PB5)
06H	PROM BYTE #6 (PB6)	PROM BYTE #6 (PB6)
07H	PROM BYTE #7 (PB7)	PROM BYTE #7 (PB7)
08H	PROM BYTE #8 (PB8)	PROM BYTE #8 (PB8)
09H	PROM BYTE #9 (PB9)	PROM BYTE #9 (PB9)
0AH	PROM BYTE #10 (PB10)	PROM BYTE #10 (PB10)
0BH	PROM BYTE #11 (PB11)	PROM BYTE #11 (PB11)
0CH	PROM BYTE #12 (PB12)	PROM BYTE #12 (PB12)
0DH	PROM BYTE #13 (PB13)	PROM BYTE #13 (PB13)
0EH	PROM BYTE #14 (PB14)	PROM BYTE #14 (PB14)
0FH	PROM BYTE #15 (PB15)	PROM BYTE #15 (PB15)

TABLE 5. NEW PAGE 0 ADDRESS ASSIGNMENT FOR MEMORY MAP

SA00..3	READ	WRITE
00H	Control 1	Control 1
01H	AT Detect	Reserved
02H	Reserved	Reserved
03H	Reserved	Reserved
04H	Reserved	Reserved
05H	Control 2	Control 2
06H	Reserved	Reserved
07H	Reserved	Reserved
08H	PROM BYTE #0 (PB0)	PROM BYTE #0 (PB0)
09H	PROM BYTE #1 (PB1)	PROM BYTE #1 (PB1)
0AH	PROM BYTE #2 (PB2)	PROM BYTE #2 (PB2)
0BH	PROM BYTE #3 (PB3)	PROM BYTE #3 (PB3)
0CH	PROM BYTE #4 (PB4)	PROM BYTE #4 (PB4)
0DH	PROM BYTE #5 (PB5)	PROM BYTE #5 (PB5)
0EH	PROM BYTE #6 (PB6)	PROM BYTE #6 (PB6)
0FH	PROM BYTE #7 (PB7)	PROM BYTE #7 (PB7)

9.6 Write Network ID Back To EEPROM

The programmer has two approaches to store Network ID back to EEPROM. They are:

1. Store Network ID only
2. Store Configuration and Network ID at the same time

For case 1, the following procedure should be followed exactly:

```
ID_STORE ( )  {
      Program_to_new_page_0 ( ) ;            / / See Register description
      if (necessary) Modify_PROM_Byte0_5 ( )  ;
      Program_to_new_page_1 ( ) ;            / / See Register description
      write (HCMR, '16H')  ;                 / / Issue IDWCMD
      value = Read (HCMR)  ;
      while  (value & IDWCMD)  {
           value = Read (HCMR)  ;
           wait ( )  ;
      }
      write (HCMR, '00H')  ;                 / / Back to Normal mode
}
```

The following pseudo C code algorithm is for case 2:

```
ALL_STORE ( )  {
      Program_to_new_page 0 ( )  ;           / / See Regsiter description
      if (necesary) Modify_PROM_BYTE0_7 ( )  ;
      Program_to_new_Page_1 ( )  ;           / / See Register description
      write (HCMR, '20H')  ;                 / / Enable All Write algorithm
      EEPROM_STORE ( )  ;                    / / Call EEPROM_STORE subroutine}
```

Note:Only PROM byte 0-7 will be written back to EEPROM when ALL_STORE() is issued.

9.6.1 7 IO BASES SUPPORTED

300H (18H) -> 240H (22H) -> 280H (34H) -> 2C0H (46H) -> 320H (59H) -> 340H (64H) -> 360H (0BH) -> 300H -> (18H) (CYCLIC)

9.6.2 15 IO BASES SUPPORTED

300H (18H) -> 240H (22H) -> 280H (34H) -> 2C0H (46H) -> 320H (59H) -> 340H (6AH) -> 360H (7BH) -> 380H (8CH) ->3A0H (9DH) -> 3C0H (AEH) -> 3E0H (BFH) -> 200H (C0H) -> 220H (D1H) -> 2A0H E5H) -> 2EH (07H) -> 300H (18H) (CYCLIC)

9.7 MULTIPLE LAN CARD AUTO CONFIGURATION

In case it is necessary for system to have more than one LAN cards plugged, the MX98905 provides a powerful solution to resolve "Multiple LAN card IO base conflict problem". It is not necessary for users to plug one LAN into the system then configure the IO base of the LAN card; then remove the first LAN card which is already configured and proceeds the second LAN card and so forth. Using MX98905, user can plug mutiple LAN cards into the system at the same time and then use software to configure these LAN cards for themselves.

To simply the mutiple LAN card auto configuration's operation, the MX98905 provides a bit, MULTI, in the HCMR. When this bit is set to 1, all LAN cards which use MX98905 will be forced to change to IO map (i.e. Novell NE2000 compaible). The "ID guess state machine" inside the MX98905 will be enables after MULTI bit is enabled. After that, software can write a certain value (will be explained in more detail in the following sub_ section) into the MX98905 by consecutive 4 write to port 378H. The following shows an example (in 8088 assembly code) for writting this certain value into MX98905:

```
mov     dx, 378
mov     al, CERTAIN_VALUER
out     dx, al
out     dx, al
out     dx,al
out     dx,al
```

When this certain value "hits" the 5th Network I.D. (the least significant byte), then IO base of this "ID hit" LAN card will be locked by MX98905 itself. i.e when writting 1 to AUTO, the IO base will not be changed.

By the way, when the guessed value is hit the Network I.D., a register call SIGNATURE (with value 78H, 'x') will be realeased by MX98905. If software can properly read the contents of SIGNATURE and ASR, then a conflit free IO base is found. If software can't access the value of SIGNATURE but ASR, then the guessed value is wrong. If software can't access the value of SIGNATURE nor ASR, then MX98905(s) is conflict with other add_on cards. In case SIGNATURE can be accessed by software, then user can write 1 to LOCKE bit of HCFR through port "NONCONFLICT_IOBASE+08H". The IO base of this LAN card will be locked all the time to prevent it from jumpping to other IO base when AUTO is issued. See application notes or call SE/FAE if you have any questions.

To faciliate one to understand the "Mutiple LAN card auto configuration ", an example is shown below: (Follow the steps shown in application note)

Condition : One LAN card with network ID 001111001001

: The second LAN card with network ID 0022220308

1. At the beginning, software first write AUTO. The IO base of both LAN card will be changed from their current IO bases to 300H.
2. Software guesses 00H, then write AUTO. Because the guessed I.D. (SID) hits the network I.D. on both LAN card, the IO bases of these two LAN cards will jump to 240H (assume software choose 7 IO bases)
3. Software guesses 01H, then issue AUTO. The software guessed I.D. (SID) hits the network I.D. (HID) of the first card, hence the IO base of the first card will stay at 240H and the IO base of the second card jumpped to 280H. Software can access "x" (78H,SIGNATURE register) from IO base 248H.
4. Software write 1 to LOCKE bit to lock the first card.
5. Software keep guessing and writing 1 to AUTO. Finally, a value, 08H, is guessed by software, and the IO base of card #2 jump to 240H. Because 240H is conflict with card #1, user can only access the value of ASR butSIGNATURE.
6. Software keep guessing and writing 1 to AUTO. The IO base of card #2 change from 240H to 280H.
7. User can access SIGNATURE and ASR from this IO base, the conflit_free IO base for card #2 is found.

Note : MX98905 uses one byte (ID byte #5) to determine SID is matched with HID or not, therefore, there is 1/256 posibility for 2 LAN cards get hit simultaneously.

The internal state machine will be reset after EEPROM_STORE is finished.

This algorithm is preliminary. For actual implementation, user can contact with our FAE by calling 886-02-7191977 for details.

10. TWISTED-PAIR INTERFACE (TPI) MODULE

The TPI has five main logical functions:

1. The Smart Squelch is responsible for determining when valid data is present on the differential receive inputs RXIP and RXIM

2. The Collision function checks for simultaneous transmission and reception of data on the TXOP, TXOM, RXIP and RXIM.

3. The Link Detector/Generator checks the integrity of the cable connecting the two twisted-pair MAUs.

4. The Jabber disables the transmitter if it attempts to transmit a longer-than-legal packet.

5. The TX Driver & Pre-emphasis transmit Manchester-encoded data to the twisted-pair network via the summing resistors and transformer/filter.

11. SMART SQUELCH

To make sure that impulse noise on the receive inputs will not be mistaken for a valid signal, the ENC carries out an intelligent receive squelch on the RX± differential inputs. The squelch circuitry uses a mix of amplitude and timing measurements.

Smart squelch checks the signal at the start of packet and any pulses that do not exceed the squelch level, either positive or negative, depending on polarity, is rejected. After this first squelch level is overcome the opposite squelch level must be exceeded within 150 ns. Finally, the signal goes beyond the original squelch level within a further 150 ns in order for the input waveform not to be rejected. The procedure entails the loss of at least three bits at the start of each packet.

When these conditions are satisfied a control signal will be generated to show the remainder of the circuitry that valid data is present. Then the smart squelch circuitry is reset.

Valid data is deemed present until either squelch level has not been generated for a time longer than 150 ns, which shows End of Packet. If good data is detected, the squelch levels are reduced to contain the noise effect which may lead to premature End-of-Packet detection.

12. COLLISION

A collision is detected by the TPI module when the receive and transmit channels are active simultaneously. If the TPI is receiving when a collision is detected it is reported to the controller immediately. If, however, the TPI is transmitting when a collision is detected the collision is not reported until seven bits have been received while in the collision state. This prevents a collision from being reported incorrectly due to noise on the network. The signal to the controller remains for the duration of the collision.

Approximately 1ms after the transmission of each packet a signal called the Signal Quality Error (SQE) consisting of typically 10 cycles of 10 MHz is generated. This 10 MHz signal, also called the Heartbeat, ensures the continued functioning of the collision circuitry.

13. LINK DETECTOR/GENERATOR

This is a timer circuit that generates a link pulse as shown in the 10BASE-T specification. With a width of 100 ns, the pulse is transmitted every 16 ms on the TXO+ output in the absence of transmit data.

The pulse checks the integrity of the connection to the remote MAU, and the link detection circuit checks for valid pulses from the remote MAU. The link detector will disable the transmit, receive, and collision detection functions if valid link pulses are not received.

To determine that a good twisted-pair link exists, the GDLNK output directly drives an LED; the LED will be on during normal conditions.

14. JABBER

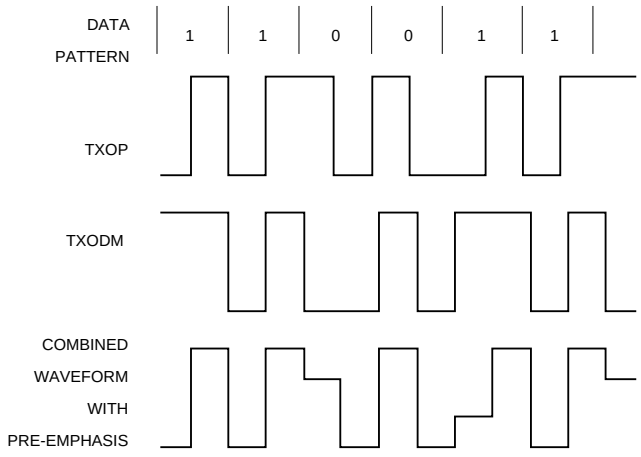
Whenever the transmitter is active for greater than 52 ms, the jabber timer monitors the transmitter and disables the transmission. In this case, the transmitter is then disabled for the time that ENDEC module's internal transmit enable is asserted. This signal has to be deasserted for about 750 ms before the jabber re-enables the transmit outputs.

15. TRANSMIT DRIVER

The transmitter has four signals, the true and complement Manchester-encoded data (TXOP and TXOM). These signals may be delayed by 50 ns (TXODP and TXODM).

These four signals are combined, TXOP with TXODM and TXOM with TXODP. Known as digital pre-emphasis, this process is required to compensate for the twisted-pair cable which acts like a low-pass filter and can greatly weaken the 10 MHz (50 ns) pulses of the Manchester-encoded waveform than the 5 MHz (100 ns) pulses.

A combination of these signals is shown below:



16. STATUS INFORMATION

This information is shown at the ENC on the CRS/RX, TXE/TX, COL and POL outputs as decribed in the pin description table. These outputs can drive status LEDs by means of an appropriate driver circuit.

Normally low, the POL output will be driven high when seven consecutive link pulses or three consecutive link pulses having reversed polarity are detected. A wiring error at either end of the TPI cable can cause polarity reversal. Upon detection of this reversal the condition is latched and POL is asserted. Correcting this error is the TP1 and will also decode received data correctly, thus getting rid of the need to check the wiring error.

17. MANCHESTER ENCODER AND DIFFERENTIAL DRIVER

On the transformer's secondary, the differential transmit pair drives up to 50 meters of twisted-pair AUI cable. These outputs are source followers requiring two 270W pulldown resistors to ground.

18. MANCHESTER DECODER

This decoder is composed of a differential receiver and a PLL to separate a Manchester-decoded data stream into internal clocks signals and data. When using the standard 78W transceiver drop cable, see that the differential input must be externally terminated with two 39W resistors connected in series. These resistors are optional in Thin Ethernet applications. A squelch circuit at the input rejects signals with levels less than -175 mV to prevent noise from triggering the decoder. And signals negative than -300 mV are decoded; data becomes valid within 5 bit times. The MX98905 may be able to take bit jitter up to 18 ns in the data that is received.

19. COLLISION TRANSLATOR

If the Ethernet transceiver, when in AUI mode, detects a collision, it generates a 10 MHz signal to the differential collision inputs (CDP and CDM) of the MX98905. When these inputs are active, the MX98905 uses this signal to cancel its current transmission and reschedule another one.

The collision differential inputs are ended in the same way as the differential receive inputs. The squelch circuitry is also similar, rejecting pulses with levels less than -175 mV.

20. RECEIVE DESERIALIZER

The receive deserializer starts to work when the input

signal Carrier Sense is asserted. It allows incoming bits to be shifted into the shift register by the receive clock provided by the SNC (Serial Network Converter). The serial receive data is also routed to the CRC generator/checker to detect CRC code. The receive deserializer includes a synch detector that detects the SFD (Start of Frame Delimiter) to establish where byte boundaries within the serial bit stream are located, i.e., when a 1,1 bit sequence is detected, it begins to collect data. After every eight receive clocks, the byte-wide data is transferred to the 16-byte FIFO (two 8-byte FIFOs) alternatively and the receive byte count is incremented. The first six bytes after the SFD are checked for valid comparison by the Address Recognition Logic. If the address recognition Logic does not recognize the packet, the FIFO is cleared.

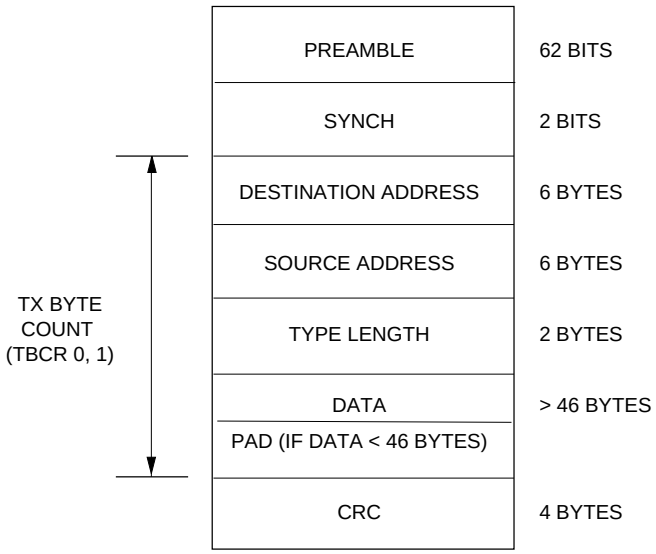
21. ADDRESS RECOGNITION LOGIC

The address recognition logic compares the destination address field (first 6 bytes of the received packet) with the physical address registers stored in the address register array, one byte at a time, by the 8th receive clock. If any one of the six bytes does not match the pre-programmed physical address, the protocol PLA rejects the packet. This means that the packet does not belong to the node. All multicast destination addresses are filtered using a hashing technique by latching the 6 most significant bits of the CRC generator. If the multicast address indexes a bit that has been set in the filter bit array of the multicast address register array, the packet is accepted. Otherwise, it is rejected by the Protocol PLA. Each destination address is also checked for all 1's, which is the reserved broadcast address.

22. PACKET TRANSMISSION

A complete transmit packet consists of Preamble, Synch, Data, and CRC fields. The data field is a contiguous assembled packet of Destination Address. Source Address, Length Field, and Data with the format are shown below. During transmit, Page Start Address Register (TPSR) and the Transmit Byte Count Registers (TBCR0,1), control the DMA transfer. As a transmit command is issued to ENC, the packet of data in buffer memory pointed 0 by these registers will be moved into the FIFO. The ENC will generate and append the preamble, synch and CRC fields. In addition, if transmitting data is smaller than 46 bytes, the packet must be padded to a minimum size of 64 bytes. The programmer is responsible for adding and stripping pad bytes.

GENERAL TRANSMIT PACKET FORMAT



23. CONDITIONS REQUIRED TO BEGIN TRANSMISSION

To initiate transmission of a packet, the TPSR (Transmit Page Start Register) and TBCR0, TBCR1 (Transmit Byte Count Registers) must be initialized and the TXP bit in the Command Register must be set. The ENC will start to prefetch transmit data from memory, if no reception is currently receiving. Three conditions must be met before transmission:

1. The Interframe Gap Timer has timed out the first 6.4ms of the Interframe Gap.

2. At least one byte has entered the FIFO, which means that burst transfer has begun.

3. If collision occurs in the ENC, the backoff timer must expire before retransmit.

If carrier sense is asserted before a byte has been loaded into the FIFO, the ENC will become a receiver.

24. COLLISION RECOVERY

If transmission has collided with another station, the buffer management logic, which monitors the transmit circuitry will reset the FIFO and restore the Transmit DMA pointers for retransmission of the packet. When collision is detected, the COL bit in TSR will be set and the NCR (Number of Collisions Register) will be incremented. If each of the 15 retransmissions results in a collision, the transmission will be terminated and the ABT bit in the TSR will be set. If excessive collisions (i.e., 16 consecutive collisions) are encountered, NCR reads as zeros and transmission is aborted.

25. TRANSMIT PACKET ASSEMBLY FORMAT

The following diagrams show the format for assembling packets before they are transmitted for different byte- ordering schemes. The various formats are selected in the Data Configuration Register.

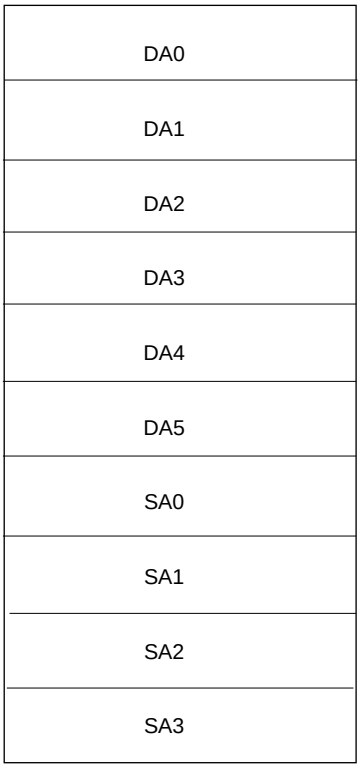
DA = Destination Address
SA = Source Address
T/L = Type/Length Field

BOS = 0, WTS -1 in Data Configuration Register. This format used with Series 32000, 808X-type processors.

BIT	D15 – D8	D7 – D0
	DA0	DA1
	DA2	DA3
	DA4	DA5
	SA0	SA1
	SA2	SA3
	SA4	SA5
	T/L0	T/L1
	DATA0	DATA1

BOS = 1, WTS = 1 in Data Configuration Register. This format is used with 68000-type processors.

BIT	D15 – D8	D7 – D0
	DA1	DA0
	DA3	DA2
	DA5	DA4
	SA1	SA0
	SA3	SA2
	SA5	SA6
	T/T1	T/L0
	DATA1	DATA0

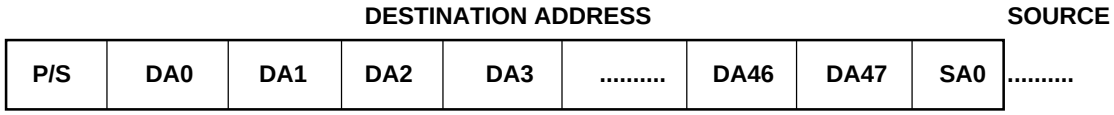


BOS = 0, WTS = 1 in data Configuration Register.
This format is used with general 8-bit CPUs.

26. PHYSICAL ADDRESS REGISTERS (PAR0-PAR5)

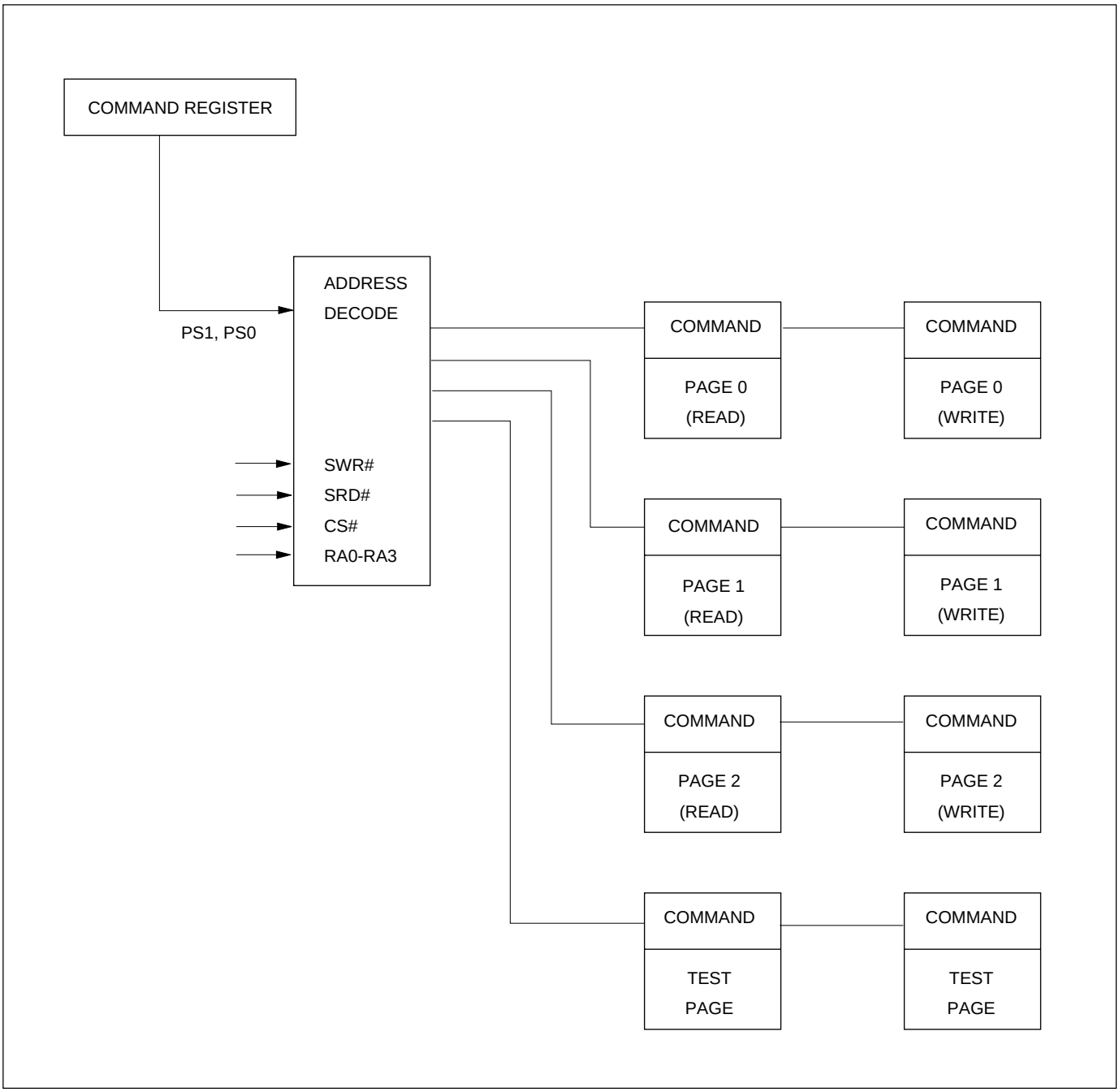
The physical address registers are used to compare the destination address of incoming packets for rejecting or accepting packets. It compares physical addresses in PAR0-PAR5 with incoming data one byte at a time. The bit assignment shown below relates the sequence in PAR0-PAR5 to the bit sequence of the received packet.

	D7	D6	D5	D4	D3	D2	D1	D0
PAR0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
PAR1	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
PAR2	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16
PAR3	DA31	DA30	DA29	DA28	DA27	DA26	DA25	DA24
PAR4	DA39	DA38	DA37	DA36	DA35	DA34	DA33	DA32
PAR5	DA47	DA46	DA45	DA44	DA43	DA42	DA41	DA40



NOTE: P/S = Preamble, Synch
DA0 = Physical/Multicast Bit

REGISTER ADDRESS MAPPING



27. DIRECT MEMORY ACCESS CONTROL (DMA)

The DMA capabilities of the ENC greatly simplify use of the MX98905 in typical configuration. The local DMA channel transfers data between FIFO, which is inside the ENC, and memory which is outside the ENC. There are two kinds of local DMA type: Local DMA Read and Local DMA Write. Local DMA Read moves data from memory into FIFO on transmission. Should a collision occur (up to 15 times), the packet is retransmitted with no processor intervention. Local DMA Write transfers data from FIFO to memory on reception.

A remote DMA channel is also provided on the ENC to accomplish transfers between a buffer memory and a system memory whenever the I/O map board design is required. The two DMA channels (local DMA and remote DMA) can alternatively be combined to form a single 32-bit address with 8- or 16-bit data.

28. DUAL DMA CONFIGURATION

Network activity is isolated on a local bus, where the ENC's local DMA channel performs burst transfers between the buffer ring and the ENC's FIFO. The remote DMA transfers data between the buffer ring and the host memory by means of a bi-directional I/O port. Meanwhile, remote DMA provides local addressing capability and is used as a slave DMA by the host. Host side addressing must be provided by a host DMA or the CPU. The ENC allows Local and Remote DMA operations to be interleaved because the ENC takes care of the bus arbitration problem itself.

29. INTERNAL REGISTERS

All internal registers are mapped into three pages and selected by two bits, PS1 and PS0, of Command Register. Input pins RA0-RA3 are used to address these internal registers which are 8-bit wide and are commonly accessed during ENC register read/write operation. For user's convenience, registers that are commonly accessed during ENC operation are mapped into page 0. Page 1 registers are used primarily for initialization while Page 2 registers are used for diagnostics. Partitioned registers make one write/read cycle possible for accessing those commonly used registers.

REGISTER DESCRIPTIONS

1. ENHANCED FEATURE NEW PAGE REGISTER ADDRESS ASSIGNMENT

NEW PAGE 1 ADDRESS ASSIGNMENT FOR I/O MAP

SA00..3	READ	WRITE
00H	Reserved	Reserved
01H	Reserved	Reserved
02H	Reserved	Reserved
03H	Reserved	Reserved
04H	Reserved	Reserved
05H	Reserved	Reserved
06H	Reserved	Reserved
07H	Reserved	Reserved
08H	Signature (x, 78H)	Reserved
09H	Hidden Config. (HCFR)	Hidden Config. (HCFR)
0AH	Hidden Command (HCMR)	Hidden Command (HCMR)
0BH	Reserved	Reserved
0CH	Configuration C (CC)	Configuration C (CC)
0DH	Reserved	Reserved
0EH	AutoStatus Reg. (ASR)	Reserved
0FH	Reserved	Reserved

NEW PAGE 1 ADDRESS ASSIGNMENT FOR MEMORY MAP

SA0..4	READ	WRITE
10H	Reserved	Reserved
11H	Reserved	Reserved
12H	Reserved	Reserved
13H	Reserved	Reserved
14H	Reserved	Reserved
15H	Reserved	Reserved
16H	Reserved	Reserved
17H	Reserved	Reserved
18H	Signature (x, 78H)	Reserved
19H	Hidden Config. (HCFR)	Hidden Config. (HCFR)
1AH	Hidden Command (HCMR)	Hidden Command (HCMR)
1BH	Reserved	Reserved
1CH	Configuration C (CC)	Configuration C (CC)
1DH	Reserved	Reserved
1EH	AutoStatus Reg. (ASR)	Reserved
1FH	Reserved	Reserved

Data Transfer ports and Reset port are always accessible no matter what the value of NPGEN and PGSEL is in I/O map design.

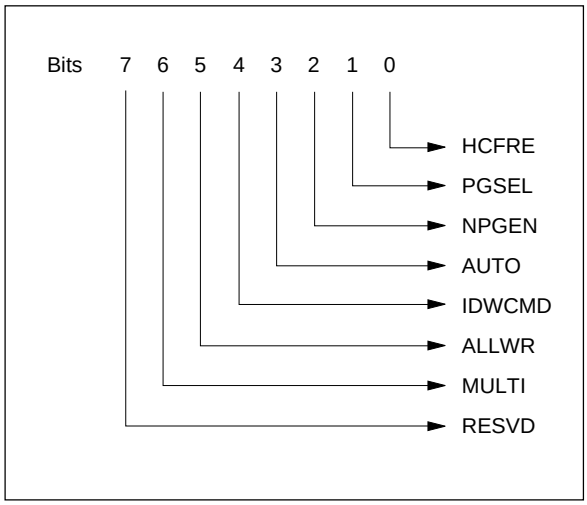
2. ENHANCED FEATURE REGISTERS

2.1 HIDDEN COMMAND REGISTER (R/W) (HCMR)

This register controls all the functions provided in enhanced mode. It can always be accessed by consecutive 2 writes to port 278H, followed by 2 consecutive 2 writes to port 378H, i.e., write ports : 278H Æ 278H Æ 378H Æ 378H (when I/O Base not sure)

After the I/O base is determined (see functional description), this register can be accessed by one I/O instruction using the address assignment shown in provious section.

NOTE: Don't write this register through Base+0AH/ Base+1AH (I/O/MEM) except it is confirmed that I/O base does not conflict with other ADD_on card.



HIDDEN COMMAND REGISTER (R/W) (HCMR)

SYMBOL	BIT	DESCRIPTION
HCFRE	D0	Register HCFRE Enable. Power on low. 0 : Disable HCFR. 1 : Enable HCFR. When user issues EESTORE in Configuration Register B, contents in figh byte of OFH of EEPROM. Whcih is reserved at
NPGEN,PGSEL	D2,D1	New Page Enable/Page Select. Power on low. 0X: Normal Mode. User can access controller's internal registers. 10 : User can access IDPROM through IOBASE + 00..OFH in I/O map. See table 4 for your reference. 11: New Page 1 selectsd. User can access HCMR, CC, ASR and SIGNATURE. See "New Page 1 address assignment for I/O map" and "New Page 1 address assignment for Memory map " for more detail information. Make sure set NPGEN to 0 before normal operation. Data port and Reset port in I/O map are accessible no matter what the value of NPGEN and PGSEL are.
AUTO	D3	Auto Jump to Next I/O base. Power on low. 0 : Write a 0 to this bit has no effect.1 : Write an 1 to this bit will cause I/O base auto jump follow the sequence described in section 9.5- - Auto Configuration. In multiple LAN cards auto configuration's application (see section 9.5), if SID hits the HID, then write an 1 to this bit has no effect. The first time writing an 1 to AUTO will cause IO base change to 300H no matter what the current IO base is. Whenever AUTO is issued, the value of IOAD2..0 in CA and PAGE in HCFR will be updated automatically by the state machine inside the MX98905. Either 7 or 15 IO bases should be determined before AUTO is issued to prevent the internal state machine getting confused. Any IORDL signal activates will reset this bit.
IDWCMD	D4	IDPROM Write Command. Power on low. 0 : Write a 0 to this bit has no effect. 1 : The MX98905 will write the first 4 words of PROM data (Net work I.D., Boardtype and Checksum) back to EEPROM when this bit is set. When the operation is completed, this bit will be reset by MX98905 itself. Don't write an 1 to this bit and EESTORE of CB simultaneously, this will cause internal state machine malfunction.
ALLWR	D5	Write CA, CB, CC, HCFR, The entire PROM content back to EEPROM. Power on low. 0 : Only CA, CB, CC and HCFR are written back to EEPROM when EESTORE bit of CB is set to 1. 1 : CA, CB, CC, HCFR, and the entire PROM content will be writtenback to EEPROM when EESTORE bit is set to 1. If new Network I.D. is necessary, make sure I.D. is updated before this bit–is set and before EESTORE bit is set to1, the following write sequence will be followed after EESTORE bit is set to 1, CA, CB -> CC, HCFR -> IDO, IDI -> ID2, ID3 -> ID4, ID5 -> and the rest of the content in PROM.

HIDDEN COMMAND REGISTER (R/W) (HCMR)(Continued)

SYMBOL	BIT	DESCRIPTION
MULTI	D6	Enable Multiple LAN card Auto Configuration 0 : Disable consecutive 4 writes to port 378H (SID buffer) . 1 : The MX98905 will be forced to I/O map, i.e. MEMIO of CA will be forced to zero. Consecutive 4 writes to port 378H will be enabled. When a 0 is written to this bit, the MX98905 will change to its original mode (I/O or memory).
RESVD	D7	Reserved. Power on low.

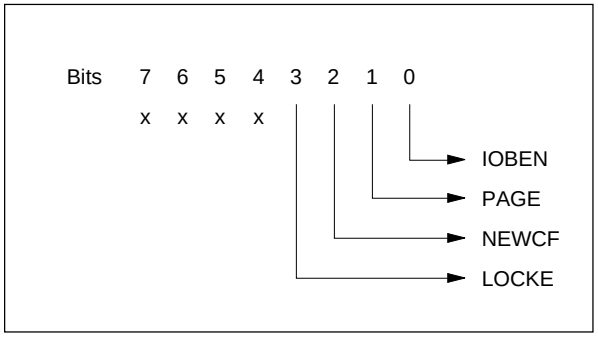
Note : HCMR can always be accessed by writing to port 278H and 378H(follow the certain sequence described above). Remember not to access this register through direct IO access unitl a conflict _free I/O base is found.

2.2 HIDDEN CONFIGURATION REGISTER (R/W) (HCFR)

This register controls all the functions provided in enhanced mode. It can always be accessed by consecutive 2 writes to port 278H, followed by 2 consecutive 2 writes to port 378H, i.e., write ports : 278H Æ 278H Æ 378H Æ 378H (when I/O Base not sure)

After the I/O base is determined (see functional description), this register can be accessed by one I/O instruction using the address assignment shown in provious section.

NOTE: Don't write this register through Base+0AH/ Base+1AH (I/O/MEM) except it is confirmed that I/O base does not conflict with other ADD_on card.



2.2 HIDDEN CONFIGURATION REGISTER (R/W) (HCFR)(Continued)

SYMBOL	BIT	DESCRIPTION
IOBEN	D0	**I/O BASE ENABLE.** Power-on low 0 : 7 I/O base (compatible with DP83905) 1 : 15 I/O bases
PAGE	D1	**PAGE SELECT FOR I/O BASE.** Power-on low only valid when IOBEN and HCFRE of HCMR is high 0 : I/O base address are the same as IOAD2..0 of Configuration A 1 : I/O base address are redefined (see I/O Base support for more detail). This bit will be updated automatically according to the sequence of AUTO configuration when IOBEN is set.
NEWCF	D2	**NEW CONFIGURATION LOADED TO CA, CB AND CC AFTER EESTORE IS EXECUTED.** Power-on low 0 : New configuration will not be loaded to CA, CB and CC after EESTORE algorithm is executed. Compatible with DP83905. 1 : New Configuration will be loaded to CA, CB and CC after EESTORE algorithm is completed. Enhanced feature.
LOCKE	D3	**LOCK ENABLE.** I/O base will not be changed when AUTO of HCMR is written into. Power-on low. 0 : Enable internal LOCK bit. Write 1 to AUTO will change I/O base 1 : Enable internal LOCK bit. Write 1 to AUTO will not change I/O base. When this bit is set, AUTO of HCMR has no effect. User CANNOT read the value of Signature Register. After I/O base is determined (see Multi_lan card conflict free for more detail), this bit should be programmed through base+09H for I/O map or Base+19H for shared memory map.

These four bits (IOBEN, PAGE, NEWCF and LOCKE) can be loaded/stored from/to EEPROM.

RESV4..1 --- Reserved bits for future use.

Note: Don't write this register through Base+09H/ Base+19H except it is confirmed that I/O Base does not conflict with other Add_on card.

2.3 SIGNATURE FOR MULTI_BOARD AUTO CONFIGURATION (R) (SGN)

This register is only used in multi_LAN card auto configuration. It is readable only when the LSB of Network ID programmed by user is matched with the contents of ID5 of PROM.

- Read port : Base + 08H/Base + 18H (I/O/ MEM)
- Read condition
  NPGEN = 1
  PGSEL = 1
- The value of signature is 78H (ASCII code for 'x')

Note : Lock status will be reset after user has read the value of signature. User should exactly follow the algorithm provided in enhanced feature description for Multi_board Lan Card auto configuration. For user's convenience, we strongly recommend that he issues EESTORE after auto configuration is done.

2.5 AUTOSTATUS REGISTER (R) (ASR)

- Read port : Base + 0EH/Base + 1EH (I/O/ MEM)
- Read condition :
  NPGEN = 1
  PGSEL = 1

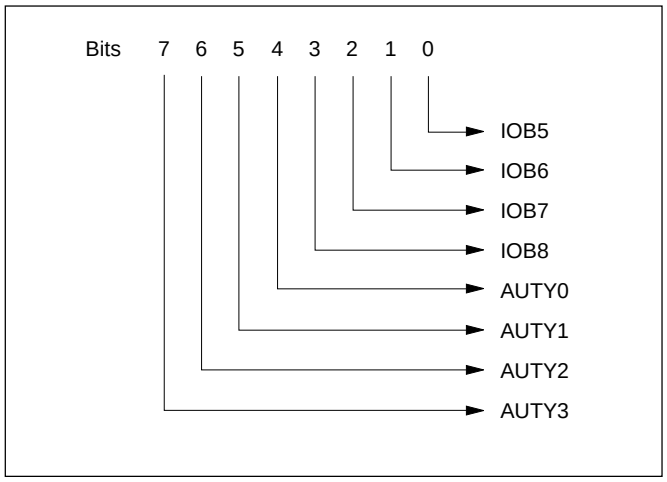
When 7 I/O bases are selected, the following value sequence will be shown on ASR whenever AUTO of HCMR is written into:

18 Æ 22 Æ 34 Æ 46 Æ 59 Æ 6A Æ 0B

When 15 I/O bases are enabled, the following sequence is available:

18 Æ 22 Æ 34 Æ 46 Æ 59 Æ 6A Æ 7B Æ 8C Æ 9D Æ AE Æ BF Æ C0 Æ D1 Æ E5 Æ 07

i.e., when AUTO is first written, the contents of ASR are 18H; if user writes AUTO again, the value of ASR changes from 18H to 22H, etc. This feature can be used in auto configuration to determine whether the I/O base of the LAN card is in conflict with the others.

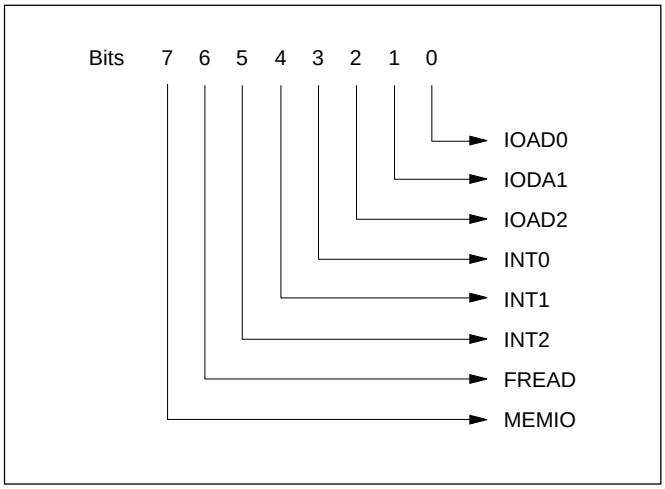


IOB8..5 : I/O base bit 8 to bit 5.
AUTY3..0 : States for Auto configuration state machine.

3. CONFIGURATION REGISTERS

3.1 CONFIGURATION REGISTER A (R/W) (CA)

This register can be accessed by reading 0AH of internal page 0 register followed by writing to that address. If other Read/Write takes place between the read and the write, then write to 0AH will access the Remote Byte Count Register 0.



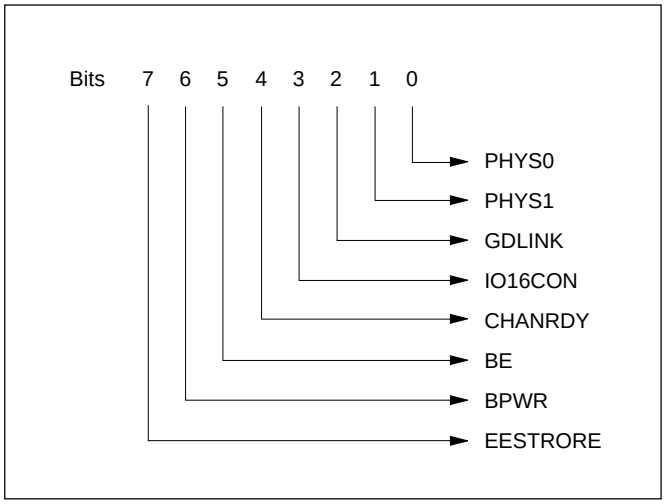
SYMBOL	BIT	DESCRIPTION
IOAD2-0	D0-D2	**I/O ADDRESS.** These three bits determine the base I/O address of the MX98905 controller when enhanced mode is disabled (NPGEN of HCMR is low). When the enhanced mode is enabled, the base I/O address will be determined by 5 bits, which are IOAD2-0 of CA, NPGEN and PGSEL of HCMR. See I/O base determination for details.
INT2-0	D3-D5	**INTERRUPT LINE USED.** Two interrupt modes are supported by the MX98905, which can be enabled by setting INTMOD of Configuration C. Direct Drive Mode : In this mode, an interupt output pin will be driven active on a valid interrupt condition (see ISR for more detail). Only one pin is driven in this mode depending on the following condition, the other three will remain TRI-STATE. **INT2 INT1 INT0 INTERUPT** X 0 0 INT0 X 0 1 INT1 X 1 0 INT2 X 1 1 INT3 Code Output Mode : INT3 is the active interrupt output while pins INT0-INT2 are programmable outputs reflecting the values on bits 3 to 5, i.e., when bits 3 and 4 of CA is high, then INT0, INT1 and INT3 are driven.

3.1 CONFIGURATION REGISTERS A (R/W) (CA) *(Continued)*

SYMBOL	BIT	DESCRIPTION
FREAD	D6	FAST READ. When this bit is set, the MX98905, in I/O mode, will begin next port fetch before system finishes reading the current data in data port. In slow ISA system, programming this bit may cause data corrupt in data port.
MEMIO	D7	MEMORY OR I/O MODE. When this bit is set to 0, I/O mode is selected. When it is set high, it is in shared memory mode.

3.2 CONFIGURATION REGISTER B (R/W) (CB)

This register can be accessed by reading 0BH of internal page 0 register followed by writing to that address. If other Read/Write takes place between the read and the write, then write to 0BH will access the Remote Byte Count Register 1. When loading from EEPROM during power-on reset, note that the value of EESTORE is always 0, i.e., the value of EESTORE can only be changed during Register Write operation.



SYMBOL	BIT	DESCRIPTION
PHYS0-1	D0-D1	**PHYSICAL LAYER INTERFACE.** **PHYS1** **PHYS0** **INTERFADCE** 0 0 TPI (10BASE-T compatible Squelch Level) 0 1 Thin Ethernet (10BASE2, THIN pin high) 1 0 Thick Ethernet (10BASE5, AUI port) 1 1 TPI (Reduced Squelch Level) The THIN pin can be used to enable the DC-DC converter required by 10BASE2 specification to provide electrical isolation.
GDLINK	D2	**GOOD LINK.** There are different definitions for this bit in Write and Read modes. Write Mode : Write 1 to this bit will disable the link pulse integrity test. Read Mode : When this bit is read, it indicates the link status, reflecting the value shown on the GDLINKL LED. 0 : A. The MX98905 is in AUI mode B. The MX98905 is in TPI mode, link enable, link bad 1 : A. Link disable B. The MX98905 is in TPI mode, link enable, link good

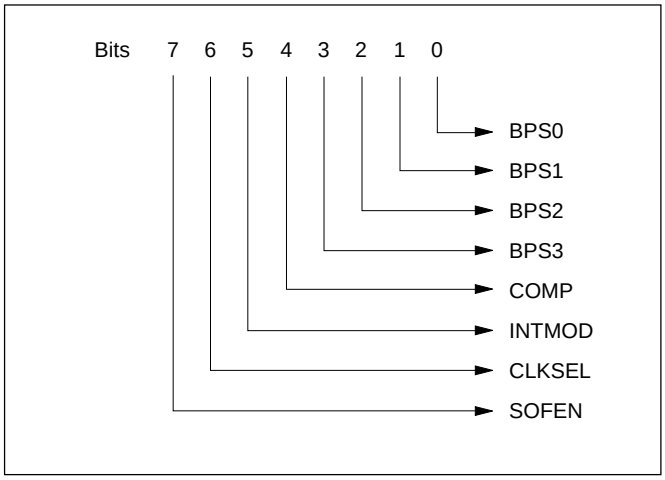
31 CONFIGURATION REGISTER B (R/W) (CB) (Continued)

SYMBOL	BIT	DESCRIPTION
IO16CON	D3	**IO16L CONTROL.** When this bit is set low, IO16L is generated only on address decode. When it is high, the MX98905 will generate IO16L after IORDL, or IOWRL go active.
CHANRD	D4	**CHRDY FROM IORDL OR IOWRL OR FROM BALE.** When this bit is set low, the MX98905 will generate CHRDY after the command strobe. When it is high, CHRDY will be generated by the MX98905 after BALE goes high.
BE	D5	**BUS ERROR.** This bit shows that the MX98905 has detected a bus error (the MX98905 attempts to insert wait state into a system access and the system terminates the cycle without monitoring the wait state). Writing a one to this bit clears it to zero, but writing a zero to this bit has no effect.
BPWR	D6	**BOOT PROM WRITE.** Write cycles will be generated to the boot PROM only when this bit is set high.
EESTORE	D7	**EEPROM STORE.** Writing a one to this bit enables the EEPROM STORE algorithm, as mentioned. This bit should not be configured to high either from switches or from an EEPROM. Note that this bit and IDWCMD of HCMR can't be set high simultaneously to prevent crashing the internal state machine of the MX98905.

3.3 HARDWARE CONFIGURATION REGISTER C (CC)

Access to Configuration Register C is allowed only in the MX98905 enhanced mode. This feature is not supported when the MX98905 is not programmed to new page 1.

- Read/write port : Base + 0CH/Base + 1CH (I/O/MEM)
- Read/write condition:
  NPGEN = 1
  PGSEL = 1



SYMBOL	BIT	DESCRIPTION
BPS0-3	D0-D3	BOOT PROM SELECT. Selects address and the size with which boot PROM begins. When the system reads within the selected memory area, the MX98905 reads the data in through MEMD0-7 and drives it onto the system data bus. The following are valid addresses and size provided by the MX98905:

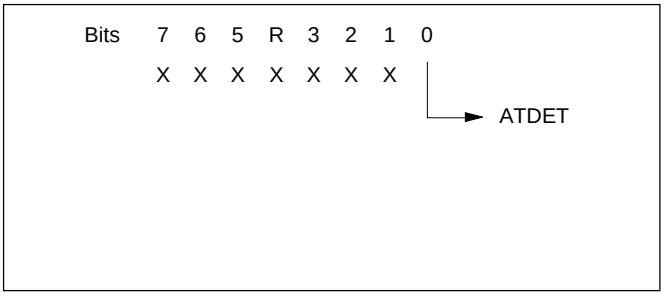
BPS3	BPS2	BPS1	BPS0	ADDRESS	SIZE (I/O SHARED MEMORY)
0	0	0	X	X	No boot prom
0	0	1	0	0C000H	8K/16K
0	0	1	1	0C400H	8K/16K
0	1	0	0	0C800H	8K/16K
0	1	0	1	0CC00H	8K/16K
0	1	1	0	0D000H	8K/16K
0	1	1	1	0D400H	8K/16K
1	0	0	0	0D800H	8K/16K
1	0	0	1	0DC00H	8K/16K
1	0	1	0	0C000H	32K/32K
1	0	1	1	0C800H	32K/32K
1	1	0	0	0D000H	32K/32K
1	1	0	1	0D800H	32K/32K
1	1	1	0	0C000H	64K/64K
1	1	1	1	0D000H	64K/64K

3.3 HARDWARE CONFIGURATION REGISTER C (CC) *(Continued)*

SYMBOL	BIT	DESCRIPTION
COMP	D4	**COMPATIBLE.** When this bit is low, the MX98905 is compatible with the EtherCard PLUS and Novell NE2000 boards. In compatible mode, only 16 kbytes RAM memory are accessible. When this bit is set high, full 64 kbytes of memory can be accessed.
INTMOD	D5	**INTERRUPT MODE.** When this bit is low, the MX98905 is in Direct Drive Interrupt mode. When it is high, Coded Output interrupt mode is selected.
CLKSEL	D6	**CLOCK SELECT.** If this bit is high, the MX9890 core is clocked by the input BSCLK pin. If it is low, the MX9890 core is clocked by the 20MHz clock from internal MCC module.
SOFEN	D7	**SOFTWARE ENABLE.** 0 : User can program Configuration Register A and B in software. 1 : CA and CB are not accessible.

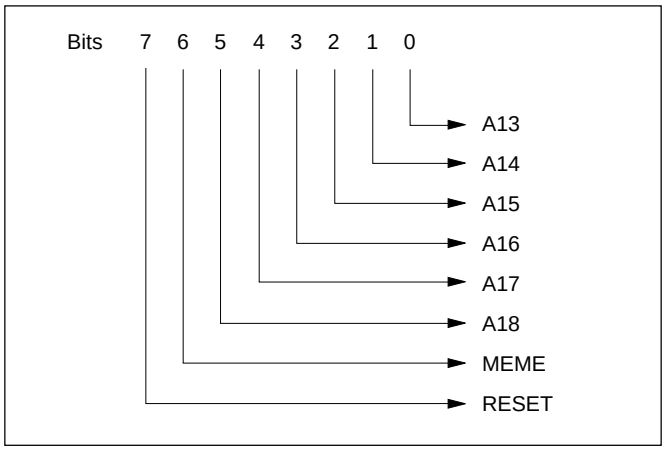
4. SHARED MEMORY MODE CONTROL REGISTERS

4.1 SHARED MEMORY AT DETECT REGSITER (R)



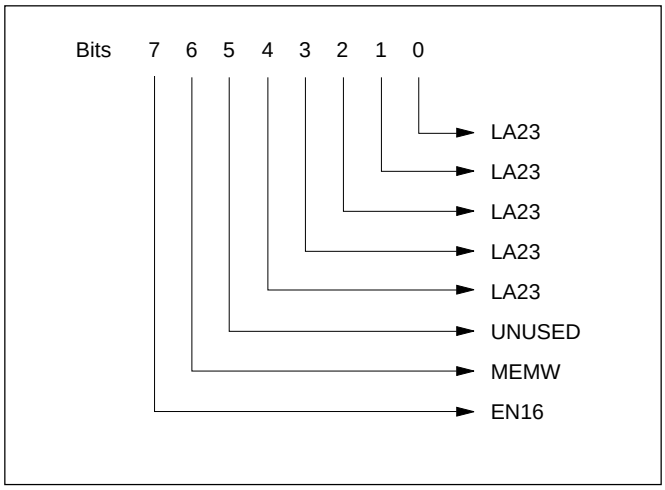
SYMBOL	BIT	DESCRIPTION
ATDET	D0	**AT DETECT.** This bit shows the value on the ATXT pin and can be accessed by software to determine whether the MX98905 is operating in an 8- or 16-bit slot. When this bit is high, the MX98905 is operating in a 16-bit slot.

4.2 SHARED MEMORY CONTROL REGISTER 1 (C1)



SYMBOL	BIT	DESCRIPTION
A13-18	D0-D5	**A13 TO A18.** Lower part of the address register used to determine the position of the memory of the MX98905 within the system memory map.
MEME	D6	**MEMORY ENABLE.** Enables external memory accesses when held high. Power-on low. To enable the memory into the system's memory map, the user must program the base memory address and set this bit high.
RESET	D7	**RESETS.** Resets the MX9890 core of the MX98905 controller.

4.3 SHARED MEMORY CONTROL REGISTER 2 (C2)



SYMBOL	BIT	DESCRIPTION
LA19-23	D0-D4	**LA19 TO LA23.** Upper part of the address register used to determine the position of the memory of the MX98905 within the system memory map.
MEMW	D6	**MEMORY WIDTH.** Sets width of external memory. When this bit is set high, external memory is accessed as word wide, i.e., in compatible mode, 16 kbytes are available and 64 kbytes are available in noncompatible mode (only when EN16 is set high also). When it is low, external memory is accessed as byte wide, so only 8 kbytes of memory are available in compatible mode and 32 kbytes of memory are available in noncompatible mode.
EN16	D7	**ENABLE 16 BIT.** Allow 16-bit system accesses to external memory when it is high. M16L output will be generated in this mode. When low, only 8-bit accesses are allowed, and M16L will stay high.

5. COMMAND REGISTER(CR) 00H (READ/WRITE)

The Command Register is used to take the controller on/ offline (STA and STP bits), initiate transmissions (TXP bit), enable or disable Remote DMA operations (RD2, RD1 and RD0 bits), and select register pages (PS1 and PS0). To issue a command, the microprocessor sets the corresponding bit(s). In addition, commands may be overlapped following the guidelines below:

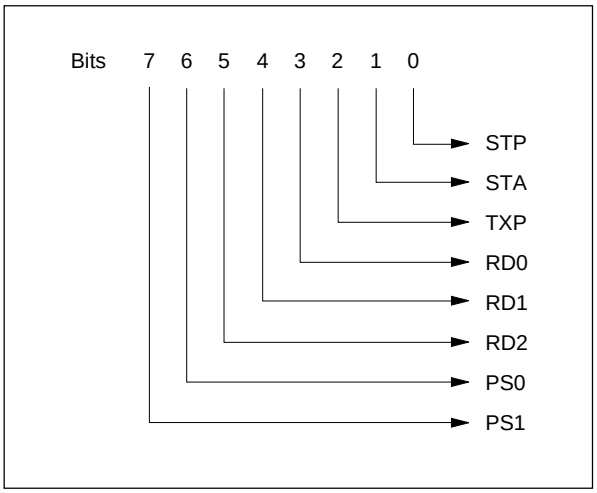
1. If a remote DMA operation overlaps a transmission, RD0, RD1 and RD2 must be written with the desired values, and a "0" or "1" may be written to the TXP bit, because writing a "0" to TXP has no effect after transmission is activated.

2. A remote write DMA may not overlap remote read operation and vice versa. Each operation must either be completed or aborted before starting the other one.

3. If a transmit command overlaps with a remote DMA operation, bits RD2, RD1 and RD0 must be maintained for the remote DMA command when setting the TXP bit.

NOTE: If a remote DMA command is reissued while giving the transmit command, the DMA will complete the process immediately if the remote byte count registers (RBCR1 and RBCR0) have not been reinitialized, i.e., user has to program RBCR0 and/or RBCR1 every time he needs remote DMA service.

4. Bits PS1, PS0, RD2 and STP can be set at any moment.

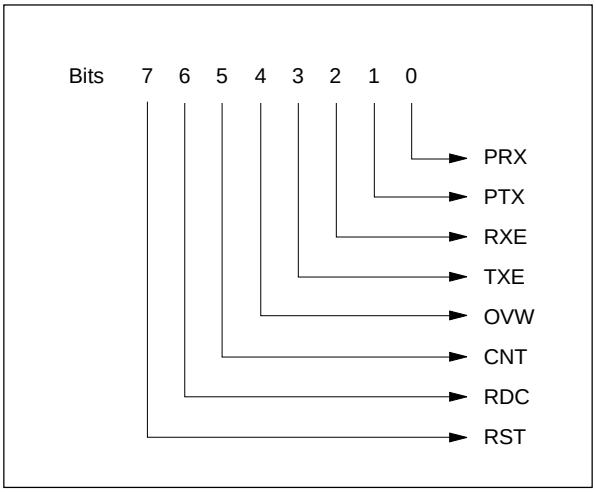


5. COMMAND REGISTERS (Continued)

SYMBOL	BIT	DESCRIPTION
STP	D0	**STOP**: Software reset command, takes the controller offline; no Packets will be received or transmitted if this bit is set high. Any reception or transmission in progress will enter the reset state after operation is completed. This bit must be cleared and the STA bit must be set high to exit the reset state. The software reset is executed only when the RST bit in the ISR is set to 1. STP powers up high. Note: If the ENC has previously been in start mode and the STP is set, both the STP and STA bits will remain set.
STA	D1	**START**: This bit is used to activate the ENC after either power-up, or when the ENC has been placed in a reset mode by software command or error. STA powers up low.
TXP	D2	**TRANSMIT PACKET**: This bit must be set to initiate transmission of a packet only after the Transmit Byte Count (TBCR1 and TBCR0) and Transmit Page Start register (TPSR) have been programmed. TXP is internally reset either after the transmission is completed or aborted.
PD0, PD1, PD2	D3, D4, D5	**REMOTE DMA COMMAND**: These three-encoded bits control operation of the Remote DMA channel. RD2 can be set to abort any Remote DMA command in progress. The Remote Byte Count Registers should be cleared by host whenever a Remote DMA has been aborted. The Remote Start Addresses are not restored to the starting address if the Remote DMA is aborted. Hence, for another remote DMA operaton, host should provide a starting address for ENC in order to operate correctly. **RD2 RD1 RD0** 0 0 0 Not Allowed 0 0 1 Remote Read 0 1 0 Remote Write 0 1 1 Send Packet 1 X X Abort/Complete Remote DMA (Note)
PS0, PS1	D6, D7	**PAGE SELECT**: These two-encoded bits select which register page is to be accessed with addresses RA0-3 **PS1 PS0** 0 0 Register Page 0 0 1 Register Page 1 1 0 Register Page 2 1 1 Reserved

6. INTERRUPT STATUS REGISTER (ISR) 07H (READ/WRITE)

This register is accessed by the host processor to determine the cause of an interrupt. Any interrupt can be masked in the Interrupt Mask Register (IMR). Individual interrupt bits are cleared by writing a "1" into the corresponding bit of the ISR. The INT signal is active as long as any unmasked signal is set; it will not go low until all unmasked bits in this register have been cleared. The ISR must be cleared after power-up by writing it with all 1's.



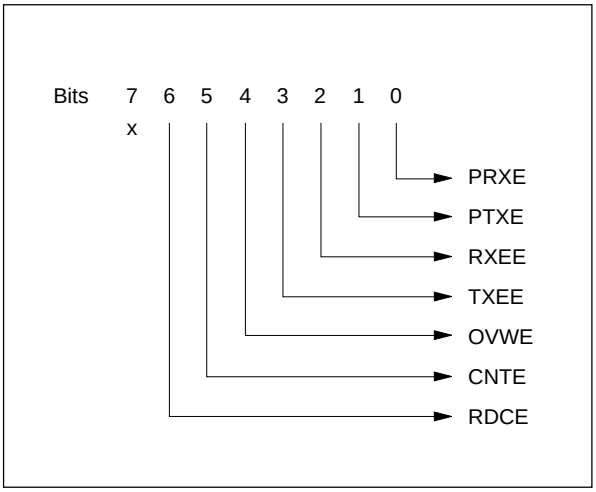
SYMBOL	BIT	DESCRIPTION
PRX	D0	**PACKET RECEIVED**: Indicates packet received with no errors.
PTX	D1	**PACKET TRANSMITTED**: Indicates packet transmitted with no errors.
RXE	D2	**RECEIVE ERROR**: Indicates that a packet was received with one or more of the following errors: - CRC Error - Frame Alignment Error - FIFO Overrun - Missed Packet
TXE	D3	**TRANSMIT ERROR**: Set when packet is transmitted with one or more of the following errors: - Excessive Collisions - FIFO Underrun
OVW	D4	**OVERWRITE WARNING:** Set when receive buffer ring storage resources have been exhausted. (Current Pointer has reached Boundary Pointer)

6. INTERRUPT STATUS REGISTER (ISR) 07H (READ/WRITE) *(Continued)*

SYMBOL	BIT	DESCRIPTION
CNT	D5	**COUNTER OVERFLOW**: Set when MSB of one or more of the Network Tally Counters has been set.
RDC	D6	**REMOTE DMA COMPLETE**: Set when Remote DMA operation has been completed.
RST	D7	**RESET STATUS**: Set when ENC enters reset state and cleared when a start command is issued to the CR. This bit is also set when a Receive Buffer Ring overflow occurs and is cleared when one or more packets has been removed from the ring. Writing to this bit has no effect. Note: This bit does not generate any interrupt; it is merely a status indicator.

7. INTERRRUPT MASK REGISTER (IMR) 0FH (WRITE)

The Interrupt Mask Register is used to mask interrupts. Each interrupt mask bit corresponds to a bit in the Interrupt Status Register (ISR). If an interrupt mask bit is set, an interrupt will be issued whenever the corresponding bit in the ISR is set. If any bit in the IMR is set low, an interrupt will not occur when the bit in the ISR is set. The IMR powers up all zeros.

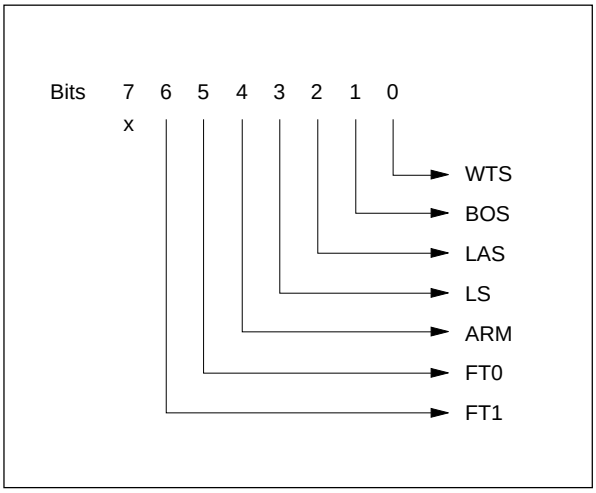


7. INTERRUPT MASK REGISTER (IMR) 0FH (WRITE) *(Continued)*

SYMBOL	BIT	DESCRIPTION
PRXE	D0	**PACKET RECEIVED INTERRUPT ENABLE** 0: Disables Interrupt when packet is received. 1: Enables Interrupt when packet is received.
PTXE	D1	**PACKET TRANSMITTED INTERRUPT ENABLE** 0: Disables Interrupt when packet is transmitted. 1: Enables Interrupt when packet is transmitted.
RXEE	D2	**RECEIVE ERROR INTERRUPT ENABLE** 0: Disables Interrupt when packet is received with error. 1: Enables Interrupt when packet is received with error.
TXEE	D3	**TRANSMIT ERROR INTERRUPT ENABLE** 0: Disables Interrupt when packet transmission results in error. 1: Enables Interrupt when packet transmission results in error.
OVWE	D4	**OVERWRITE WARNING INTERRUPT ENABLE** 0: Disables Interrupt when Buffer Management Logic lacks sufficient buffers to store an incoming packet. 1: Enables Interrupt when Buffer Management Logic lacks sufficient buffers to store an incoming packet.
CNTE	D5	**COUNTER OVERFLOW INTERRUPT ENABLE** 0: Disables Interrupt when MSB of one or more of the Network Statistics Counters has been set. 1: Enables Interrupt when MSB of one or more of the Network Statistics Counters has been set.
RDCE	D6	**DMA COMPLETE INTERRUPT ENABLE** 0: Disables Interrupt when Remote DMA transfer has been completed. 1: Enables Interrupt when Remote DMA transfer has been completed.
RESERVED	D7	**Reserved**

8. DATA CONFIGURATION REGISTER (DCR) 0EH (WRITE)

This register is used to program the ENC for 8- or 16-bit memory interface, select normal or loopback operation, select byte ordering in 16-bit application, and establish FIFO threshold. The DCR must be initialized prior to loading the Remote Byte Count Registers. LAS is set on power-up.



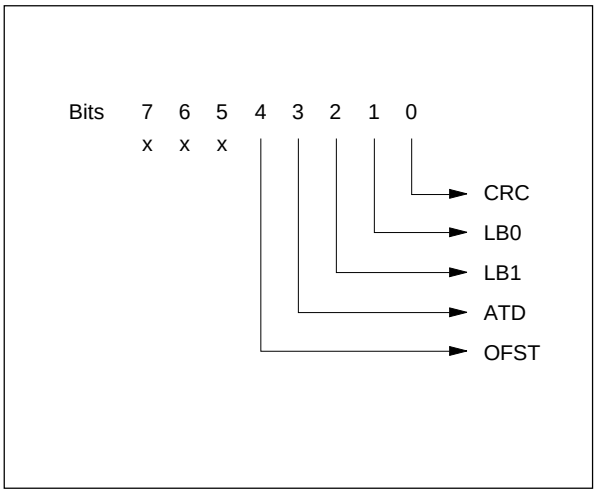
SYMBOL	BIT	DESCRIPTION
WTS	D0	**WORD TRANSFER SELECT** 0: Selects byte-wide DMA transfers 1: Selects word-wide DMA transfers WTS establishes byte or word transfer for both Remote and Local DMA transfers. Note: When word-wide mode is selected, up to 32K words are addressable; A0 remains low.
BOS	D1	**BYTE ORDER SELECT** 0: MS byte placed on AD15-AD8 and LS byte on AD7-AD0 (32000, 8086) 1: MS byte placed on AD7-AD0 and LS byte on AD15-AD8 (68000); ignored when WTS is low.
LAS	D2	**LONG ADDRESS SELECT** 0: Dual 16-bit DMA mode 1: Single 32-bit DMA mode When LAS is high, the contents of the Remote DMA Registers RSAR0, 1 are issued as A16-A31. Power-up high.

9. DATA CONFIGURATION REGISTER (DCR) 0EH (WRITE) *(Continued)*

SYMBOL	BIT	DESCRIPTION
LS	D3	**LOOPBACK SELECT** 0: Loopback mode select. Bits LB0, LB1 o f the TCR must be programmed for loopback operation. 1: Normal Operation. Ignore the values of LB1 and LB0 of TCR.
ARM	D4	**AUTO-INITIALIZE REMOTE** 0: Send Command not executed, all packets removed from Buffer Ring under program control. 1: Send Command executed, Remote DMA auto-initialize to remove packets from Buffer Ring Note: Send Command cannot be used with 68000-type processors and should be issued right after reception of packet is completed.
FT0, FT1	D5,D6	**FIFO THRESHOLD SELECT**: Encoded FIFO threshold; establishes point at which bus is requested when filling or emptying the FIFO. During reception, the FIFO threshold indicates the number of bytes (or words) the FIFO has filled serially from the network. During transmission, the FIFO threshold indicates the number of bytes (or words) the FIFO has filled from the Local DMA. Thus, the transmission threshold is 16 bytes less than the received threshold. Note: FIFO threshold setting determines the Local DMA burst length. RECEIVE THRESHOLDS **FT1 FT0 WORD WIDE BYTE WIDE** 0 0 1 word 2 bytes 0 1 2 words 4 bytes 1 0 4 words 8 bytes 1 1 6 words 12 bytes

10. TRANSMIT CONFIGURATION REGISTER (TCR) 0DH (WRITE)

Before transmission of a packet on the network, the Transmit Configuration Register is configured to establish the actions of the transmitter section of the ENC during transmission of a packet on the network. LB1 and LB0 select loopback mode power-up as 0.



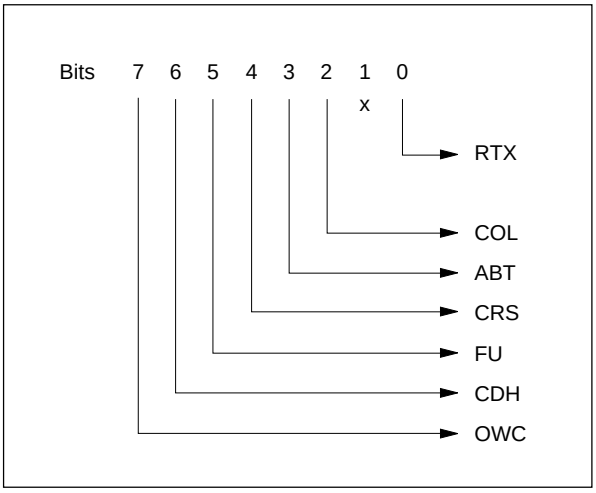
SYMBOL	BIT	DESCRIPTION
CRC	D0	**INHIBIT CRC** 0: CRC appended by transmitter 1: CRC inhibited by transmitter In loopback mode CRC can be enabled or disabled to test the CRC logic.
LB0, LB1	D1, D2	**ENCODED LOOPBACK CONTROL**: The type of loopback to be performed is determined by the following encoded bits. **LB1 LB2** Mode 0 0 0 Normal Operation Mode 1 0 1 Internal Loopback Mode 2 1 0 External Loopback to SNI Mode 3 1 1 External Loopback to TP
ATD	D3	**AUTO TRANSMIT DISABLE**: Setting this bit allows another station to disable the ENC's transmitter by transmission of a particular multicast packet. The transmitter can be re-enabled by resetting this bit, or by reception of a second particular multicast packet. 0: Normal Operation 1: Reception of multicast address hashing to bit 62 disables transmitter; reception of multicast address hashing to bit 63 enables transmitter.

11 TRANSMIT CONFIGURATION REGISTER (TCR) 0DH (WRITE) *(Continued)*

SYMBOL	BIT	DESCRIPTION
OFST	D4	**COLLISION OFFSET ENABLE**: This bit modifies the backoff algorithm to allow prioritization of modes. 0: Normal Backoff algorithm 1: Forces Backoff algorithm modification to 0 to 2 min (3+n, 10) slot times for first three collisions, then follows standard backoff.(For first three collisions station has higher average backoff delay making a low-priority mode.)
RESERVED	D5	**Reserved**
RESERVED	D6	**Reserved**
RESERVED	D7	**Reserved**

12. TRANSMIT STATUS REGISTER (TSR) 04H (READ)

Each particular bit of this register is set when the corresponding event occurs on the media during transmission of a packet. The contents of this register are not specified until after the first transmission and are cleared upon the start of the next transmission initiated by the host. A read of this register is necessary after each transmission.

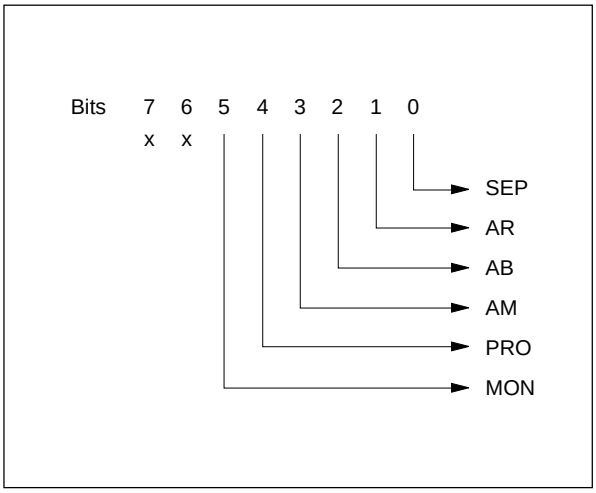


12. TRANSMIT STATUS REGISTER (TSR) 04H (READ) *(Continued)*

SYMBOL	BIT	DESCRIPTION
PTX	D0	**PACKET TRANSMITTED**: Set when transmitted without error. (No excessive collisions or FIFO underrun) (abt = "0", FU = "0")
	D1	**Reserved**
COL	D2	**TRANSMIT COLLIDED:** Set when transmission collided at least once with another station on the network. The number of collisions is recorded in the Number of Collisions Registers (NCR).
ABT	D3	**TRANSMIT ABORTED**: Set when transmission is aborted because of excessive collisions. (Total number of transmission attempts equals 16).
CRS	D4	**CARRIER SENSE LOST**: Set when carrier is lost during transmission of a packet. Carrier Sense is monitored from the end of Preamble/Synch until TXEN is dropped. Note that transmission is not aborted on loss of carrier.
FU	D5	**FIFO UNDERRUN**: Set when ENC cannot gain access of the bus before the FIFO empties. Transmission of the packet will be aborted.
CDH	D6	**CD HEARTBEAT**: Set when the transceiver fails to issue a collision signal after transmission of a packet. The Collision Detect (CD) heartbeat signal must commence during the first 6.4ms of the Interframe Gap following a transmission. In some collisions, however, the CD heartbeat bit will be set even when the transceiver is not performing the CD heartbeat test.
OWC	D7	**OUT-OF-WINDOW COLLISION**: Set when a collision occurred after a slot time (51.2ms). Transmission will not be aborted.

13. Receive Configuration Register (RCR) 0CH (WRITE)

This register determines what types of packets to be accepted and what mode the ENC will be in. The types include address type and error type. In the error type, when any one bit of SEP and AR is clear and the packet received matches the condition set in SEP or AR, the packet is rejected.



SYMBOL	BIT	DESCRIPTION
SEP	D0	**SAVE ERROR PACKETS.** 0: Packets with CRC and Frame Alignment errors are rejected. 1: Packets with CRC and Frame Alignment errors are accepted.
AR	D1	**ACCEPT RUNT PACKETS**: This bit allows the receiver to accept packets that are smaller than 64 bytes. The packet must be at least 8 bytes long to be accepted as a runt. 0: Packets with fewer than 64 bytes rejected. 1: Packets with fewer than 64 bytes accepted.
AB	D2	**ACCEPT BROADCAST**: Enables the receiver to accept a packet with an all 1's destination address. 0: Packets with broadcast destination address rejected. 1: Packets with broadcast destination address accepted.
AM	D3	**ACCEPT MULTICAST**: Enables the receiver to accept a packet with a multicast address; all multicast addresses must pass the hashing array. 0: Packets with multicast destination address not checked. 1: Packets with multicast destination address checked.

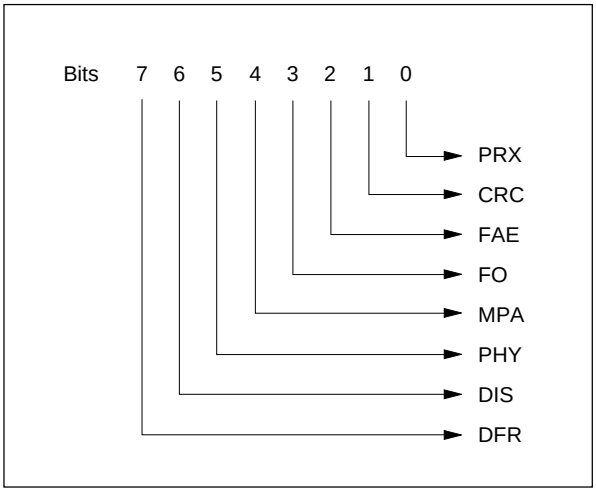
13. RECEIVE CONFIGURATION REGISTER (RCR) 0CH (WRITE)

SYMBOL	BIT	DESCRIPTION
PRO	D4	**PROMISCUOUS PHYSICAL:** Enables the receiver to accept all packets with a physical address. 0: Physical address of mode must match the station address programmed in PAR0-PAR5. 1: All packets with physical addresses accepted.
MON	D5	**MONITOR MODE**: Enables the receiver to check addresses and CRC on incoming packets without buffering to memory. The Missed Packet Tally Counter will be incremented for each recognized packet. 0: Packets buffered to memory. 1: Packets checked for address match, good CRC and frame alignment but not buffered to memory.
RESERVED	D6	**Reserved**
RESERVED	D7	**Reserved**

Note: D2 and D3 are "OR'd" together, i.e., if D2 and D3 are set the ENC will accept broadcast and multicast addresses as well as its own physical address. To establish full promiscuous mode, bits D2, D3 and D4 should be set. In addition, the multicast hashing array must be set to all 1's in order to accept all multicast addresses.

14. RECEIVE STATUS REGISTER (RSR) 0CH (READ)

This register records status of the received packet. It includes information on errors, the type of address match, either physical or multicast, and the aborted packet type. The contents of this register are written to buffer memory by the DMA after receiving a good packet. If packets with errors are to be saved the receive status is written to memory at the head of the erroneous packet, when an erroneous packet is received. If packets with errors are to be rejected the RSR will not be written to memory. The contents will be cleared when the next packet arrives. CRC errors, frame alignment errors and missed packets are counted internally by the ENC, which relinquishes the host from reading the RSR in real time to record errors for Network Management Functions. The contents of this register are not specified until after the first reception.



SYMBOL	BIT	DESCRIPTION
PRX	D0	**PACKET RECEIVED CORRECTLY**: Indicates packet received without error. (Bits CRC, FAE, FO and MPA are zero for the received packet.) Set when packets are received complete.
CRC	D1	**CRC ERROR**: Indicates packet received with CRC error. Increments Tally Counter (CNTR1). This bit will also be set for Frame Alignment errors. Set when packets are received complete.
FAE	D2	**FRAME ALIGNMENT ERROR**: Indicates that the incoming packet did not end on a byte boundary and the CRC did not match at last byte boundary. Increments Tally Counter (CNTR0). Set when packets are received complete.
FO	D3	**FIFO OVERRUN:** This bit is set when the FIFO is not serviced causing overflow during reception. Reception of the packet will be aborted.
MPA	D4	**MISSED PACKET**: Set when packet intended for node cannot be accepted by ENC because of a lack of receive buffers, or if the controller is in monitor mode and did not buffer the packet to memory increments Tally Counter (CNTR2).

14. RECEIVE STATUS REGISTER (RSR) 0CH (READ) *(Continued)*

SYMBOL	BIT	DESCRIPTION
PHY	D5	**PHYSICAL/MULTICAST ADDRESS**: Indicates whether received packet has a physical or multicast address type. Set/reset when Destination Address has been received. 0: Physical Address Match 1: Multicast/ Broadcast Address Match
DIS	D6	**RECEIVER DISABLED:** Set when receiver is disabled by entering Monitor mode. Reset when receiver is re-enabled when exiting the Monitor mode.
DFR	D7	**DEFERRING**: Set when CRS or COL inputs are active. If the transceiver has asserted the CD line as a result of the jabber, this bit will stay set indicating the jabber condition.

Note: The following coding applies to CRC and FAE bits

FAE	CRC	Type of Error
0	0	No Error (Good CRC and < 5 Dribble Bits)
0	1	CRC Error
1	0	Illegal, will not occur
1	1	Frame Alignment Error and CRC Error

15. REGISTER ADDRESS ASSIGNMENTS (Continued)

PAGE 0 ADDRESS ASSIGNMENTS (PS1 = 0, PS0 = 0)

RA3-RA0	READ	WRITE
00H	Command Register (CR)	Command Register (CR)
01H	Current Local DMA Address 0 (CLDA0)	Page Start Register (PSTART)
02H	Current Local DMA Address 1 (CLDA1)	Page Stop Register (PSTOP)
03H	Boundary Pointer (BNRY)	Boundary Pointer (BNRY)
04H	Transmit Status Register (TSR)	Transmit Page Start Address (TPSR)
05H	Number of Collisions Register (NCR)	Transmit Byte Count Register 0 (TBCR0)
06H	FIFO (FIFO)	Transmit Byte Count Register 1 (TBCR1)
07H	Interrupt Status Register (ISR)	Interrupt Status Register (ISR)
08H	Current Remote DMA Address 0 (CRDA0)	Remote Start Address Register 0 (RSAR0)
09H	Current Remote DMA Address 1 (CRDA1)	Remote Start Address Register 1 (RSAR1)
0AH	Reserved	Remote Byte Count Register 0 (RBCR0)
0BH	Reserved	Remote Byte Count Register 1 (RBCR1)
0CH	Receive Status Register (RSR)	Receive Configuration Register (RCR)
0DH	Tally Counter 0 (Frame Alignment Error) (CNTR0)	Transmit Configuration Register (TCR)
0EH	Tally Counter 1 (CRC Error) (CNTR1)	Data Configuration Register (DCR)
0FH	Tally Counter 2 (Missed Packet Error) (ENTR2)	Interrupt Mask Register (IMR)

15. REGISTER ADDRESS ASSIGNMENTS (Continued)

PAGE 1 ADDRESS ASSIGNMENTS (PS1 = 0, PS0 = 1)

RA3-RA0	READ	WRITE
00H	Command Register (CR)	Command Register (CR)
01H	Physical Address Register 0 (PAR0)	Physical Address Register 0 (PAR0)
02H	Physical Address Register 1 (PAR1)	Physical Address Register 1 (PAR1)
03H	Physical Address Register 2 (PAR2)	Physical Address Register 2 (PAR2)
04H	Physical Address Register 3 (PAR3)	Physical Address Register 3 (PAR3)
05H	Physical Address Register 4 (PAR4)	Physical Address Register 4 (PAR4)
06H	Physical Address Register 5 (PAR5)	Physical Address Register 5 (PAR5)
07H	Current Page Register (CURR)	Current Page Register (CURR)
08H	Multicast Address Register 0 (MAR0)	Multicast Address Register 0 (MAR0)
09H	Multicast Address Register 1 (MAR1)	Multicast Address Register 1 (MAR1)
0AH	Multicast Address Register 2 (MAR2)	Multicast Address Register 2 (MAR2)
0BH	Multicast Address Register 3 (MAR3)	Multicast Address Register 3 (MAR3)
0CH	Multicast Address Register 4 (MAR4)	Multicast Address Register 4 (MAR4)
0DH	Multicast Address Register 5 (MAR5)	Multicast Address Register 5 (MAR5)
0EH	Multicast Address Register 6 (MAR6)	Multicast Address Register 6 (MAR6)
0FH	Multicast Address Register 7 (MAR7)	Multicast Address Register 7 (MAR7)

15. REGISTER ADDRESS ASSIGNMENTS

PAGE 2 ADDRESS ASSIGNMENTS (PS1 = 1, PS0 = 0)

RA3-RA0	READ	WRITE
00H	Command Register (CR)	Command Register (CR)
01H	Page Start Register (PSTART)	Current Local DMA Address 0 (CLDA0)
02H	Page Start Register (PSTOP)	Current Local DMA Address 1 (CLDA1)
03H	Remote Next Packet Pointer	Remote Next Packet Pointer
04H	Transmit Page Start Address (TPSR)	Reserved
05H	Local Next Packet Pointer	Local Next Packet Pointer
06H	Address Counter (Upper) (ACU)	Address Counter (Upper) (ACU)
07H	Address Counter (Lower) (ACL)	Address Counter (Lower) (ACL)
08H	Reserved	Reserved
09H	Reserved	Reserved
0AH	Reserved	Reserved
0BH	Reserved	Reserved
0CH	Receive Configuration Register (RCR)	Reserved
0DH	Transmit Configuration Register (TCR)	Reserved
0EH	Data Configuration Register (DCR)	Reserved
0FH	Interrupt Mask Register (IMR)	Reserved

Note: Page 2 registers should only be accessed for diagnostic purposes. They should not be modified during normal operation.
Page 3 should never be modified.

REGISTER DESCRIPTION (Continued)

16. DMA REGISTERS

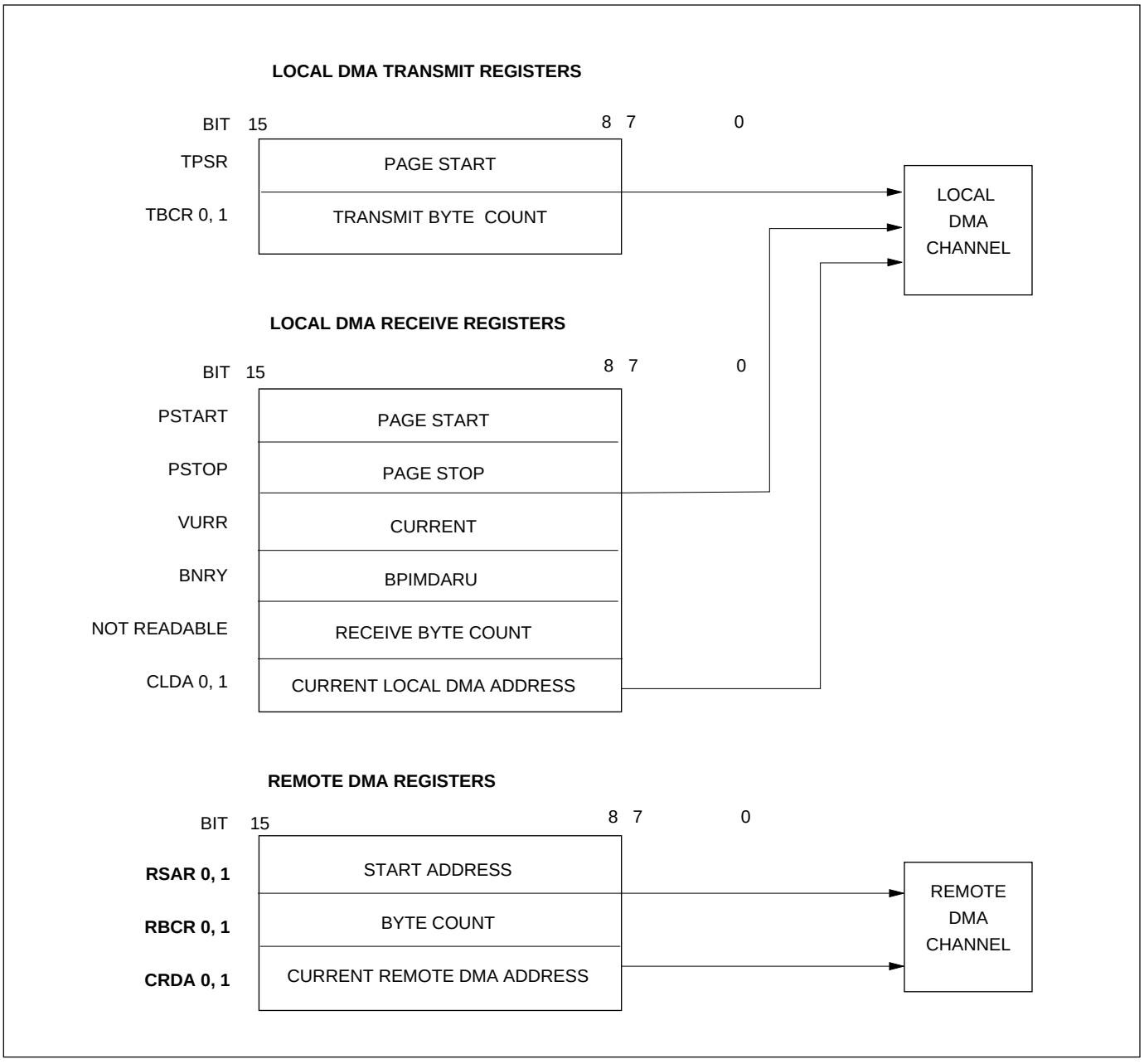
The DMA Registers are partitioned into three groups: Transmit, Receive, and Remote DMA Registers, as the diagram shows on the next page.

The Transmit group contains three registers: TPSR, TBCR0 and TBCR1. Registers in this group are used to initialize the Local DMA channel for transmission of packets.

PSTART, PSTOP, CURR, BNRY, Receive Byte Counter, CLDA0 and CLDA1 are located in the receive group. They are used to initialize the Local DMA channel for packet reception. Meanwhile, the Page Start, Page Stop, Current and Boundary Registers are also used by the Buffer Management Logic to supervise the Receive Buffer Ring.

The Remote DMA Registers are used to initialize the Remote DMA. Six registers are included: RSAR0, RSAR1, RBCR0, RBCR1, CRDA0 and CRDA1.

The diagram on the next page shows 8- and 16-bit registers. For slave mode read/write, the 16-bit internal registers are also accessed as 8-bit registers by the host. Thus, the 16-bit Transmit Byte Count Register is broken into two 8-bit registers, namely, TBCR0 and TBCR1. Similarly, Remote Start Address and Remote Byte Count are broken into RSAR0, RSAR1, and RBCR0, RBCR1. Registers TPSR, PSTART, PSTOP, CURR and BNRY only check or control the upper 8 bits of address information on the bus. Thus, they are shifted to position 15-8, as shown in the diagram on the next page.


LOCAL DMA TRANSMIT REGISTERS
BIT 15
8 7
0
TPSR
PAGE START
TBCR 0, 1
TRANSMIT BYTE COUNT
LOCAL DMA CHANNEL
LOCAL DMA RECEIVE REGISTERS
BIT 15
8 7
0
PSTART
PAGE START
PSTOP
PAGE STOP
VURR
CURRENT
BNRY
BPIMDARU
NOT READABLE
RECEIVE BYTE COUNT
CLDA 0, 1
CURRENT LOCAL DMA ADDRESS
REMOTE DMA REGISTERS
BIT 15
8 7
0
RSAR 0, 1
START ADDRESS
RBCR 0, 1
BYTE COUNT
CRDA 0, 1
CURRENT REMOTE DMA ADDRESS
REMOTE DMA CHANNEL

16. DMA REGISTERS (Continued)

TRANSMIT DMA REGISTER (TPSR)

This register points to the page where the assembled packet is ready to be transmitted. Only the eight higher order addresses are specified since all transmit packets are assembled on 256-byte page boundaries. The bit assignment is shown below. The values placed in bits D7-D0 will be used to initialize the higher order address (A15-A8) of the Local DMA for transmission while the lower order bits (A7-A0) are initialized to zero.

Bit assignment

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TPSR	A15	A14	A13	A12	A11	A10	A9	A8

(A7-A0 initialized to zero)

TRANSMIT BYTE COUNT REGISTER 0, 1 (TBCR0, 1)

These two registers indicate the length of the packet to be transmitted in bytes. The count must include the number of bytes in the source, destination, length and data fields (CRC field is exclusive). The maximum number of transmit bytes allowed is 64 kbytes. The ENC will not truncate transmissions whenever packet length is longer than 1500 bytes. Hence, in order to meet the IEEE 802.3 standard, software driver on upper layer must take care of maximum length problem by itself. The bit assignment is shown below:

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBCR1	L15	L14	L13	L12	L11	L10	L9	L8

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBCR0	L7	L6	L5	L4	L3	L2	L1	L0

16. DMA REGISTERS *(Continued)*

LOCAL DMA RECEIVE REGISTERS

PAGE START/STOP REGISTERS (PSTART, PSTOP)

The Page Start and Stop Registers program the starting and stopping page address of the Receive Buffer Ring. Since the ENC uses fixed 256-byte buffers aligned on page boundaries, only the upper eight bits of the start and stop address are specified.

PSTART, PSTOP bit assignment.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSTART,								
PSTOP	A15	A14	A13	A12	A11	A10	A9	A8

BOUNDARY REGISTER (BNRY)

This register is used to prevent overflow of the Receive Buffer Ring. Buffer Management compares the contents of this register to the next buffer address when linking buffers together. If the contents of this register match the next buffer address, the Local DMA operation is aborted and the corresponding bit in ISR will be set.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BNRY	A15	A14	A13	A12	A11	A10	A9	A8

CURRENT PAGE REGISTER (CURR)

This register is used internally by the buffer management logic as a backup register for reception. CURR contains the address of the first buffer to be used for a packet reception, and is used to restore DMA pointers if receive errors occur. This register is initialized to the same value as PSTART and should not be written to unless the controller is reset.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CURR	A15	A14	A13	A12	A11	A10	A9	A8

16. DMA REGISTERS *(Continued)*

CURRENT LOCAL DMA REGISTER 0, 1 (CLDA0, 1)

The temporary local DMA address will be stored in these two registers after each burst transfer is completed. When another burst transfer is ready to start, values within these two registers will be loaded into the Address Counters (ACU and ACL) to generate address for local DMA channel.

These two registers can be accessed to determine the current local DMA address.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLDA1	A15	A14	A13	A12	A11	A10	A9	A8

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLDA0	A7	A6	A5	A4	A3	A2	A1	A0

REMOTE DMA REGISTER

REMOTE START ADDRESS REGISTERS (RSAR0, 1)

Remote DMA operations are programmed through the Remote Start Address (PSAR0, 1) and Remote Byte Count (RBCR0, 1) registers. The Remote Start Address is used to point to the start of the block of data to be transferred, while the Remote Byte Count is used to indicate the length of the block (in bytes)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSAR1	A15	A14	A13	A12	A11	A10	A9	A8

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSAR0	A7	A6	A5	A4	A3	A2	A1	A0

16. DMA REGISTER *(Continued)*

REMOTE BYTE COUNT REGISTERS (RBCR0, 1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBCR1	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBCR0	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0

Note:
- RSAR1 programs the start address bits A8-A15
- RSAR0 programs the start address bits A0-A7
- Address incremented by two for word transfers, and by one for byte transfers
- RBCR1 programs MSB byte count
- RBCR0 programs LSB byte count
- Byte count decremented by two for word transfers, and by one for byte transfers

CURRENT REMOTE DMA ADDRESS (CRDA0, 1)

The Current Remote DMA Registers contain the current address of the Remote DMA. CRDA1/0 are similar to CLDA1/0 except that CRDA1/0 store the temporary address of the Remote DMA. The bit assignment is shown below:

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRDA1	A15	A14	A13	A12	A11	A10	A9	A8

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRDA0	A7	A6	A5	A4	A3	A2	A1	A0

16. DMA REGISTER *(Continued)*

FIFO

This is an 8-bit register which allows the CPU to examine the contents of the FIFO after loopback. The FIFO will contain the last 8 data bytes transmitted in the loopback packet. Sequential reads from the FIFO will advance a pointer in the FIFO automatically and reading of all 8 bytes.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Note: The FIFO should only be read when the ENC has been programmed in the loopback mode.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Supply Voltage (VCC)	4.75V to +5.5V
DC Input Voltage (VIN)	-0.5V to VCC +0.5V
DC Output Voltage (VOUT)	-0.5V to VCC +0.5V
Storage Temperature Range (TSTG)	-65℃ to +150℃
Power Dissipation (PD)	500 mW
Lead Temp. (TL) (Soldering, 10 sec.)	260℃
ESD rating (RZAP=1.5K, CZAP=120pF)	1600V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
SUPPLY CURRENT					
ICC	Average Active (Transmitting/Receiving) Supply Current	10	100	mA	X1=20MHz Clock VIN=Switching
ICCIDLE	Average Idle Supply Current	10	100	mA	X1=20MHz Clock VIN=VCC or GND
LCCLP	Low Power Supply Current	10	80	uA	X1=Undriven
TTL INPUTS					
VIL	Maximum Low Level Input Voltage		0.8	V	
VIH	Minimum High Level Input Voltage	2.0			V
IIN	INput Current	-1.0	1.0	uA	VI=VCC of GND
3SH TRI-STATE HIGH DRIVE I/O					
VOH	Minimum High Level Output Voltage	2.4		V	IOH=-3mA
VOL	Maximum Low Level Output Voltage		0.5	V	IOL=24mA
VIL	Maximum Low Level Input Voltage		0.8	V	
VIH	Minimum High Level Input Voltage	2.0		V	
IIN	Input Current	-1.0	1.0	uA	VI=VCC or GND
IOZ	Maximum TRI-STATE Output Leakage Current	-10.0	10.0	uA	VOUT=VCCor GND

DC CHARACTERISTICS *(Continued)*

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
MOS INPUTS, OUTPUTS AND I/O					
VOH	Minimum High Level Output Voltage	VCC-0.1		V	IOH=-20uA
VOL	Maximum Low Level Output Voltage		0.1	V	IOL=20uA
VIL	Maximum Low Level Input Voltage		0.8	V	
VIH	Minimum Low Level Input Voltage	2.0		V	
IIN	Input Current	-1.0	1.0	uA	VI=VCC or GND
IIN	Input Current TEST, DWID Pulldown Register	50	2000	uA	VI=VCC
IOZ	Maximum TRI-STATE Output Leakage Current	-10.0	10.0	uA	VOUT=VCC or GND
OCH COLLECTOR HIGH DRIVE OUTPUT					
VOL	Maximum Low Level Output Voltage		0.5	V	IOL=24mA
LED DRIVER OUTPUT					
VOL	Maximum Low Level Output Voltage		0.5	V	IOL=16mA
THIN DRIVER OUTPUT					
VOH	Minimum High Level Output Voltage	2.4		V	IOH=-8mA
VOL	Maximum Low Output Voltage		0.5	V	IOL=2mA
OSCILLATOR PINS (X1 AND X2)					
VIH	X1 Input High Voltage	2.0		V	X1 is connected to an oscillator
VIL	X1 Input Low Voltage		0.8	V	X1 is connected to an oscillator
IOSC	X1 Input Current		1	mA	X1 is connected to an oscillator VIN=VCC or GND

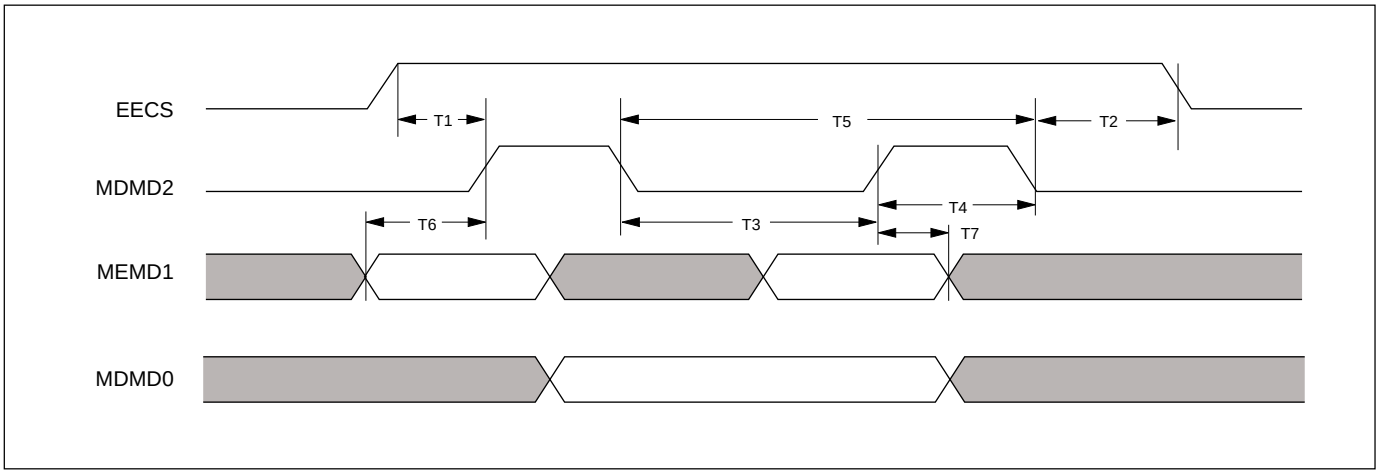
DC CHARACTERISTICS *(Continued)*

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
AUI					
VOD	Differential Output Voltage (TX±)	±550	1250	MV	78 ohm Termination and 270 ohm from each to GND
VOB	Differential Idle Output Voltage	Typical : 40mV		mV	78 ohm Termination and 270 ohm from each to GND
VU	Undershoot Voltage (TX±)	Typical : 80mV		mV	78 ohm Termination and 270 ohm from each to GND
VDS	Diff. Squelch Threshold (RX±, CD±)	-175	-300	mV	
VCM	Diff. Input Common Mode Voltage (RX±, CD±)	0	5.25	V	
TPI					
RTOL	TXOD±, TXO± Low Level Output Resistance		15	ohm	IOL=25mA
RTOH	TXOD±, TXO± High Level Output Resistance		15	ohm	OH=-25mA
VSRON1	Receive Threshold Turn-On Voltage 10BASE-T Mode	±300	-585	mV	
VSRON1	Receive Threshold Turn-Off Voltage Reduced Threshold	±75	±300	mV	
VSROFF	Receive Threshold Turn-Off Voltage	±75	±300	mV	
VDIFF	Differential Mode Input Voltage Range	-3.1	3.1	V	VCC=5.0V

AC CHARACTRISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T1	EECS setup to SK	300		ns
T2	EECS hold after SK	300		ns
T3	MSD2 Low time	500		ns
T4	MSD2 High time	500		ns
T5	MSD2 Clock period	1		ms
T6	Data In, setup to MSD2 high	200		ns
T7	Data In hold from MSD2 high	300		ns

SERIAL EEPROM TIMING

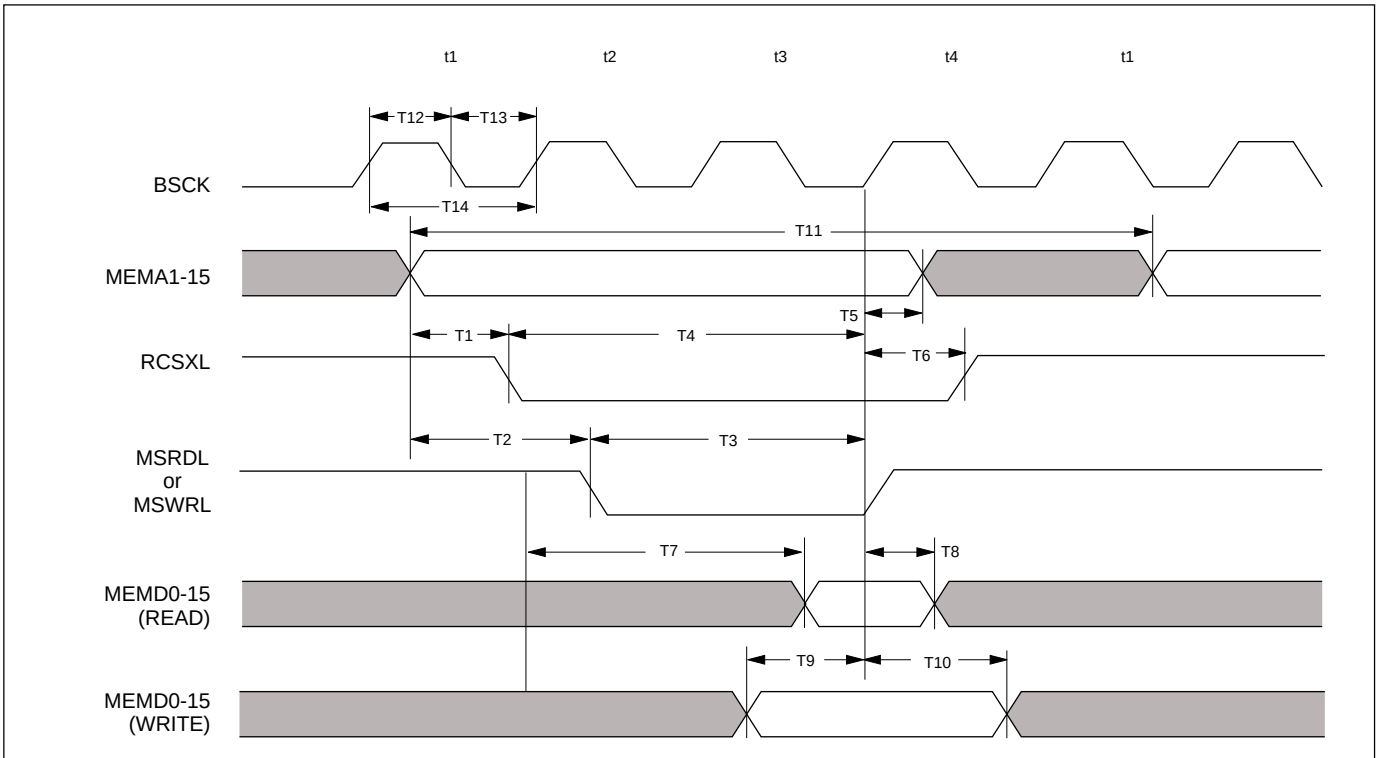


AC CHARACTRISTICS

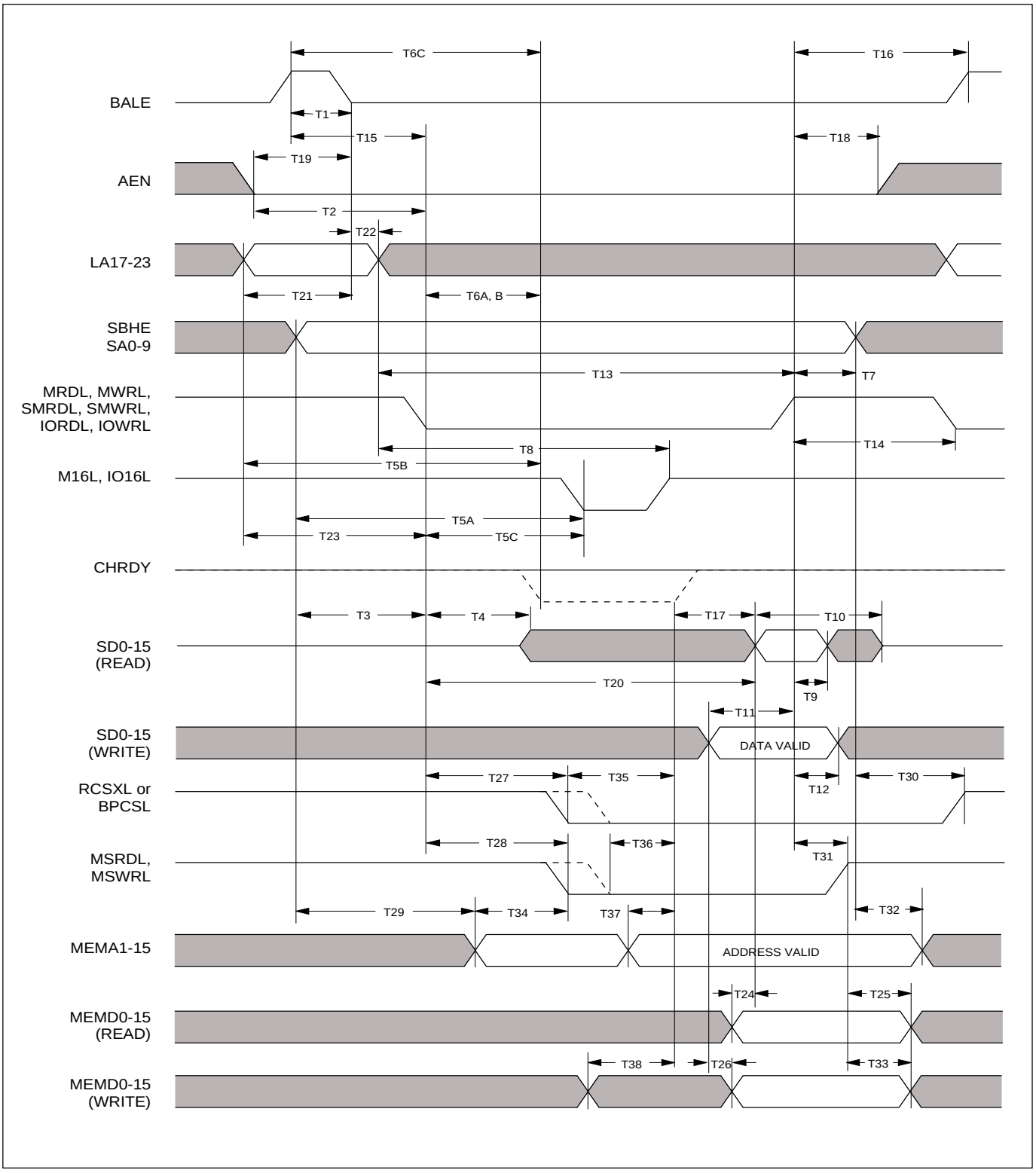
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T1	MEMA1-15 valid before RSCXL Asserted (Note1)		30	ns
T2	MEMA1-15 Valid before MSRD/MSWR asserted	20		ns
T3	MSRDL-WRL Width	2		bcyc
T4	MEMA1-15 Valid to MSRDL or MSWRL Deasserted	40		ns
T5	MEMA1-15 Valid after MSRDL-WRL Deasserted	10		ns
T6	RCSXL Held after MSRDL-WRL Deasserted (Note1)	200	400	ns
T7	RCXL and MEMA1-15 valid to MEMD0-15 valid		100	ns
T8	Read Data Hold from MSRDL Deasserted	0		ns
T9	Write Data Set-Up to MSWRL Deasserted	60		ns
T10	Write Data Held from MSWRL Deasserted	10		ns
T11	Time Between Transfers	4		bcyc
T12	Minimum bus Clock High Time (bch)	10		ns
T13	Minimum Bus Clock Low Time (bcl)	20		ns
T14	Minimum Bus Clock Cycle Time (bcyc)	50		ns

Note 1 : In 8-bit mode RCSXL refers to RCS1L only. In 16-bit mode RCSXL refers to both RCS1L and RCS2L.

MEMORY SUPPORT BUS ACCESSES (FOR I/O PORT OR FIFO TRANSFERS)



ISA SLAVE ACCESSES



AC CHARACTRISTICS

SYMBOL	PARAMETER	8 BIT		16 BIT		UNIT
		MIN.	MAX.	MIN.	MAX.	
T1	BALE width	20		20		ns
T2	AEN valid before command strobe active	40		40		ns
T3	SBHEL & SA0-9 valid before command asserted	20		20		ns
T4	IORDL, MRDL asserted to SD0-15 driven (Note 3)	0		0		ns
T5a	SBHEL & SA0-9 valid before IO16L valid (Notes 1 & 9)				45	ns
T5b	LA17-23 valid to M16L valid (Note 1)				30	ns
T5c	SBHEL & SA0-9 valid and IORDL or IOWRL active before IO16L valid (Notes 1 & 10)				20	ns
T6a	IORDL, IOWRL asserted to CHRDY negated (Notes 2 & 5)		35		35	ns
T6b	MRDL, MWRL asserted to CHRDY negated (Note 2)		35		35	ns
T6c	BALE asserted & SA0-9 valid to CHRDY negated (Notes 2 & 4)	15		15		ns
T7	IORDL deasserted before SBHEL & SA0-9 invali	15		15		ns
T8	LA17-23 invalid to M16L invalid (Note 1)		0		ns	
T9	IORDL, MRDL deasstered to SD0-15 (Note 3)Read Data Invalid	0		0		ns
T10	IORDL, MRDL deasserted to SD0-15 floating (Note 3)			30	30	ns
T11	D0-15 write data valid to IOWRL deasstered (Note 3)	60		20		ns
T12	IOWRL, MWRL negated to SD0-15 write data invalid (Note 3)	15		15		ns
T13a	IORDL, IOWRL Active width (Note 3)	300		140		ns
T14a	IORDL, IOWRL inactive width	85		85		ns
T14b	MRDL, MWRL inactive width SMRDL, SMWRL					

AC CHARACTRISTICS *(Continued)*

SYMBOL	PARAMETER	8 BIT		16 BIT		UNIT
		MIN.	MAX.	MIN.	MAX.	
T15	BALE asserted before MRDL, MWRL asserted			25		ns
T16	MRDL, MWRL deasserted before next BALE asserted			20		ns
T17	CHRDY asserted to SD0-15 I/O read data valid (Notes 2, 3, & 6)	60		60		ns
T18	IORDL, IOWRL negated before AEN invalid	25			50	ns
T19	AEN valid before BALE deassereted	50			25	ns
T20	IORDL asserted to SD0-15 read data valid (Notes 3 & 7)	150			150	ns
T21	LA17-23 valid before BALE negated					
T22	BALE negated before LA17-23 invalid					
T23	LA17-23 valid before MRDL, MWRL asserted					
T24	Read data valid on MSD0-15 to valid on SD0-15		40		40	ns
T25	MSRDL deasserted to MSD0-15 read data Invalid (Note 3)	0		0		ns
T26	Write data valid on SD0-15 to valid on MEMD0-15		30		30	ns
T27	SA0-19 valid to /RCS XL or /BPCSL asserted (Note 11)	40		40		ns
T28	MRDL, MWRL asserted to MSRDL, MSWRL asserted		30		30	ns
T29	SA0-19 valid to MEMA1-15 valid		30		30	ns
T30	SA0-19 invalid to RCSXL or BPCSL negated (Note 11)	30		20	ns	
T31	MRDL, MWRL deasserted to MSRDL, MSWRL deasserted	0	30	0	45	ns
T32	MSWRL deasserted to MEMA1-15 invalid	10		10		ns

AC CHARACTRISTICS *(Continued)*

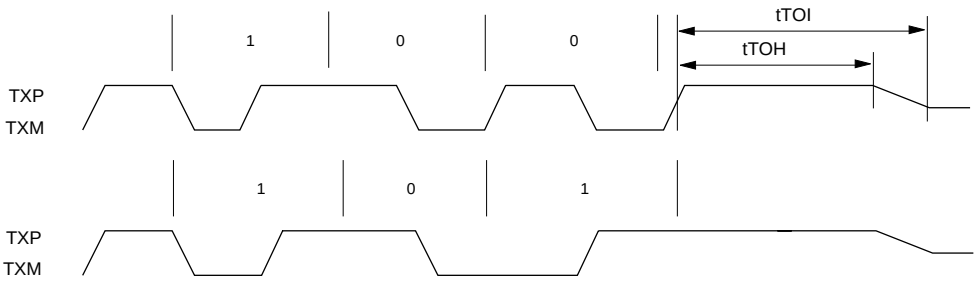
SYMBOL	PARAMETER	8 BIT		16 BIT		UNIT
		MIN.	MAX.	MIN.	MAX.	
T33	MSWR1deasserted to MSMD0-15 invalid (Note 3)	20		20		ns
T34	MEMA1-15 valid before /MSWRL asserted	20		20		ns
T35	RCSXL or /BPCSL asserted to CHRDY asserted (Note 11)	15		15		ns
T36	MSRDL, MSWRL asserted to CHRDY asserted	0		0		ns
T37	MEMA1-15 valid to CHRDY asserted	15		15		ns
T38a	Driving data from SD0-15 on to MEMD0-15 to CHRDY asserted for RAM access	60		60		ns
T38b	Driving data from SD0-15 to CHRDY asserted for Boot PROM access	260		260		ns

Note 1: M16L, IO16 are only asserted for 16-bit transfers.
Note 2: CHRDY is only deasserted if the NIC core cannot service the access immediately. It is held deasserted until the NIC core is ready, causing the system to insert wait states.
Note 3: On 8-bit trnasfers only 8 bits of MEHD0-15 and D0-7 are driven.
Note 4: This is the earty CHRDY timing required by some machines, where CHRDY is referenced to BALE. In this mode of operation, under certain circumstances, CHRDY will be asserted for cycles which are not for this device i.e., memory cycles or I/O cycles where SA0-9 match our address before reaching their valid state. In such a case the time to assert CHRDY, from MRDL, MWRL or SA0-9 invalid, will be the same as the deassertion time specified.
Note 5: This is the standard CHRDY timing where CHRDY is asserted after IORDL or IOWRL.
Note 6: Read data valid is referenced to CHRDY when wait states have been inserted.
Note 7: If no wait states are inserted read data valid can be measured from IORDL.
Note 8: This is a minimum timing with no additional wait states.
Note 9: This is the standard I/O 16 timing where /IO16 is asserted after a valid address decode and IORDL or IOWRL going active.
Note 10: This is the late IO16L timing, required by some machines. Where IO16L is asserted after a valid address decode and IORDL or IOWRL going active.
Note 11: BPCS is asserted for a boot PROM access. RCSL for a RAM access. RCSXL refers to RCS1L and RCS2L Depending on the mode of operation either or both can be asserted. See the Functional Bus Timing section for further explanation.
Note 12: Specifications which measure delays from an active state to a high impedance state are not guaranteed by production test, but are characterized and correlated to determine true driver turn-off time by simulating inherent R-C delay times. In test measurements.

AC CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
tTOH	Transmit Output High before (Half Step)	200		ns
tTOL	Transmit Output Idle Time (Half Step)		8000	ns

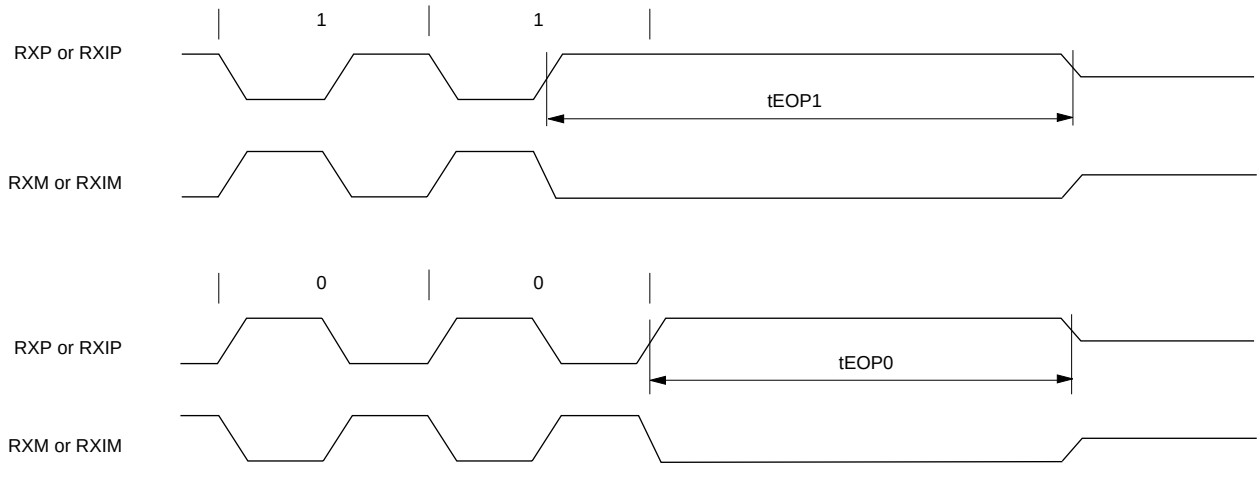
AUI TRANSMIT TIMING (END-OF-PACKET)



SYMBOL	PARAMETER	MIN.	MAX.	UNIT
tEOP1	Receive End-Of-Packet Hold Time after Logic "1" (Note 1)	250		ns
tEOP 0	Receive End-Of-Packet Hold Time after Logic "0" (Note 1)	250		ns

NOTE:
1. This parameter is guaranteed by design and is not tested.

AUI/API RECEIVE END-OF-PACKET TIMING

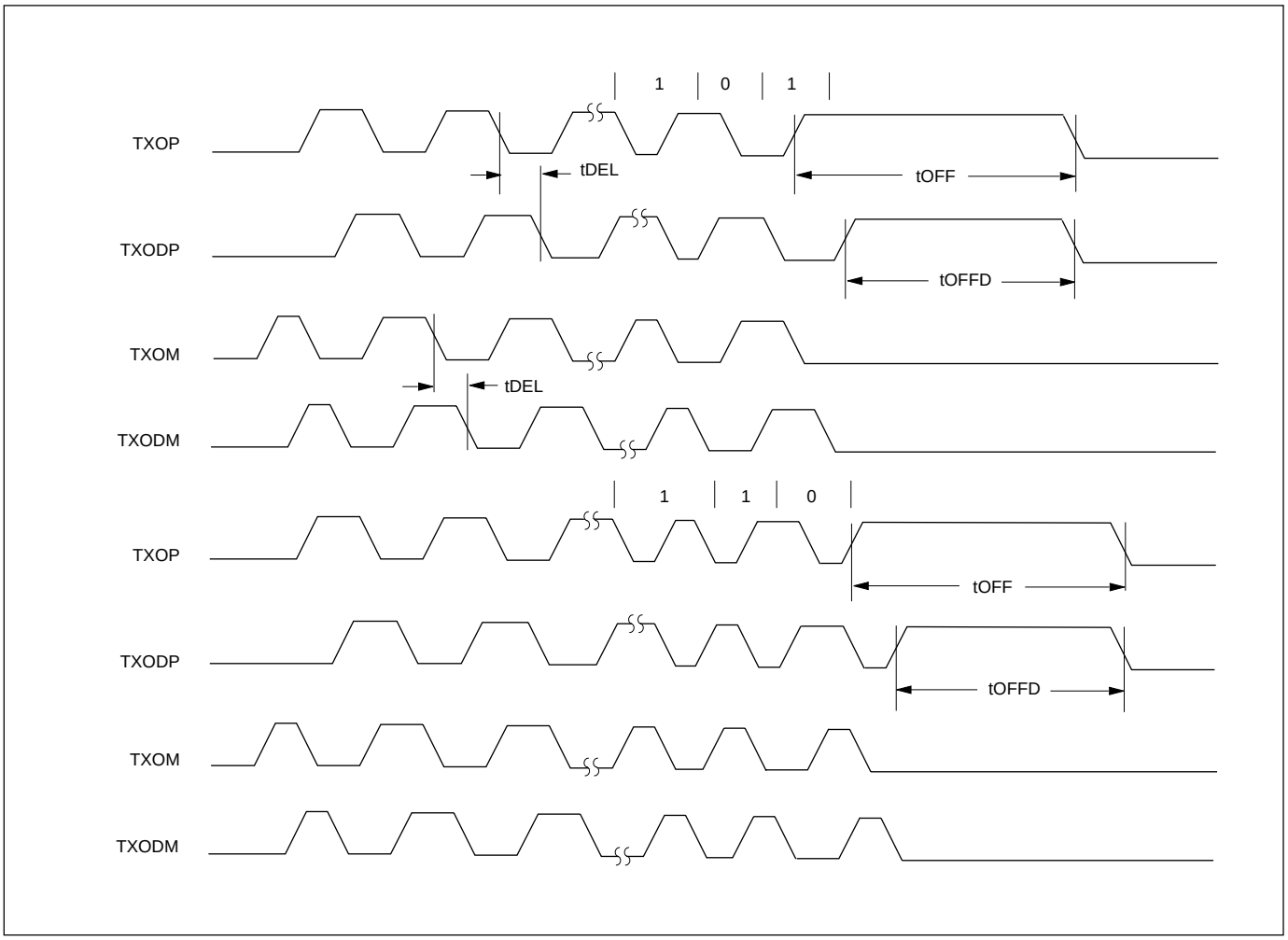


AC CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
tDEL	Pre-Emphasis Output Delay (TXOP,TXOM to TXODP,TXODM) (Note 1)	46	54	ns
tOFF	Transmit Hold Time at End-Of-Packet (TXOP,TXOM) (Note 1)	250		ns
tOFFD	Transmit Hold Time at End-Of-Packet (TXODP,TXODM) (Note 1)	200		ns

NOTE: 1. This parameter is guaranteed by design and is not tested.

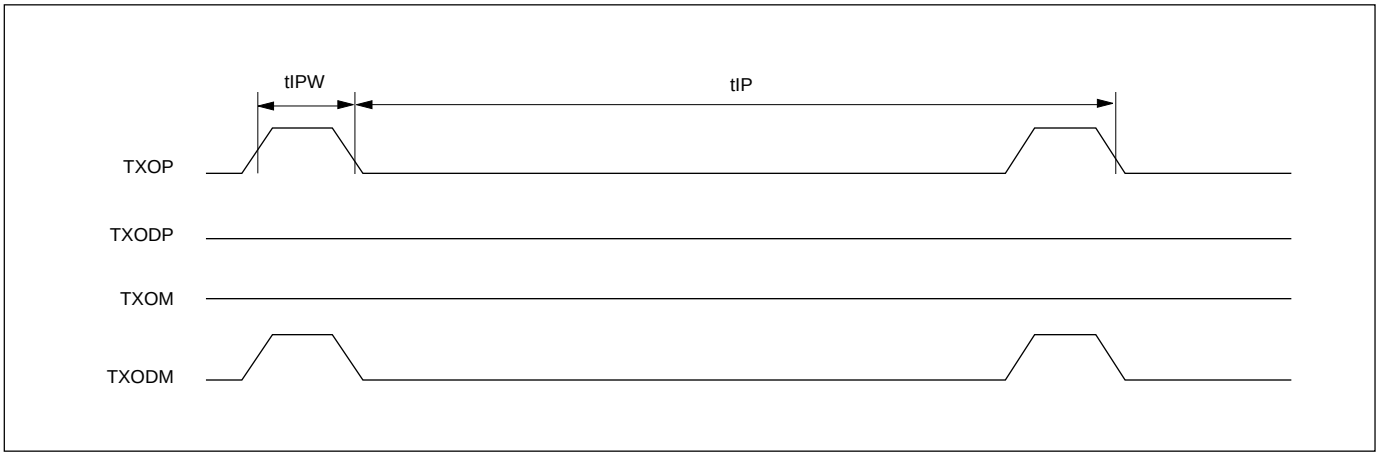
TPI TRANSMIT AND END-OF-PACKET TIMING



AC CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
tIP	Time between Link Output Pulses	8	24	ms
tIPW	Link Integrity Output Pulse Width	80	130	ns

LINK PULSE TIMING



ORDERING INFORMATION

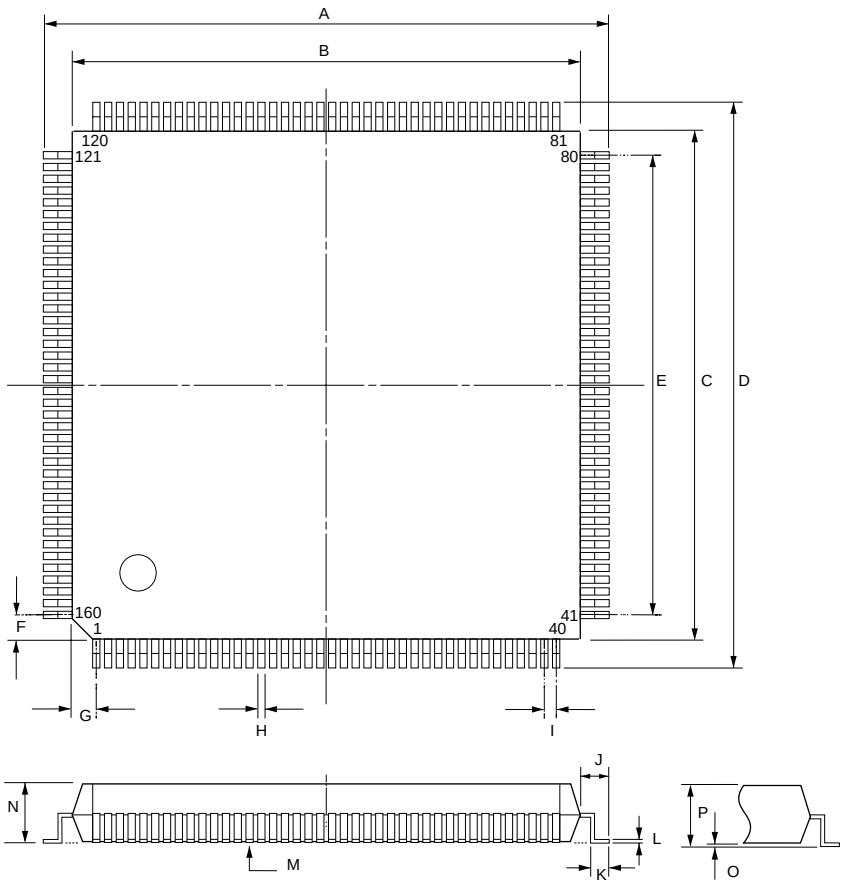
PART NO.	PACKAGE
MX98905BFC	160 Pin PQFP

PACKAGE INFORMATION

160-Pin PQFP

ITEM	MILLIMETERS	INCHES
A	31.20 ± .30	1.228 ± .012
B	28.00 ± .10	1.102 ± .004
C	28.00 ± .10	1.102 ± .004
D	31.20 ± .30	1.228 ± .012
E	25.35	.999
F	1.33 [REF]	.052 [REF]
G	1.33 [REF]	.052 [REF]
H	.30 [Typ.]	.12 [Typ.]
I	.65 [Typ.]	.026 [Typ.]
J	1.60 [REF]	.063 [REF]
K	.80 ± .20	.031 ± .008
L	.15 [Typ.]	.006 [Typ.]
M	.10 max.	.004 max.
N	3.35 max.	.132 max.
O	.10 min.	.004 min.

NOTE: Each lead centerline is located within .25mm[.01 inch] of its true position [TP] at a maximum material condition.



MACRONIX INTERNATIONAL CO., LTD.

HEADQUARTERS:
TEL:+886-3-578-8888
FAX:+886-3-578-8887

EUROPE OFFICE:
TEL:+32-2-456-8020
FAX:+32-2-456-8021

JAPAN OFFICE:
TEL:+81-44-246-9100
FAX:+81-44-246-9105

SINGAPORE OFFICE:
TEL:+65-747-2309
FAX:+65-748-4090

TAIPEI OFFICE:
TEL:+886-3-509-3300
FAX:+886-3-509-2200

MACRONIX AMERICA, INC.

TEL:+1-408-453-8088
FAX:+1-408-453-8488

CHICAGO OFFICE:
TEL:+1-847-963-1900
FAX:+1-847-963-1909

http : //www.macronix.com