I/O Channel Ready Considerations for the DP83902EB-AT

National Semiconductor
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INTRODUCTION

Some PC-AT® compatible systems that use bus interface chip sets with modified timing characteristics such as some Chips & Technologies or VLSI technologies chip sets have different timing requirements that require modification to 16-bit I/O mapped designs to operate properly. 8-bit I/O mapped designs do not require this modification.

This paper describes the timing issues associated with the DP83902EB-AT and methods of fixing these timing incompatibilities.

OVERVIEW

The timing inconsistency is the time of assertion and deassertion of the IOCHRDY bus signal. IOCHRDY floats active (ready) when not driven by an I/O card. Normally, an I/O card should drive IOCHRDY low (not ready) to insert wait states only after the address and I/O read or write signal are asserted. However, on some PC-AT buses, during a 16-bit I/O operation the bus controller actually samples the IOCHRDY signal before the I/O read or write signal is asserted. To correct the early sampling of IOCHRDY by the bus controller, the I/O card can drive IOCHRDY based only on an address decode, thus allowing IOCHRDY to be asserted earlier and in the proper state when it is sampled by the bus controller.

Remote read cycles are executed by National Semiconductor's DP83902 ST-NIC™, Network Interface Controller with integrated twisted pair, during packet reception. A remote read cycle will be used to illustrate how the early sampling of IOCHRDY is compensated. Also, the PAL® equations needed to generate IOCHRDY and the necessary modifications to account for the early sampling of IOCHRDY for the DP83902EB-AT will be described.

REMOTE READ CYCLE

The ST-NIC receives data from the network and transfers the data to the local buffer memory using the local DMA channel. The ST-NIC then executes a remote DMA read to transfer the received data from the buffer memory to the host memory through the I/O port latch.

Referring to *Figure 2*, the remote read cycle functions as follows:

1. The ST-NIC reads a word from local buffer memory asserting $\overline{\text{MRD}}$ and writes the word into the I/O port latch asserting $\overline{\text{PWR}}$.
2. The ST-NIC asserts the request line (PRQ) to inform the host a word is in the I/O port latch.
3. The host reads the I/O port asserting $\overline{\text{IOR}}$. IOCHRDY is asserted if $\overline{\text{IOR}}$ occurs before PRQ to extend the assertion time of $\overline{\text{IOR}}$, effectively wait-stating the host so that the host-I/O handshake can occur.
4. $\overline{\text{RACK}}$ is asserted to signal to the ST-NIC that the host has read the word from the I/O port latch.

Steps 1–4 are repeated until all words are transferred.

"NORMAL" IOCHRDY TIMING DURING A REMOTE READ CYCLE

The "normal" IOCHRDY PAL equations are shown in *Figure 1* and the complete PAL equations for U2 in the DP83902EB-AT are shown in AN-752 in the 1992 Local Area Network Databook. The corresponding timing diagram is shown in *Figure 2*. Referring to *Figure 1* and AN-752, whenever NRDYEN is true, IOCHRDY is driven, otherwise it will be held TRI-STATE®. The first two terms in the NRDYEN function are for a slave read and write, respectively. The next two terms are for remote read and write, respectively. There are 7 unique variables in the function NRDYEN. Namely, NSTNICB, NIOR, NIOW, NACK, PRQ, SA4 and SA3. A brief explanation of each follows.

```
NRDYEN = !( !NSTNICB & !NIOR & !SA4 & NACK
         #!NSTNICB & !NIOW & !SA4 & NACK
         #!NSTNICB & !PRQ & !NIOR & SA4 & !SA3
         #!NSTNICB & !PRQ & !NIOW & SA4 & !SA3);
enable NIOCHRDY = !NRDYEN;

NIOCHRDY = (0);
```

FIGURE 1. "Normal" IOCHRDY PAL Equations for DP83902EB-AT

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NSTNICB—(SA9–SA5) chip select the I/O card. This is the base address of the I/O card.

NIOR—($\overline{IOR}$) the I/O read command signal.

NIOW—($\overline{IOW}$) the I/O write command signal.

NACK—($\overline{ACK}$) Used during slave read/write cycles to indicate a successful register (byte) transfer.

PRQ—Used during remote read/write cycles to inform the host that the NIC has written a word in the I/O port latch.

SA4 and SA3—Address signals from the I/O bus. The states of these signals determine if the address on the I/O bus is for the I/O port latch or the NIC registers.

The on board IOCHRDY signal will only be driven to wait state the host until the NIC writes to the I/O port latch and asserts PRQ.

The remote word transfer is complete after the $\overline{RACK}$ signal is asserted indicating the host has read the word from the I/O port latch.

MODIFIED IOCHRDY TIMING DURING A REMOTE READ CYCLE

The modified IOCHRDY PAL equations shown in *Figure 4* implement both the ''normal'' IOCHRDY timing and the modified IOCHRDY timing. These equations replace the section of the U2 PAL equations in AN-752 shown in *Figure 1*. The modified IOCHRDY schematic and timing diagram are shown in *Figures 3* and *5* respectively.

NIOCHR and NIOCHR.OE (enable NIOCHR) together are for slave read and remote read. Also, NIOCHW and NIOCHW.OE (enable NIOCHW) together are for slave write and remote write. These signals (NIOCHR and NIOCHW) together produce the ''normal'' IOCHRDY signal.

NIOCHC and NIOCHC.OE (enable NIOCHC) together modify the IOCHRDY timing. In the modified IOCHRDY timing, IOCHRDY is driven when the I/O card address is decoded, thus driving IOCHRDY before it is sampled by the host.

By driving IOCHRDY on an address decode the possibility exists that it may be driven on a memory access instead of an I/O access. IOCHRDY must be held TRI-STATE if the host issues a memory access command signal ($\overline{MEMR}$ or $\overline{MEMW}$) because if these signals become active after an address decode to the I/O card this means that the address was a memory address and not an I/O address. Thus, the address was not intended for the I/O card and driving IOCHRDY may cause contention with the memory.

PRQ is held TRI-STATE until the ST-NIC's Data Configuration Register (DCR) is programmed. A pull-up resistor is needed to guarantee PRQ is asserted while its TRI-STATE to prevent IOCHRDY from ''getting stuck'' low and effectively locking up the host.

Driving IOCHRDY early must be an option since this has been seen to cause problems on some PC's, but fixes problems on others. The variable CLONEN is a jumper used to switch the IOCHRDY signal characteristics to ''normal'' or modified timing. The inverted SYSCLK (System Clock) and BALE (Bus Address Latch Enable) signals are AT bus signals and are used to assert CLONEN when the bus address is valid, which is indicated by BALE. CLONEN is asserted when BALE is asserted and deasserted after BALE is deasserted and the next SYSCLK rising edge occurs, allowing enough time for the I/O command signal to occur. At this point, the modified IOCHRDY timing is TRI-STATE and the ''normal'' IOCHRDY timing is enabled.

EN16 is used to determine if the data transfer is 8 or 16 bits. The modified IOCHRDY is necessary only during 16-bit I/O accesses because the early sampling of IOCHRDY only occurs during 16-bit I/O accesses.

To incorporate the IOCHRDY modification in the DP83902EB-AT, replace the section of the U2 PAL equations shown in *Figure 1* with the PAL equations of *Figure 4* and add a 74F74 D flip-flop and a jumper to the evaluation board to hard-wire CLONEN to U2.

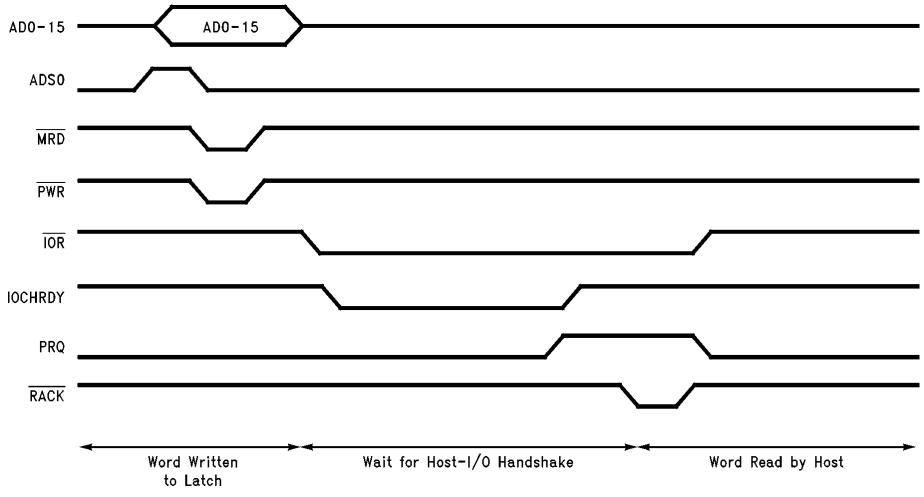

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FIGURE 2. ''Normal'' Remote Read Cycle for DP83902EB-AT

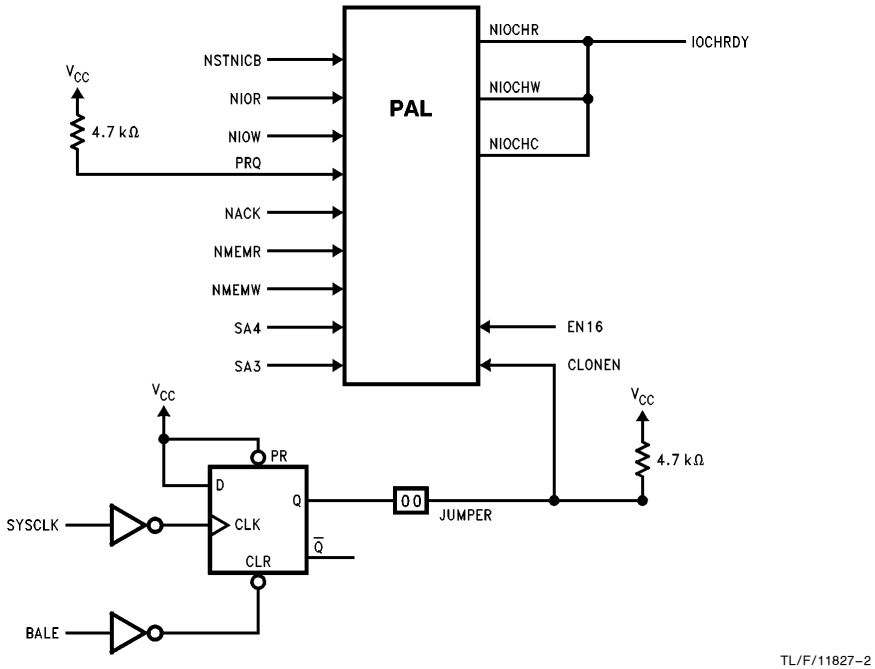

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FIGURE 3. Schematic of IOCHRDY Modification Showing Signals Required for IOCHRDY Change

```
NIOCHR = !(!PRQ & SA4 & !SA3 # NACK & !SA4);
enable NIOCHR = !(!NSTNICB & !NIOR);

NIOCHW = !(!PRQ & SA4 & !SA3 # NACK & !SA4);
enable NIOCHW = !(!NSTNICB & !NIOW);

NIOCHC = (0);
enable NIOCHC = !(!NSTNICB & NMEMR & NMEMW & !PRQ & !EN16 & !CLONEN & SA4 & !SA3);
```

FIGURE 4. Modified PAL Equations for DP83902EB-AT

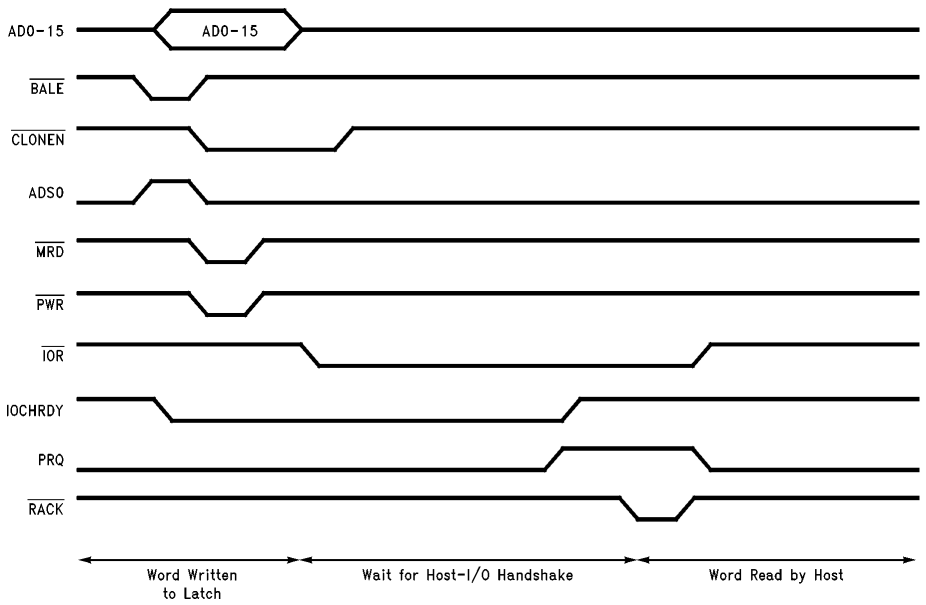

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FIGURE 5. Modified Remote Read Cycle for DP83902EB-AT

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