

4

SYSTEM DESIGN

OVERVIEW

The S3C44B0X, SNASUMG's 16/32-bit RISC microcontroller is cost-effective and high performance microcontroller solution for hand-held device and general application. The integrated on-chip functions of S3C44B0X are

- 2.5V Static ARM7TDMI CPU Core with 8KB cache (SAMBAs bus architecture up to 75MHz)
- External memory controller (FP/EDO/SDRAM Control, Chip Select logic)
- LCD Controller (up to 256 color DSTN) with 1-ch LCD-dedicated DMA
- 2-ch general DMAs / 2-ch peripheral DMAs with external request pins
- 2-ch UART / 1-ch SIO (IRDA1.0, 16-byte FIFO)
- 1-ch multi-master IIC-BUS controller & 1-ch IIS-BUS controller
- 5-ch PWM Timers & 1-ch internal timer
- Watch Dog Timer
- 71-bit general purpose I/O ports / 8-ch External Interrupt Source
- Power control : Normal, Slow, Idle and Stop mode
- 8-ch 10-bit ADC
- RTC with calendar function
- On-chip clock generator with PLL

Therefore, you can use S3C44B0X as amount types of system.

APPLICABLE SYTEM WITH S3C44B0X

If your product need to be networked, the S3C44B0X, SNASUMG's 16/32-bit RISC microcontroller can be reduce your system cost. There are sample system, it can be designed with S3C44B0X.

- GPS phone
- PDA (Personal Data Assistance)
- Fish Finder
- Portable Game Machine
- Fingerprint Identification System
- TWM (Two Way Messaging) Terminal
- Car Navigation System
- MP3 Player etc.

MEORY INTERFACE DESIGN

BOOT ROM DESIGN

When system reset, a S3C44B0X access 0x00000000 address. And S3C44B0X should be configure some system variable after reset. Therefore this special code (BOOT ROM image) should be located on address 0x00000000. A boot ROM can have a various width of data bus, and it is controlled by OM[1:0] pins.

Table 4-1. Data Bus Width for ROM Bank 0

OM[1:0]	Data Bus Width
00	8-bit (byte)
01	16-bit (half-word)
10	32-bit (word)
11	Test Mode

ONE BYTE BOOT ROM DESIGN

A design with one byte boot ROM is shown in Figure 4-1.

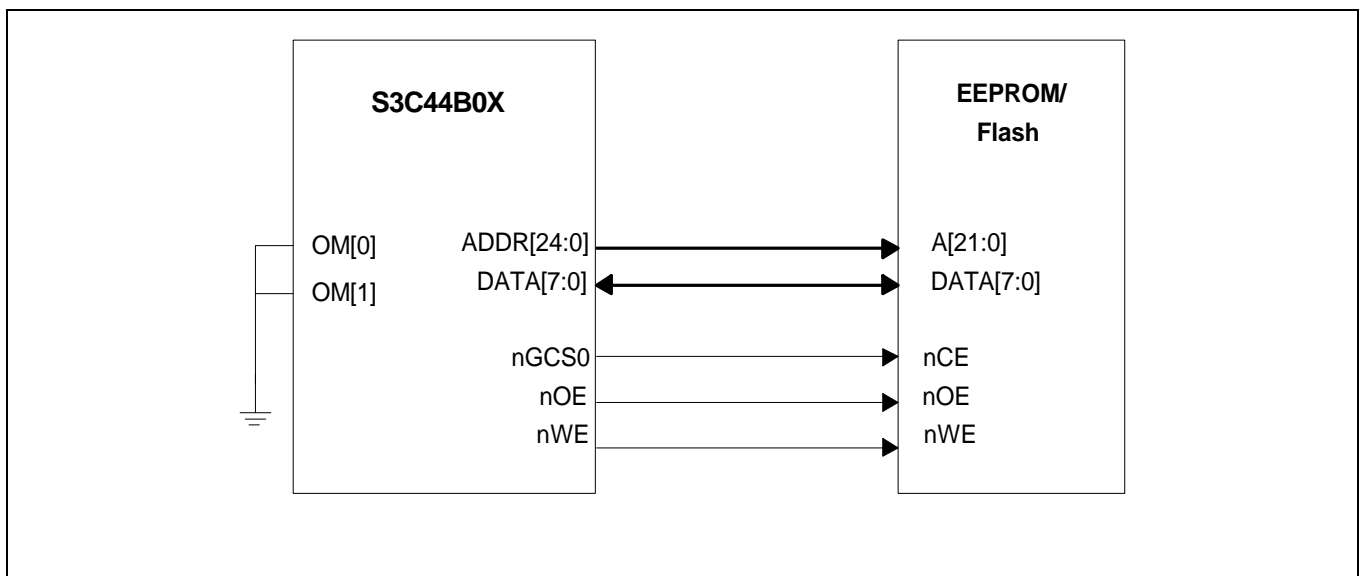


Figure 4-1. One Byte Boot ROM Design

MAKE AND FUSING ONE BYTE ROM IMAGE

When make one byte ROM image, you can use the binary file that made from compile and link.

HALF-WORD BOOT ROM DESIGN WITH BYTE EEPROM/FLASH

A design with half-word boot ROM with byte EEPROM/Flash is shown in Figure 4-2.

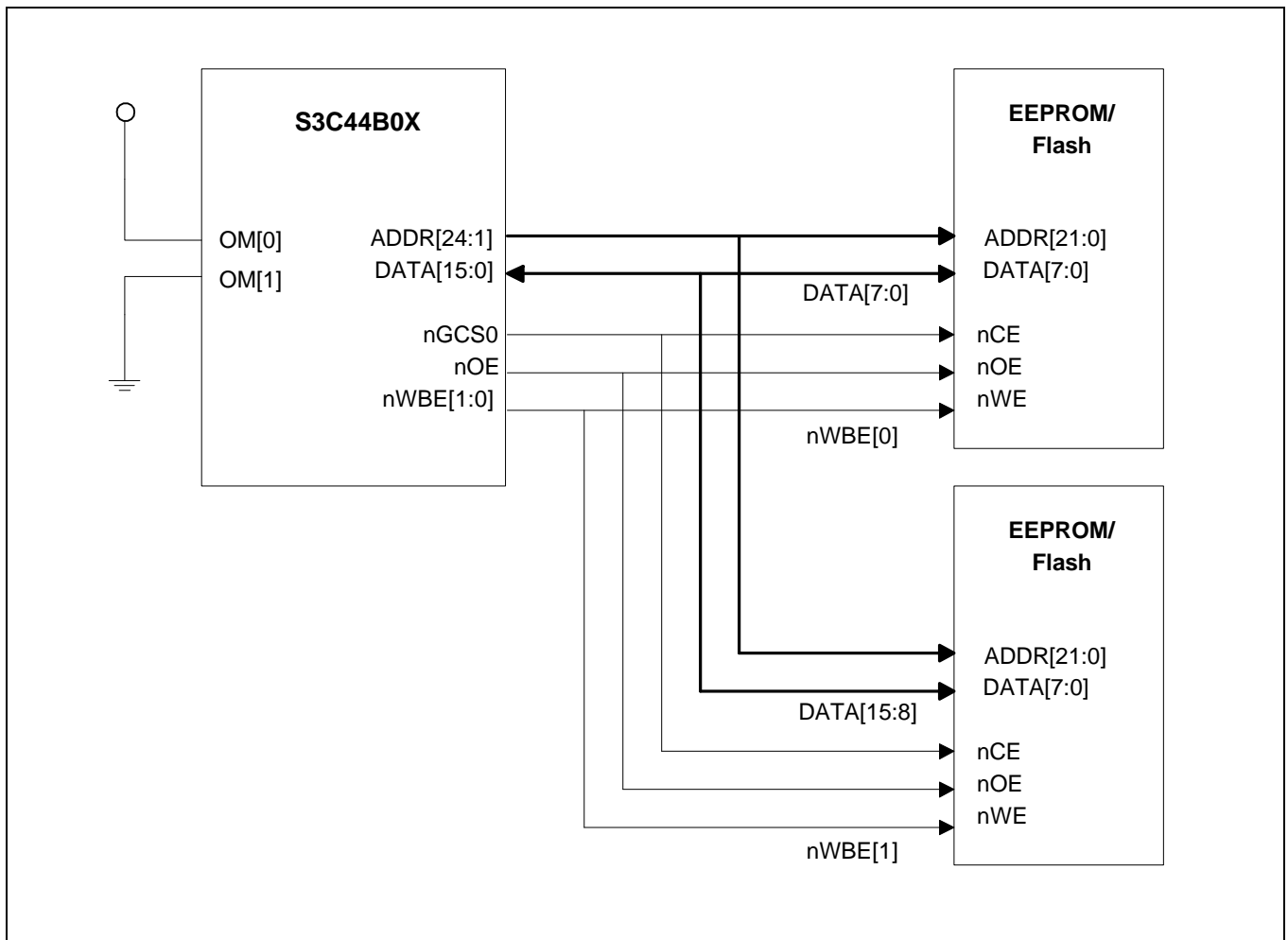


Figure 4-2. The Half-Word Boot ROM Design with Byte EEPROM/Flash

MAKE AND FUSING HALF-WORD ROM IMAGE WITH BYTE EEPROM/FLASH

When make half-word ROM image, you can split two image files, EVEN and ODD.

Table 4-2 Relationship ROM Image and Endian

	Big Endian	Little Endian
DATA[7:0]	Odd	Even
DATA[15:8]	Even	Odd

HALF-WORD BOOT ROM DESIGN WITH HALF-WORD EEPROM/FLASH

A design with half-word boot ROM with byte EEPROM/Flash is shown in Figure 4-3.

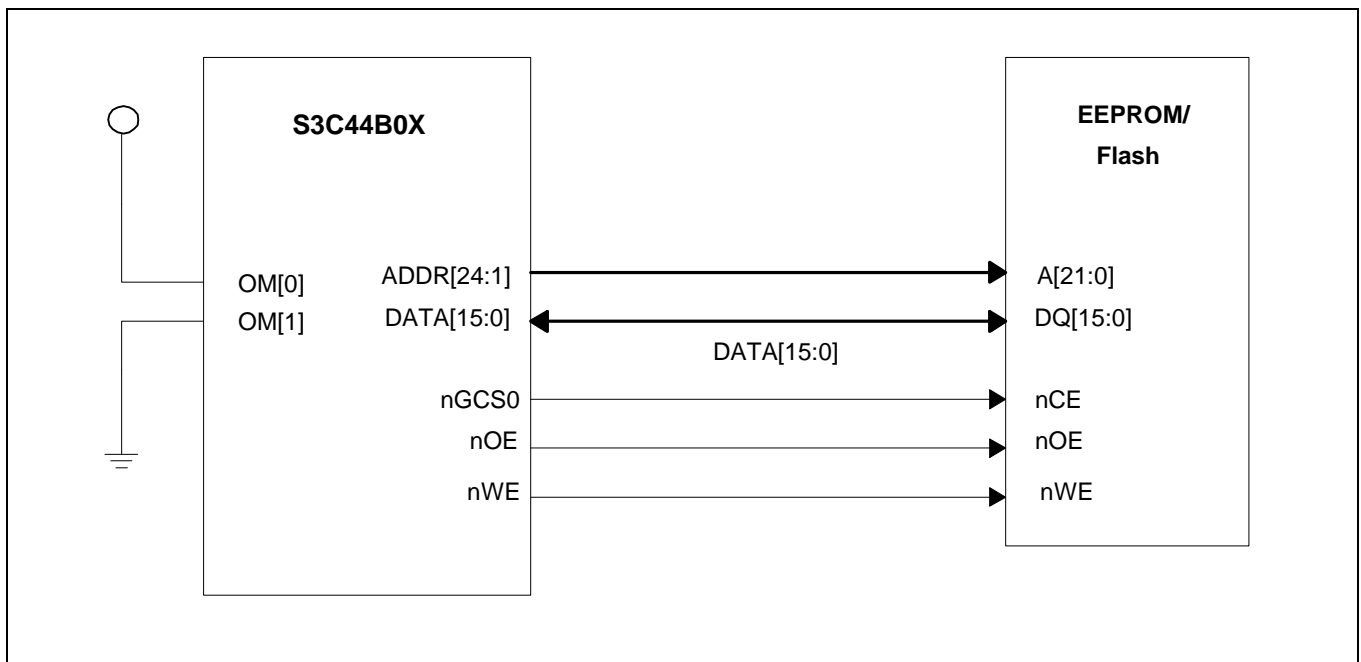


Figure 4-3. The Half-Word Boot ROM Design with Half-Word EEPROM/Flash

WORD BOOT ROM DESIGN WITH HALF-WORD EEPROM/FLASH

A design with word boot ROM with byte EEPROM/Flash is shown in Figure 4-4.

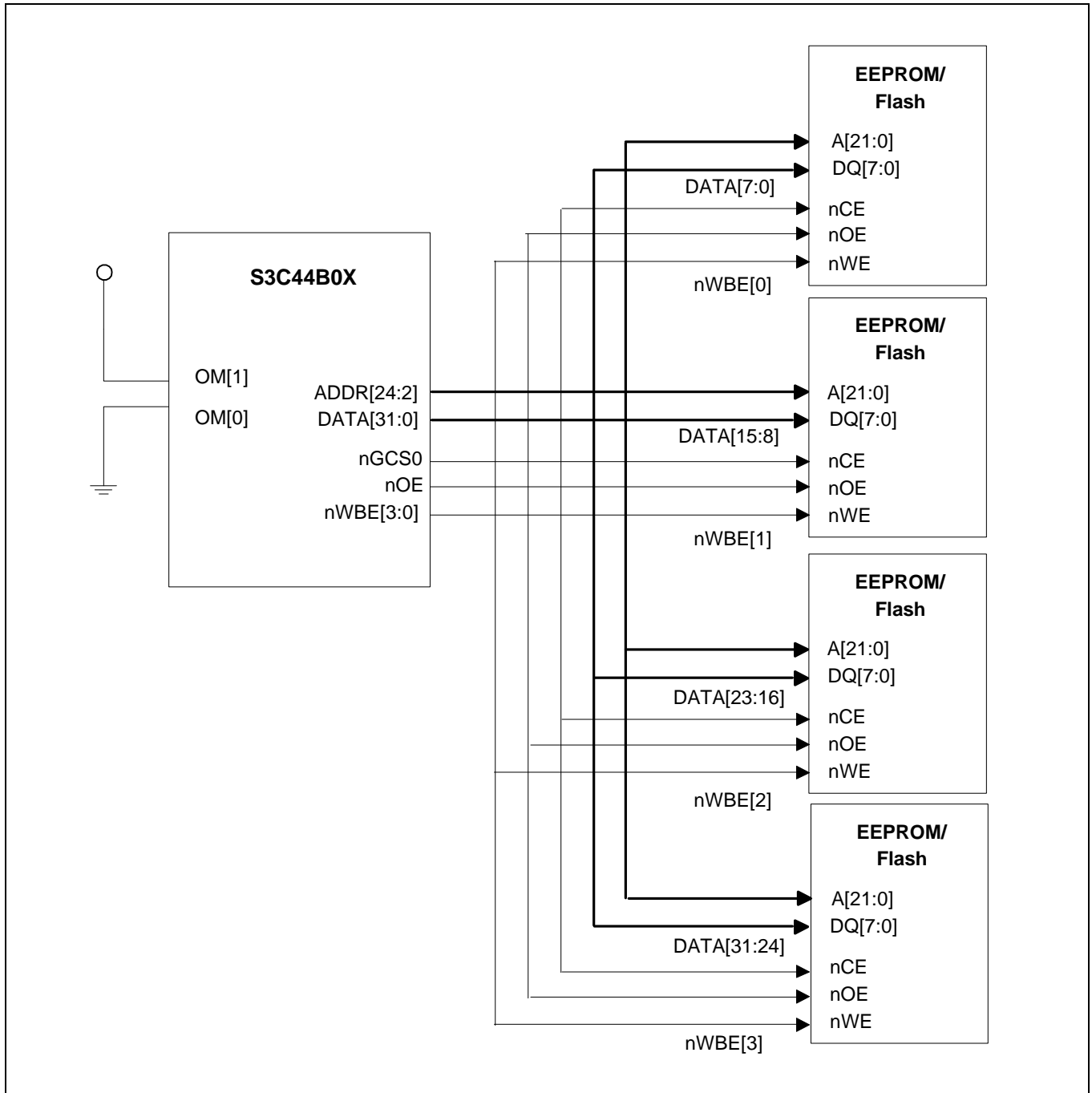


Figure 4-4. The Word Boot ROM Design with Byte EEPROM/Flash

MAKE AND FUSING WORD ROM IMAGE WITH BYTE EEPROM/FLASH

When you make word ROM image, you can split four image file.

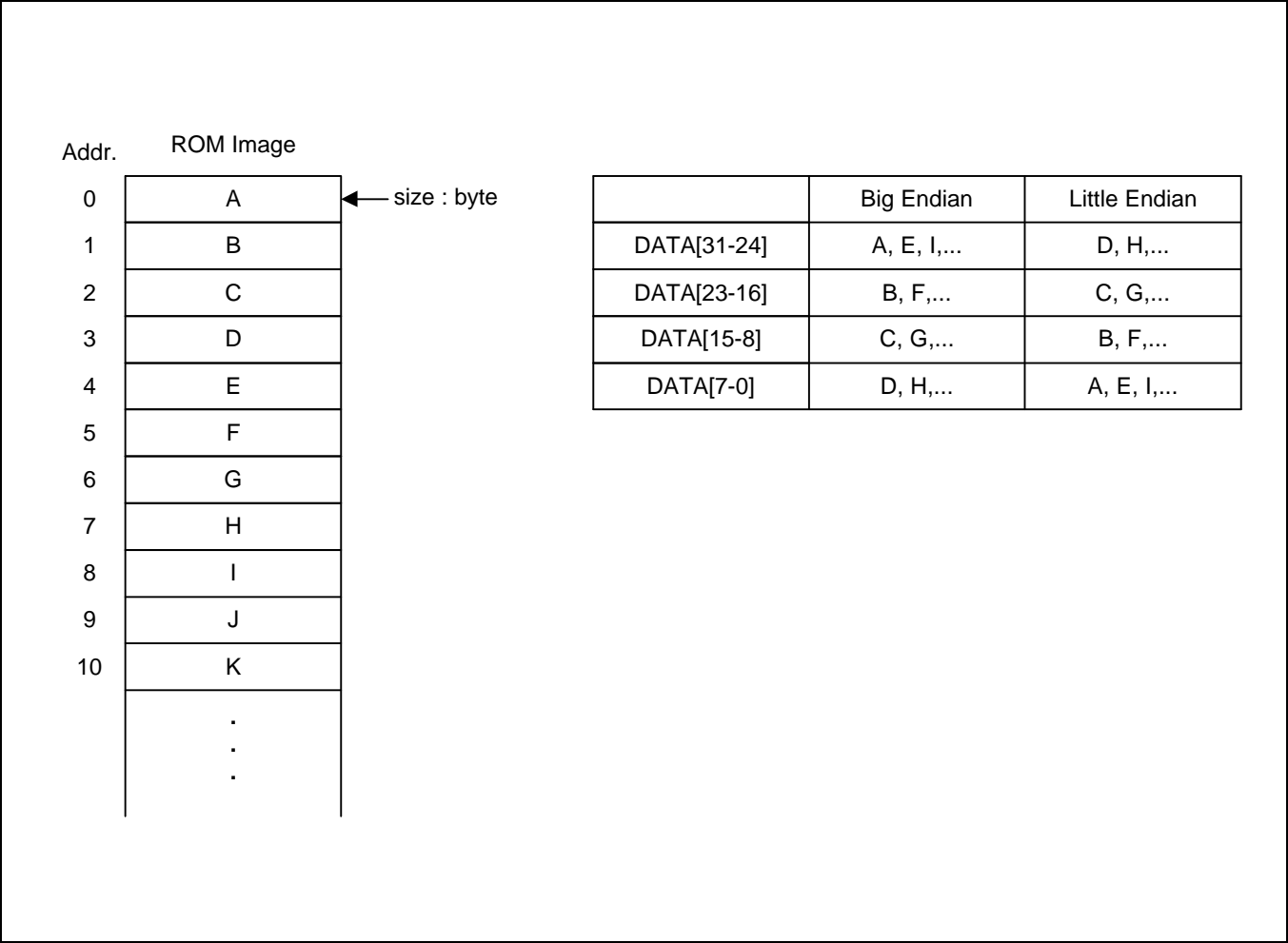


Figure 4-5 Relationship ROM Image and Endian

MEMORY BANKS DESIGN AND CONTROL

The S3C44B0X has 6 ROM/SRAM banks (ROM0 bank for boot ROM) and 2 ROM/SRAM/FP/EDO/SDRAM banks. The system manager on S3C44B0X can control access time, data bus width for each banks by S/W. The access time of ROM/SRAM banks and FP/EDO/SDRAM banks is controlled by BANKCON0~7 and BANKCON6~7 control register on system manager. The type memory of bank6 & 7 has to be same. (example ROM & ROM, SDRAM & SDRAM) The data bus width for each ROM/SRAM/DRAM banks is controlled by BWSCON control register.

The ROM bank 0 is used for boot ROM bank, therefore bank 0 is controlled by H/W, OM[1:0] is used for this purpose.

The control of BWSCON, BANKCON0-7, REFRESH, BANKSIZE, MRSRB6/7 is performed when system reset, by special command, LDMIA and STMIA. Sample code for special register configuration is described below.

Sample code for special register configuration

```

LDR      r0, =SMRDATA
LDMIA    r0, {r1-r13}
LDR      r0, =0x01c80000    ;BWSCON Address
STMIA    r0, {r1-r13}

. . . . .

SMRDATA
DCD 0x22221210    ;BWSCON
DCD 0x00000600    ;GCS0
DCD 0x00000700    ;GCS1
DCD 0x00000700    ;GCS2
DCD 0x00000700    ;GCS3
DCD 0x00000700    ;GCS4
DCD 0x00000700    ;GCS5
;DCD 0x0001002a    ;GCS6 EDO DRAM(Trcd=3,Tcas=2,Tcp=1,CAN=10)
;DCD 0x0001002a    ;GCS7 EDO DRAM(Trcd=3,Tcas=2,Tcp=1,CAN=10)
DCD 0x00018000    ;GCS6 SDRAM(Trcd=2,SCAN=8)
DCD 0x00018000    ;GCS7 SDRAM(Trcd=2,SCAN=8)
DCD 0x00a60000+953;Refresh(REFEN=1,TREFMD=0,Trp=3.5(D)or 4(SD),
;          Trc=5(S), Tchr=3(D),Ref CNT)
DCD 0x0           ;Bank size, 32MB/32MB
DCD 0x20          ;MRSR 6(CL=2)
DCD 0x20          ;MRSR 7(CL=2)

```

ROM/SRAM BANKS DESIGN

The ROM/SRAM banks 1-7, can have a various width of data bus, and the bus width is controlled by S/W. A sample design for ROM/SRAM bank 1-7 is shown in Figure 4-6, Figure 4-7, Figure 4-8 and Figure 4-9.

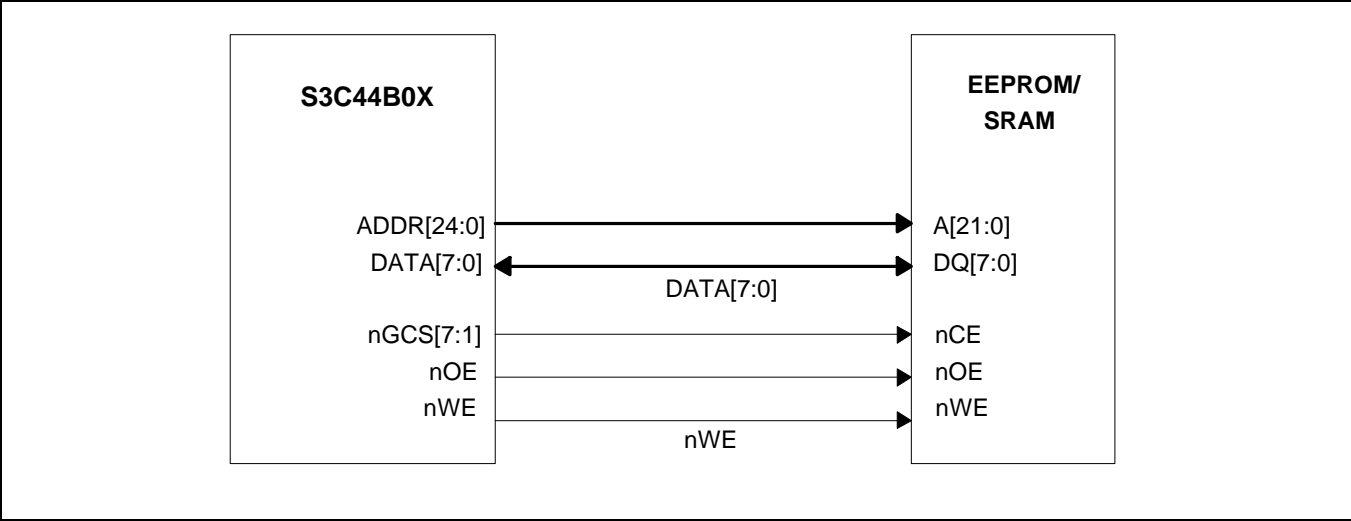


Figure 4-6 One-byte EEPROM/SRAM Banks Design

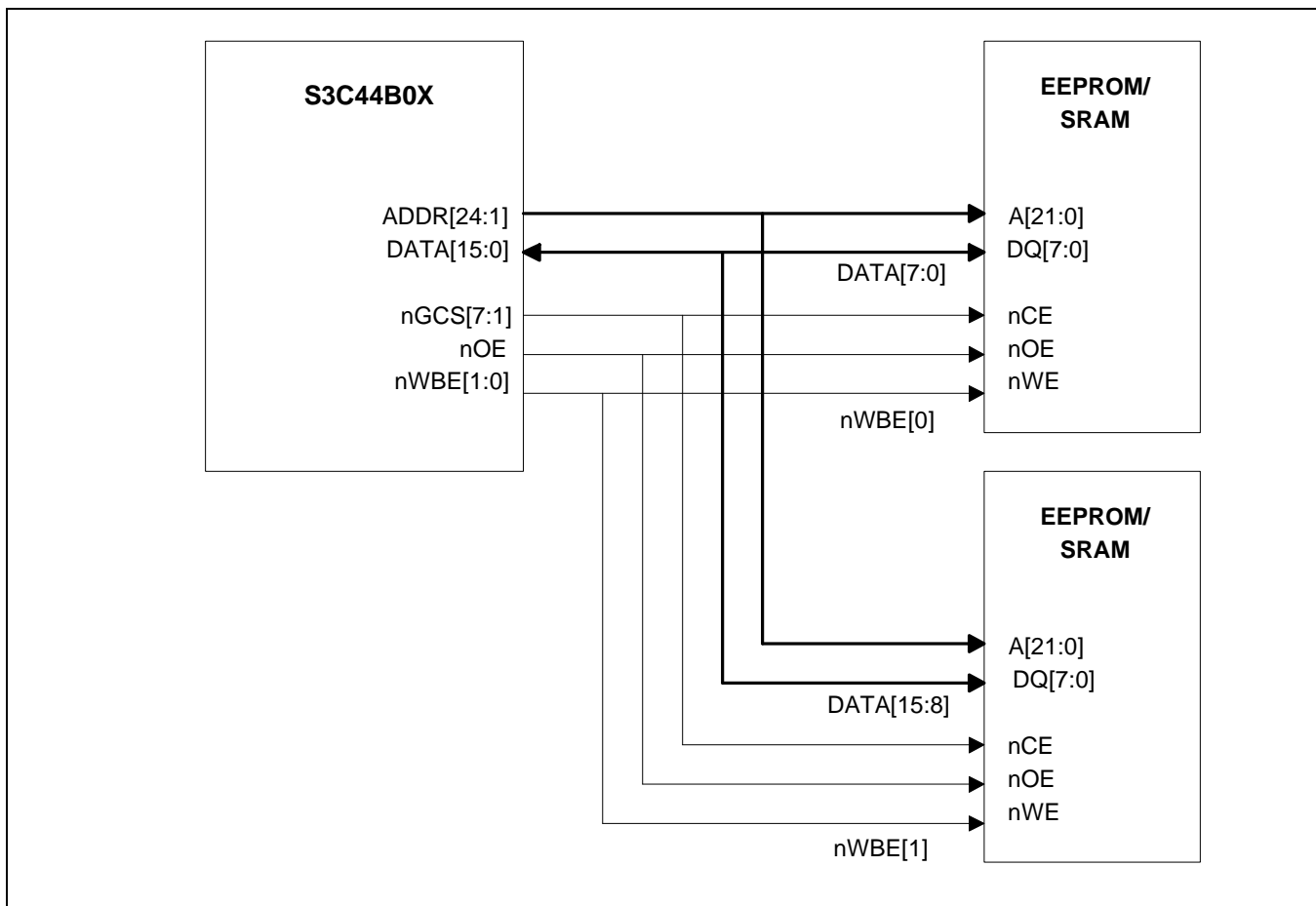


Figure 4-7 Half-word EEPROM/SRAM Banks Design

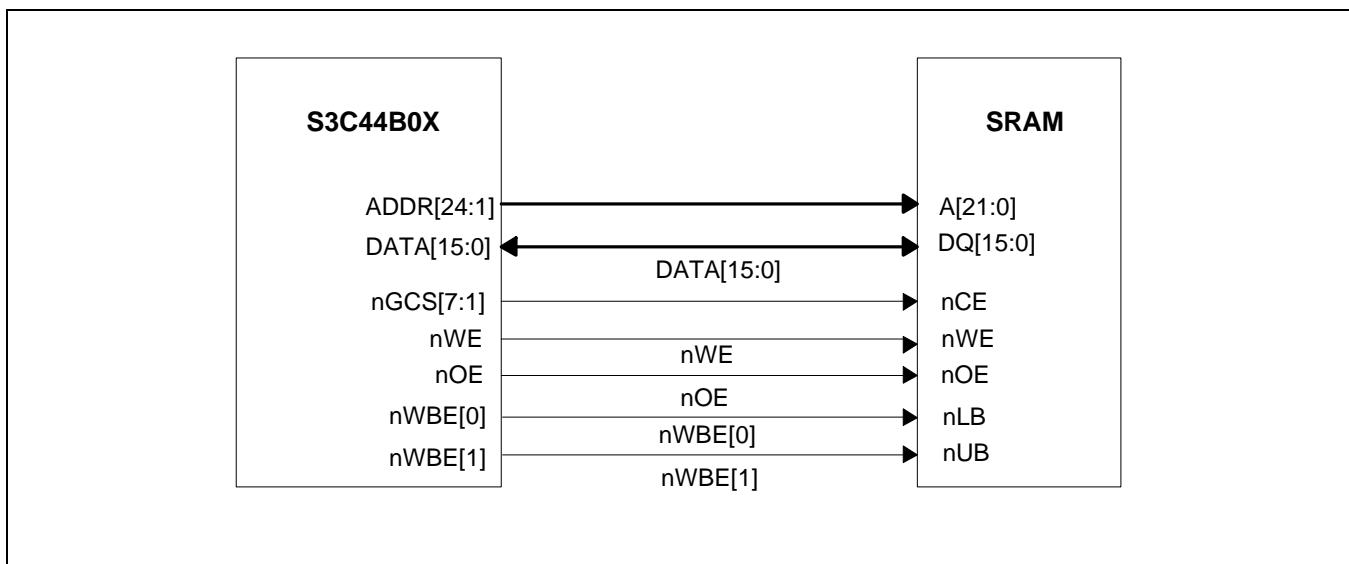


Figure 4-8 Half-word SRAM Banks Design with Half-word SRAM

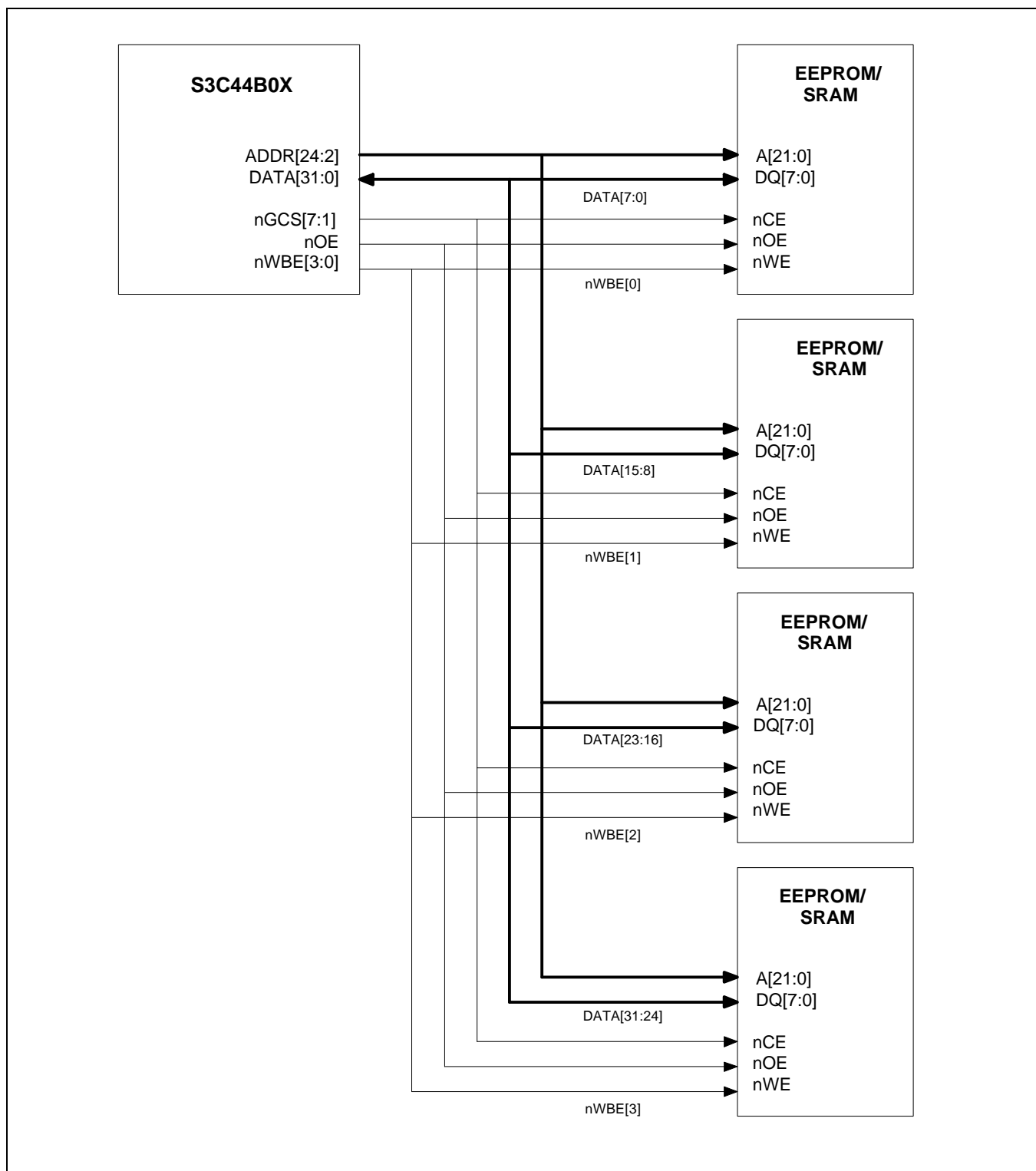


Figure 4-9 Word EEPROM/SRAM banks design

EDO DRAM BANKS DESIGN FOR S3C44B0X

The DRAM banks 6-7, can have a various width of data bus, and the bus width is controlled by S/W, A BWSCON special register set. A sample design for DRAM bank 6-7 is shown in Figure 4-10 and Figure 4-11.

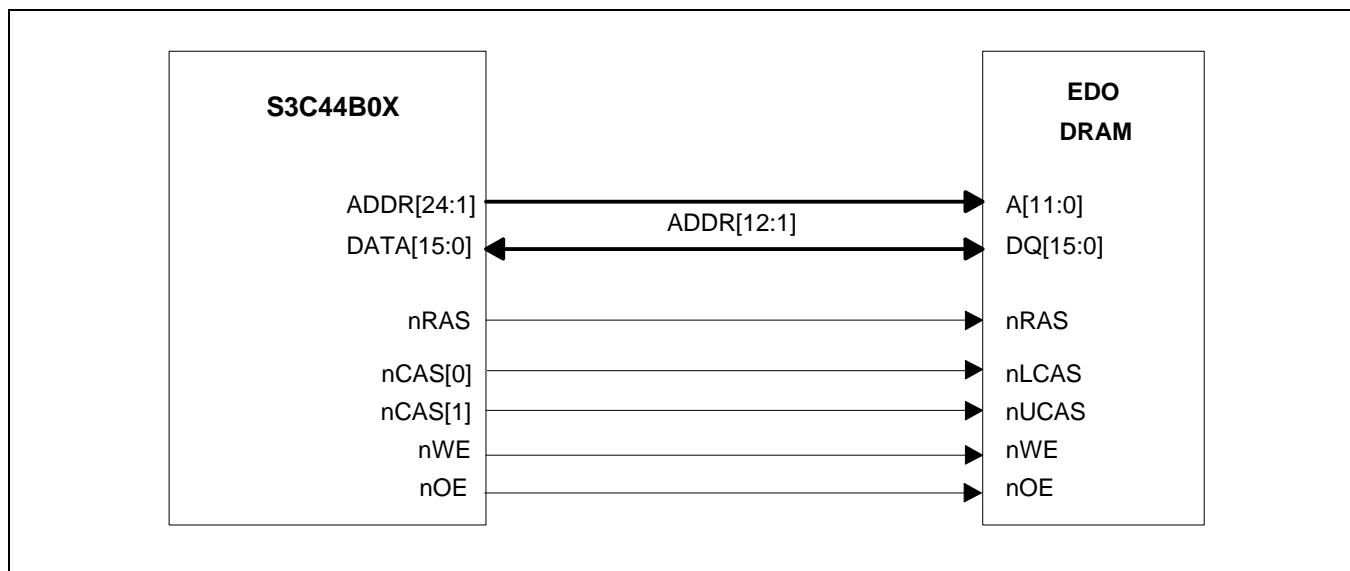


Figure 4-10 Half-Word EDO/Normal DRAM Banks Design

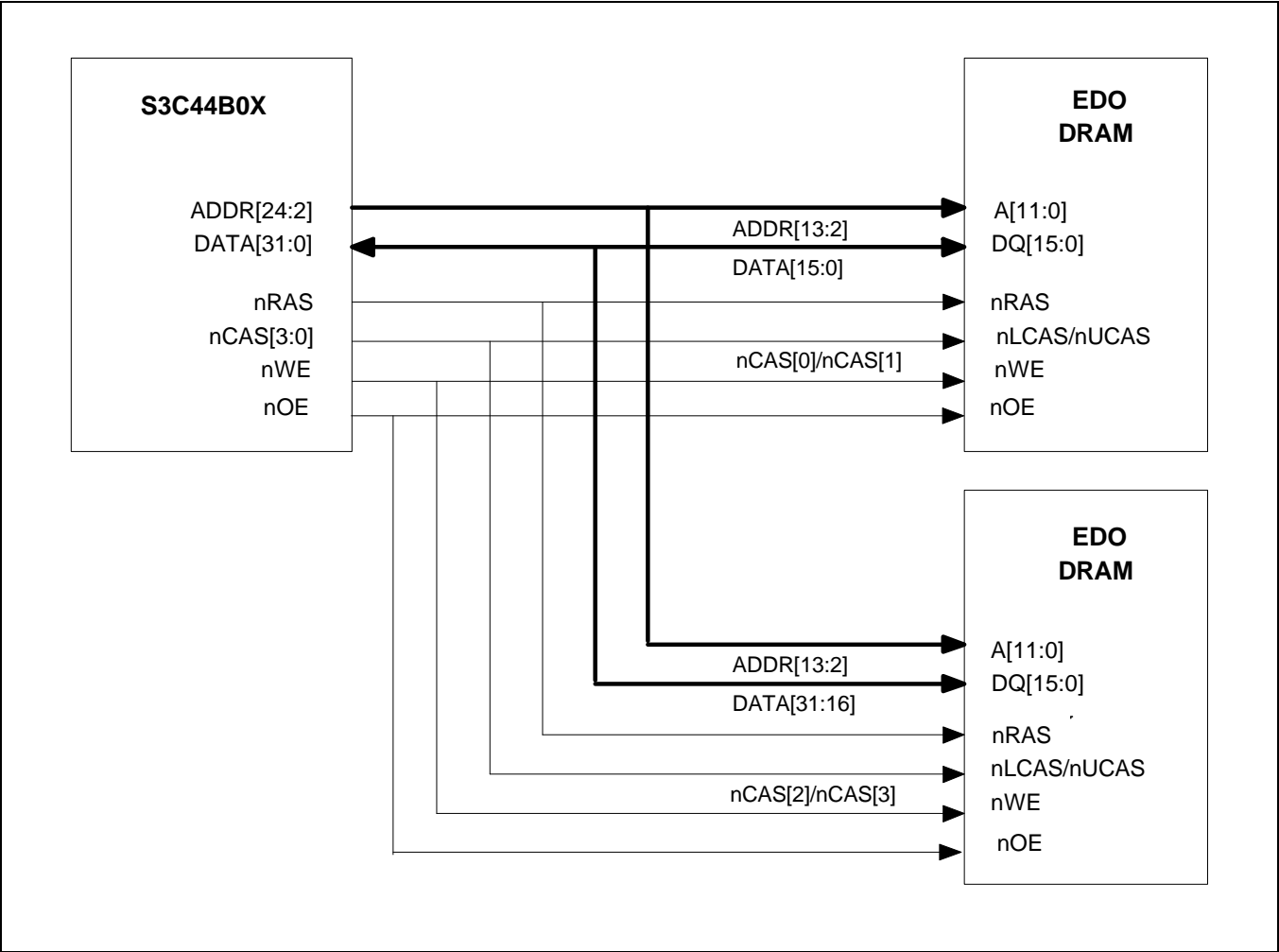


FIGURE 4-11 WORD EDO/NORMAL DRAM BANK

SDRAM BANKS DESIGN FOR S3C44B0X

The S3C44B0X Synchronous DRAM interface features are as follows :

- Maximum column address of SDRAM: 10 bit
- CAS latency: 2/3 cycle

Table 4-3 SDRAM Bank Address configuration

Bank Size	Bus Width	Base Component	Memory Configuration	Bank Address
2MByte	x8	16Mbit	(1M x 8 x 2Bank) x 1	A20
	x16		(512K x 16 x 2B) x 1	
4MB	x8	16Mb	(2M x 4 x 2B) x 2	A21
	x16		(1M x 8 x 2B) x 2	
	x32		(512K x 16 x 2B) x 2	
8MB	x16	16Mb	(2M x 4 x 2B) x 4	A22
	x32		(1M x 8x 2B) x 4	
	x8	64Mb	(4M x 8 x 2B) x 1	A[22:21]
	x8		(2M x 8 x 4B) x 1	
	x16		(2M x 16 x 2B) x 1	A22
	x16		(1M x 16 x 4B) x 1	A[22:21]
	x32		(512K x 32 x 4B) x 1	
16MB	x32	16Mb	(2M x 4 x 2B) x 8	A23
	x8	64Mb	(8M x 4 x 2B) x 2	
	x8		(4M x 4 x 4B) x 2	A[23:22]
	x16		(4M x 8 x 2B) x 2	A23
	x16		(2M x 8 x 4B) x 2	A[23:22]
	x32		(2M x 16 x 2B) x 2	A23
	x32		(1M x 16 x 4B) x 2	A[23:22]
	x8	128Mb	(4M x 8 x 4B) x 1	
	x16		(2M x 16 x 4B) x 1	
32MB	x16	64Mb	(8M x 4 x 2B) x 4	A24
	x16		(4M x 4 x 4B) x 4	A[24:23]
	x32		(4M x 8 x 2B) x 4	A24
	x32		(2M x 8 x 4B) x 4	A[24:23]
	x16	128Mb	(4M x 8 x 4B) x 2	
	x32		(2M x 16 x 4B) x 2	
	x8	256Mb	(8M x 8 x 4B) x 1	
	x16		(4M x 16 x 4B) x 1	

The required SDRAM interface pin is CKE, SCLK, nSCS[1:0], nSCAS, nSRAS, DQM[3:0], ADDR[12]/AP. The sample design with SDRAM is shown in Figure 4-12, and Figure 4-13.

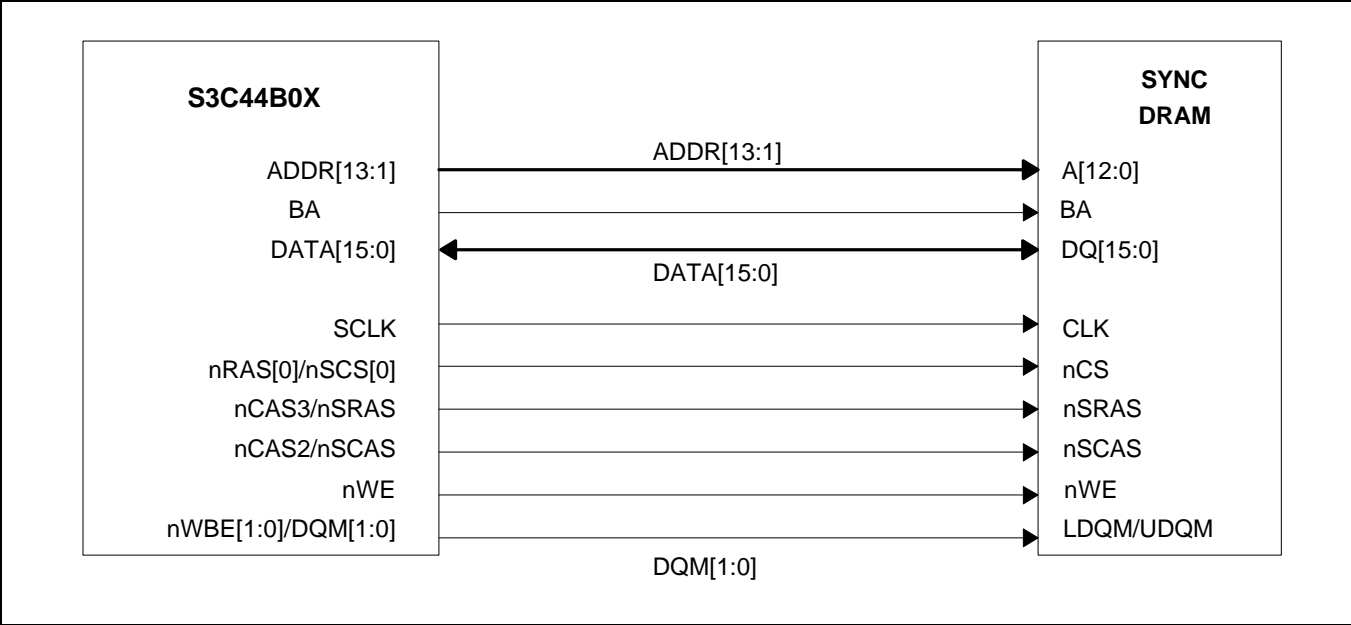


Figure 4-12 Half-word SDRAM Design with Half-word Component

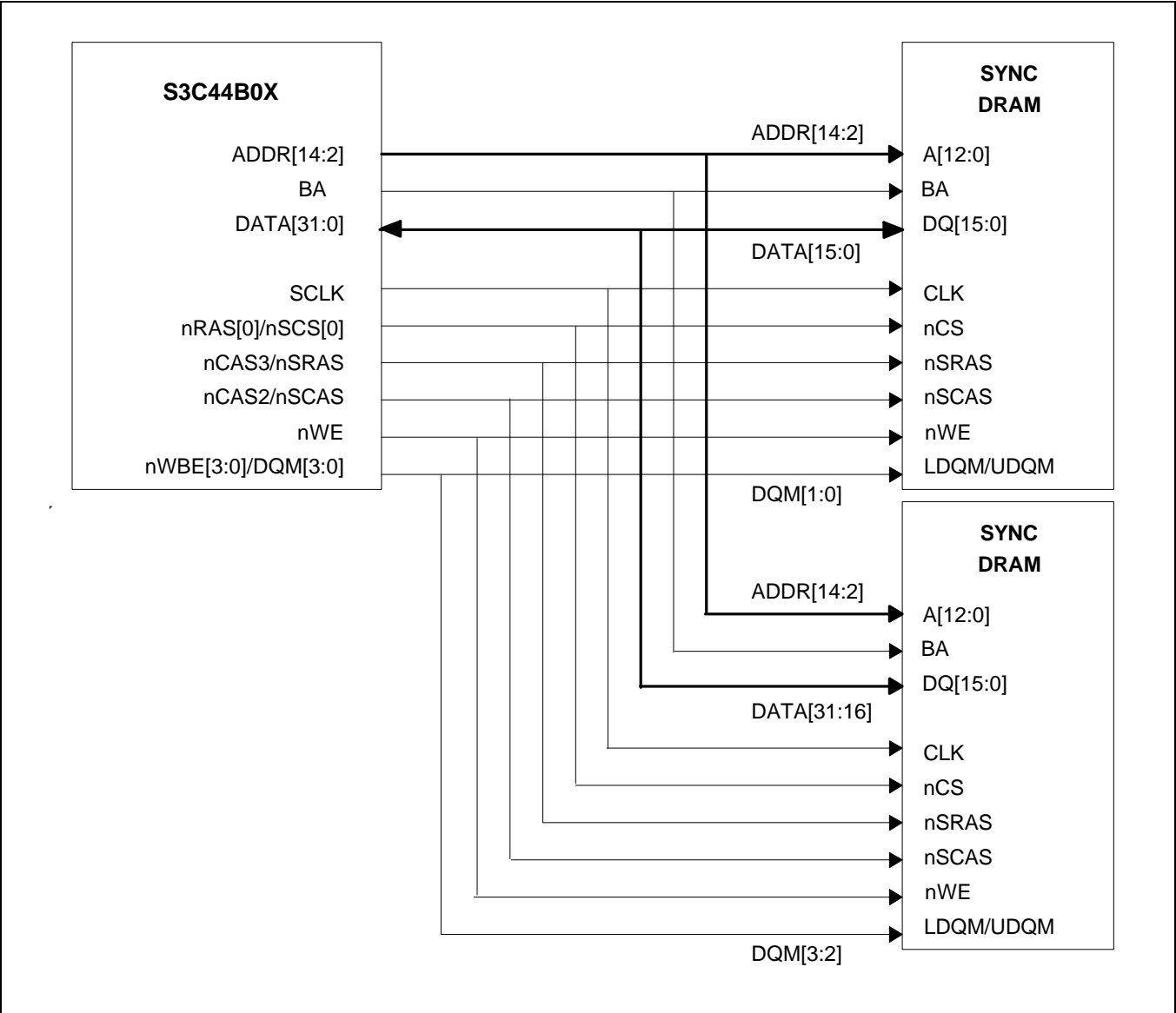


Figure 4-13 Word SDRAM Design with Half-word Component

I/O PORT CONFIGURATION

S3C44B0X has multiplexed input/output/function port pins. The SMDK41100 demo board uses only some functions, then some pins are float or some pins have selectable function port with 0 ohm resistor, therefore users must define the pin's configuration and attach the 0 ohm resistor on the proper place before running the main program.

For reducing the power consumption in SMDK41100, the port state and usage of internal pull-up resistor are decided very carefully. The followings are the sample port configuration for SMDK41100.

Port A : Memory address pins

Port	H/W connection	@Normal	@Stop	@Idle
PA0	OPEN	ADDR0		
PA1	ADDR16	ADDR16		
PA2	ADDR17	ADDR17		
PA3	ADDR18	ADDR18		
PA4	ADDR19	ADDR19		
PA5	ADDR20	ADDR20		
PA6	BA0	ADDR21		
PA7	BA1	ADDR22		
PA8	OPEN	ADDR23		
PA9	OPEN	ADDR24		
PDATA	-	-		
PCONA	-	0x3ff		

Port B : Memory control and output(LED) pins

Port	H/W Connection	@Normal	@Stop(data)	@Idle
PB0	SCKE	SCKE		
PB1	SCLK	SCLK		
PB2	nSCAS	nSCAS		
PB3	nSRAS	nSRAS		
PB4	DQM0	nWBE2/nBE2/DQM2		
PB5	DQM1	nWBE3/nBE3/DQM3		
PB6	OPEN	nGCS1		
PB7	OPEN	nGCS2		
PB8	OPEN	nGCS3		
PB9	LED	Output	Output(High)	Output
PB10	LED	Output	Output(High)	Output
PDATB	-	-	0x600	-
PCONB	-	0x1ff		

Port C : IIS, LCD data and UART control pins.

Not used function pins are defined input port with pull-up resistor enabled to reduce the power consumption. If the UART function is not used the pins should be disabled pull-up resistor, output signal(Tx, nRTS) is defined output port and input signal(Rx, nCTS) is defined input port avoid conflicting the signals of MAX3232.

Port	H/W Connection	@ Normal(data, pull-up)	@ Stop(data, pull-up)	@ Idle(data, pull-up)
PC0	IISLRCK	Input(pull-up enable)		
PC1	IISDO	Input(pull-up enable)		
PC2	IISDI	Input(pull-up enable)		
PC3	IISCLK	Input(pull-up enable)		
PC4	VD7	Input(pull-up enable)		
PC5	VD6	Input(pull-up enable)		
PC6	VD5	Input(pull-up enable)		
PC7	VD4	Input(pull-up enable)		
PC8	OPEN	Input(pull-up enable)		
PC9	OPEN	Input(pull-up enable)		
PC10	nRTS1	Output(High, pull-up disable)		
PC11	nCTS1	Input(pull-up disable)		
PC12	TxD1	Output(High, pull-up disable)		
PC13	RxD1	Input(pull-up disable)		
PC14	nRTS0	Output(High, pull-up disable)		
PC15	nCTS0	Input(pull-up disable)		
PDATC	-	0x5400		
PUPC	-	0xfc00		
PCONC	-	0x11100000		

Port D : LCD data and LCD control pins.

Port	H/W Connection	@ Normal(pull-up)	@ Stop(data, pull-up)	@ Idle(pull-up)
PD0	VD0	VD0(pull-up disable)	Output(High,pull-up disable)	VD0(pull-up disable)
PD1	VD1	VD1(pull-up disable)	Output(High,pull-up disable)	VD1(pull-up disable)
PD2	VD2	VD2(pull-up disable)	Output(High,pull-up disable)	VD2(pull-up disable)
PD3	VD3	VD3(pull-up disable)	Output(High,pull-up disable)	VD3(pull-up disable)
PD4	VCLK	VCLK(pull-up disable)	Output(High,pull-up disable)	VCLK(pull-up disable)
PD5	VLINE	VLINE(pull-up disable)	Output(High,pull-up disable)	VLINE(pull-up disable)
PD6	VM	VM(pull-up disable)	Output(High,pull-up disable)	VM(pull-up disable)
PD7	VFRAME	VFRAME(pull-up disable)	Output(High,pull-up disable)	VFRAME(pull-up disable)
PDATD	-	-	0xff	-
PUPD	-	0xff	0xff	0xff
PCOND	-	0xaaaa	0x5555	0xaaaa

Port E : UART control pins and ENDIAN pin.

PE8 port should be defined input port with disabled pull-up resistor, because the PE8 pin is connected to GND for little endian mode in SMDK41100 demo board.

Port	H/W Connection	@Normal(pull-up)	@Stop(pull-up)	@Idle(pull-up)
PE0	OPEN	Input(pull-up enable)		
PE1	TxD0	TxD0(pull-up disable)		
PE2	RxD0	RxD0(pull-up disable)		
PE3	OPEN	Input(pull-up enable)		
PE4	OPEN	Input(pull-up enable)		
PE5	OPEN	Input(pull-up enable)		
PE6	OPEN	Input(pull-up enable)		
PE7	OPEN	Input(pull-up enable)		
PE8	ENDIAN	ENDIAN(pull-up disable)		
PDATE	-	-		
PUPE	-	0x106		
PCONE	-	0x28		

Port F : IIS and SIO control pins.

PF0 and PF1 pins should be defined disabled pull-up resistor input port, because these pins are connected pull-up resistors by hardware.

Port	H/W Connection	@Normal(pull-up)	@Stop(pull-up)	@Idle(pull-up)
PF0	IIC_SCL	Input(pull-up disable)		
PF1	IIC_SDA	Input(pull-up disable)		
PF2	OPEN	Input(pull-up enable)		
PF3	OPEN	Input(pull-up enable)		
PF4	OPEN	Input(pull-up enable)		
PF5	SIOTxD	Input(pull-up enable)		
PF6	SIORDY	Input(pull-up enable)		
PF7	SIORxD	Input(pull-up enable)		
PF8	SIOCLK	Input(pull-up enable)		
PDATAF	-	-		
PUPF	-	0x3		
PCONF	-	0x0		

Port G : External interrupt pins.

The SMDK41100 demo board is using PG4 and PG5 ports as external interrupt ports with button.

Port	H/W Connection	@Normal(pull-up)	@Stop(pull-up)	@Idle(pull-up)
PG0	EINT0	Input(pull-up enable)		
PG1	EINT1	Input(pull-up enable)		
PG2	EINT2	Input(pull-up enable)		
PG3	EINT3	Input(pull-up enable)		
PG4	EINT4	Input(pull-up disable)		
PG5	EINT5	Input(pull-up disable)		
PG6	OPEN	Input(pull-up enable)		
PG7	OPEN	Input(pull-up enable)		
PDATG	-	-		
PUPG	-	0x30		
PCONG	-	0x0		

Special pull-up resistor control register

In normal operation, the pull-up resistor should be disabled but in stop mode it is enabled for power consumption.

Connection	@Normal	@Stop	@Idle
SPUCR0	Pull-up disable	Pull-up enable	Pull-up disable
SPUCR1	Pull-up disable	Pull-up enable	Pull-up disable
Hz@STOP	Previous state	High-impedance	Previous state
SPUCR	0x7	0x0	0x7

NOTE : To reduce power consumption users shall consider the state of pins and refer to the table below.

Usage of Pins	Pull-up resistor + Data
Unused input port pins	Pull-up enable
Normal output port pins	Pull-up disable + Data High
Function(address, data, control) pins	Pull-up disable

LCD CONNECTION WITH S3C44B0X

The S3C44B0X LCD interface example circuit is as follows :

- UG-32F04(320x240 mono STN LCD) from SAMSUNG DISPLAY DEVICES CO.,LTD (refer to Figure 4-14)
. TL497CAN can be used to make VEE(-25V).
- UG-24U03A(320x240 mono STN LCD) from SAMSUNG DISPLAY DEVICES CO.,LTD (refer to Figure 4-15)
. VEE is generated by the circuit on LCD module.
. VL is 2.4V typically.
. DISPON H : display on, L : display off
. nEL_ON H : EL off L : EL on
- KHS038AA1AA-G24 (256 color STN LCD) from KYOCERA Co. (refer to Figure 4-16)
. DISP signal can be made using I/O port, or power control circuit, or nRESET circuit.
. V1-V5 can be made using the power circuit recommended by the LCD specification.

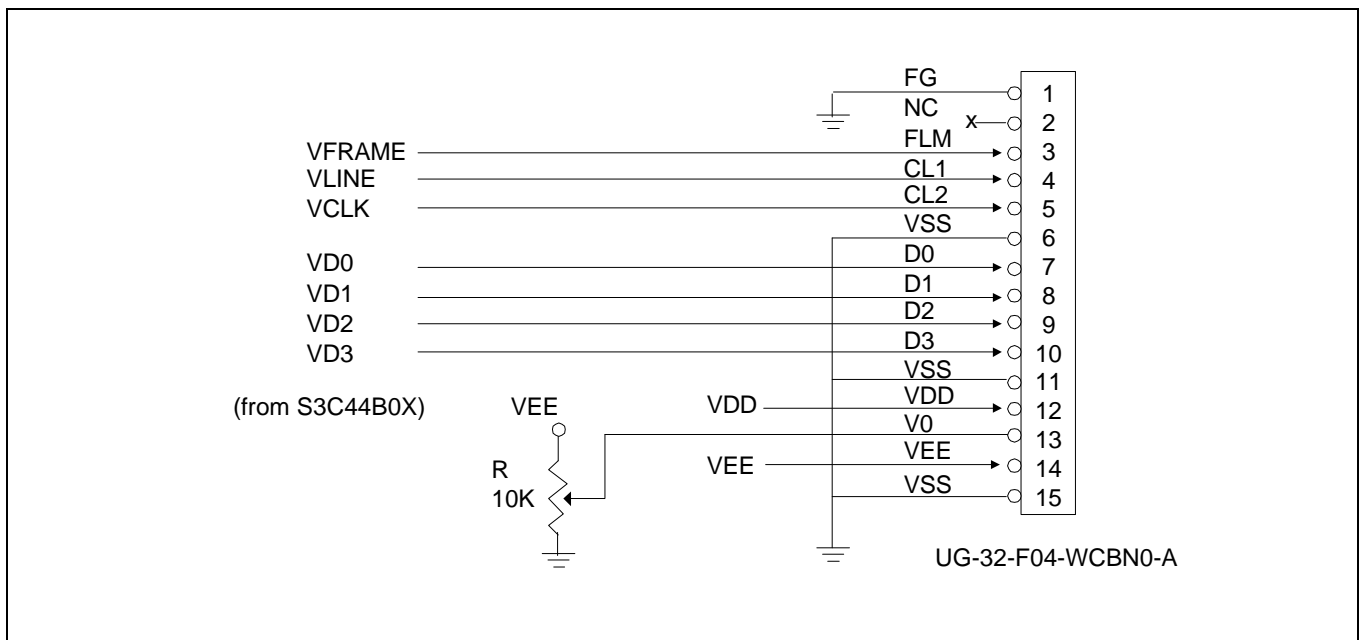


Figure 4-14 UG-32F04 connection with S3C44B0X(320x240 mono STN LCD)

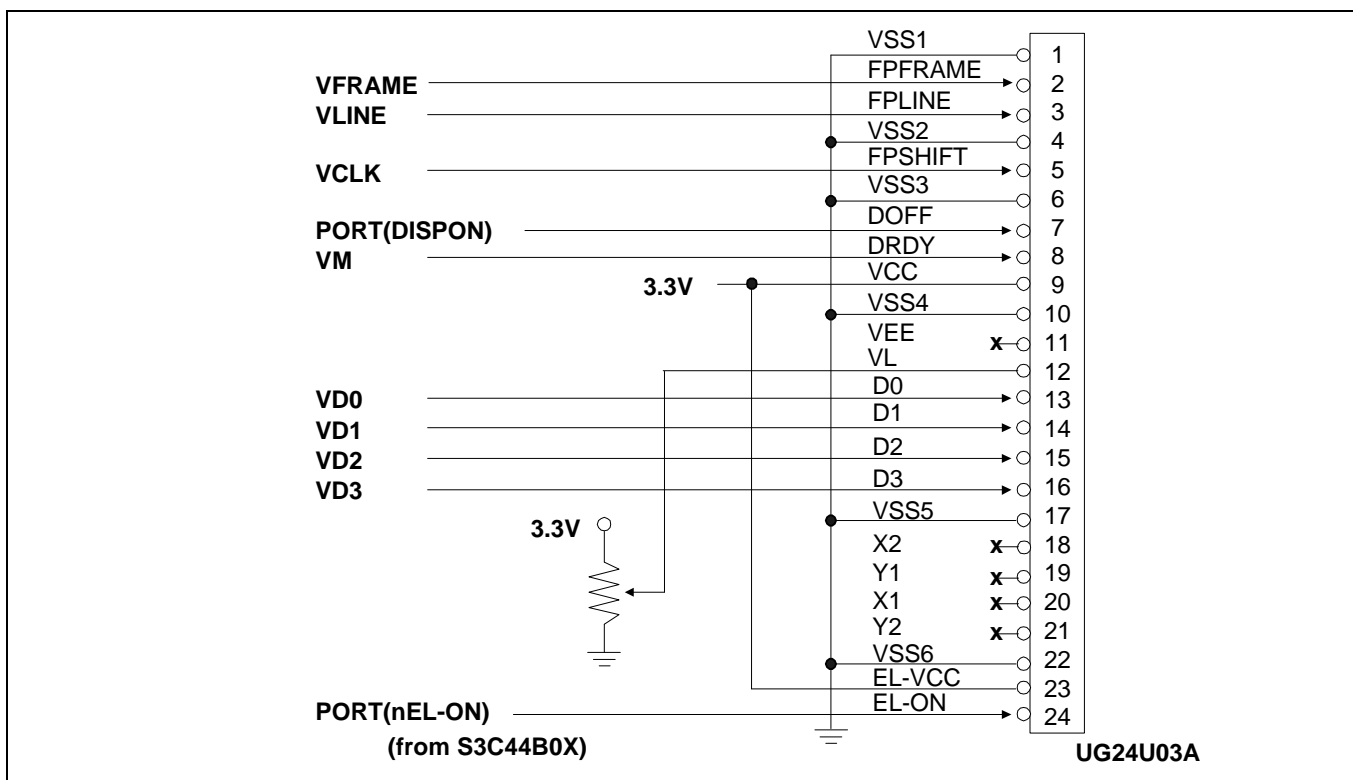


Figure 4-15 UG24U03A connection with S3C44B0X (320x240 mono STN LCD)

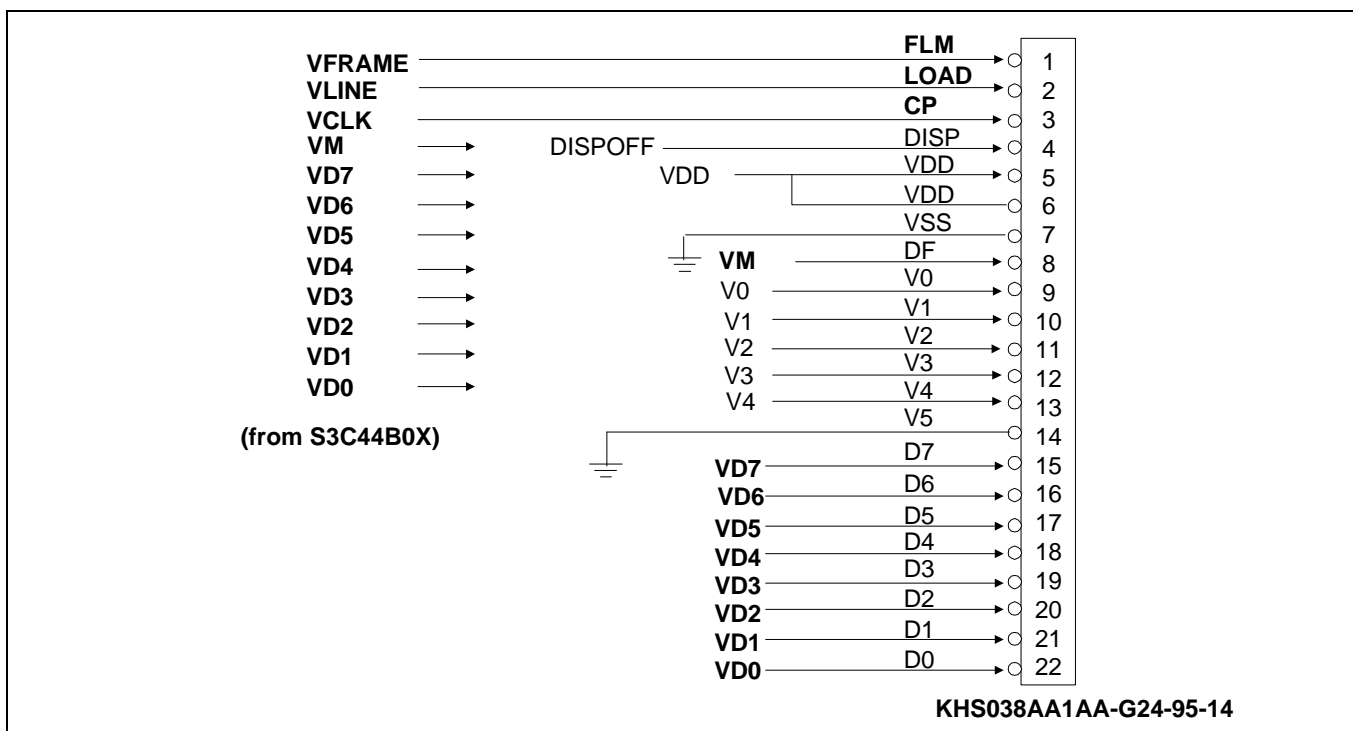


Figure 4-16 KHS038AA1AA-G24 connection with S3C44B0X (256 color STN LCD)

SYSTEM DESIGN WITH DEBUGGER SUPPORT

EmbeddedICE Macrocell and EmbeddedICE Interface

The S3C44B0X has an EmbeddedICE macrocell that provides debug support for ARM cores. The EmbeddedICE macrocell is programmed in serial using the TAP(Test Access Port) controller on the S3C44B0X. The EmbeddedICE interface is a JTAG protocol conversion unit. It translates a debug protocol message generated by the debugger into a JTAG signal which is sent to the built-in serial and parallel ports.

JTAG port for EmbeddedICE Interface

When you build a system with the S3C44B0X EmbeddedICE interface, you should design a JTAG port for EmbeddedICE interface. Usually, the interface connector is a 14-way box header, and this plug is connected to the EmbeddedICE interface module using 14-way IDC cable.

The JTAG port signals, nTRST, TDI, TMS, TCK have to be connected pulled-up register(10K ohm) externally.

When you operate normal mode without EmbeddedICE, nRESET signal on S3C44B0X is connected nTRST via JP1 (jumper1). In debugger mode, nRESET signal on S3C44B0X is surely separated nTRST via JP1 (jumper1).

The pin configuration and a sample design are described in Figure 4-17, 4-18, respectively.

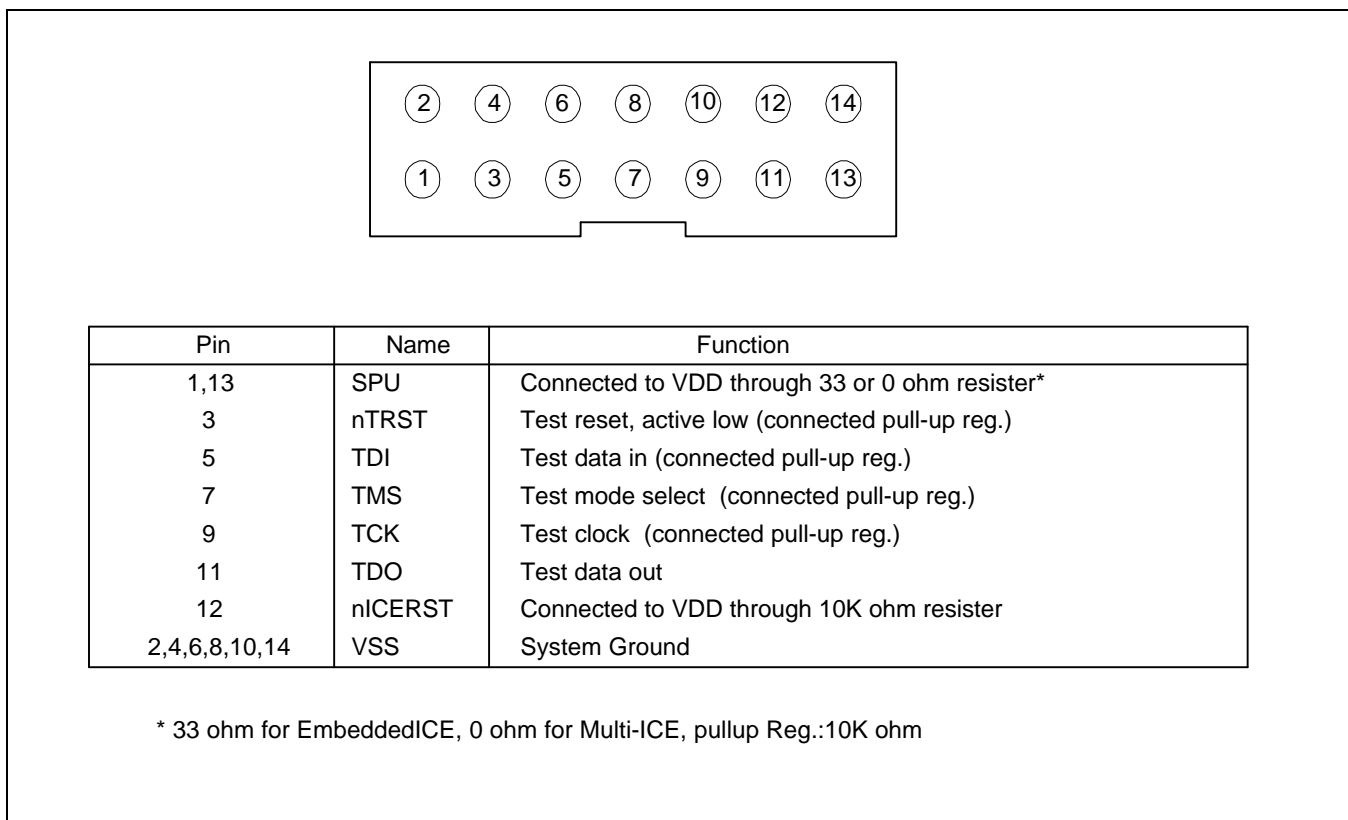


Figure 4-17 EmbeddedICE Interface JTAG Connector

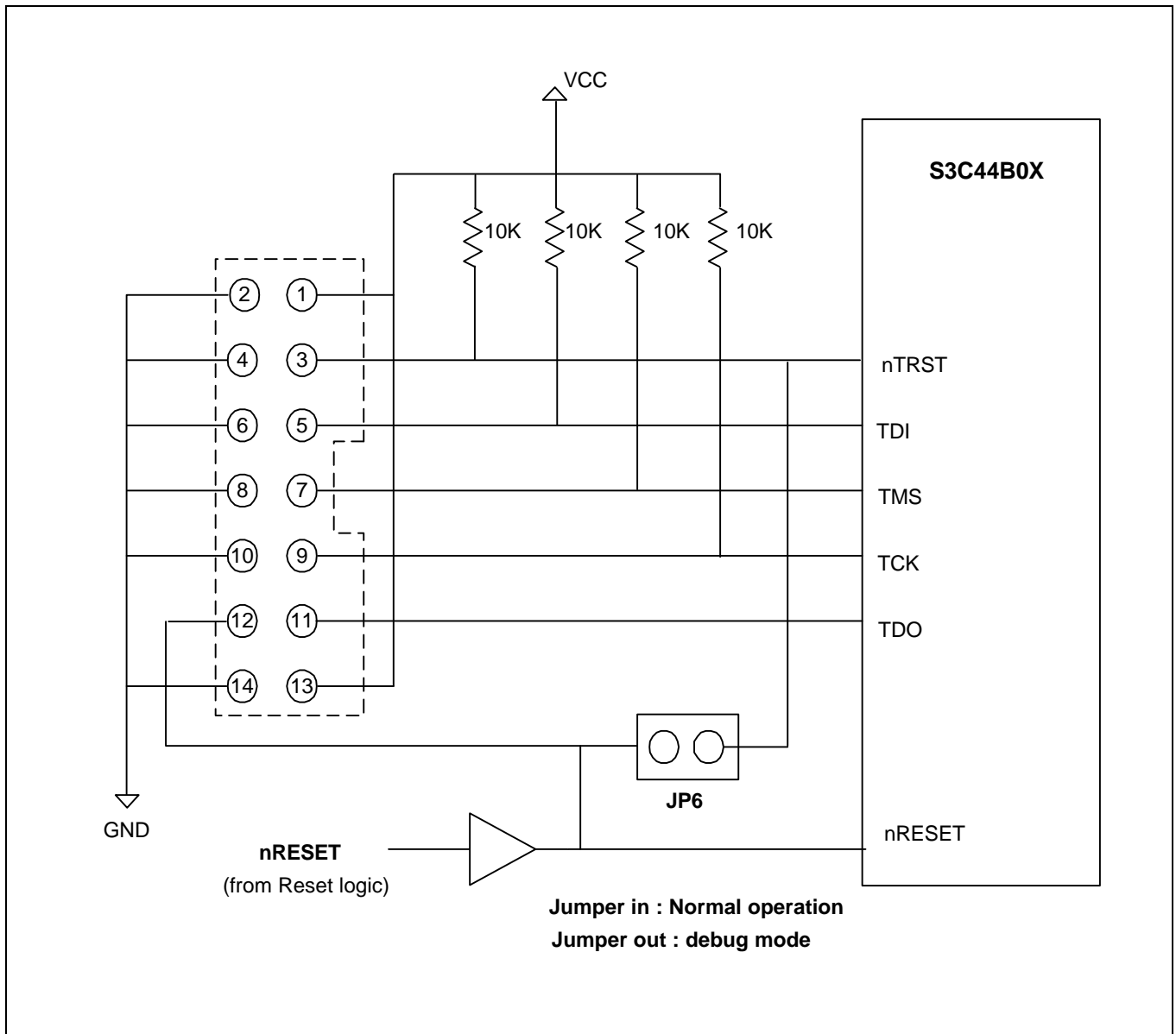


Figure 4-18 EmbeddedICE Interface Design Example

CHECK LIST FOR SYSTEM DESIGN WITH S3C44B0X

When you design a system with the S3C44B0X, you should check a number of items to build a good system. The check list is described below.

- The OM[3:0] and ENDIAN pin have to be configured.
- To run the CPU without using JTAG(ICE), connect nTRST and nRESET pin.
- If EXTCLK pin is used for MCLK, XTAL0 has to be connected to VDD. If XTAL0 pin is used for MCLK, EXTCLK has to be connected to VDD.
- If an input pin is unused, connect the pin to VDD or GND. If the pin is float, S3C44B0X may not operate.
- nGCS6,7 do not support DRAM & SDRAM combination,

Please configure memory type to below combination in bank6 & 7 :

DRAM & DRAM, SDRAM & SDRAM , SRAM & SRAM, SRAM & DRAM, SRAM & SDRAM.

NOTES