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ABOUT SMDK41100 BOARD

SYSTEM OVERVIEW

SMDK41100 (Samsung MCU Development Kit) for S3C44B0X is a platform that is suitable for code development of SAMSUNG's S3C44B0X 16/32-bit RISC microcontroller (General ARM) for hand-held device and general applications.

S3C44B0X consists of 16-/32-bit RISC (ARM7TDMI) CPU core, 8KB cache, optional internal SRAM, LCD controller (up to 256 color DSTN), 2-ch UART with hand-shake(IRDA1.0,16-byte FIFO), 4-ch DMA, System manager (chip select logic, FP/ EDO/SDRAM controller), 6-ch timers with PWM, 71-bit general purpose I/O ports, RTC, 8-ch 10-bit ADC, IIC-BUS interface, IIS-BUS interface, Sync. SIO interface and PLL for clock.

SMDK41100 (Samsung MCU Development Kit) consist of S3C44B0X, boot EEPROM (Flash ROM), EDO DRAM, SDRAM, LCD connect, two serial communication ports, configuration switches, RTC, JTAG interface and status LEDs.

SMDK41100 OVERVIEW

The SMDK41100 (Samsung MCU Development Kit) shows the basic system-based hardware design which uses the S3C44B0X. It can evaluate the basic operations of the S3C44B0X and develop codes for it as well.

When the S3C44B0X is contained in the SMDK41100 (Samsung MCU Development Kit), you can use an in-circuit emulator (ICE).

This allows you to test and debug a system design at the processor level. In addition, the S3C44B0X with embeddedICETM capability can be debugged directly using the EmbeddedICE Interface.

The SMDK41100 (Samsung MCU Development Kit) function blocks are shown in Figure 1-1.

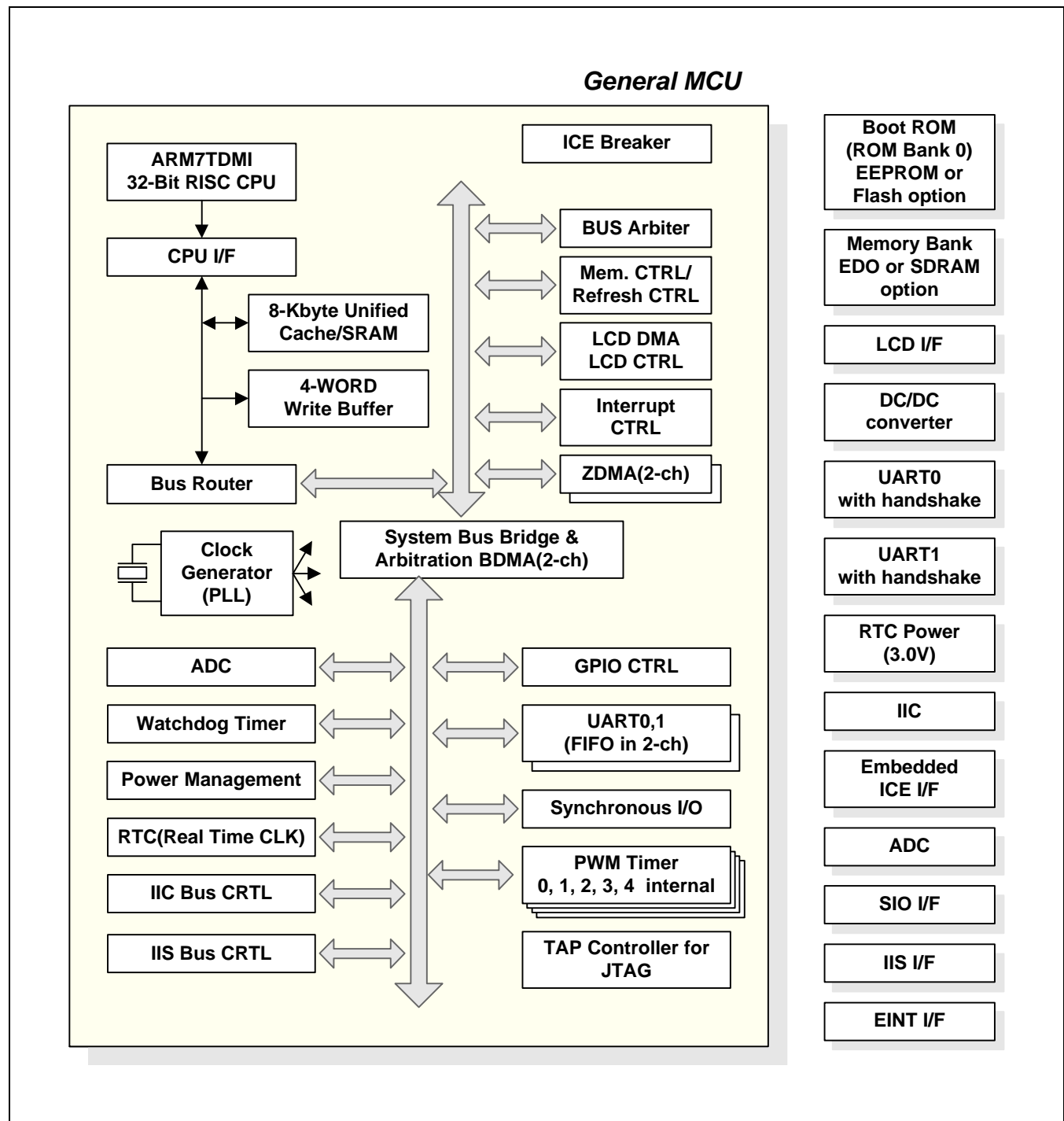


Figure 1-1. SMDK41100 Function Block Diagram

FEATURES

- S3C44B0X: 16/32-bit RISC microcontroller
- X-tal operation
- Boot ROM: 512 K bit, 1 M bit, 8 M bit, support half-word size boot ROM
- DRAM: 4 M x 16 EDO DRAM support
- SDRAM: 4 M x 16 SDRAM support
- 8-bit LCD connector
- General I/O: GIP 2-port & GOP 2-port
- Two-channel UART
- EmbeddedICE™ Interface
- RTC X-tal input & power logic
- IIC : KS24C080 support
- ADC I/F
- SIO I/F
- IIS I/F
- EINT I/F

CIRCUIT DESCRIPTION

SMDK41100 (Samsung MCU Development Kit) consists of logic components, several control/status display block, and a debug interface block. SMDK41100's detailed block diagram, and its components are shown in figure 1-3.

POWER SUPPLY

SMDK41100 (Samsung MCU Development Kit) is designed to operate at 2.5V for core and 3.3V for I/O. Power to SMDK41100 (Samsung MCU Development Kit) is supplied through a DC jack power adapter which supports the voltage between 5V and 9V and drives the current at least 850 mA .

SMDK41100 has distributed power plane, with power going separately to the MCU and the main power plane. For this reason, power jumpers J1, J2, J3 and JP5 are inserted (see Figure 1-2) .

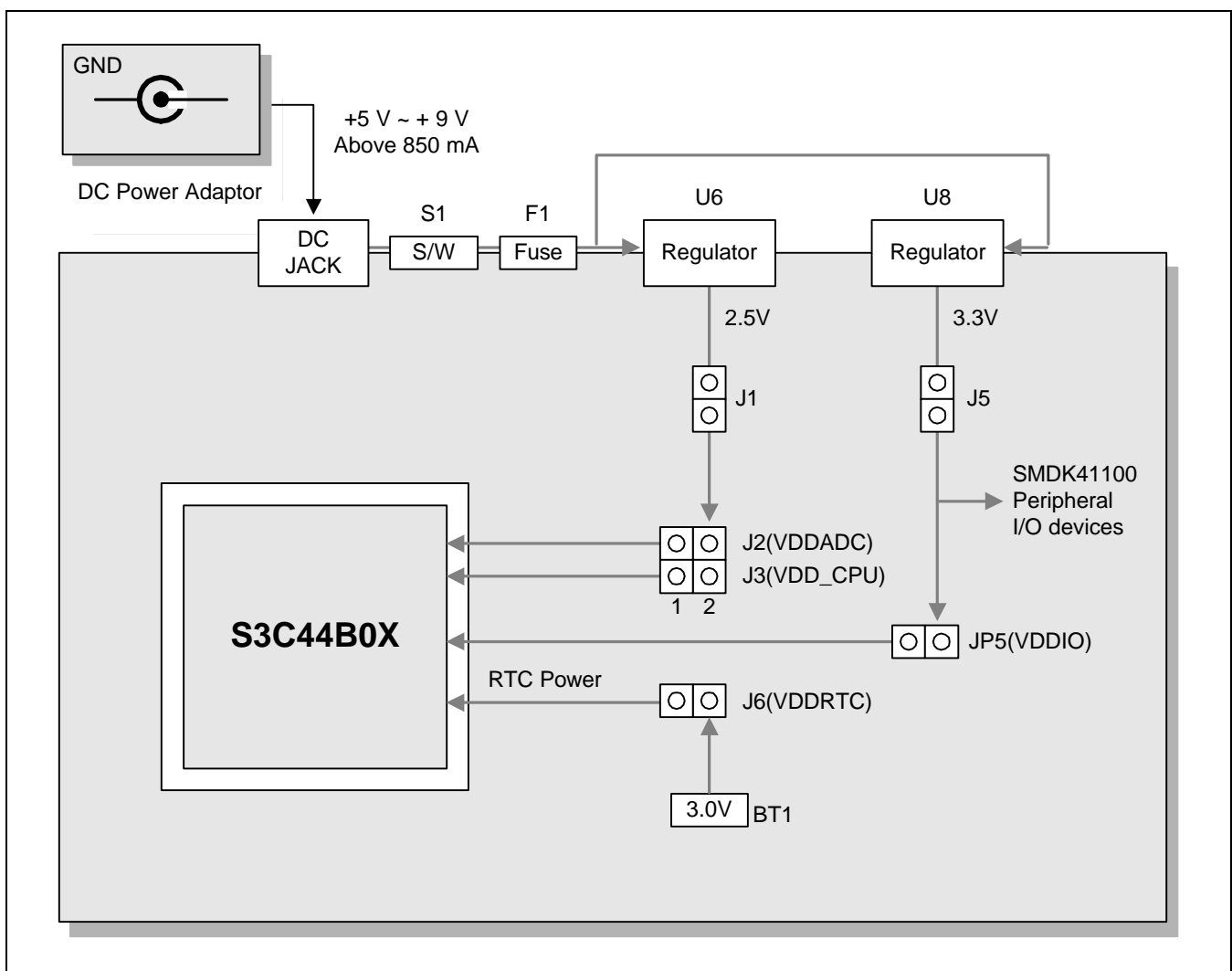


Figure 1-2. SMDK41100 Power Plane

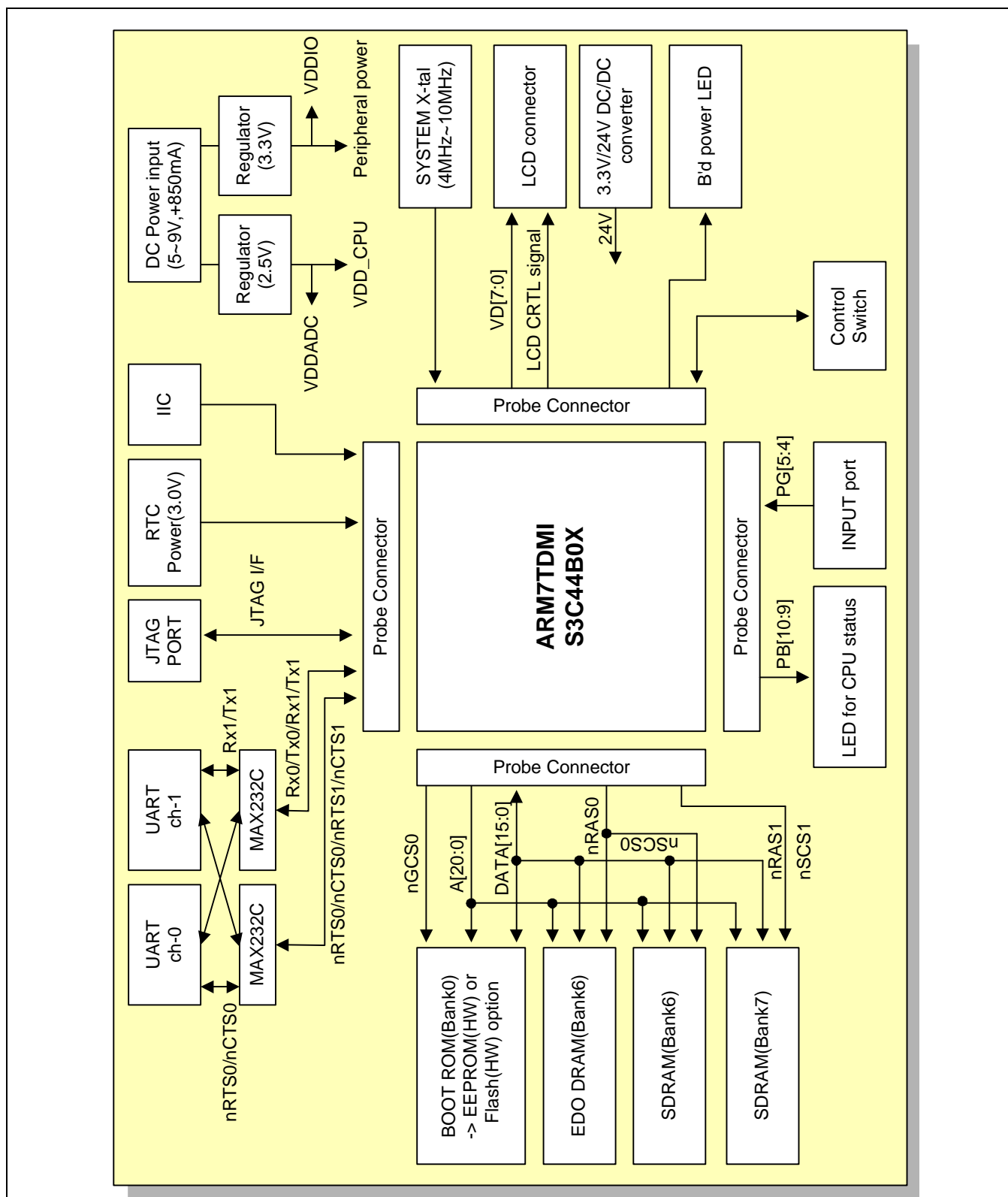


Figure 1-3. Detailed SMDK41100 Board Diagram

CLOCK SOURCE AND DISTRIBUTION

The Following clock source is supported at SMDK41100 target board.

System Clock (MCLK)

Table 1-1 shows the relationship between the mode control pin(OM2 & 3) combination and the clock operating mode. The OM[3:2] status is latched at rising edge of nRESET. (See, Figure 1-4)

Table 1-1. System clock configuration

CLOCK MODE(JUMPER)	Pin Value OM[3:2]	Descriptions	PIN Status
JP9			
Short	00	XTAL0, PLL-on	EXTCLK(#67)=Vdd

NOTES:

1. SMDK41100 provides only XTAL. If you'd like to use oscillator as a external clock, you have to modify our board.
2. If the EXTCLK is used, XTAL0 has to be in H level. If XTAL0, EXTAL0 is used, EXTCLK also has to be in H level.
3. Although the PLL starts to operate just after reset, the PLL output is not used as Fout. Until S/W writes valid settings to the PLLCON register, the crystal clock will be used as Fout directly. After S/W writes to the PLLCON, the PLL output is used as Fout.

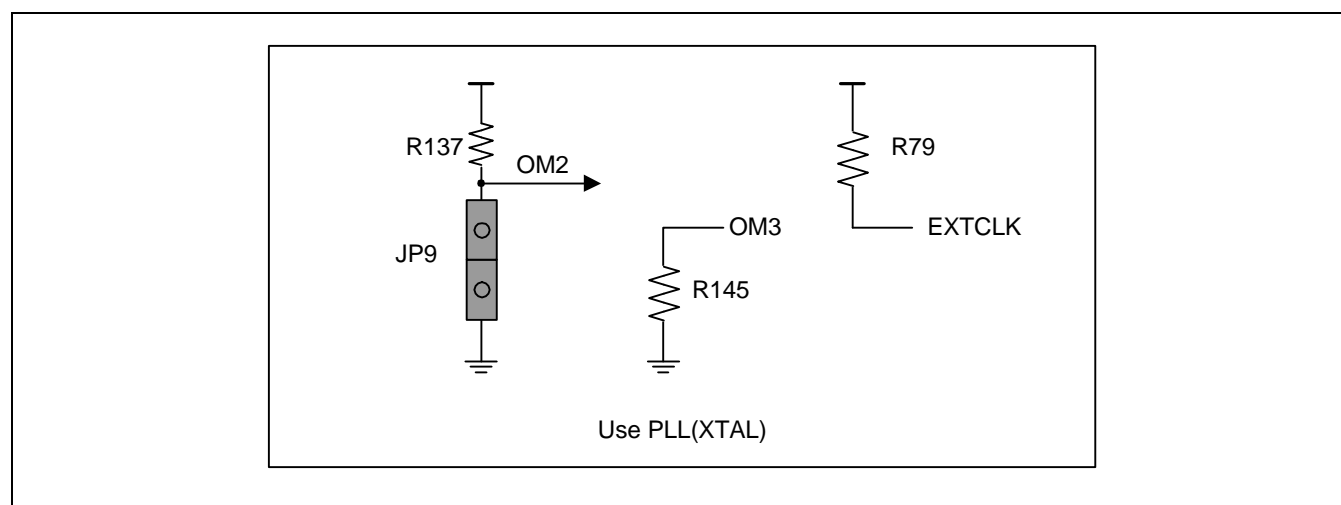


Figure 1-4. SMDK41100 Board System Clock (MCLK) Configurations

RESET LOGIC

The nRESET(System Reset Signal) must be held to low level at least 5 CLK to recognize the reset signal and it takes 128 CLK between the nRESET and internal nRESET. nRESET and nTRST(JTAG Reset signal) should be merged by jumper option. But, if you want to use circuit emulator (ex, Embedded ICE) for debug without BOOT ROM, you should have the nTRST be pull-up. If not, whenever the ADW (ARM Debug Window) were invoked SW interrupt will be occurred.

SMDK41100 SYSTEM CONFIGURATIONS

S3C44B0X supports Big-/Little-endian mode and Byte/Half-word/Word access the data bus. But SMDK41100 supports only Half-word data access in BOOT ROM.

BOOT ROM

You can select EEPROM or Flash memory using jumper option(JP13) for BOOT ROM.

The data bus width of BOOT ROM bank is fixed by Half-word data in SMDK41100.

In EEPROM, you have to open JP13 but in Flash memory you have to remove EEPROM and to close JP13.

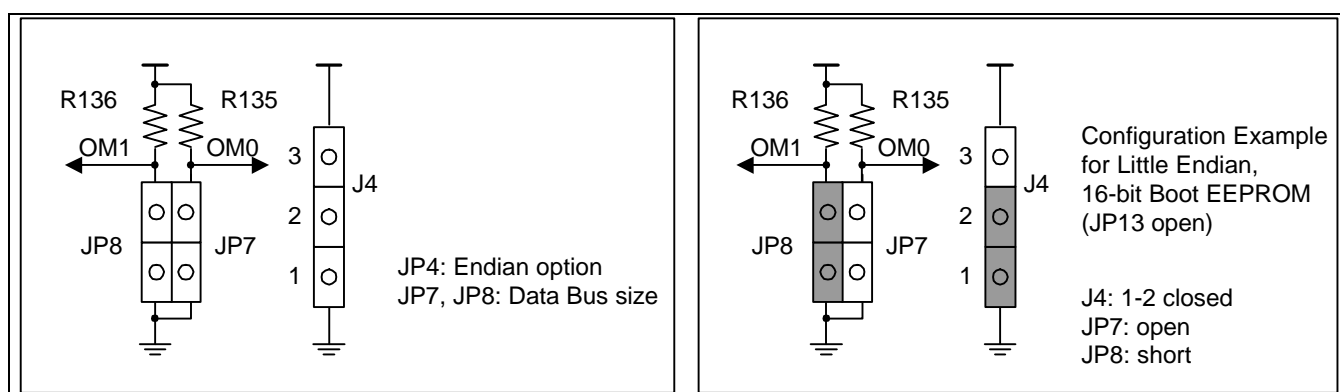


Figure 1-5 SMDK41100 Board Configurations

Table 1-3. ROM Bank0 Data Bus Width

PIN FUNCTIONS	JP8	JP7	PIN value, OM[1:0]	DESCRIPTIONS
ROM Bank0 Data Bus Width Configuration	Short	Open	"01"	16_bit mode

Table 1-4. Endian Mode Configuration

PIN FUNCTIONS	J4(1-2)	J4(2-3)	PIN value	DESCRIPTIONS
Endian Mode Selection	closed	open	"0"	Little endian mode
	open	closed	"1"	Big endian mode.

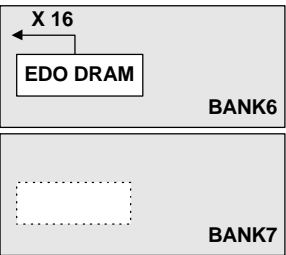
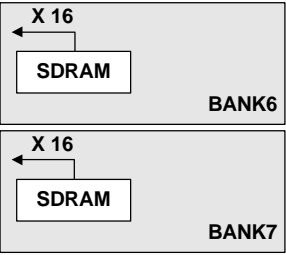
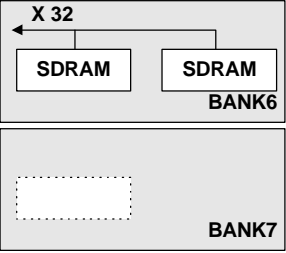
DRAM/SDRAM CONFIGURATIONS

S3C44B0X supports FP DRAM, EDO DRAM and Synchronous DRAM. S3C44B0X's nRAS0 signal simultaneously can be used EDO DRAM and Sync. DRAM on SMDK41100. SDRAM or EDO DRAM can be selected alternatively using SYSCFG register (rBANKCON).

R76/R81 are resistors for selecting memory type of BANK6 and R100/R111 are resistors for selecting the data bus width of BANK6 or BANK7.

So, SMDK41100's DRAM/SDRAM configuration can be summarized in three cases(16bit EDO DRAM mode/16bit SDRAM mode/ 32bit SDRAM mode)

Table 1-5. DRAM/SDRAM Configuration of BANK6 and BANK7

Number of case	R76	R81	R100	R111	Memory Mode	
					Descriptions	Block Diagram
1	Closed	Open	Open	Open	16bit EDO DRAM mode	
2	Open	Closed	Open	Closed	16bit SDRAM mode	
3	Open	Closed	Closed	Open	32bit SDRAM mode	

NOTES:

1. If 32bit data bus width is used in SMDK41100, optional resistors(Data option:R62-R71, R74, R75, R78, R80, R82-R85, R87, R89, R91, R92, R94, R95, R99, R101, R103, R104, R106, R109, R110, R113-R125, R175, R176, Address option:r1-r40) have to be set properly.
2. When the user set the data option, please consider other options(IIS, LCD, UART0 and UART1)

General I/O PORTS

S3C44B0X's general I/O ports are used for DEMO B'd key interrupt input and LED status display. The function of control switch and the status of LED can be defined by user software.

Table 1-6. General I/O Configurations on SMDK41100

General I/O port number	I/O type	Descriptions
PB[10:9]	Output	LED display
PG[5:4]	Input	Key input pad (External interrupt input pins).

LCD INTERFACE

S3C44B0X has LCD controller. The LCD controller has some signal, such as VD[7:0], VM, VFRAME, VCLK. SMDK41100 provides the LCD control signals as follows;

Table 1-7. LCD Interface on SMDK41100

# of hole	Descriptions	# of hole	Descriptions	# of hole	Descriptions	# of hole	Descriptions
1	VSS	6	NC	11	VD0	16	VD5
2	VDD	7	VM	12	VD1	17	VD6
3	VFRAME	8	NC	13	VD2	18	VD7
4	VLINE	9	NC	14	VD3	19	NC
5	VCLK	10	NC	15	VD4	20	NC

SIO INTERFACE

S3C44B0X has SIO(Synchronous I/O). SMDK41100 provides the SIO(JP11) signals as follows;

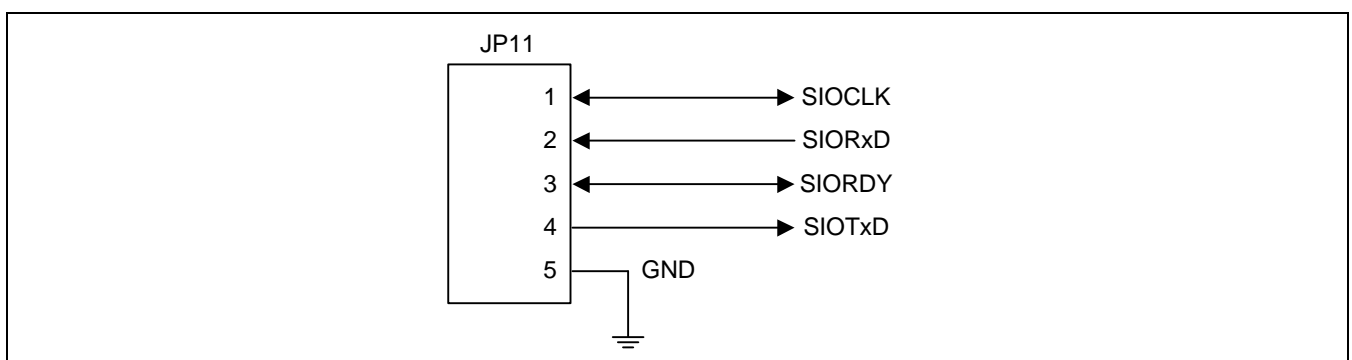


Figure 1-6 SIO Interface on SMDK41100

IIS Interface

S3C44B0X has IIS(Inter IC Sound).
SMDK41100 provides the IIS(JP10) signals as follows;

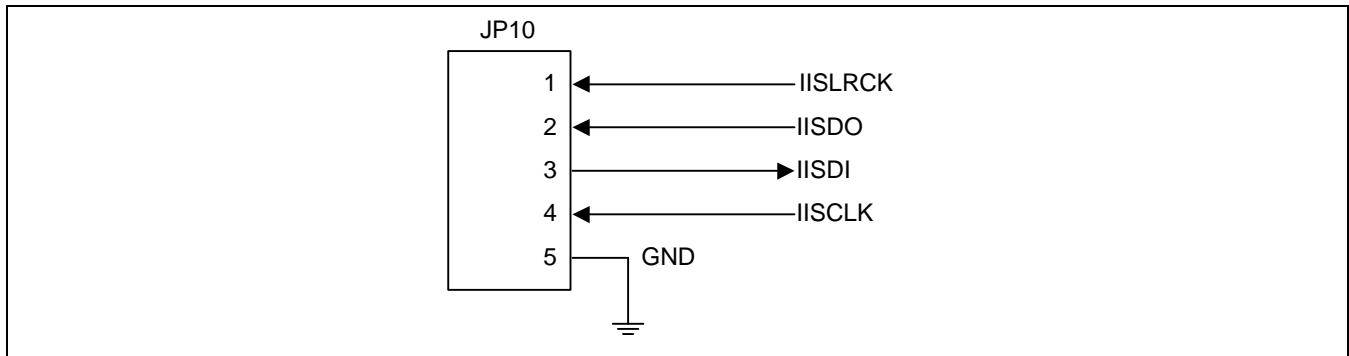


Figure 1-7 IIS Interface on SMDK41100

ExINT INTERFACE

There are four ExINT(External Interrupt) interface in SMDK41100. SMDK41100 provides the ExINT(JP14) signals as follows;

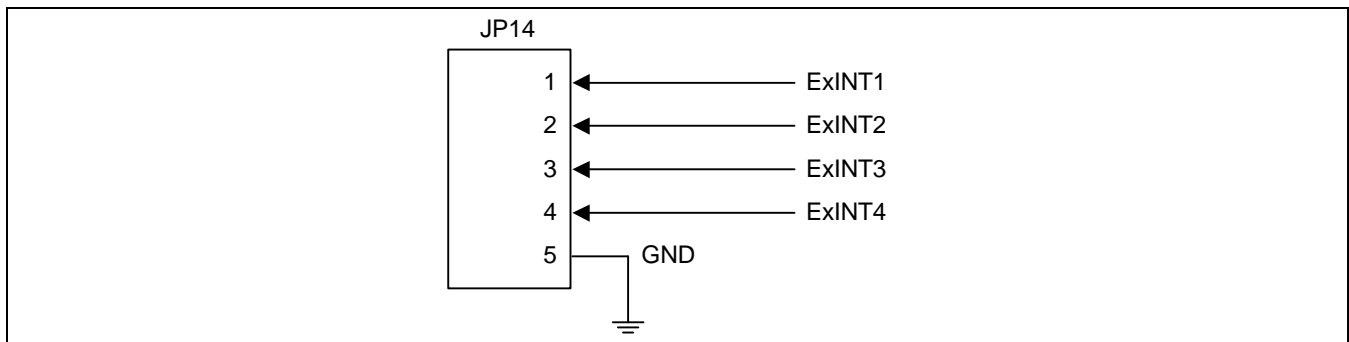


Figure 1-8 ExINT Interface on SMDK41100

A/D CONVERTER INTERFACE

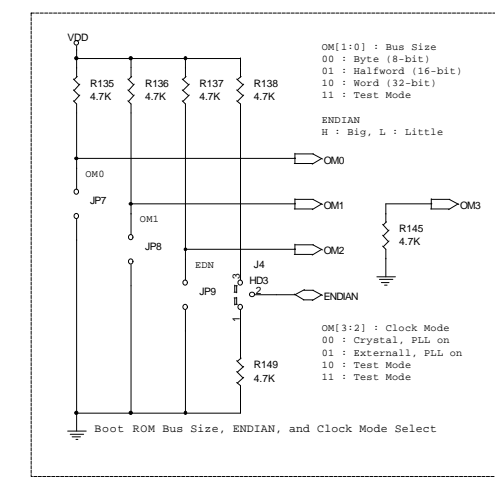
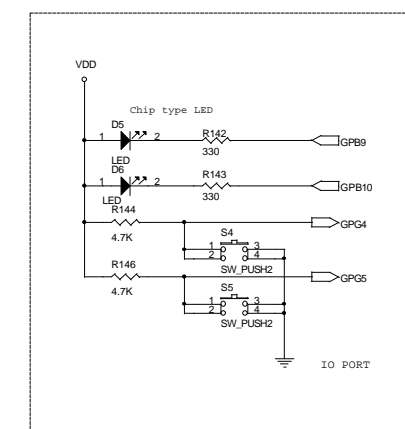
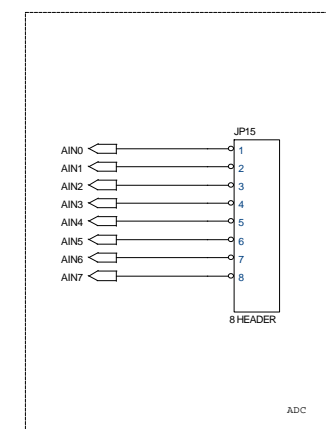
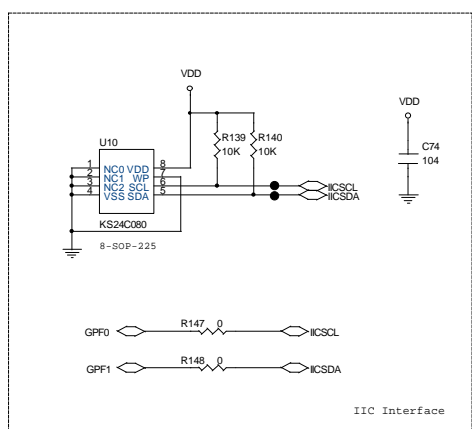
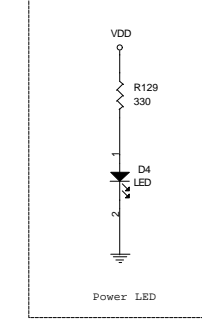
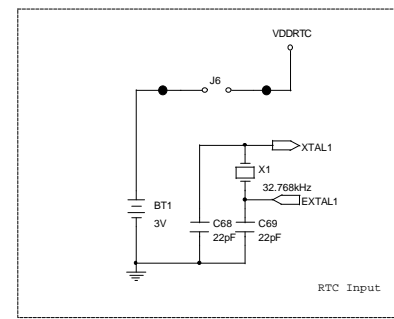
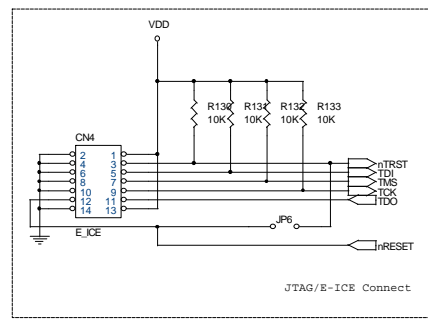
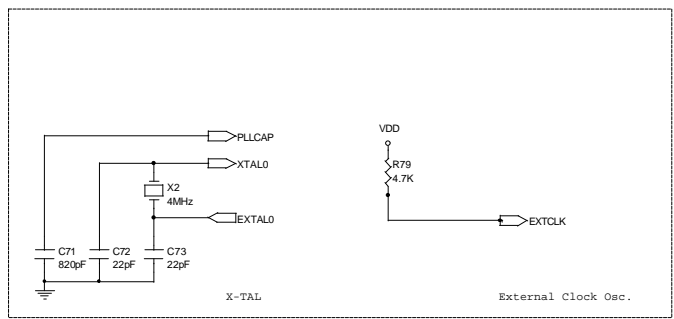
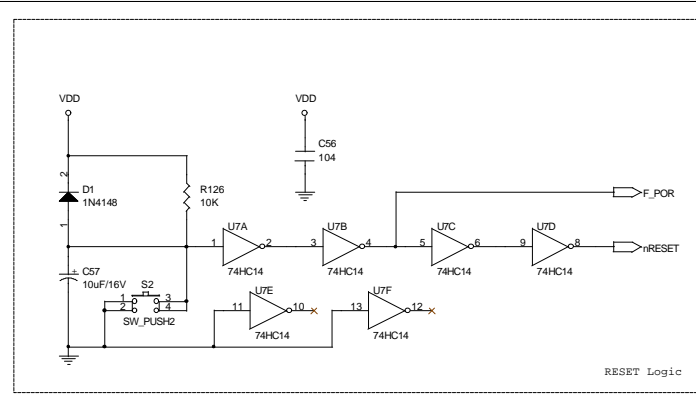
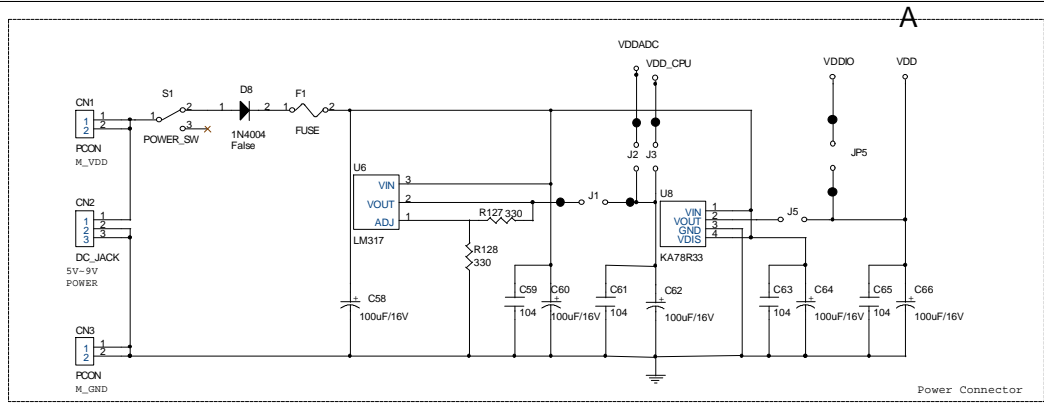
S3C44B0X has ADC(Analog to Digital Converter). The ADC has 8-ch analog input signals.
SMDK41100 provides the ADC(JP15) signals as follows;

Table 1-8. ADC Interface on SMDK41100

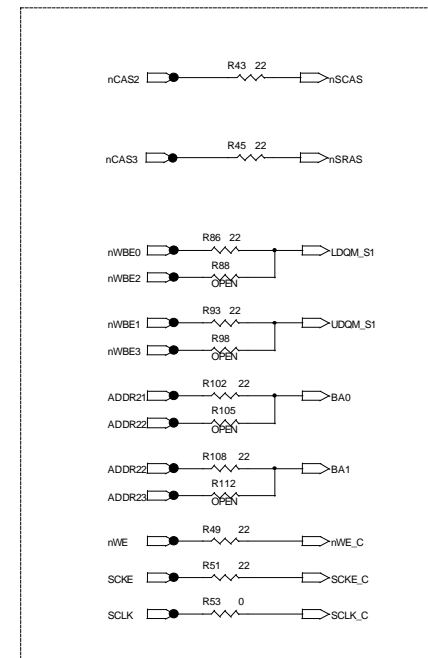
# of hole	Descriptions	# of hole	Descriptions	# of hole	Descriptions	# of hole	Descriptions
1	AIN0	2	AIN1	3	AIN2	4	AIN3
5	AIN4	6	AIN5	7	AIN6	8	AIN7

SMDK41100 REV. 1.0. BOARD SCHEMATICS

1. General MCU(S3C44B0X) device interface
2. Etc.(Power/JTAG/Clock . . .)
3. SDRAM/DRAM
4. EEPROM/Flash
5. UART
6. LCD

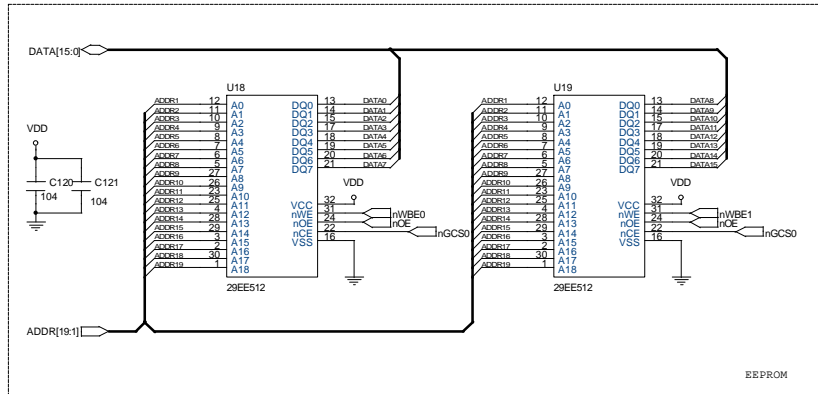


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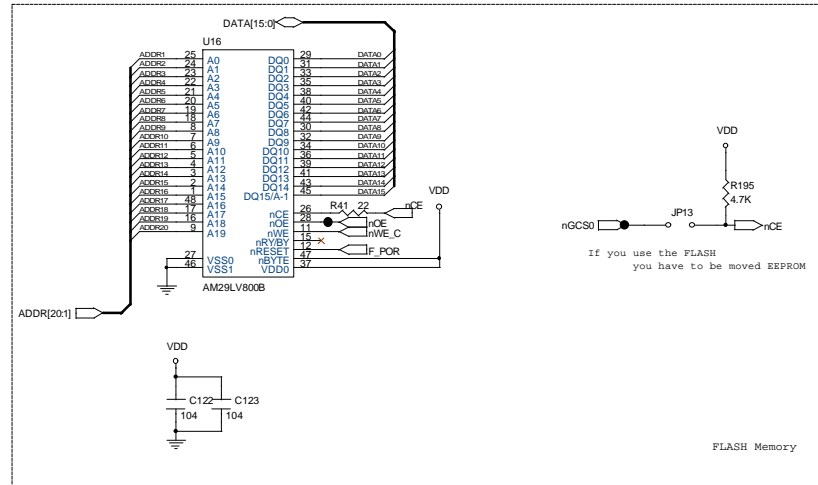


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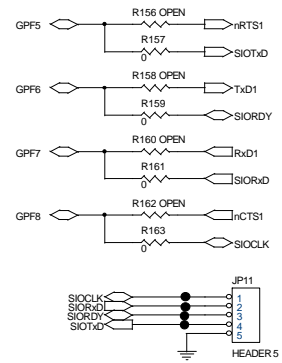
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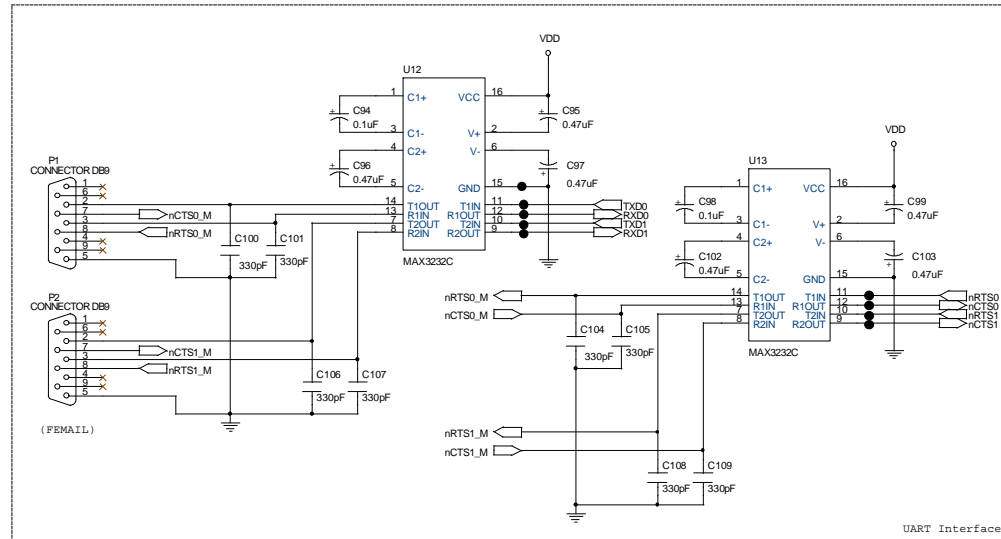
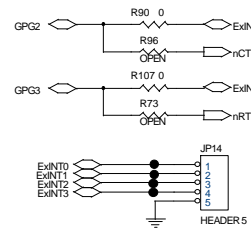
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In 32-bit data mode be supported below,
 -UART2 channel with RTS/CTS
 -or UART0's Rx/D/TxD with RTS/CTS & SIO



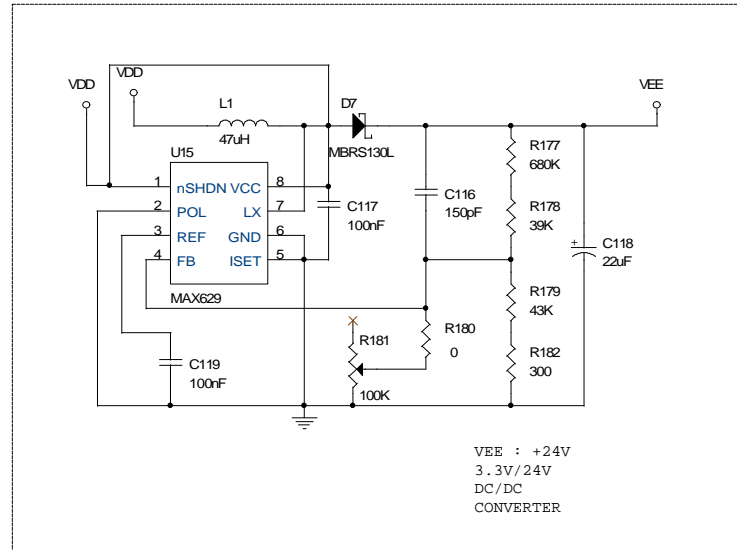
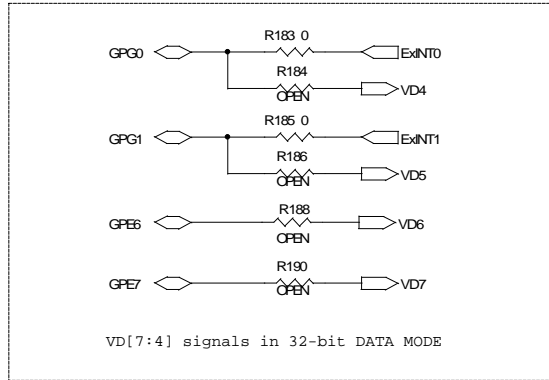
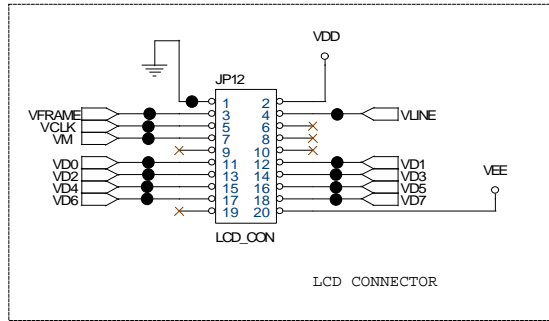
In 32-bit mode , UART0 Handshake



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