SPECTRUM DIGITAL INCORPORATED

TMS320C54V90/ TMS320C54CST/ TMS320VC5406 Evaluation Module

Technical Reference

2001 ***DSP Development Systems***

TMS320C54V90/
TMS320C54CST/
TMS320VC5406
Evaluation Module
Technical Reference

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Contents

About This Manual

This document describes the board level operations of the TMS320C54V90, TMS320C54CST, TMS320VC5406 evaluation module (EVM) which is based on the Texas Instruments TMS320C54V90, TMS320C54CST, and TMS320VC5406 Digital Signal Processor respectively.

This EVM is a table top card to allow engineers and software developers to evaluate certain characteristics of the host DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320C54V90, TMS320C54CST, and TMS320VC5406 will sometimes be referred to as the VC54XX.

The evalaution module for the TMS320C54V90, TMS320C54CST, and TMS320VC5406 will sometimes be referred to as the TMS320VC5406 EVM, VC5406 EVM, or VC5406 Evalaution Module.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320VC54X Users Guide
Texas Instruments TMS320VC54X Fixed Point Assembly Language Users Guide
Texas Instruments TMS320VC54X Fixed Point C Language Users Guide
Texas Instruments TMS320VC54X Fixed Point C Source Debugger Users Guide

Table 1: Board History

Revision	History
A	- Initial Release
B	- Changed DB9 connector from pin to socket - Relayout of PCB to shorten path on signal pin 73 of VC5406
C	- Added control I/O and Status I/O bits
D	- Added Programmable Reset

Table 2: Manual History

Revision	History
C	- Made corrections in text
D	- Made corrections in text
E	- Added information for the TMS320V54V90 and TMS320C54CST

Chapter 1

Introduction to the TMS320VC5406 Evaluation Module

Chapter One provides a description of the TMS320VC5406 Evaluation Module along with the key features and a block diagram of the circuit board.

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1.0 Overview of the TMS320VC5406 EVM

The TMS320VC5406 evaluation module (EVM) is a stand-alone modem card. It allows evaluators to examine certain characteristics of the TMS320VC5406, TMS320C54V90, and TMS320C54CST digital signal processors (DSP) to determine if it meets their application requirements as well as having on board modem circuitry and ROM code. Furthermore, the module is an excellent platform to develop and run software on the VC5406 family of processors.

The EVM allows full speed verification of VC5406 code. With 40K words of on-chip memory, 256K words of onboard RAM, Flash ROM, and an onchip UART, the board can solve a variety of problems as shipped. Two expansion connectors are provided for any necessary evaluation circuitry not provided on the as shipped configuration.

To simplify code development and shorten debugging time, debuggers providing assembly language and ‘C’ high level language debug are available with JTAG emulators.

1.1 Key Features of the TMS320VC5406 EVM

The VC5406 EVM has the following features:

- VC5406 operating at 10-120 MHz.
- 256K words of on board RAM
- On board DAA/Line Interface circuitry
- Onchip UART
- 1 megaword of onboard Flash ROM
- 2 Expansion Connectors (memory, peripheral)
- On board IEEE 1149.1 JTAG Connection for Optional Emulation
- +5-Volt Only Operation

1.1.1 Key Features of the TMS320C54V90 EVM

The evaluation module which has the TMS320C54V90 has the following additional feaures:

- Modem standards (V.90, V.34, V.32bis, V.32, V.22bis, V.22, V.23, V.21, and V.23 reversible, Bwll 103)
- Caller ID

1.2 Functional Overview of the TMS320VC5406 EVM

Figure 1-1 shows a block diagram of the basic configuration for the VC5406 EVM. The major interfaces of the EVM include the target RAM and ROM interface, DAA, and expansion interface.

The C5406 interfaces to 256K Words of onboard static memory. An external I/O interface supports 65,000 parallel I/O ports and optional high speed synchronous serial port. A Flash Boot ROM is mapped into program memory space. A phone jack provides input and outputs to and from the modem to the telephone line, and the UART allows interfacing to a personal computer.

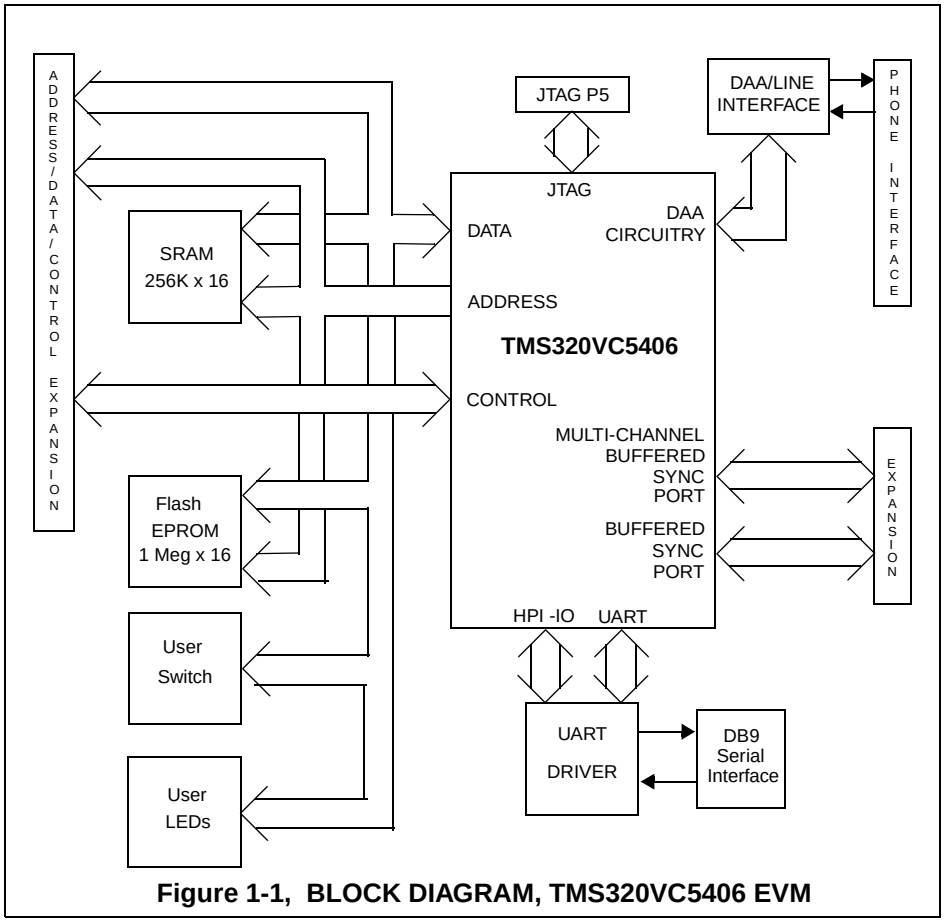

Figure 1-1, BLOCK DIAGRAM, TMS320VC5406 EVM

Chapter 2

Operation of the TMS320VC5406 Evaluation Module

This chapter describes the operation of the TMS320VC5406 Evaluation Module, the key interfaces and an outline of the circuit board.

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2.0 The TMS320VC5406 EVM Operation

This chapter describes the VC5406 Evaluation module, key components, and how they operate. It also provides information on the EVM's various interfaces.The VC5406 EVM consists of five major blocks of logic.

- VC5406 external memory
- DAA/Line interface
- User Switches and LEDs
- Expansion interface
- JTAG Interface

2.1 The TMS320VC5406 EVM Board

The VC5406 EVM is a 6.5 by 3.45 inch (165 x 88 mm.) board which is powered by an external +5 Volt only power supply. Figure 2-1 shows the layout of the VC5406 EVM.

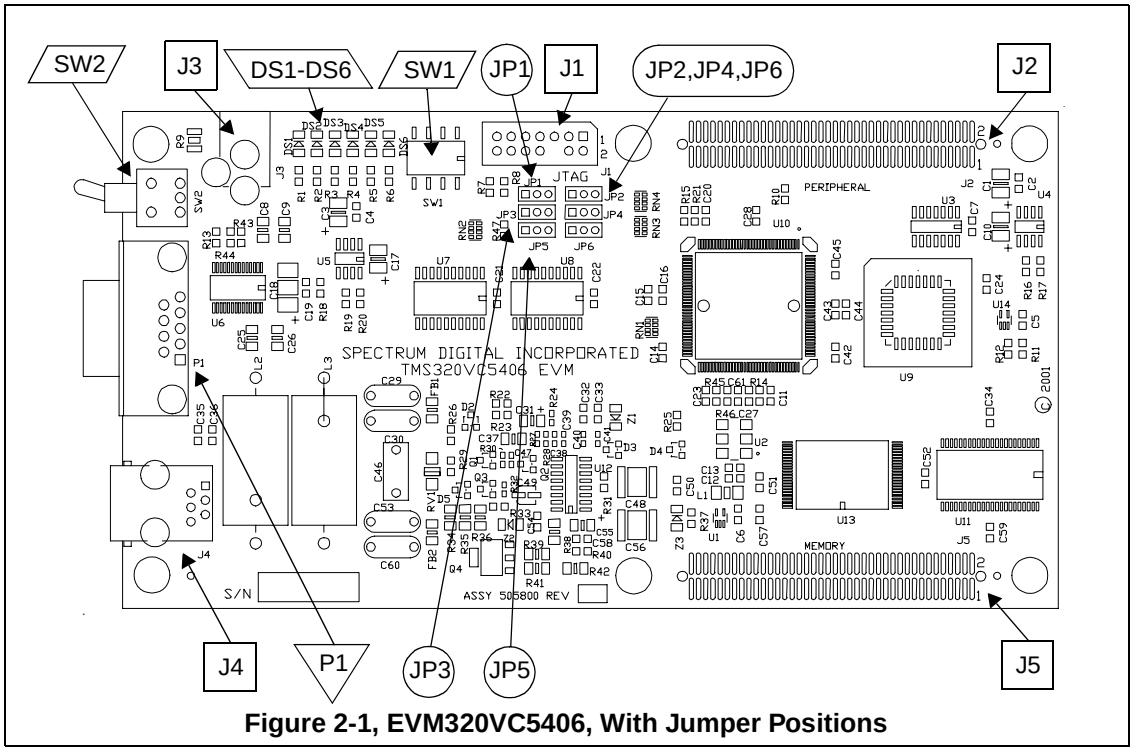

Figure 2-1, EVM320VC5406, With Jumper Positions

2.1.1 Power Connector

The VC5406 is powered by a 5 Volt only power supply which is available with the module. The board requires less than one (1) amp. The power is supplied via a 2 millimeter jack J1. If expansion boards are connected to the module a higher amperage power supply may be necessary. The board also has +3.3 and +1.5 volt regulators to provide power to the lower voltage components.

2.2 TMS320VC5406 Memory Interface

The EVM includes 224k Words of on board program ram memory and 32k words of on board data ram memory, providing a total of 256k words of off chip static ram. The board also features one mega-word of flash ROM for boot loading and program storage.

It is important to remember that internal memory has a higher precedence than the external memory. For more information on the memory in the device populated in your EVM card please refer to Texas Instruments TMS320VC5406 Users Guide. Futhermore, it is important to take into account that external memory is affected by wait-states. Wait state generation for off-chip memory space (data, program, or I/O) is done with the Software Wait State Generation Register (SWWSR). To obtain one waitstate off-chip memory bits in the SWWSR must be appropriately programmed. The board powers up with 7 wait-states. The EVM board does not generate wait states via the ready signal for external program and data memory accesses, only I/O accesses use the ready signal.

External memory decode is done via U9 a GAL20V8. The generic array device selects the RAM, FLASH ROM, or on board peripherals. The equations for the GAL are included in Appendix A. The figure below shows a one wait state program space RAM read followed by a data space memory write.

One page of the external Flash ROM is mapped into the upper 32K words of the first page 0 of program space for boot loading in microprocessor mode. Refer to the memory map for mapping of the other pages. Note that this memory requires multiple wait states. The main purpose of this memory is to allow for the boot loading of programs. An external latch provides 2 bits that allow dynamic memory remapping. This allows the flash to boot, then copy itself into RAM for high speed execution.

The figure below shows the memory timing for the EVM320VC5406 Evaluation Module.

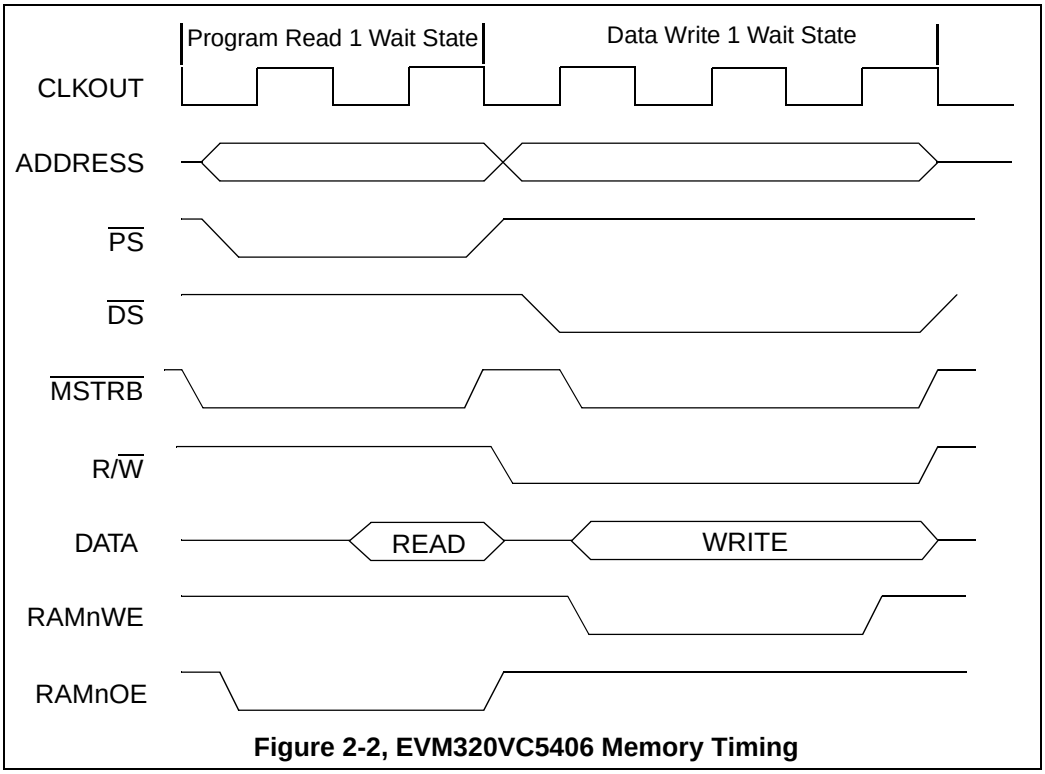

Figure 2-2, EVM320VC5406 Memory Timing

2.2.1 Program Memory

There are two items that affect program memory mapping. The first is the 54X's OVLY bit, the second is the MP/MC- pin or bit in the PMST register. When in OVLY mode, addresses 0x0000 - 0x8000 are internal for every page. In this mode, there are five (5) 32K word pages of external program RAM and one (1) 32K word page of internal RAM. This is the standard operating mode. When the microprocessor mode is chosen some of the addresses that are typically mapped as internal boot ROM are now mapped externally. The following figures is for the VC5406 processor.

MP Mode, MP/MC- = 1

Hex	
0x000000 0x00007F	External (OVLY=1) or Reserved (OVLY=0)
0x000080 0x007FFF	On-chip DARAM(OVLY=1) or External(OVLY=0)
0x008000 0x009FFF	DARAM (if OVLY=1) External if OVLY=0
0x00A000 0x00FF7F	External RAM
0x00FF80 0x00FFFF	Interrupts and Reserved (External)

MP Mode, MP/MC- = 0

Hex	
0x000000 0x00007F	External (OVLY=1) or Reserved (OVLY=0)
0x000080 0x005FFF	On-chip DARAM(OVLY=1) or External(OVLY=0)
0x006000 0x007FFF	On-chip ROM (8K Words)
0x008000 0x00BFFF	On-chip ROM (16K Words)
0x00C000 0x00FEFF	On-chip ROM (16K Words)
0x00FFF0 0x00FFFF	Interrupts and Reserved (On-chip)

Figure 2-3A, EVM320VC5406 Program Space - Page 0

Overlay Mode, OVLY = 1

Hex	
0x000000 0x00FFFF	See figure 2-3A
0x010000 0x017FFF	Page 1 External/Internal, OVLY=1
0x018000 0x01FFFF	Page 1 On-chip ROM
0x020000 0x027FFF	Page 2 External/Internal, OVLY=1
0x020000 0x02FFFF	Page 2 On-chip ROM
0x030000 0x037FFF	Page 3 External/Internal, OVLY=1
0x038000 0x03FFFF	Page 3 On-chip ROM
0x040000 0x047FFF	Page 4 External/Internal, OVLY=1
0x048000 0x04FFFF	Page 4 External RAM Page 1/ Flash Page 4
0x050000 0x057FFF	Page 5 External/Internal, OVLY=1
0x058000 0x05FFFF	Page 5 External RAM Page 2/ Flash Page 5
0x060000 0x067FFF	Page 6 External/Internal, OVLY=1
0x068000 0x06FFFF	Page 6 External RAM Page 3/ Flash Page 6
0x070000 0x077FFF	Page 7 External/Internal, OVLY=1
0x078000 0x07FFFF	Page 7 External RAM Page 4/ External FLASH Page 7
0x080000 0x087FFF	Page 8 External/Internal, OVLY=1
0x088000 0x08FFFF	Page 8 External RAM Page 5/ External FLASH Page 8

Hex	
0x090000 0x097FFF	Page 9 External/Internal, OVLY=1
0x098000 0x09FFFF	Page 9 External RAM Page 6/ External FLASH Page 9
0x0A0000 0x0A7FFF	Page 10 External/Internal, OVLY=1
0x0A8000 0x0AFFFF	Page 10 External RAM Page 7/ External FLASH Page 10
	▪ ▪ ▪
0x1F0000 0x1F7FFF	Page 32 External/Internal, OVLY=1
0x1F8000 0x1FFFFF	Page 32 Pages 31-38 (4K Sections) External FLASH
0x200000 0x207FFF	
0x208000 0x20FFFF	Image of External FLASH, Page 0
0x210000 0x217FFF	
0x218000 0x21FFFF	External FLASH, Page 1
0x220000 0x22FFFF	
0x228000 0x20FFFF	External FLASH, Page 2
0x230000 0x237FFF	
0x238000 0x23FFFF	External FLASH, Page 3

Figure 2-3B, EVM320VC5406 Program Space

2.2.2 Data Memory

The data memory configuration is shown below. The external data memory is mapped from 0xA000 to 0xFFFF.

Figure 2-4 shows the data space memory map for the VC5406 processor.

Hex	
0x0000 0x005F	Memory-Mapped Registers
0x0060 0x007F	Scratch Pad RAM
0x0080 0x7FFF	32K Dual Access RAM (DARAM)
0x8000 0x9FFF	DARAM 8K Words
0xA000 0xBFFF	External RAM
0xC000 0xFFEF	ROM(DROM=1) External RAM(DROM=0)
0xFF00 0xFFFF	Reserved(DROM=1) External RAM(DROM=0)

Figure 2-4, EVM320VC5406 Data Space

2.2.3 I/O Space

The I/O map for the TMS320VC5406 EVM is shown below:

Hex	
0x0000 0x07FF	I/O Latch on Write Cycles I/O Buffer on Read Cycles
0x0800 0x7FFF	Expansion
0x8000 0xFFFF	Expansion

Figure 2-5, EVM320VC5406 I/O Space

2.2.4 I/O Latch and I/O Buffer

There is an external latch and external buffer mapped at I/O location 0x0000. This latch and buffer are mirrored from 0x0000-0x7FFF.

At Reset the latch is set to 0. Both the latch and buffer are connected to Data Bits D0-D7. Below is definition of data bits for the buffer.

Table 1: Buffer Data Bit Definitions

Data Bit	Definition
D0	Switch SW1-1
D1	Switch SW1-2
D2	Switch SW1-3
D3	Switch SW1-4
D4	DC_STAT0
D5	DC_STAT1
D6	Read Memory Option 0
D7	Read Memory Option 1

Below is definition of data bits for the latch.

Table 2: Latch Data Bit Definitions

Data Bit	Definition
D0	LED DS3
D1	LED DS4
D2	LED DS5
D3	LED DS6/DC_RESET
D4	DC_CNTL0
D5	DC_CNTL1
D6	Set Memory Option 0
D7	Set Memory Option 1

2.2.4.1 Memory Option Latch

The I/O latch mapped at Location 0x0000 dynamically controls the memory decoder for the program space. Data bits D6 and D7 are mapped to MEMOPT0 and MEMOPT1 respectively. These option bits control decode of the Flash ROM and program memory. These options control read and writes from RAM and Flash. The table below shows the memory option latch signals and the options they create.

Table 3: Memory Option Latch

MEMOPT0	MEMOPT1	Description	Read	Write
0	0	Flash Only (Default)	Flash	Flash
0	1	Copy Flash To RAM	Flash	RAM
1	0	Reserved	N/A	N/A
1	1	RAM	RAM	RAM

2.3 Oscillator Selection

The TMS320VC5406 EVM is equipped with a 14.7456 Megahertz oscillator. When the processor resets the PLL Clock Module defaults to 14.7 Mhz CLKOUT in divide mode. The PLL can then be programmed to obtain a variety of clock frequencies. If the PLL frequency is required to change after the programming the part must be returned to the divide mode before the programming of the new PLL frequency. The user should refer to the “PLL Clock Module” section in the TMS320VC5406 User’s guide for valid clock configurations. This oscillator frequency is specifically selected to generate the appropriate modem frequencies.

2.4 Expansion Connectors

The TMS320VC5406 EVM has two expansion connectors which bring out all of the signals from the DSP. This expansion bus allows the user to design custom circuitry to be used with his application without having to design a CPU card.

This expansion connectors are double row header connectors. This section contains the signal definitions and pin numbers for each of the connectors.

Table 4: Expansion Bus Connectors

Connector	Function
J5	Memory Expansion
J2	Peripheral Expansion

2.4.1 J5, Memory Expansion Connector for VC5406

Table 5: J5, Memory Expansion Connector

Pin #	Signal Name	Pin #	Signal Name
1	+5 Volts	2	+5 volts
3	A19	4	A18
5	A17	6	A16
7	A15	8	A14
9	A13	10	A12
11	GND	12	GND
13	A11	14	A10
15	A9	16	A8
17	A7	18	A6
19	A5	20	A4
21	+5 Volts	22	+5 Volts
23	A3	24	A2
25	A1	26	A0
27	A21	28	A20
29	GND	30	GND
31	GND	32	GND
33	RESERVED	34	RESERVED
35	RESERVED	36	RESERVED
37	RESERVED	38	RESERVED
39	RESERVED	40	RESERVED
41	+3.3 Volts	42	+3.3 Volts
43	RESERVED	44	RESERVED
45	RESERVED	46	RESERVED
47	RESERVED	48	RESERVED
49	RESERVED	50	RESERVED
51	GND	52	GND
53	D15	54	D14
55	D13	56	D12
57	D11	58	D10
59	D9	60	D8
61	GND	62	GND
63	D7	64	D6
65	D5	66	D4
67	D3	68	D2
69	D1	70	D0
71	GND	72	GND
73	R-/W	74	MEMnWE-
75	MEMnOE-	76	RDY-
77	MSTRB-	78	DS-
79	GND	80	GND

2.4.2 J2, Peripheral Expansion Connector for VC5406

Table 6: J2, Peripheral Expansions Connector

Pin #	Signal Name	Pin #	Signal Name
1	RESERVED	2	RESERVED
3	GND	4	GND
5	+5 Volts	6	+5 Volts
7	GND	8	GND
9	+5 Volts	10	+5 Volts
11	HD1	12	RESERVED
13	UART_TX	14	RESERVED
15	HD0	16	HD5
17	RESERVED	18	HD4
19	+3.3 Volts	20	+3,3 Volts
21	BCLKX0	22	UART_RX
23	BFSX0	24	BDX0
25	GND	26	GND
27	BCLKR0	28	HD2
29	BFSR0	30	BDR0
31	GND	32	GND
33	BCLKX1	34	HD3
35	BFSX1	36	BDX1
37	GND	38	GND
39	BCLKR1	40	RESERVED
41	BFSR1	42	BDR1
43	GND	44	GND
45	TOUT	46	RESERVED
47	RESERVED	48	INT1-
49	XF	50	BIO-
51	GND	52	GND
53	INT0-	54	IACK-
55	RESERVED	56	IOSTRB-
57	MSC-	58	IAQ-
59	DC_RESET- *	60	RESERVED
61	GND	62	GND
63	DC_CNTL1 *	64	DC_CNTL0 *
65	DC_STAT1 *	66	DC_STAT0 *
67	INT2-	68	INT3-
69	PS-	70	IS-
71	RESERVED	72	RESERVED
73	RESERVED	74	RESERVED
75	GND	76	GND
77	GND	78	CLKOUT
79	GND	80	GND

*** Rev C or Newer**

2.5 J1, JTAG Interface.

The TMS320VC5406 Evaluation Module is supplied with a 14 pin header interface, J1. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown figure 2-6 below:

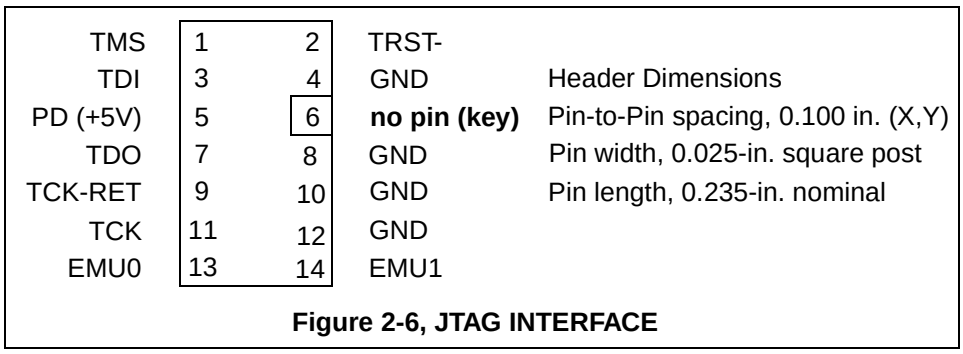

Figure 2-6, JTAG INTERFACE

The signal names for each pin are shown in the table below.

Table 7: P1, JTAG Interface

Pin #	Signal Name
1	TMS
2	TRST-
3	TDI
4	GND
5	PD
6	no pin
7	TDO
8	GND
9	TCK-RET
10	GND
11	TCK
12	GND
13	EMU0
14	EMU1

2.6 On Chip Serial Interface

The EVM320VC5406 has a an on chip UART which provides a serial interface. This UART is mapped into data space at locations 0x0044 to 0x0045. The UART is accessed via address sub-register at 0x0044 and data register at 0x0045. There are 8 UART registers. For example to access the UART register 4, first write 0x0004 to the address sub-register and then read or write the Data Register at 0x0045.

This UART is brought out to connector P1 on the EVM320VC5406. Connector P1 is a DB9 female connector on Rev-B printed circuit boards and a male connector on Rev-A EVMs. The pin positions for the P1 connector as viewed from the edge of the EVM320VC5406.

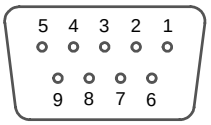

Figure 2-7, P1, DB9 Female Connector

The pin numbers and their corresponding signals are shown in the table below:

Table 8: P1, RS232 Pinout

Pin #	PC	VC5406 EVM	VC5406 Direction
1	DCD	HPI HD4	Output
2	RX	UART TX	Output
3	TX	UART RX	Input
4	DTR	HPI HD0	Input
5	GND	GND	GND
6	DSR	HPI HD3	Output
7	RTS	HPI HD1	Input
8	CTS	HPI HD2	Output
9	RI	HPI HD5	Input

2.7 EVM320VC5406 Jumpers

The EVM320VC5406 has 6 jumpers which determine how features on the EVM are utilized. The table below lists the jumpers and their function. The following sections describe the use of each jumper.

Table 9: EVM320VC5406 Jumpers

Jumper #	Size	Function
JP1	1 x 3	Host Port Enable
JP2, JP4, JP6	1 x 3	Oscillator Mode Select
JP3	1 x 3	MC/MP Enable
JP5	1 x 3	HPI Mode Select

Each jumper on the TMS320VC5406 EVM is a 1 x 3 jumper. Each 1 x 3 jumper must have the selection 1-2 or 2-3. The #2 pin is the center pin. The #1 pin has a square solder pad and can be seen from the solder side of the printed circuit board. This pin is usually marked with a '1' on the boards silkscreen. A top view of both types of jumpers is shown below:

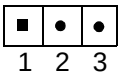

Figure 2-9 1x3 Jumper Layout

WARNING!
Unless noted otherwise, all 1x3 jumpers must be installed in either the 1-2 or 2-3 position

2.7.1 Jumper Positions

The figure 2-1 shows the locations of the jumpers on the EVM320VC5406 EVM.

2.7.2 JP1, Host Port Enable

Jumper JP1 is used to select the state of the HPIENA signal on the DSP. The standard configuration is to use the host port so HPIENA is disabled. The table below shows the jumper positions and their functions:

Table 10: JP1, Host Port Enable

Position	Function
1-2	HPIENA driven high, Enabled
2-3	HPIENA driven low, Disabled

2.7.3 JP2, JP4, JP6, Oscillator Selection

Jumpers JP2, JP4, and JP6 are used together to select different clock modes and speeds for the VC5406 DSP. The EVM320VC5406 is equipped with a 14.7456 megahertz oscillator.

The VC5406 PLL can be configured in one of the two provided clock modes:

- The input clock (CLKIN) is divided by 2 or 4; this is called DIV mode
- The input clock (VLKIN) is multiplied by one of 31 possible ratios which range from 0.25 to 15. These ratios are achieved with the Analog Voltage controlled Oscillator (VCO).; this mode is called PLL mode.

When the PLL clock mode is not used, VCO and all the analog parts are disabled in order to minimize the power dissipation

The PLL clock mode can be determined by setting 3 external clock mode pins during reset or by software. In software, a 16 bit register (CLKMD) controls the behavior of the PLL and sets the mode.

At start-up the clock mode is selected with the values on input pins CLKMD1, CLKMD2, and CLKMD3. These these pins are tied to jumpers JP2, JP4, and JP6 respectively.

The 2-3 position drives the respective CLKMode pin low. The 2-3 position drives the respective CLKMode pin high.

The configuration is shown in the table below.

Table 11: JP2, JP4, JP6, Clock Mode Table

JP2, CLKMD1	JP4, CLKMD2	JP6, CLKMD3	C54V90 DSP	C54CST
2-3	2-3	2-3	RESERVED	1/2,PLL Disabled, OSC disabled
2-3	2-3	1-2	RESERVED	PLL x 10
2-3	1-2	2-3	RESERVED	PLL x 5
2-3	1-2	1-2	RESERVED	RESERVED
1-2	2-3	2-3	RESERVED	PLL x 1
1-2	2-3	1-2	117 MIPS, PLL x 8	1/4 (PLL Disabled)
1-2	1-2	2-3	RESERVED	1/2 (PLL Disabled)
1-2	1-2	1-2	58 MIPS, PLL x 4	RESERVED

2.7.4 JP3, MC/MP Enable

Jumper JP3 can be used to determine if the VC5406 is operating in Micro-controller mode or Microprocessor mode. When position 1-2 is used the VC5406 will operate in the Microprocessor mode. If position 2-3 is selected the VC5406 will operate in the Micro-controller mode. The jumper settings are shown in the table below:

Table 12: JP3, MC/MP Enable

JP13 Position	Processor Mode
1-2	Microprocessor Mode
2-3	Micro-controller Mode

2.7.5 JP5, HPI Mode Select

Jumper JP5 is used to select if the Host Port Interface is in the 16 bit mode or the 8 bit mode. Since the Host Port Interface is used for bit I/O the default is HPI16 pin low which selects the HPI 8 bit mode. If the jumper is in the 1-2 position, the 16 bit mode is used. If position 2-3 is selected, the 8 bit mode is used. The table below shows the two positions and their functions:

Table 13: JP5, HPI Mode Select

Position	Function
1-2	HPI in 16 bit mode
2-3	HPI in 8 bit mode

2.8 LEDs

The EVM320VC5406 EVM has six (6) light emitting diodes. DS1 indicates the presence of +5 volts and is ‘on’ when power is applied to the board. DS2 is tied to the UART Ring Indicator. DS3-DS6 are user defined and driven by the latch mapped into the I/O space at address 0x0000. When this address is written to the state of the LEDs are controlled by D0-D3. The functions of the LEDs are shown in the table below:

Table 14: EVM320VC5406 EVM LEDs

LED #	Color	Controlling Signal	On Signal State
DS1	Green	+5 Volts	1
DS2	Green	Ring Indicator	1
DS3	Green	I/O Latch, D0	1
DS4	Green	I/O Latch, D1	1
DS5	Green	I/O Latch, D2	1
DS6	Green	I/O Latch, D3	1

2.9 Switches

The EVM320VC5406 has a 4 position DIP switch. All 4 positions are available for user applications. This switch is read at I/O address 0x0000. The 4 least significant data bits represent the state of the switch positions. The table below shows this mapping.

Table 15: EVM320VC5406 Switches

Switch Position	Data Bit
SW1-1	D0
SW1-2	D1
SW1-3	D2
SW1-4	D3

2.10 Resets

The reset is generated by the power on reset circuit. This circuit waits until power is within the specified range before releasing the power on reset pin to the TMS320VC5406.