SPECTRUM DIGITAL INCORPORATED

TMS320F243
Evaluation Module

Technical Reference

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DSP Development Systems

TMS320F243
Evaluation Module
Technical Reference

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About This Manual

This document describes the board level operations of the TMS320F243 evaluation module (EVM). The EVM is based on the Texas Instruments TMS320F243 Digital Signal Processor.

The TMS320F243 EVM is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320F243 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320F243 will sometimes be referred to as the F243 or C24X.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = rw &! strb;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320F243 Users Guide
Texas Instruments TMS320 Fixed Point Assembly Language Users Guide
Texas Instruments TMS320 Fixed Point C Language Users Guide
Texas Instruments TMS320 Fixed Point C Source Debugger Users Guide

Chapter 1

Introduction to the TMS320F243 Evaluation Module

This chapter provides you with a description of the TMS32F243 Evaluation Module along with the key features and a block diagram of the circuit board.

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1.0 Overview of the TMS320F243 EVM

The TMS320F243 evaluation module(EVM) is a stand-alone card that lets evaluators examine certain characteristics of the F243 digital signal processor(DSP) to determine if this DSP meets their application requirements. Furthermore, the module is an excellent platform to develop and run software on the F243 family of processors.

The F243 EVM is shipped with a TMS320F243 DSP. The EVM allows full speed verification of F243 code. With 544 words of onchip data memory, 128K words of onboard memory, onchip flash rom, on chip UART, and an MP7680 Digital to Analog Converter, the board can solve a variety of problems as shipped. Four expansion connectors are provided to interface to any necessary evaluation circuitry not provided on the as shipped configuration.

To simplify code develop and shorten debugging time a number of user interfaces are available.

1.1 Key Features of the TMS320F243 EVM

The F243 EVM has the following features:

- F243 operating at 20 MIPS with 128K words of zero wait state memory
- 8 channels of 10 bit onchip Analog to Digital Conversion
- Multiple PWM & capture channels onchip
- MP7680 Four(4) Channel Digital to Analog converter
- Onchip UART with RS232 Drivers
- 8K words of onchip Flash ROM
- CAN Interface with drivers
- User Switches and LEDs
- 4 Expansion Connectors (data, address, I/O, and control)
- On board IEEE 1149.1 JTAG Connection for Optional Emulation
- 5 Volt Only Operation

1.2 Functional Overview of the TMS320F243 EVM

Figure 1-1 shows a block diagram of the basic configuration for the F243 EVM. The major interfaces of the EVM include the target ram, analog interface, CAN interface, user leds and switches, RS232 interface, and expansion interface.

The F243 interfaces to 128K Words of zero wait-state static memory. An external I/O interface supports 65,000 parallel I/O ports. An onchip CAN and RS232 serial port are available on the expansion connector.

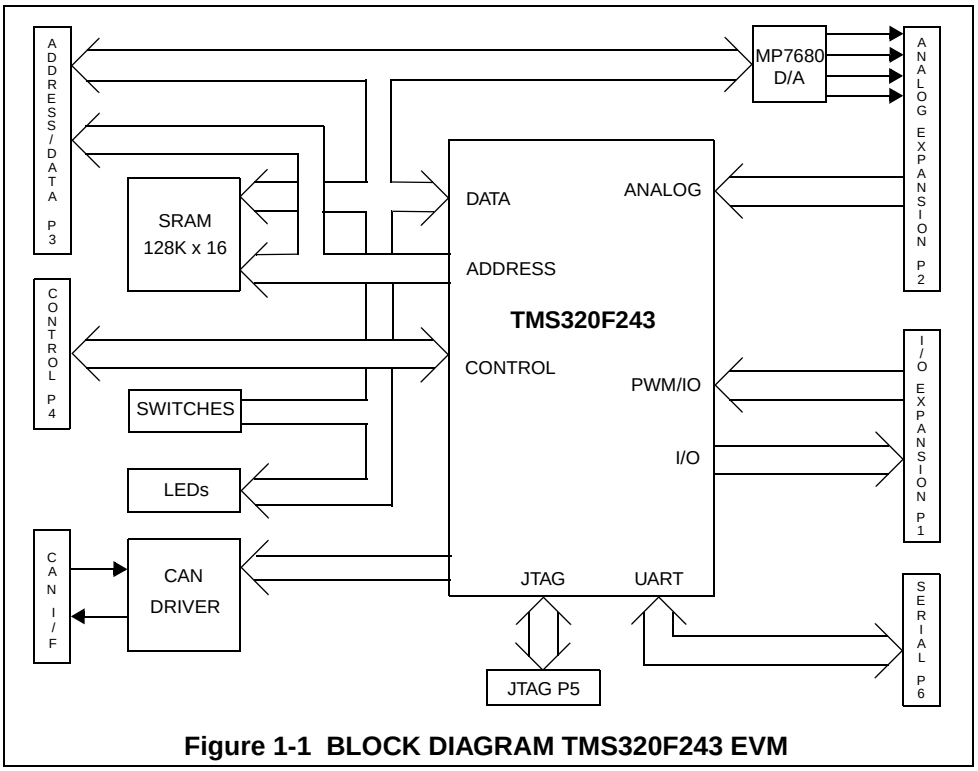

Figure 1-1 BLOCK DIAGRAM TMS320F243 EVM

Chapter 2

Operation of the TMS320F243 Evaluation Module

This chapter describes the operation of the TMS32F243 Evaluation Module along with the key interfaces and an outline of the circuit board.

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2.0 The TMS320F243 EVM Operation

This chapter describes the F243 Evaluation module, its key components, and how they operate. It also provides information on the EVM's various interfaces.The F243 EVM consists of six major blocks of logic.

- F243 external memory
- Digital to Analog Interface
- On Chip Serial Interface
- LEDs and Switches
- On Chip CAN Interface
- Expansion interface
- JTAG Interface

2.1 The TMS320F243 EVM Board

The F243 EVM is a 3U sized board which is powered by an external 5 Volt only power supply. Figure 2-1 shows the layout of the F243 EVM.

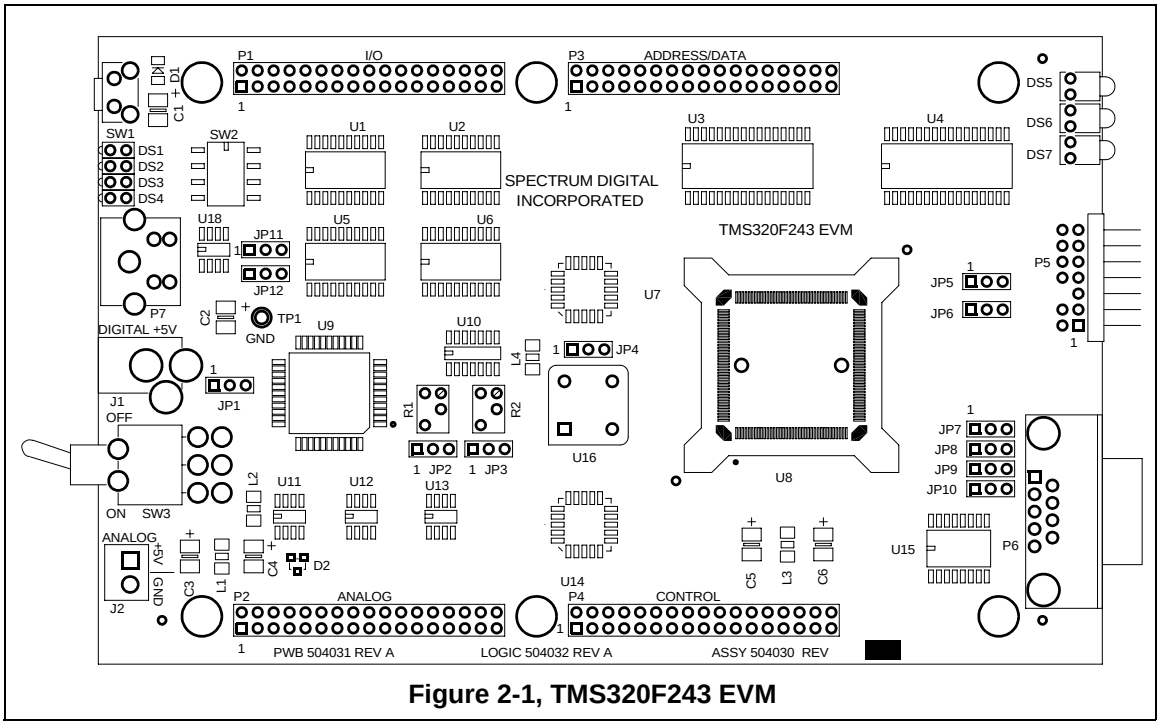


Figure 2-1, TMS320F243 EVM

2.1.1 Power Connector

The F243 is powered by a 5 Volt only power supply which is available with the module. The board requires 750 milliamps. The power is supplied via 2 millimeter jack J1. If expansion boards are connected to the module a higher amperage power supply may be necessary.

2.2 TMS320F243 Memory Interface

The EVM includes 64k Words of zero wait-state program ram memory and 64k words of zero wait-state data ram memory, providing a total of 128k words of off chip static ram.

It is important to remember that internal memory has a higher precedence than the external memory. For more information on the memory in the device populated in your EVM card please refer to Texas Instruments TMS320F243 Users Guide. Futhermore, it is important to take into account that external memory is affected by wait-states. Wait state generation for off-chip memory space (data, program, or I/O) is done with the Wait State Generation Register(WSGR). To obtain zero waitstate off-chip memory bits in the WSGR must be appropriately programmed. The board powers up with 7 wait-states. The EVM board does not generate wait states via the ready signal for external program and data memory accesses.

External memory decode is done via U7 a GAL16V8. The generic array device selects the RAM, or on board peripherals. The equations for the GAL are included in Appendix A. The figure below shows a zero wait state program space memory read followed by a data space memory write.

Figure 2-3 below shows the memory timing on the EVM320F243.

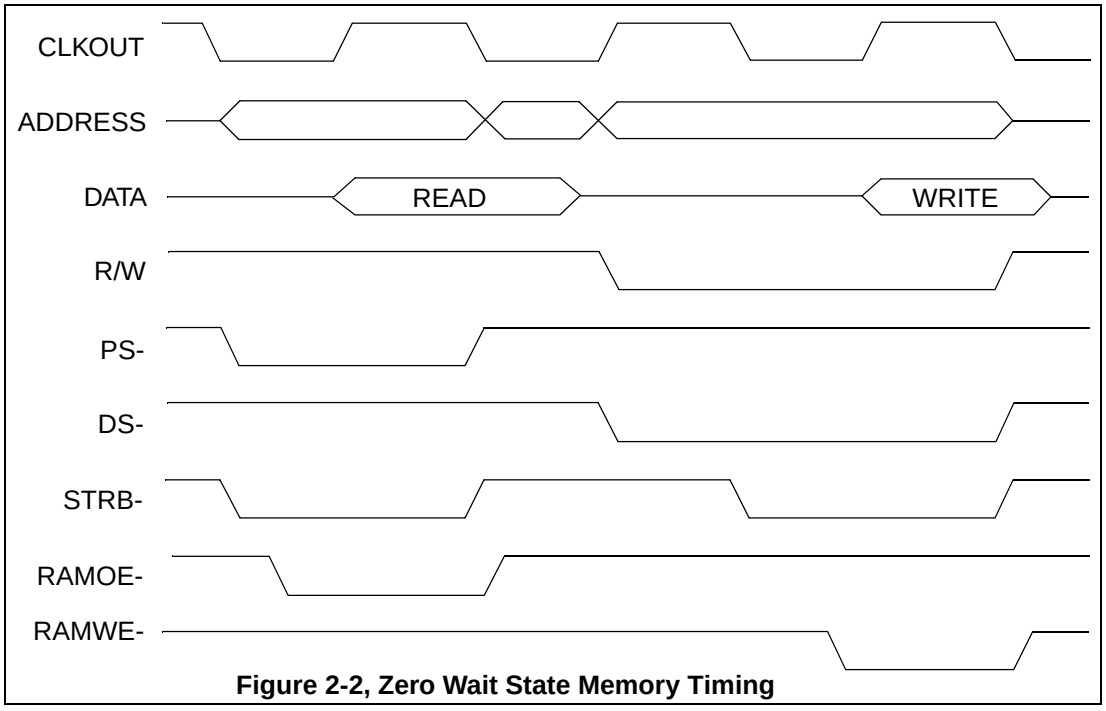


Figure 2-2, Zero Wait State Memory Timing

2.2.1 Program Memory

There are two configurations for program memory. The selection of these configurations is done by the position of jumper, JP6. If JP6 is in the 2-3 position then the DSP is in microcomputer mode and the internal flash memory is enabled from 0x0000 to 0x1fff. If JP6 is in position 1-2 then the internal FLASH/ROM is disabled and the entire program address range is available to external memory.

Shown below are the two program memory configurations:

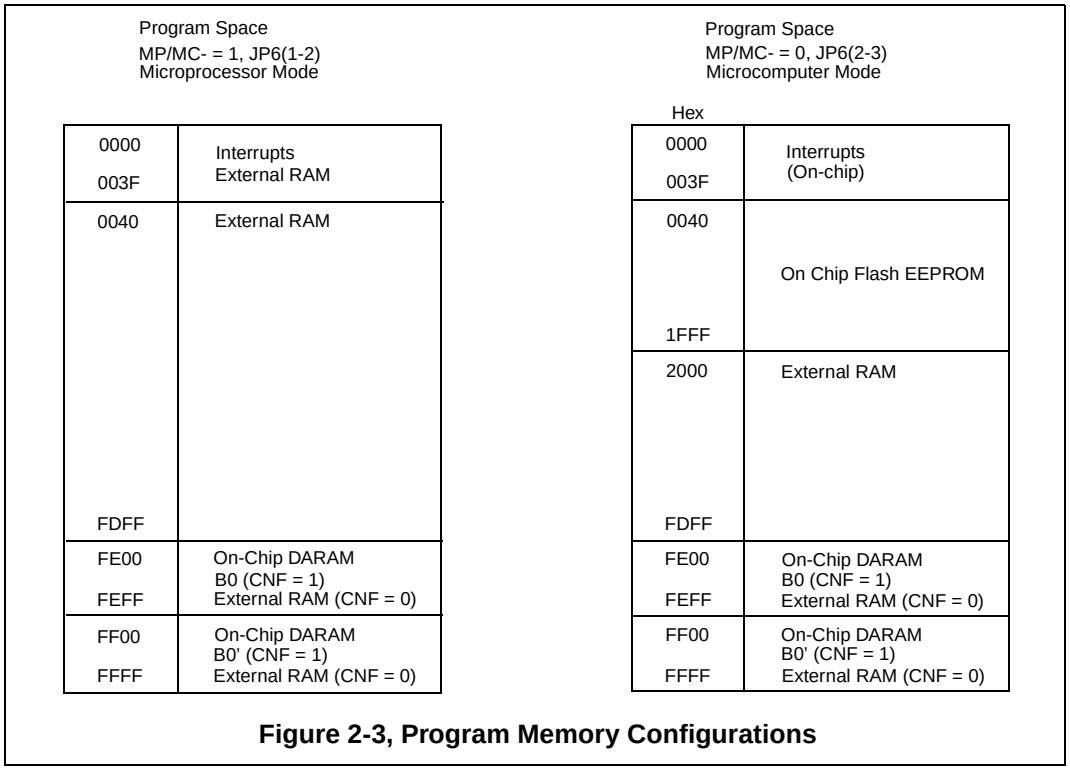


Figure 2-3, Program Memory Configurations

2.2.2 Data Memory

The data memory configuration is shown below. External RAM is enabled from 0x8000-0xffff. Loading the GREG register will disable all or part the external memory, depending on the value, and allow devices connected to the expansion bus to be accessed.

Hex	
0000 005F	Memory-Mapped Register and Reserved
0060 007F	On-Chip DARAM B2
0080 00FF	Reserved
0100 01FF	On-Chip DARAM B0 (CNF = 0) Reserved (CNF = 1)
0200 02FF	On-Chip DARAM B0' (CNF = 0) Reserved (CNF = 1)
0300 03FF	On-Chip DARAM B1
0400 04FF	On-Chip DARAM B1'
0500 07FF	Reserved
0800 6FFF	Illegal
7000 73FF	Peripheral Memory-Mapped Registers (System, ADC, SCI, SPI, I/O, Interrupts)
7400 743F	Peripheral Memory-Mapped Registers (Event Manager)
7440 77FF	Reserved
7800 7FFF	Illegal
8000 FFFF	External RAM JP7 = 1-2

Figure 2-4, Data Memory Configuration

2.2.3 I/O Space

The I/O map for the TMS320F243 EVM is shown below:

Hex	
0000 0004	D/A Converter
0005 0007	Reserved
0008	4 Position DIP Switch
0009 000B	Reserved
000C	LEDs
000D 7FFF	Reserved
8000 FFFF	External

Figure 2-5, I/O Space Configuration

2.3 User Switches and LEDs

The TMS320F243 EVM has 4 switches and 4 LEDs that are available for user applications.

These devices are I/O mapped at locations 0x0008 and 0x000C respectively on data bits D0-D3 as shown in the table below:

Table 1: Switch & LED Data Bits

Data Bit	LED #	Switch SW2
D0	DS1	Position 1
D1	DS2	Position 2
D2	DS3	Position 3
D3	DS4	Position 4

To access these devices the “IN” and “OUT” instructions are used.

2.4 Oscillator Selection

The TMS320F243 EVM is equipped with a 5 Megahertz oscillator. When the processor resets the PLL Clock Module defaults to CLKIN/4 yielding a 20 Mhz clkout. The user should refer to the “PLL Clock Module” section in the TMS320F243 User’s guide for more information.

2.5 Digital to Analog Converter

The TMS320F243 EVM provides four(4) 12-bit D/A channels. The output is from 0 to 5 volts DC. The converter is mapped into I/O address space 0x0000 to 0x0004. Locations 0x0000 through 0x0003 are used for the data holding registers for channels 1-4 respectively. I/O address 0x0004 is used to transfer values in the holding registers to the converters. For instance you can write to the 4 holding registers and transfer all 4 to the converters at the same time. Information about programming this converter can be found in Appendix C.

Table 2: DAC I/O Addresses

I/O Address	Channel #
0x0000	1
0x0001	2
0x0002	3
0x0003	4
0x0004	Transfer

2.6 Expansion Bus

The TMS320F243 EVM has an expansion bus which brings out all of the signals from the DSP. This expansion bus allows the user to design custom circuitry to be used with his application without having to design a CPU card. In addition this interface is used by Spectrum Digital for all of its add-on modules.

2.6.1 TMS320F243 EVM Expansion Connector

Expansion boards interface to the TMS320F243 EVM via an expansion bus. This expansion bus is divided into 4 double row header connectors. This section contains the signal definitions and pin numbers for each of the connectors.

2.6.1.1 Expansion I/O Connector

The definition of P1, which has the I/O signals is shown below.

Table 3: P1 I/O

Pin #	Signal	Pin #	Signal
1	VCC, +5 Volts	2	VCC, +5 Volts
3	PWM1/CMP1/IOPA6	4	† PWM2/CMP2/IOPA7
5	PWM3/CMP3/IOPB0	6	† PWM4CMP4/IOPB1
7	PWM5/CMP5/IOPB2	8	† PWM6/ CMP6/IOPB3
9	† PWM2/CMP2/IOPA7	10	† PWM4/CMP4/IOPB1
11	† CMP6/IOPB3	12	T1CMP/IOPB4
13	T2CMP/IOPB5	14	IOPD5
15	TDIR/IOPB6	16	TCLKIN/IOPB7
17	GND	18	GND
19	XF/IOPC0	20	BIO/IOPC1
21	CAP1/QEP0/IOPA3	22	CAP2/QEP1/IOPA4
23	CAP3/IOPA5	24	IOPD4
25	RESERVED	26	PDPINT-
27	SCITXD/IOPA0	28	SCIRXD/IOPA1
29	SPISIMO/IOPC2	30	SPISOMI/IOPC3
31	SPICLK/IOPC4	32	SPISTE/IOPC5
33	GND	34	GND

† Duplicated for compatibility with the F240 EVM.

2.6.1.2 Expansion Analog Connector

The definition of P2, which has the analog signals is shown below.

Table 4: P2 Analog

Pin #	Signal	Pin #	Signal
1	VCCA, +5V Analog	2	VCCA, +5V Analog
3	IOPD7	4	IOPD6
5	ADCIN0	6	ADCIN1
7	ADCIN2	8	ADCIN3
9	RESERVED	10	RESERVED
11	RESERVED	12	RESERVED
13	ADCIN4	14	ADCIN5
15	ADCIN6	16	ADCIN7
17	AGND	18	AGND
19	RESERVED	20	RESERVED
21	VREFHI	22	VREFLO
23	AGND	24	AGND
25	DACOUT1	26	DACOUT2
27	DACOUT3	28	DACOUT4
29	RESERVED	30	RESERVED
31	RESERVED	32	† XINT2-/ADCSOC/IOPD1
33	AGND	34	AGND

† Duplicated for compatibility with the F240 EVM.

2.6.1.3 Expansion Address and Data Connector

The definition of P3, which has the address and data signals is shown below.

Table 5: P3 Address/Data

Pin #	Signal	Pin #	Signal
1	A0	2	A1
3	A2	4	A3
5	A4	6	A5
7	A6	8	A7
9	A8	10	A9
11	A10	12	A11
13	A12	14	A13
15	A14	16	A15
17	GND	18	GND
19	D0	20	D1
21	D2	22	D3
23	D4	24	D5
25	D6	26	D7
27	D8	28	D9
29	D10	30	D11
31	D12	32	D13
33	D14	34	D15

2.6.1.4 Expansion Control Connector

The definition of P4, which has the control signals is shown below.

Table 6: P4 Control

Pin #	Signal	Pin #	Signal
1	VCC, +5 Volts	2	VCC, +5 Volts
3	DS-	4	PS-
5	IS-	6	BR-
7	WE-	8	RD-
9	STRB-	10	R/W-
11	READY	12	RESERVED
13	RS-	14	TRGRESET-
15	NMI-	16	XINT1-/IOPA2
17	GND	18	GND
19	† XINT2-/ADCSOC/IOPD1	20	RESERVED
21	VISCLK	22	VISOE
23	CANTX/IOPC6	24	CANRX/IOPC7
25	RESERVED	26	RESERVED
27	IOPD3	28	IOPD2
29	RESERVED	30	RESERVED
31	CLKIN	32	CLKOUT/IOPD0
33	GND	34	GND

† Duplicated for compatibility with the F240 EVM.

2.7 JTAG Interface.

The TMS320F243 Evaluation Module is supplied with a 14 pin header interface, P5. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown below:

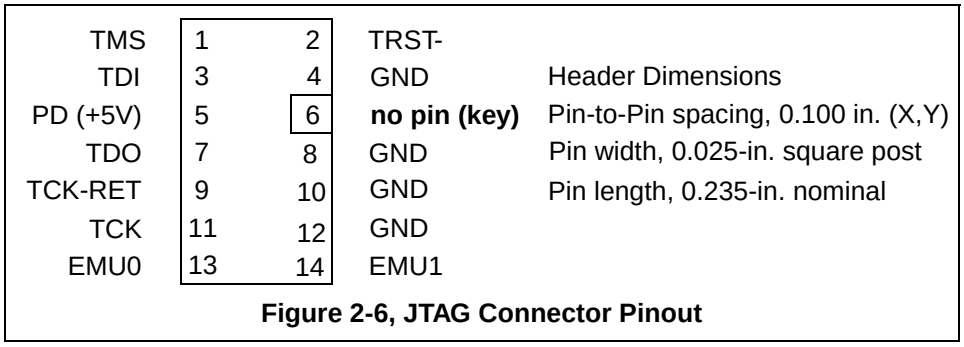
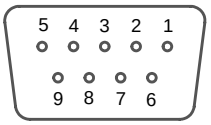


Figure 2-6, JTAG Connector Pinout

2.8 On-Chip Asynchronous Serial Port

The TMS320F243 DSP has an on-chip asynchronous serial port. This port is brought out to connector P6 on the EVM320F243. Connector P6 is a DB9 female connector. This RS232 connector allows the user to connect an external instrument or computer to the EVM320F243. This means data can be logged or commands given to the control algorithm. The user should refer to documentation on jumpers JP8 - JP11 prior to using this serial port. The pin positions for the P6 connector as viewed from the edge of the EVM320F243.



The pin numbers and their corresponding signals are shown in the table below:

Table 7: P6 RS232 Pinout

Pin #	PC (female)	SD EVM
2	Rx, input	Tx, output
3	Tx, output	Rx, input
4	DTR, output	Reset/CTS, input
5	GND	GND
8	CTS, input	RTS, output

2.9 CAN Interface

The EVM320F243 has a CAN interface which provides an additional high speed serial interface. A 4 pin mini-DIN female connector, P7, is used to interface to the CAN bus. The pinouts for this connector are shown in the figure and table below. The CAN termination resistor is controlled by jumper JP12.

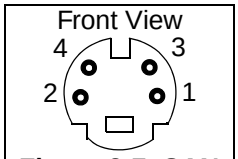


Figure 2-7, CAN Connector

Table 8: CAN Connector Signals

Pin #	Signal
1	CANH
2	CANL
3	GND
4	No Connection

2.9.1 CAN Mating Plugs

A 4 pin min-DIN male plug can be used to mate with the P7 connector. A source for these plugs is shown in the table below:

Table 9: CAN Mating Plugs

Vendor	Part #
Digikey	CP-2040
LZR Electronics	MD40

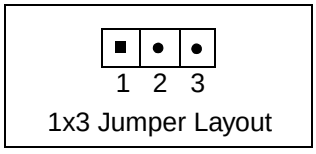
2.10 EVM320F243 Jumpers

The TMS320F243 EVM has 12 jumpers which determine how features on the EVM are utilized. The table below lists the jumpers and their function. The following sections describe the use of each jumper.

Table 10: EVM320F243 Jumpers

Jumper #	Size	Function
JP1	1 x 3	Analog Power Select
JP2	1 x 3	VREF HI Select
JP3	1 x 3	VREF LO Select
JP4	1 x 3	Clock Input Select
JP5	1 x 3	Flash/Watchdog Select
JP6	1 x 3	MP/$\overline{MC}$ Select
JP7	1 x 3	DTS/RTS Select
JP8	1 x 3	SCI Receive Select
JP9	1 x 3	Host Reset Select
JP10	1 x 3	BIO Hardware Handshaking
JP11	1 x 2	CAN Input Select
JP12	1 x 3	CAN Termination Select

Each jumper on the TMS320F243 EVM is a 1x3 jumper. Each jumper must have the selection 1-2 or 2-3. The #2 pin is the center pin. The #1 pin has a square solder pad and can be seen from the solder side of the printed circuit board. This pin is usually marked with a ‘1’ on the boards silkscreen. A top view of this type of jumper is shown below:



1x3 Jumper Layout

WARNING !
Unless noted otherwise, all jumpers must be installed in either the 1-2 or 2-3 position

2.10.1 Jumper JP1, Analog Power Supply Select

Jumper JP1 selects the source of the power for the analog logic on the EVM320C243. In the 1-2 position filtered digital power is used to power the analog logic on the EVM. If the 2-3 position is used, power to the analog section of the EVM is supplied via terminal block connector P2. The table below shows the positions and their functions:

Table 11: Jumper JP1

Position	Function
1-2	Selects digital power for analog logic
2-3	Selects connector P2 as analog power source

2.10.2 Jumper JP2, VREFHI Select

Jumper JP2 is used to select the source for the VREFHI pin on the TMS320F243. Position 1-2 selects the VCCA power which is +5 volts. If position 2-3 is used trim pot R1 is used which allows a variable VREF High from 0-5 volts. The table below shows the positions and their functions:

Table 12: Jumper JP2

Position	Function
1-2	VCCA (+5V VrefH)
2-3	Trim Pot R1 (0-5V VrefH)

2.10.3 Jumper JP3, VREFLO Select

Jumper JP3 is used to select the source for the VREFLO pin on the TMS320F243. Position 1-2 selects the Analog ground. If position 2-3 is used trim pot R2 is used The table below shows the positions and their functions:

Table 13: Jumper JP3

Position	Function
1-2	Analog Ground (VrefL)
2-3	Trim Pot R2 (0-5V VrefL)

2.10.4 Jumper JP4, Oscillator Source Select

Jumper JP4 is used to select the source of the TMS320F243 Clockin. Jumper position 1-2 selects the onboard oscillator. If position 2-3 is used the clock is from pin 31 on the Control connector P4. The table below shows the positions and their functions:

Table 14: Jumper JP4

Position	Function
1-2	Selects Onboard Oscillator
2-3	Selects Pin 31 on Control connector P4

2.10.5 Jumper JP5, Enable/Disable Flash Programming

Jumper JP5 is connected to the VCCP pin of the TMS320F243. On the F243 device this pin enables the programming of the internal flash memory. It also allows disabling the watchdog timer module. Refer to the F243 User's Guide for the programming sequence to disable the watchdog timer. The table below shows the positions and their functions:

Table 15: Jumper JP5

Position	Function
1-2	Disable Flash Programming
2-3	Enable Flash Programming

2.10.6 Jumper JP6, MP/$\overline{\text{MC}}$ - Enable/Disable Internal FLASH ROM

Jumper JP6 is connected to the MP/$\overline{\text{MC}}$ pin on the TMS320F243. When the jumper is in position 1-2 the internal FLASH ROM is disabled. If the shorting plug is in the 2-3 position the internal memory is then enabled. The table below shows the positions and their functions:

Table 16: Jumper JP6

Position	Function
1-2	Internal ROM/FLASH disabled (microprocessor mode)
2-3	Internal ROM/FLASH enabled (microcomputer mode)

2.10.7 Jumper JP7, DTS/RTS Select

Jumper JP7 is used to select the DTS or RTS signal for interrupts to the DSP. If position 1-2 is selected the DTS signal is used to interrupt the DSP. Using position 2-3 allows the RTS signal to interrupt the DSP. The table below shows the positions and their functions:

Table 17: Jumper J7

Position	Function
1-2	DTS is selected
2-3	RTS is selected

2.10.8 Jumper JP8, Enable/Disable RXD to SCIRXD/IOPA1

Jumper JP8 enables the serial port P6 RXD to the DSP's SCIRXD/IOPA1 pin. If position 1-2 is selected this features is enabled. Selecting position 2-3 disables this feature and the SCIRXD/IOPA! pin is available on the expansion connector.

Note:
If this feature is enabled (1-2) then the SCIORXD/IO pin from the Control connector P4 is ignored.

The table below shows the positions and their functions:

Table 18: Jumper JP8

Position	Function
1-2	Enables P6 RXD to DSP SCIRXD/IO
2-3	Disables P6 RXD to DSP SCIRXD/IO

2.10.9 Jumper JP9, Enable/Disable Host Reset via DTR-

Jumper JP9 allows the generation of system resets from the serial port P7. When position 2-3 is used this feature is enabled meaning the system is reset when pin 4 (DTR-) is pulled low. This feature is disabled when position 1-2 is used. The table below shows the positions and their functions:

Table 19: Jumper JP9

Position	Function
1-2	Disabled
2-3	Reset from P4, pin4 (DTR-) enabled

2.10.10 Jumper JP10, Enable/Disable RTS to BIO-/IOPC1

Jumper JP4 enables the serial port P6 RTS- to the DSP's BIO-/IOPC1 pin. Using position 1-2 disables this feature, while position 2-3 enables it. This is used when hardware handshaking is required on a serial port communication protocol.

Note:

If this feature is enabled (2-3) then you **must not** drive the BIO-/IOPC1 pin from the control connector P4

The table below shows the positions and their functions:

Table 20: Jumper JP10

Position	Function
1-2	Disables P6 RTS- to BIO-/IOPC3
2-3	Enables P6 RTS- to BIO-/IOPC3

2.10.11 Jumper JP11, CAN Input Select

Jumper JP11 is used to select the source of the CANRX input signal. If position 1-2 is selected the CAN input signal is connected to the CAN receiver. Using position 2-3 allows the CANRX/IOPC7 connected to the expansion connector P4, pin 24 to be used as the signal source. The table below shows the positions and their functions:

Table 21: Jumper J11

Position	Function
1-2	CAN Connector, P7
2-3	Expansion Connector

2.10.12 Jumper JP12, Enable/Disable CAN Terminator

Jumper JP12 enables or disables the CAN termination resistor. Using position 2-3 enables the termination resistor. If position 1-2 is used the termination resistor is disabled. The table below shows the positions and their functions:

Table 22: Jumper J12

Position	Function
1-2	Disable Termination Resistor
2-3	Enable Termination Resistor

2.11 Status LEDs

The TMS320F243 EVM has three status light emitting diodes. Two of these are under software control. DS7 is ‘on’ when power is applied. These are shown in the table below:

Table 23: Status LEDs

LED #	Color	Controlling Signal	On Signal State
DS5	Red	XF/IOPC0 on DSP	1
DS6	Yellow	BIO-/IOPC1 on DSP	1
DS7	Green	Power On	N/A

2.12 Resets

There are multiple resets for the TMS320F243 EVM. The first reset is the power on reset which is generated by the U17. This device waits until power is within the specified voltage range before releasing the power on reset pin to the TMS320F243.

There is also a system reset RS- which is both input and output from the TMS320F243. Internal conditions such as a watchdog time-out will cause the RS- pin to go low. External sources such as the push button(SW1), Host reset pin 4 on P4, and pin 13 on the Control connector P4 can generate a reset condition.

2.13 ON/OFF Switch

Switch SW3 controls both the analog and digital power. Flipping this switch to the “ON” position powers up the EVM.

2.14 Reset Switch

Switch SW1 is the user RESET switch. By momentarily depressing this switch the $\overline{RS}$ signal is asserted to the TMS320F243 DSP.

2.15 Test Point

One test point is provided on the TMS320F243 EVM that is connected to the GND plane. This is used for connecting a scope’s ground signal.

[redacted]

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