SPECTRUM DIGITAL INCORPORATED

TMS320C203/F206/LC206 Evaluation Module

Technical Reference

2000 ***DSP Development Systems***

TMS320C203/F206/LC206
Evaluation Module
Technical Reference

503481-0001 Rev. C
April 2000

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Contents

About This Manual

This document describes the board level operations of the TMS320C203/TMS320F206 evaluation module (EVM). The EVM is based on the Texas Instruments TMS320C20X Digital Signal Processor.

The TMS320C20X EVM table top card allows engineers and software developers to evaluate certain characteristics of the TMS320C203 and TMS320F206 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320C203 will sometimes be referred to as the C203 or C20X.

The TMS320F206 will sometimes be referred to as the F206 or C20X.

The TMS320LC206 will sometimes be referred to as the LC206 or C20X.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320C2XX Users Guide
Texas Instruments TMS320 Fixed Point Assembly Language Users Guide
Texas Instruments TMS320 Fixed Point C Language Users Guide
Texas Instruments TMS320 Fixed Point C Source Debugger Users Guide
Texas Instruments TLC320AD50 Data Manual

Chapter 1

Introduction to the TMS320C20X Evaluation Module

This chapter provides you with a description of the TMS32C20X Evaluation Module, key features and circuit board block diagram.

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1.0 Overview of the TMS320C20X EVM

The TMS320C20X evaluation module(EVM) is a stand-alone card that allows evaluators examine certain characteristics of the TMS320C203, TMS320F206, or TMS320LC206 digital signal processor(DSP) to determine if this DSP meets their application requirements. Furthermore, the module is an excellent platform to develop and run software on the C20X family of processors.

The C20X EVM is shipped with a choice of DSPs; the TMS320C203, the TMS320CF206, TMS320LC206, or other pin compatible family members as they become available. The EVM allows full-speed verification of C20X code. With at least 544 words of on-chip memory, 128K words of onboard memory, onchip/onboard boot Flash ROM, on-chip UART, onboard UART, and a TLC320AD55 sigma-delta codec, the board can solve a variety of problems as shipped. Four expansion connectors are provided for any necessary evaluation circuitry not provided on the as shipped configuration.

To simplify code development and shorten debugging time, a number of optional user interfaces are provided.

1.1 Key Features of the TMS320C20X EVM

The C20X EVM has the following features:

- C203/LC206 operating at 40 MIPS with 128K words of zero-wait state memory or F206 operating at 20 MIPS
- TLC320AD50 Sigma-Delta Codec with RCA Jack input and output
- On-Chip UART with RS232 Drivers
- Onboard UART
- 32K words on board Flash ROM
- 32K words on-chip Flash ROM when using F206
- 4 Expansion Connectors
- On board IEEE 1149.1 JTAG Connection for Optional Emulation
- 5-Volt Only Operation (on board 3.3-volt regulator for LC206)

1.2 Functional Overview of the TMS320C20X EVM

Figure 1-1 shows a basic configuration block diagram of the C20X EVM. The major interfaces of the EVM include the target RAM and ROM interface, target UART, analog interface, and expansion interface.

The C20X interfaces to 128K Words of zero-wait state static memory. An external I/O interface supports 65,000 parallel I/O ports and optional high-speed synchronous serial port. A Flash ROM is mapped into the global memory interface. RCA jacks provide input and outputs to and from the AD55 sigma-delta codec.

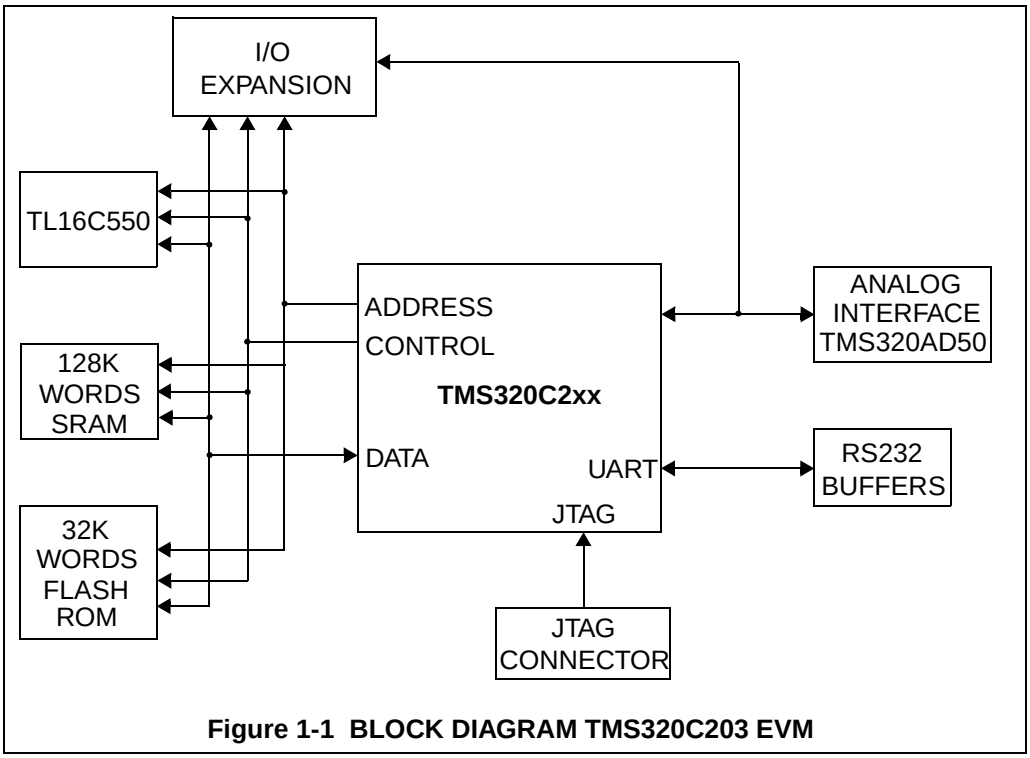

Figure 1-1 BLOCK DIAGRAM TMS320C203 EVM

Chapter 2

Operation of the TMS320C20X Evaluation Module

This chapter describes the operation of the TMS32C20X Evaluation Module, key interfaces and circuit board outline.

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2.0 The EVM320C20X Operation

This chapter describes the C20X Evaluation module, key components, and operation. It also provides information on the various interfaces of the EVM. The C20X EVM consists of six major blocks of logic.

- C20X memory interface
- Analog Interface
- On-chip serial interface
- On board serial interface
- Expansion connector interface
- JTAG interface

2.1 The TMS320C20X EVM Board

The EVM320C20X is a 3U sized board which is powered by an external 5-Volt only power supply. Figure 2-1 shows the layout of the C20X EVM.

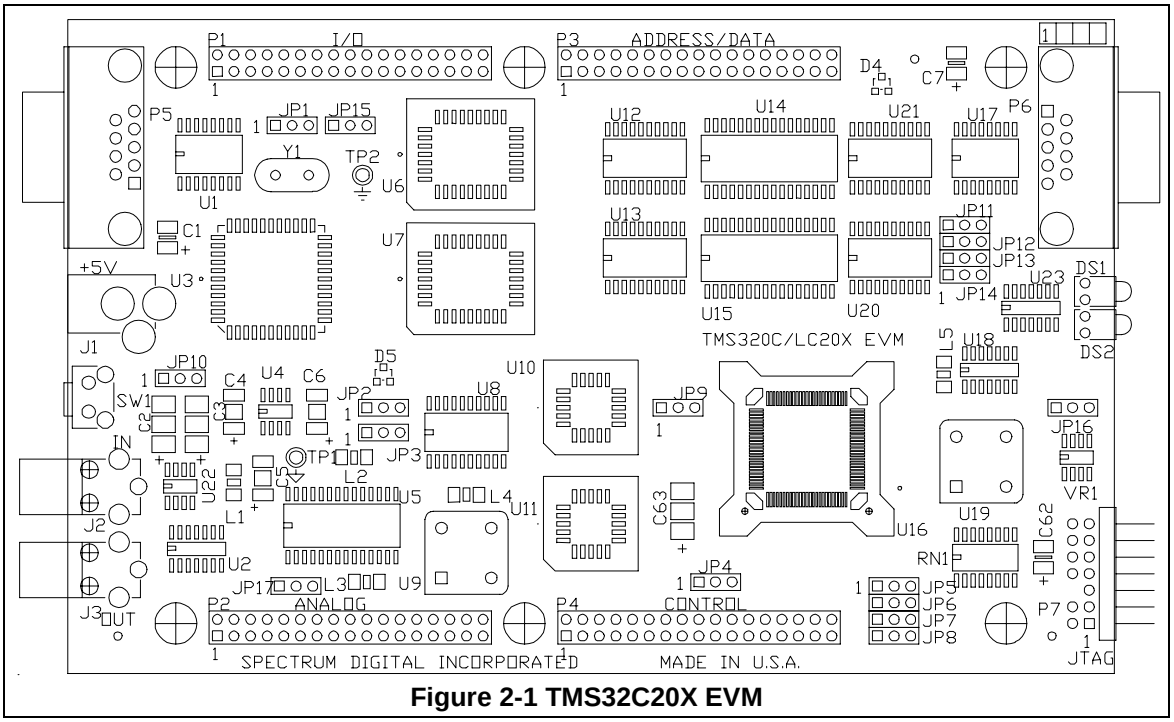


Figure 2-1 TMS32C20X EVM

2.1.1 Power Connector, J1

The C20X is powered by a 5-Volt only power supply available with the module. The board requires 750 milliamps. The power is supplied via 2 millimeter jack J1. If expansion boards are connected to the module a higher amperage power supply may be necessary.

2.2 TMS320C20X Memory Interface

The EVM includes 64K words of zero-wait state program RAM memory and 64k words of zero-wait state data RAM memory, providing a total of 128K words of off-chip static RAM. The board also features 2 external 32KB Flash ROMs. These ROMs are located in the global memory space and can be used to boot load programs with the on-chip boot loader or can be mapped in program space and copied into RAM and disabled on the pseudo boot loader. A jumper (JP8) is connected to the MC/MP pin and allows users to enable or disable boot loading at power up, or use the F206's internal Flash instead of the onboard external Flash.

Figure 2-2 shows the EVM's memory map. It is important to remember internal memory has a higher precedence than external memory. For more information on the memory in the device populated in your EVM card, please refer to Texas Instruments TMS320C2XX Users Guide. Futhermore, it is important to take into account external memory is affected by wait-states. Wait states generation is done both on-chip with the WSGR on-chip wait state generation register and off-chip with the ready signal. To obtain zero-wait state memory in both the program and data memory spaces the on-chip wait-state generators must be appropriately programmed. The board powers up with 7-wait states. The EVM board does not generate wait states via the ready signal for external program and data memory accesses. Only external I/O accesses to on-board peripherals generate a not ready signal. The I/O Wait States should not be set to less than 3 in the WSGR Register.

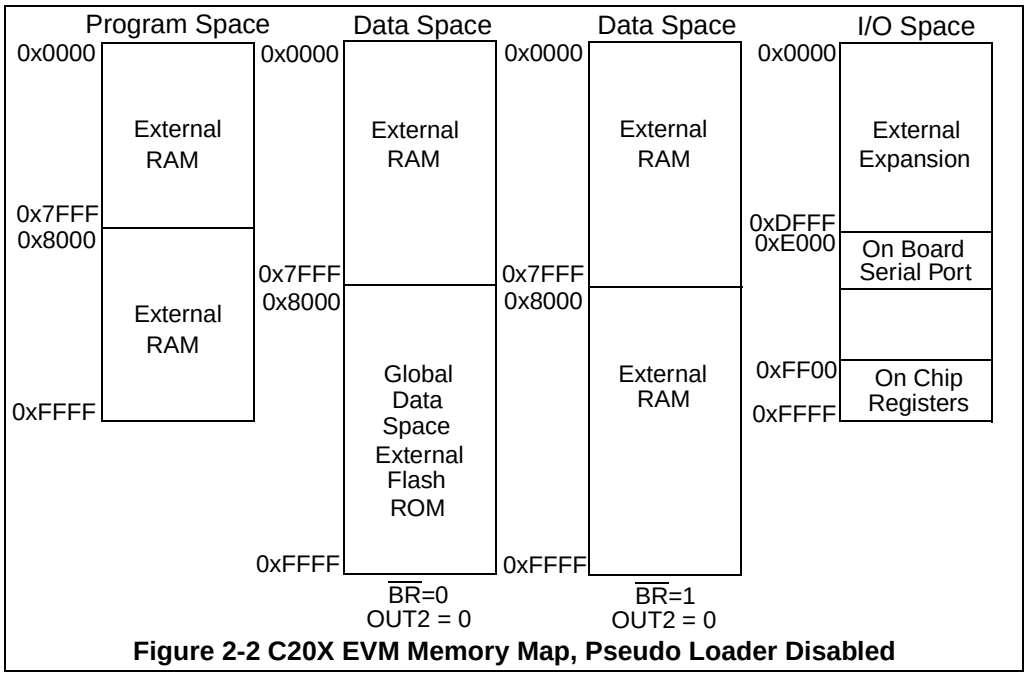


Figure 2-2 C20X EVM Memory Map, Pseudo Loader Disabled

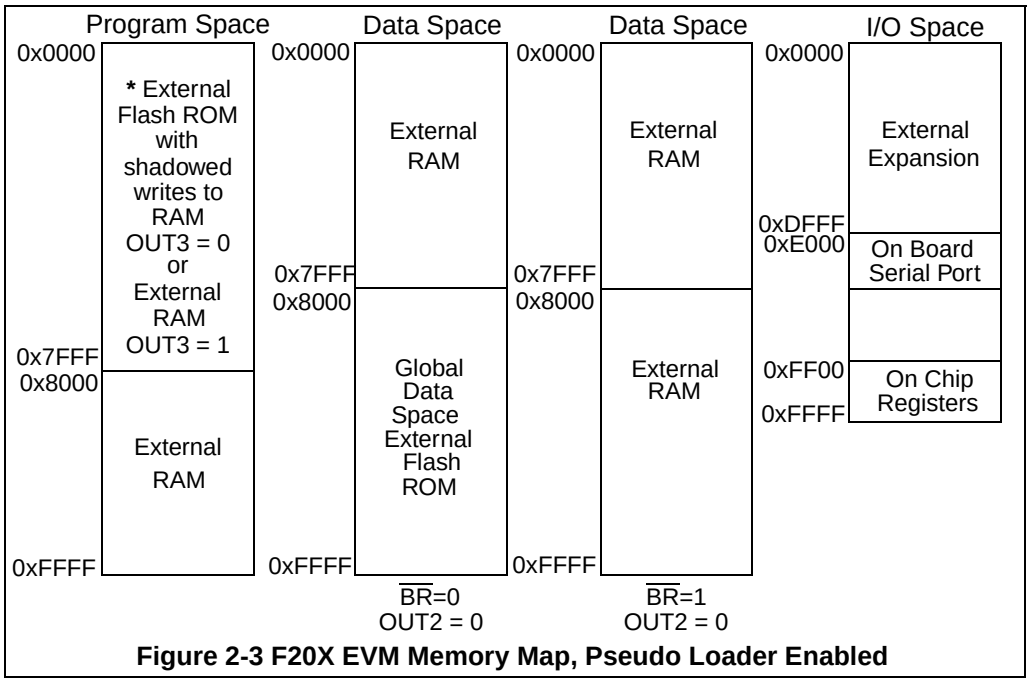


Figure 2-3 F20X EVM Memory Map, Pseudo Loader Enabled

*Note: When JP8 is installed in the 1-2 position for F206 internal Flash memory has precedence and is mapped in this space

The C20X EVM can be configured in a variety of ways. The following is a brief outline of configuration for both the C203 and F206.

NOTE

All references to OUT1, OUT2, and OUT3 refer to control registers as outlined in Table 1. The pin states are inverted.

The standard configuration, for the C203, is in pseudo boot load mode (JP8, 2-3 and JP9, 2-3). However, to use the on-chip boot loader jumper, both JP8 and JP9 are set to the 1-2 position. In this mode, the processor loads programs from the lower 8-bits of global data memory and then begins execution. The external Flash ROM is enabled in global memory at boot. However by setting the OUT2 bit to ‘1’ the boot ROM is disabled. Jumper JP9 is used to distinguish between using the pseudo boot loader or having the entire memory map RAM based.

The standard configuration on the F206 is in a pseudo boot load mode. Jumper JP8 is in position 2-3 disabling the on-chip Flash. Jumper JP9 is in position 2-3 notifying the external memory decoder that a pseudo boot loader is active. In this mode the external Flash ROM is mapped in both global data space (for programming) and in read-only mode at program address 0x0000-0x7FFF. The external program RAM is shadowed in locations 0x0000-0x7FFF so that writing to these locations allow the contents of the external Flash to be copied into external RAM. By setting OUT3 to a ‘1’ the external flash is entirely removed from the program space. By setting OUT2 to a ‘1’ the external flash is removed from the external global data space.

2.2.1 Memory Mapping

Memory mapping is controlled by two jumpers (JP8 and JP9), and two software controlled output pins (OUT2 and OUT3) from the TL16C550 UART.

Table 1: Memory Map control Bits

OUT2	OUT3(DTR)	Description
0	0	External Flash Read/Write
0	1	External Flash Shadowed
1	0	External Flash Disabled
1	1	External Flash Disabled

External memory decode is done via U10, a GAL16V8. The generic array device selects the RAM, FLASH ROM, onboard peripherals, or off board peripherals. The equations for the GAL are included in Appendix A. Figure 2-4 shows a zero-wait state program space memory read followed by a data space memory write.

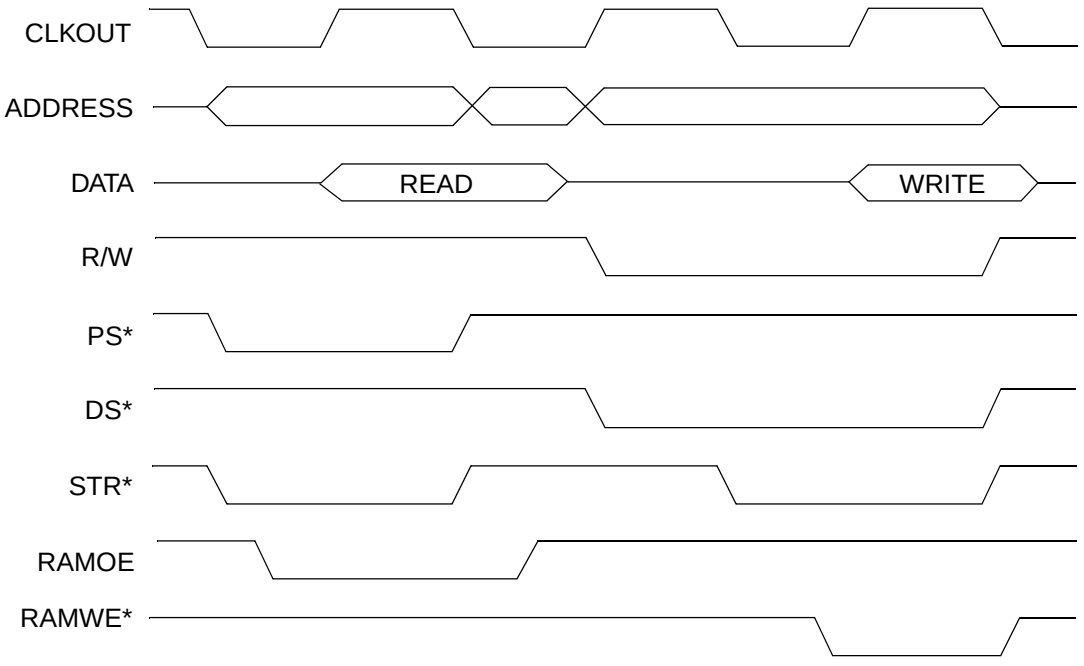


Figure 2-4 Zero-Wait State Memory Timing

The external Flash ROM is mapped into the global data space or program space. Note this memory requires multiple wait states. The main purpose of this memory is to allow for the boot loading of programs from either the C203's internal boot loader or the pseudo boot loader created in external Flash. For more information on the boot loader please refer to the Texas Instruments TMS320C2XX Users Guide.

2.3 Expansion Bus

The TMS320C20X EVM has 4 expansion connectors. Each of these carry a specific type of signals. These connectors are used for hardware expansion or customization to meet the application's unique requirements.The four connectors are:

Table 2: Expansion Connectors

Connector	Function
P1	I/O
P2	Analog
P3	Address/Data
P4	Control

I/O accesses from 0x0000 to 0xDFFF are mapped onto the I/O connector. The address data and control lines are not buffered onto these buses. The expansion I/O buses are meant to execute with at least 2-wait states in the WSGR register to accommodate the onboard UART. However the ready signal can be asserted if a longer access time is required. The next 4 tables describe these connectors.

2.3.1 Expansion I/O Connector, P1

The definition of P1, which has the I/O signals is shown below.

Table 3: P1 I/O

Pin #	Signal	Pin #	Signal
1	VCC, +5 Volts	2	VCC, +5 Volts
3	TOUT	4	Reserved
5	Reserved	6	Reserved
7	Reserved	8	Reserved
9	Reserved	10	Reserved
11	Reserved	12	Reserved
13	OUT1	14	OUT 2
15	OUT3	16	Reserved
17	GND	18	GND
19	XF	20	BIO
21	Reserved	22	Reserved
23	I/O 0 (20X)	24	I/O 2 (20X)
25	I/O 1 (20X)	26	I/O 3 (20X)
27	TX (20X)	28	RX (20X)
29	IN1	30	IN3
31	IN2	32	Reserved
33	GND	34	GND

2.3.2 Expansion Analog Connector, P2

The definition of P2, which has the analog signals is shown below.

Table 4: P2 Analog

Pin #	Signal	Pin #	Signal
1	VCCA, +5V Analog	2	VCCA, +5V Analog
3	ADCIN 0 (AD50)	4	Reserved
5	Reserved	6	Reserved
7	Reserved	8	Reserved
9	Reserved	10	Reserved
11	FLAG 0 (AD50)	12	Reserved
13	Reserved	14	Reserved
15	Reserved	16	Reserved
17	Reserved	18	Reserved
19	Reserved	20	Reserved
21	Reserved	22	-5V
23	AGND	24	AGND
25	DACOUT 0 (AD50)	26	Reserved
27	Reserved	28	Reserved
29	Reserved	30	Reserved
31	Reserved	32	Reserved
33	AGND	34	AGND

2.3.3 Expansion Address and Data Connector, P3

The definition of P3, which has the address and data signals is shown below.

Table 5: P3 Address/Data

Pin #	Signal	Pin #	Signal
1	A0	2	A1
3	A2	4	A3
5	A4	6	A5
7	A6	8	A7
9	A8	10	A9
11	A10	12	A11
13	A12	14	A13
15	A14	16	A15
17	GND	18	GND
19	D0	20	D1
21	D2	22	D3
23	D4	24	D5
25	D6	26	D7
27	D8	28	D9
29	D10	30	D11
31	D12	32	D13
33	D14	34	D15

2.3.4 Expansion Control Connector, P4

The definition of P4, which has the control signals is shown below.

Table 6: P4 Control

Pin #	Signal	Pin #	Signal
1	VCC, +5 Volts	2	VCC, +5 Volts
3	DS-	4	PS-
5	IS-	6	BR-
7	WE-	8	RD-
9	STRB-	10	R/W
11	READY	12	Reserved
13	RS-	14	TRGRESET-
15	NMI-	16	INT1-
17	GND	18	GND
19	INT2-	20	INT3-
21	DR	22	Reserved
23	DX	24	Reserved
25	FSR	26	Reserved
27	FSX	28	Reserved
29	CLKXR	30	Reserved
31	Reserved	32	CLKOUT
33	GND	34	GND

2.4 Analog Interface

The C20X synchronous serial port can be used to access either the onboard TLC320AD50 sigma-delta codec, or be jumpered to the expansion connector. Jumper JP2 (1-2) is used to interconnect the serial port to the AD50. If the serial port is to be used from the expansion connector the plug should be in the 2-3 position.

.

Table 7: AIC Signal source

JP2 Position	Signal Source
1-2	TLC320AD50
2-3	Expansion Connector P4

Programming information for the TLC320AD50 is contained in appendix D.

2.4.1 Analog Input, J2

The analog input is driven from either RCA Jack J2 or expansion connector P2. The analog input can be either AC or DC coupled. Jumper JP10 determines if the input is AC or DC coupled.

Table 8: J2 Coupling

JP10 Position	Input Coupling
1-2	DC Coupled
2-3	AC Coupled

2.4.2 Analog Output, J3

The analog output is driven to RCA Jack J3 and expansion connector P2.

2.4.3 Bias Selection

Either the internal voltage bias or external voltage bias can be used with the AD50 by selecting the appropriate position on jumper JP17. When JP17 is in the 1-2 position, the external bias is used. This allows for AC or DC inputs to the EVM. When the 2-3 position is selected AC biasing should be used. RC1 and RC2 should be replaced with .1uF capacitors in this mode.

2.5 JTAG Interface, P7

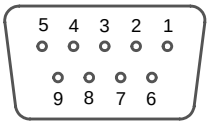
The TMS320C20X Evaluation Module is supplied with a 14 pin header interface. This interface is labeled P7 and is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown below:

TMS	1	2	TRST-	
TDI	3	4	GND	Header Dimensions
PD (+5V)	5	6	**no pin (key)**	Pin-to-Pin spacing, 0.100 in. (X,Y)
TDO	7	8	GND	Pin width, 0.025-in. square post
TCK-RET	9	10	GND	Pin length, 0.235-in. nominal
TCK	11	12	GND	
EMU0	13	14	EMU1	

Figure 2-5 JTAG Interface

2.6 On-Chip Asynchronous Serial Port, P6

The TMS320C203 DSP has an on-chip asynchronous serial port. This port is routed to connector P6 on the EVM320C203. Connector P6 is a DB9 female connector. This RS232 connector allows the user to connect an external instrument or computer to the EVM320C20X. Data can be logged or commands given to the control algorithm using this serial port. The pin positions for the P6 connector as viewed from the edge of the EVM320C203.



The pin numbers and their corresponding signals are shown in the table below:

Table 9: P6 RS232 Pinout

Pin #	PC (female)	SD EVM
2	Rx, input	Tx, output
3	Tx, output	Rx, input
5	GND	GND
7	RTS, output	CTS, input
8	CTS, input	RTS, output

Furthermore, there are 4 jumpers which allow the on chip asynchronous serial port to be used on the expansion bus as shown in the table below:

Table 10: P6 Signal Routing

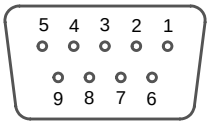
Jumper	Position	Routing
JP11	1-2	Tx to P6
	2-3	Tx to expansion bus P1
JP12	1-2	Rx to P6
	2-3	Rx to expansion bus P1
JP13	1-2	I/O2 to P6
	2-3	I/O2 to expansion bus
JP14	1-2	I/O3 to P6
	2-3	I/O3 to expansion bus

2.7 Onboard Serial Interface, P5

The EVM320C203 has a TL16C550 UART (U3) which provides an additional serial interface. This UART is mapped into I/O space at locations 0xE000 to 0xE008. This device allows users to use this resource for data logging, code debugging and other applications.

The programming of the TL16C550 UART is described in appendix C.

This UART is brought out to connector P5 on the EVM320C20X. Connector P5 is a DB9 female connector. The pin positions for the P5 connector as viewed from the edge of the EVM320C20X.



The pin numbers and their corresponding signals are shown in the table below:

Table 11: P5 RS232 Pinout

Pin #	PC (female)	SD EVM
2	Rx, input	Tx, output
3	Tx, output	Rx, input
4	DTR, output	Reset/CTS, input*
5	GND	GND
8	CTS, input	RTS, output

* Jumper JP15 can also be used to configure pin 4 to pin 7 on P5. This allows for normal handshaking. The jumper setting are shown in to table below:

Table 12: JP15 Settings

JP15 Position	CTS Routing
1-2	P5 pin 4 used on CTS input
2-3	P5 pin 7 used on CTS input

Connector P5 pin 4 can be jumpered via JP5 to generate different interrupt levels. The type of interrupt is shown in the table below:

Table 13: Onboard UART Interrupt Selection

JP5 Position	Interrupt Level
1-2	NMI
2-3	INT1

2.8 EVM320C20X Jumpers

The EVM320C20X has 15 jumpers which determine how features on the EVM are utilized. The table below lists the jumpers and their function. The following sections describe the use of each jumper.

Table 14: EVM320C20X Jumpers

Jumper #	Size	Function
JP1	1 x 3	UART Reset/CTS
JP2	1 x 3	Synchronous Port Routing
JP3	1 x 3	AD50 Reset Option
JP4	1 x 3	Ready Option
JP5	1 x 3	Onboard UART Interrupt Select
JP6, JP7	1 x 3	Oscillator Multiply Select
JP8	1 x 3	C203 Bootloader Enable
JP9	1 x 3	Pseudo Boot Loader Enable
JP10	1 x 3	J2 Input Coupling
JP11	1 x 3	Onchip UART Tx Routing
JP12	1 x 3	Onchip UART Rx Routing
JP13	1 x 3	I/O2 Routing
JP14	1 x 3	I/O3 Routing
JP15	1 x 3	P5 pin 4 Routing
JP16	1 x 3	DSP Core Vcc
JP17	1 x 3	AD50 Bias

The figure below shows the position of the jumpers on the C20X EVM.

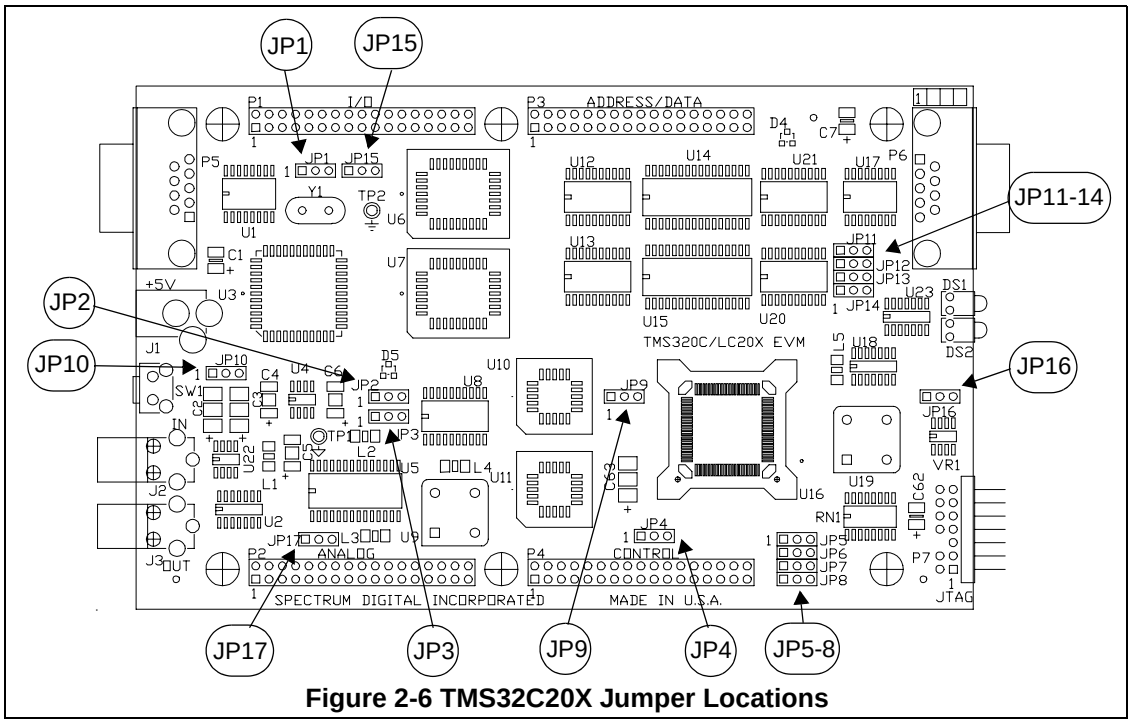
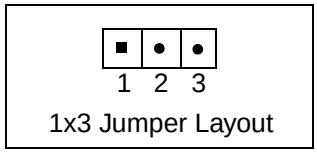


Figure 2-6 TMS32C20X Jumper Locations

Each jumper on the EVM320C20X is a 1x3 jumper. Each 1x3 jumper **must** have the selection 1-2 or 2-3. The #2 pin is the center pin. The #1 pin has a square solder pad and can be seen from the solder side of the printed circuit board. This pin is usually marked with a '1' on the board's silkscreen. A top view of this type of jumper is shown below:



1x3 Jumper Layout

WARNING !
Unless noted otherwise all jumpers must be installed in either the 1-2 or 2-3 position

2.8.1 UART Reset Jumper, JP1

Jumper JP1 is used to select either a system reset from the P5, pin 4 DTR line or to connect the DTR line to the UART's CTS pin. When position 1-2 is selected the DTR activates the reset. The 2-3 position connects DTR to CTS.The table below shows the positions and their functions:

Table 15: UART Reset

JP1 Position	Function
1-2	DTR activates Reset
2-3	Connects DTR to CTS*

* See jumper JP15 for choice of pin 4 or pin 7 to CTS on the onboard UART.

2.8.2 Synchronous Serial Port Routing Jumper, JP2

The JP2 jumper is used to select the source of data for the synchronous serial port on the C20X. By selecting position 1-2 the synchronous serial port is connected to TLC320AD50 AIC. Position 2-3 connects the serial port to the expansion connector P4.

Table 16: Synchronous Serial Port Routing

JP2 Position	Signal Source
1-2	TLC320AD50
2-3	Expansion Connector P4

2.8.3 AD50 Reset Jumper, JP3

The AD50 Codec can be reset either by the system reset or the I/O0 pin on the C20X. Position 1-2 allow the AD50 to be reset by the system reset. In position 2-3 the AD50 is reset from the I/O0 pin on the DSP. The table below shows the positions and their functions:

Table 17: AD50 Reset

JP3 Position	Function
1-2	System reset activates AD50 reset
2-3	C20X I/O0 pin activates AD50 reset

2.8.4 Ready Routing Jumper, JP4

READY to the C20X device from the GAL U11 can be deactivated if necessary. Of course this prevents use of the onboard UART if the wait state generator is set to less than 7 wait states. In normal mode (position 1-2) external READY from the I/O connector is routed through GAL U11. When JP4 is in the 2-3 position the READY signal is routed directly from the expansion connector to the C20X device. The table below shows the positions and their functions:

Table 18: READY Routing

JP4 Position	Function
1-2	READY from GAL U11
2-3	READY directly from I/O expansion connector

2.8.5 Onboard UART Interrupt Select Jumper, JP5

The jumper JP5 is used to select which interrupt the onboard UART will use. Position 1-2 will cause an NMI interrupt. Position 2-3 will cause INT1.

Table 19: Onboard UART Interrupt Selection

JP5 Position	Signal
1-2	NMI
2-3	INT1

This option is used to allow a debug monitor to be placed in ROM or for the serial port to be used with application software which requires interrupt masking.

2.8.6 Oscillator Selection Jumpers, JP6 and JP7

Jumpers JP6 and JP7 are used together to allow the selection of 4 different clock speeds for the TMS320C20X DSP. The TMS320C203 EVM is equipped with a 10 megahertz oscillator. The board comes shipped from the factory with a multiply by two option for the system clock. This allows for 20 MIPS performance. However the user can change the multiply option via jumpers JP6 and JP7. The table below shows the options:

Table 20: Jumpers JP6, JP7

JP7 Position	JP6 Position	Multiply Option	Output Clock
2-3	1-2	0.5X	5 Mhz
2-3	2-3	1X	10 Mhz
1-2	1-2	2X	20 Mhz
1-2	2-3	4X	40 Mhz

2.8.7 Bootload Jumper, JP8

Jumper JP8 is used to enable or disable the bootloader on the TMS320C203 or enable the flash ROM on the F206. The table below describes the two positions:

Table 21: Bootload Enable/Disable

JP8 Position	Function
1-2	Boot enabled on C203/Onchip Flash enabled on F206
2-3	Boot disabled on C203/Onchip Flash disabled on F206

2.8.8 Pseudo Boot Loader Enable Jumper, JP9

Jumper JP9 is used to indicate whether the pseudo boot loader is enabled on the EVM. This input is used by the memory decode logic. When the pseudo boot loader is enabled external flash is mapped in at 0x0000-0x8000 in program space. When the pseudo loader is disabled the entire program space is RAM.

Table 22: Jumper JP9

JP9 Position	Device Selected
1-2	Pseudo Boot Loader Disabled
2-3	Pseudo Boot Loader Enabled

2.8.9 J2 Input Coupling Select Jumper, JP10

Jumper JP10 is used to select the coupling for the analog input. If position 1-2 is selected the coupling is DC. The 2-3 selection will provide AC coupling.

Table 23: J2 Coupling

JP10 Position	Input Coupling
1-2	DC Coupled
2-3	AC Coupled

2.8.10 Tx Signal Routing Jumper, JP11

Jumper JP11 is used to select the destination of the Tx signal from the onchip UART. Position 1-2 on the jumper will route the Tx signal to the 9 pin D-connector, P6. When the 2-3 position is used the Tx signal will be routed to the expansion bus P1.

Table 24: Tx Signal Routing

JP11 Position	Routing
1-2	P6 D-connector
2-3	Expansion Bus P1

2.8.11 Rx Signal Routing Jumper, JP12

Jumper JP12 is used to select the source of the Rx signal to the onchip UART. Position 1-2 on the jumper will 9 pin D-connector, P6, as the source. When the 2-3 position is used the Rx signal will come from the expansion bus P1.

Table 25: Rx Signal Routing

JP12 Position	Routing
1-2	P6 D-connector
2-3	Expansion Bus P1

2.8.12 I/O2 Signal Routing Jumper, JP13

Jumper JP13 is used to select the routing of the I/O2 signal from the DSP. Position 1-2 on the jumper will connect the I/O2 signal to the 9 pin D-connector, P6. When the 2-3 position is used the I/O2 signal will be connected to the expansion bus P1.

Table 26: I/O2 Signal Routing

JP13 Position	Routing
1-2	P6 D-connector
2-3	Expansion Bus P1

2.8.13 I/O3 Signal Routing Jumper, JP14

Jumper JP14 is used to select the routing of the I/O3 signal from the DSP. Position 1-2 on the jumper will connect the I/O3 signal to the 9 pin D-connector, P6. When the 2-3 position is used the I/O3 signal will be connected to the expansion bus P1.

Table 27: I/O3 Signal Routing

JP14 Position	**Routing**
1-2	P6 D-connector
2-3	Expansion Bus P1

2.8.14 Onboard UART CTS Routing Jumper, JP15

Jumper JP15 is used to configure the source of the CTS signal on the onboard UART. When position 1-2 is used the pin 4 on P5 is used as the CTS input. If position 2-3 is chosen pin 7 on P5 is used as the CTS input.

Table 28: Onboard UART CTS Routing

JP15 Position	CTS Routing
1-2	P5 pin 4 used on CTS input
2-3	P5 pin 7 used on CTS input

2.8.15 DSP Core Vcc Selection Jumper, JP16

Jumper JP16 is used to select the core voltage supplied to the DSP. When position 1-2 is used the 3.3 volts is supplied to the DSP core. If position 2-3 is chosen 5 volts is supplied to the core. The table below shows the voltage selection that should be used with various processors.

Table 29: DSP Core Vcc Selection

JP16 Position	Voltage Selected	Processor
1-2	3.3 volts	LC206
2-3	5 volts	C203/F206

WARNING !

Using the wrong core voltage selection may damage the DSP.

2.8.16 AD50 Bias Selection, JP17

Jumper JP17 is used to select the bias voltage source for the AD50. Either the internal voltage bias or external voltage bias can be used with the AD50. When JP17 is in the 1-2 position, the external bias is used. This allows for AC or DC inputs to the EVM. When the 2-3 position is selected AC biasing should be used. RC1 and RC2 should be replaced with.1uF capacitors in this mode.

Table 30: AD50 Bias Selection

JP17 Position	Bias Selected
1-2	External
2-3	Internal

2.9 LEDs

The TMS320C230 EVM has two light emitting diodes. DS1 indicates the presence of +5 volts and is normally ‘on’ when power is applied to the EVM320C20x board. DS2 is under software control. It is tied to the XF signal on the DSP. These are shown in the table below:

Table 31: LEDs

LED #	Color	Controlling Signal	On Signal State
DS1	Green	+5 Volts	1
DS2	Red	XF	1

2.10 Resets

There are multiple resets for the TMS320C203 EVM. The first reset is the power on reset. This circuit waits until power is within the specified range before releasing the power on reset pin to the TMS320C20X.

External sources such as the push button(SW1), Host reset pin 4 on P4 UART interface, and pin p13 on the Control connector P4 can generate a reset condition.

[redacted]

SPECTRUM DIGITAL INCORPORATED

Printed in U.S.A., November 1999
503481-0001 Rev. C