SPECTRUM DIGITAL INCORPORATED

TMS320VC5470/5471 Evaluation Module

Technical Reference

2002 DSP Development Systems

TMS320VC5470/5471
Evaluation Module
Technical Reference

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SPECTRUM DIGITAL, INC.
12502 Exchange Drive, Suite 440 Stafford, TX. 77477
Tel: 281.494.4505 Fax: 281.494.5310
sales@spectrumdigital.com www.spectrumdigital.com

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Contents

About This Manual

This document describes the board level operations of the TMS320VC5470/5471 evaluation module (EVM). The EVM is based on the Texas Instruments TMS320VC5470/5471 Digital Signal Processor.

The TMS320VC5471 EVM is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320VC5471 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320VC5470/5471 will sometimes be referred to as the VC5470 or VC5471 respectively.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320VC54XX Users Guide
Texas Instruments TMS320VC54XX Fixed Point Assembly Language Users Guide
Texas Instruments TMS320VC54XX Fixed Point C Language Users Guide
Texas Instruments TMS320VC54XX Code Composer Studio Users Guide
Texas Instruments TMS470 Users Guide
Texas Instruments TMS470 Assembly Language Users Guide
Texas Instruments TMS470 C Language Users Guide
Texas Instruments TMS470 Code Composer Users Guide

Table 1: Manual History

Revision	History
A	- Initial Release

Table 2: Board History

Revision	History
A	- Initial Release
B	- Reordered user LEDs, corrected wiring error

Table 3: Device Status

Revision	History
A	- Currently I^2C does not operate correctly. Bit I/O is used to implement I^2C protocol.

Chapter 1

Introduction to the TMS320VC5471 Evaluation Module

Chapter One provides a description of the TMS32VC5471 Evaluation Module (EVM) along with the key features and a block diagram of the circuit board.

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1.0 Overview of the TMS320VC5471 Evaluation Module

The TMS320VC5471 Evaluation Module is a stand-alone card. It allows evaluators to examine certain characteristics of the VC5471 processors (ARM7/VC54xx) to determine if it meets their application requirements. Furthermore, the module is an excellent platform to develop and run software on the VC5471 family of processors.

The Evaluation Module allows full speed verification of ARM7 and C54xx code. The ARM7 side has 2 megabytes of SRAM, 8 megabytes of FLASH ROM, 16 megabytes of SDRAM, 1 ethernet port, UART, display interface, user switches, user LEDs, and expansion connectors.

The C54xx side has 256 kilobytes of RAM, AIC23 stereo codec, and expansion connectors.

The board is an excellent development platform for streaming audio, intelligent telephone, PDA, or a variety of other applications.

The expansion connectors on the ARM7 and C54xx allow users to interface custom logic or expansion circuitry no produced on the as shipped configuration.

To simplify code development and shorten debugging time, a number of user interfaces are provided. Debuggers providing assembly language and ‘C’ high level language debug are available with JTAG emulators.

1.1 Key Features of the TMS320VC5471 Evaluation Module

The VC5471 Evaluation Module has the following features:

- VC54xx core operating at 100 MHz with 256K words of two (2) wait state memory
- ARM7 core operating at 45 MHz
- AIC23 Stereo Codec
- 2 Megabytes of static RAM on the ARM7
- 512 Kilobytes of static SDRAM on the C54xx
- 8 Megabytes of Flash ROM
- 16 Megabytes of SDRAM
- Optional Display/keyboard interface
- 1 ethernet port on VC5471
- On board UART
- 54xx and ARM7 expansion connectors
- On board parallel port JTAG controller
- On board IEEE 1149.1 JTAG Connection for optional emulation
- 5-Volt Only Operation

1.2 Functional Overview of the TMS320VC5471 EVM

Figures 1-1 and 1-2 show the block diagram of the basic configuration for the VC5471 EVM. The major ARM7 interfaces of the module include: SDRAM, FLASH, SRAM, ENET, Expansion and a keyboard/display interface.

The major 54xx interfaces of the module include: SRAM, AIC23, and expansion interface.

The block diagram for the ARM7 portion of the EVM320VC5471 is shown below.

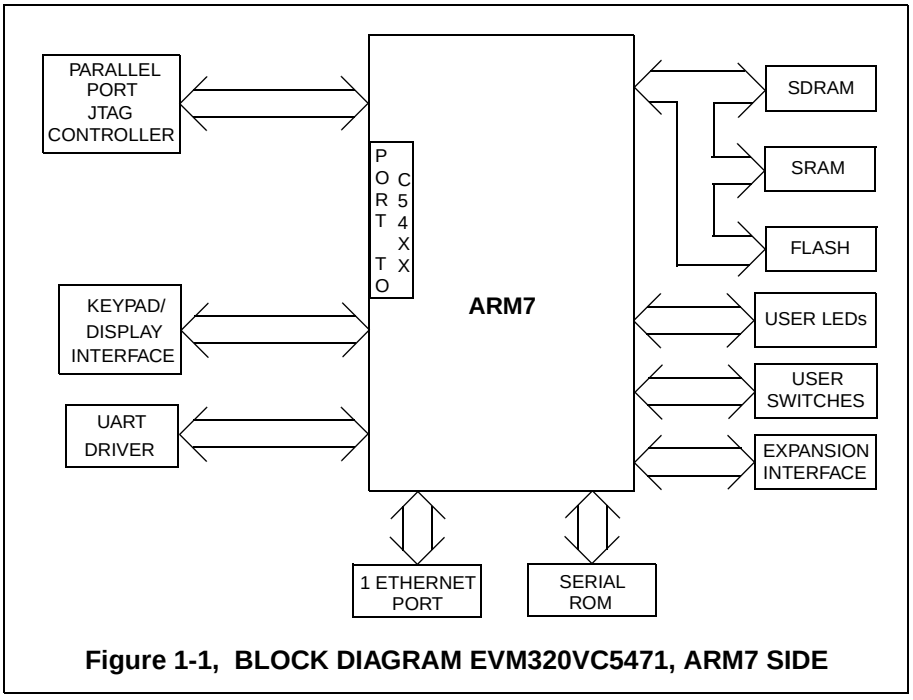

Figure 1-1, BLOCK DIAGRAM EVM320VC5471, ARM7 SIDE

The block diagram for the VC54xx portion of the EVM320VC5471 is shown below.

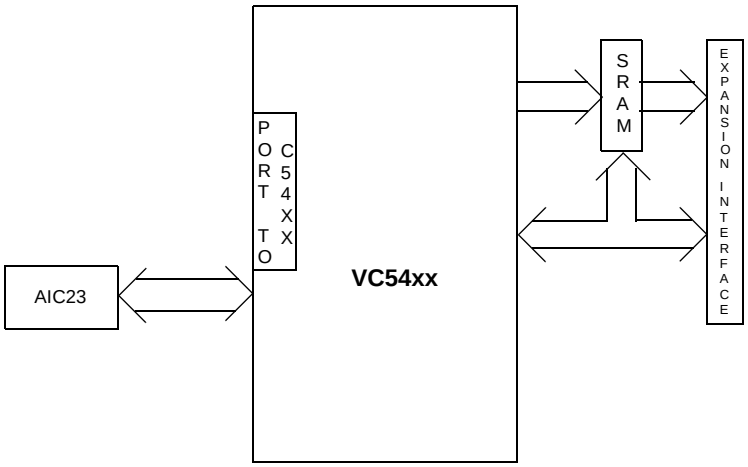

Figure 1-2, BLOCK DIAGRAM EVM320VC5471, VC54xx SIDE

Chapter 2

Operation of the TMS320VC5471 Evaluation Module

This chapter describes the operation of the TMS320VC5471 Evaluation Module, the key interfaces and an outline of the circuit board.

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2.0 The EVM320VC5471 Operation

This chapter describes the TMS320VC5471 Evaluation Module, key components, and how they operate. It also provides information on the EVM320VC5471's various interfaces. The EVM320VC5471 consists of nine major blocks of logic.

- ARM7 external memory
- C54xx external memory
- AIC23 Interface
- ARM7 expansion interface
- C54xx expansion interface
- Ethernet interface
- Keypad/display interface
- User switches and LEDs
- JTAG Interface

2.0.1 Universal Keypad/Display Operation

This chapter also describes the Universal Keypad/Display Module that is included with the TMS320VC5471 EVM. The key components and interfaces of the Keypad/Display Module are described in this chapter. The features of the Keypad/Display module are:

- Liquid Crystal Display (128 x 64) with serial interface
- 2 User potentiometers
- 9 Push button keys

2.1 The EVM320VC5471 Board

The outline of the EVM320VC5471 is shown in the figure below.

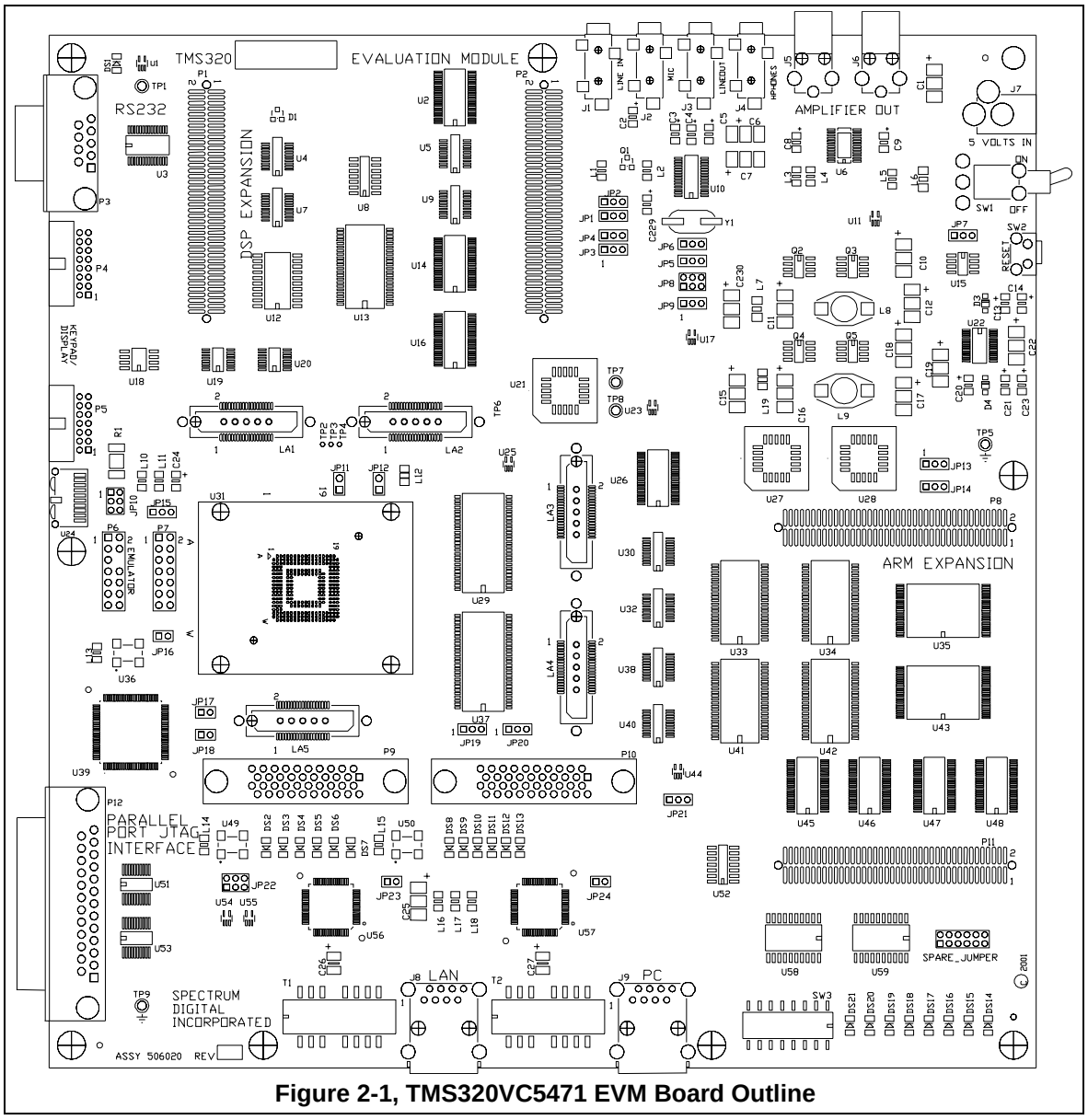

Figure 2-1, TMS320VC5471 EVM Board Outline

2.1.1 The Universal Keypad/Display Module

The TMS320VC5471EVM interfaces to the Universal Keypad/Display Module via connectors P4 and P5. A ribbon cable will attach to connectors P1 and P2 on the Keypad/Display Module. The outline of the Keypad/Display Module is shown in the figure below.

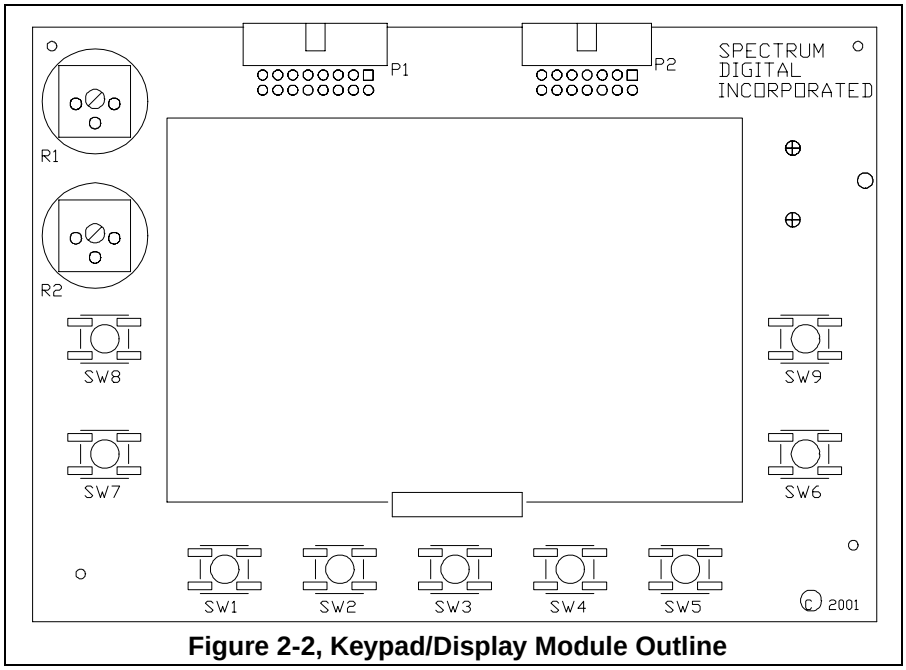

Figure 2-2, Keypad/Display Module Outline

2.1.2 Power Connector

The EVM320VC5471 is powered by a +5 Volt, 4 Amp power supply which is available with the module. The board requires 1.5 amps. The power is supplied via 2 millimeter jack J7. If expansion boards are connected to the module a higher amperage power supply may be necessary. The board also has a 3.3 and 1.8 volt regulator to provide power to the lower voltage components.

2.2 TMS320VC5471/ARM7 Memory Interface

The EVM320VC5471 includes 8 megabytes of on board FLASH ROM, 2 megabytes of SRAM, 16 megabytes of on board SDRAM, a keypad/display interface, and expansion interface.

External memory decode is done via internal chip selects and a generic array device U27. Expansion decode is done via GAL U28.

The external Flash and SRAM can be mapped either at memory address 0x00000000 (CS0) or at 0x00800000 (CS1). Since the ARM7 has reset vectors in low memory configuring the SRAM low is helpful in the evaluation cycle. This is controlled via the board configuration bits 1 and 2 which are mapped to GPIO0 and GPIO1. The use of these configuration bits is shown in the table below.

Table 1: Configuration Bits

GPIO0	GPIO1	Flash	SRAM
0	0	CS1	CS0
0	1	Reserved	Reserved
1	0	Write CS0	Read CS0
1	1	CS0	CS1

Shown below is a portion of a Code Composer Studio GEL file that will configure GPIO0 and GPIO1.

```
ramlow()
{
   // This function configures the 5471 for CS0=SRAM, CS1=FLASH
   (*(long*)0xffff2804) &= 0xfffffffc;   /* Configure GPIO0,1 as outputs */
   (*(long*)0xffff2800) &= 0xfffffffc;   /* Set GPIO0, 1 low */
}
```

2.2.1 ARM7 Memory Interface

The ARM7 memory space provides 6 external chip selects. The mapping of these to physical devices is shown in the table below.

Table 2: ARM7 Chip Selects

Chip Select	Start Address	End Address	Size	Device
nCS0	0x00000000	0x007FFFFF	8 megabytes	SRAM 2 megabyte or Flash 8 megabyte
nCS1	0x00800000	0x00FFFFFF	8 megabytes	Flash 8 megabytes or SRAM 2 megabyte
nCS2	0x01000000	0x017FFFFF	8 megabytes	User Switches & LEDs
nCS3	0x01800000	0x01FFFFFF	8 megabytes	Expansion
nCS4	0x02000000	0x027FFFFF	8 megabytes	Expansion
SDRAM-ncs	0x10000000	0x11FFFFFF	32 megabytes	16 megabytes

The following figures show the various ARM7 timing interfaces for SRAM, FLASH, SDRAM, keypad/display, and expansion memory.

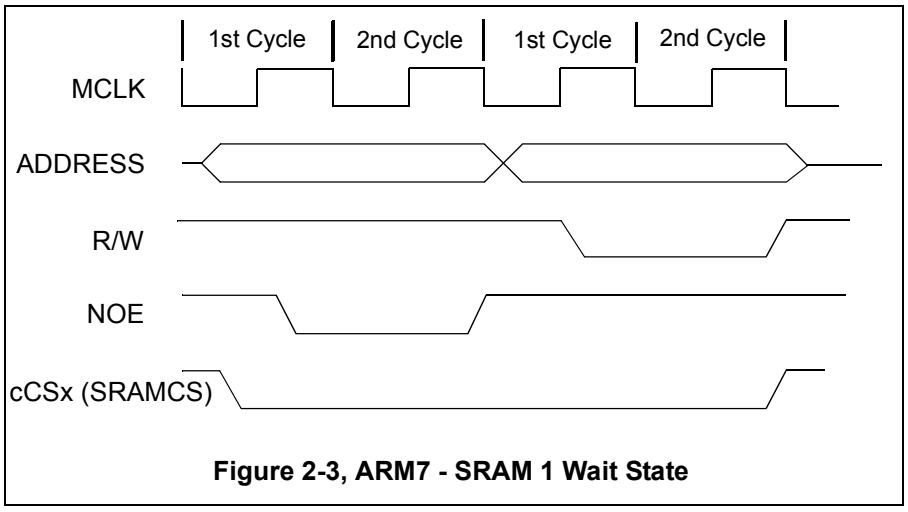

Figure 2-3, ARM7 - SRAM 1 Wait State

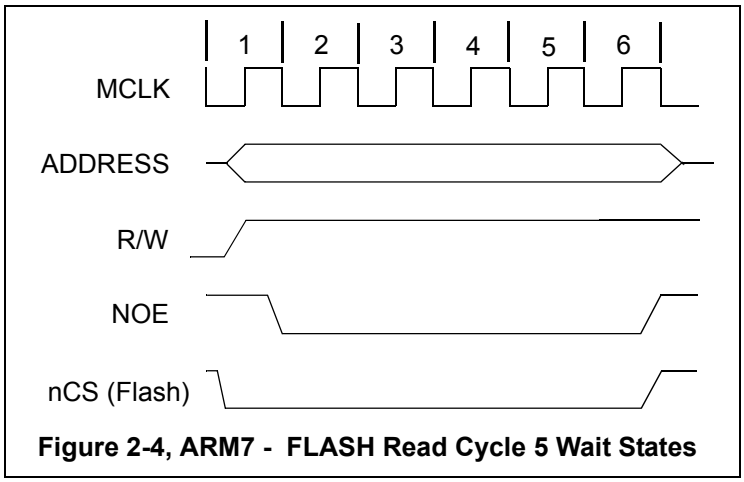

Figure 2-4, ARM7 - FLASH Read Cycle 5 Wait States

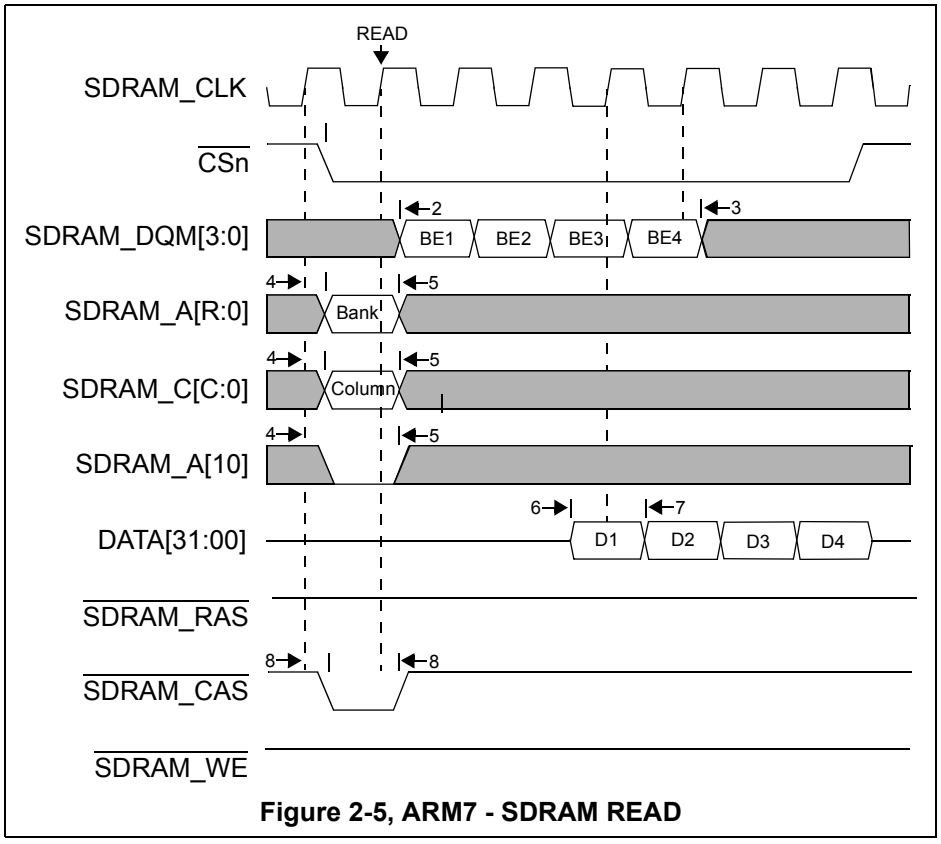

Figure 2-5, ARM7 - SDRAM READ

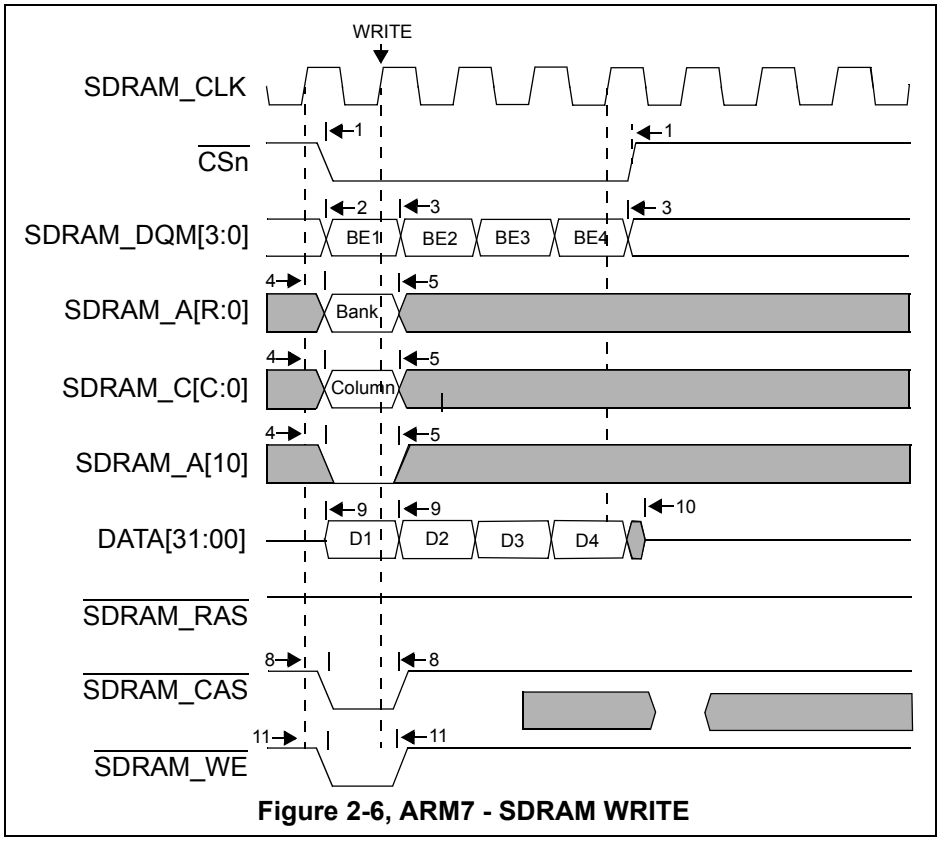

Figure 2-6, ARM7 - SDRAM WRITE

The MCLK for the ARM7 is 45 Mhz. which provides a cycle time of 22 ns. The table below shows the access times and wait states for the various memory interfaces on the ARM7.

Table 3: Configuration Bits

Memory Interface	Access Times	# Wait States
SRAM + Decoder	15 + 12	1
FLASH + Decoder	120 + 12	5

The SDRAM is interfaced via the VC5471's on chip SDRAM controller each access requires multiple cycles to execute. Refer to the data sheet for the device for more information.

2.2.2 DSP Memory Interface

The C54xx portion of the EVM320VC5471 includes 256k Words (16 bits) of on board program/data ram memory. The memory in data space is mirrored in program space.

It is important to remember that internal memory has a higher precedence than the external memory. For more information on the memory in the device populated in your evaluation module please refer to Texas Instruments TMS320VC5471 Users Guide.

Futhermore, it is important to take into account that external memory is affected by wait-states. Wait state generation for off-chip memory space (data, program, or I/O) is done with the Software Wait State Generation Register(SWWSR). To obtain one waitstate off-chip memory bits in the SWWSR must be appropriately programmed. The board powers up with 7 wait-states. The evaluation module board does not generate wait states via the ready signal for external program and data memory accesses, only I/O accesses use the ready signal.

External memory decode is done via U21 a GAL16V8. The generic array device selects the RAM or expansion bus. The equations for the GAL are included in Appendix A. The figure below shows a one wait state program space memory read followed by a data space memory write.

The figure below shows the memory timing for the C54xx processor on the EVM320VC5471.

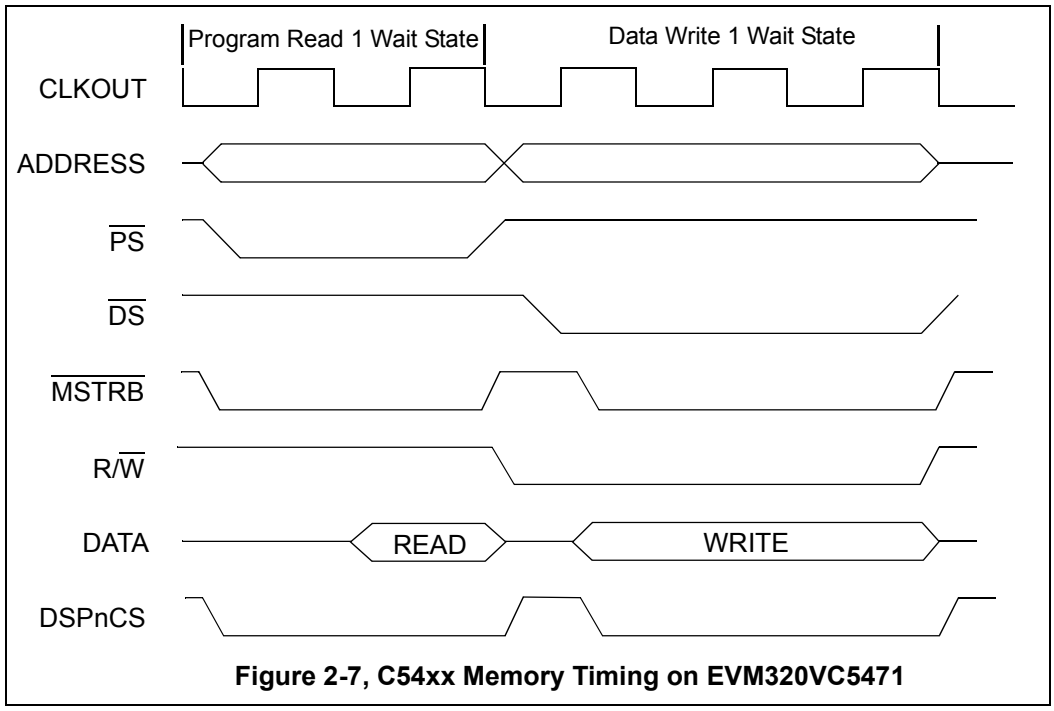

Figure 2-7, C54xx Memory Timing on EVM320VC5471

2.2.3 DSP Program Memory

There are two configurations for program memory. The selection of these configurations is done by the 54xx's OVLY bit. Furthermore the MP/MC bit affects internal memory mapping. Both of the control bits are in the C54xx's PMST register. When in OVLY mode, addresses 0x0000 - 0x8000 are internal for every page. There are eight (8) 32K word pages of external program memory.

The figure below shows the internal/external program RAM mapping for the first 64K words of program space.

Hex	Page 0 Program MP/MC=1 (Microprocessor Mode)	
0x00000	OVLY=1	OVLY=0
0x0007F	Reserved	External Program Space Memory
0x00080	On-chip DARAM	External Program Space Memory
0x01FFF		
0x02000	On-chip DARAM API-accessible	External Program Space Memory
0x03FFF		
0x04000	On-chip SARAM	External Program Space Memory
0x05FFF		
0x06000	On-chip SARAM (8K words, program only)	
0x07FFF		
0x08000	External Program Space Memory	
0x0F7FF		
0x0F800	APIBN=1	APIBN=0
0x0FFFF	External Program Memory Space	Shadow of Data space from 0x3800 to 0x3FFF (2K Words)

Hex	Page 0 Program MP/MC=0 (Microcomputer Mode)	
0x00000	OVLY=1	OVLY=0
0x0007F	Reserved	External Program Space Memory
0x00080	On-chip DARAM	External Program Space Memory
0x01FFF		
0x02000	On-chip DARAM API-accessible	External Program Space Memory
0x03FFF		
0x04000	On-chip SARAM	External Program Space Memory
0x05FFF		
0x06000	On-chip SARAM (8K words, program only)	
0x07FFF		
0x08000	On-chip SARAM (8K words, program only)	
0x09FFF		
0x0A000	On-chip SARAM (8K words, program only)	
0x0BFFF		
0x0C000	On-chip SARAM (8K words)	
0x0DFFF		
0x0E000	On-chip SARAM (8K words)	
0x0F7FF		
0x0F800	APIBN=1	APIBN=0
0x0FFFF	On-chip SARAM (2K Words)	Shadow of Data space from 0x3800 to 0x3FFF (2K Words)

Figure 2-8, EVM320VC5471 DSP Program Space, 0-0xFFFF

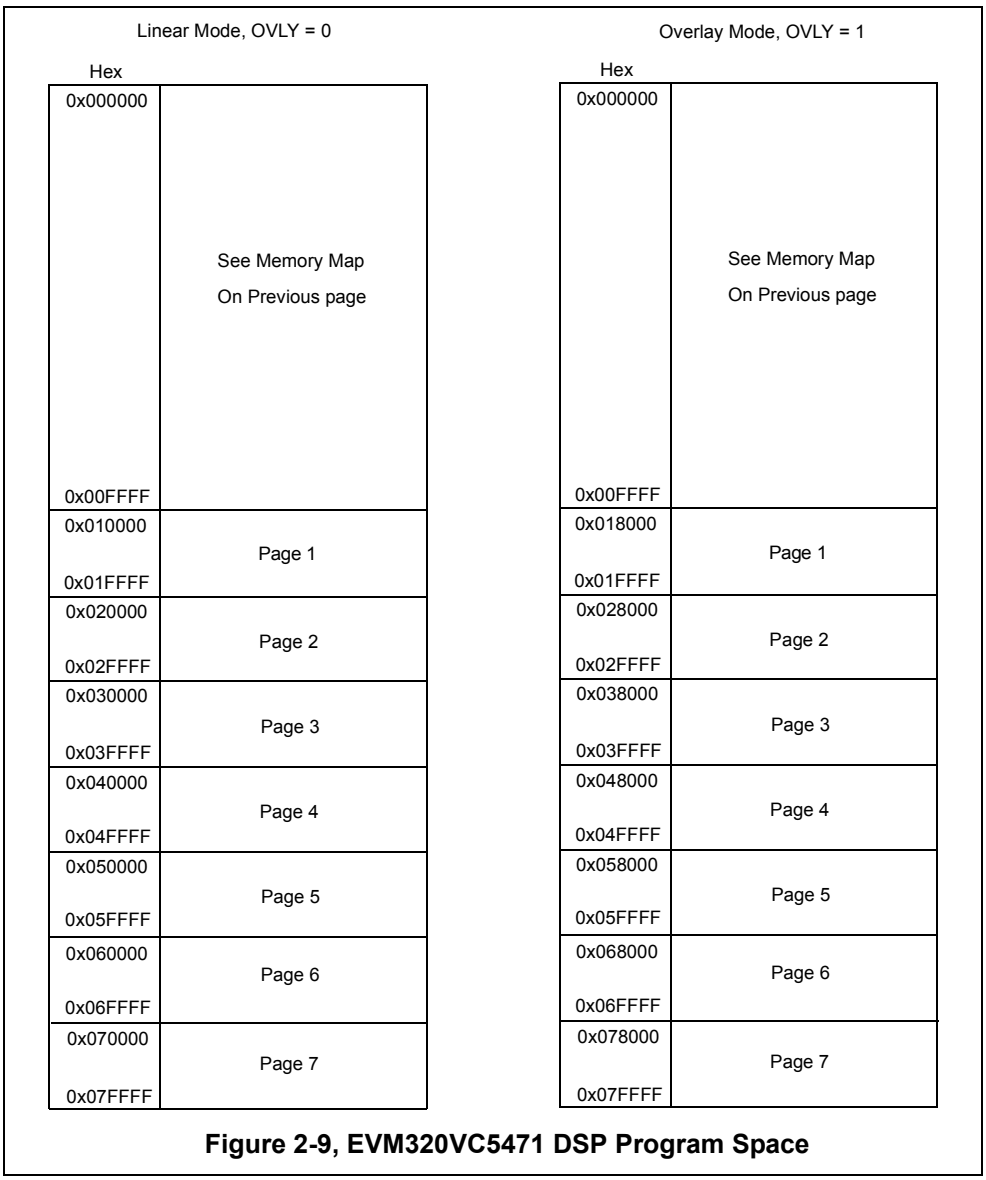

Figure 2-9, EVM320VC5471 DSP Program Space

2.2.4 DSP Data Memory

The DSP data memory configuration is shown below. The external data memory is mapped from 0x8000 to 0xFFFF for the C54xx processor. This external page is mirrored with the program memory space from 0x08000 to 0x0FFFF.

Hex	Data	
0x00000 0x0007F	Memory Mapped Registers Scratch-Pad RAM	
0x00080 0x01FFF	On-chip DARAM (8K-0x80 Words)	
0x02000 0x03FFF	On-chip DARAM, API-Accessible (8K Words)	
0x04000 0x05FFF	On-chip SARAM (8K Words)	
0x06000 0x07FFF	On-chip SARAM (8K Words, data only)	
0x08000 0x0BFFF	External Data Space Memory	
0x0C000	DROM=1	DROM=0
0x0F7FF	On-chip SARAM	External Data-space Memory
0x0F800 0x0FFFF	Reserved	External Data-space Memory

Figure 2-10, EVM320VC5471 DSP Data Space

2.2.5 EVM320VC5471 DSP I/O Space

The I/O map for the DSP on the EVM320VC5471 is shown below:

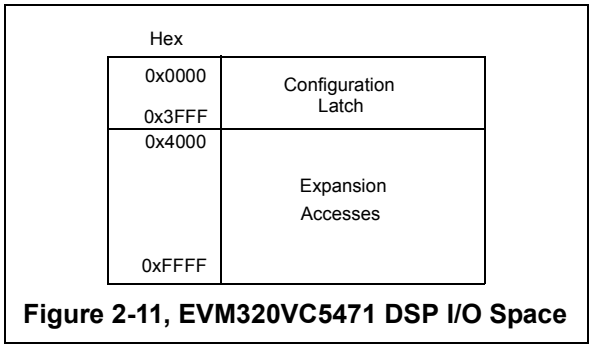

Figure 2-11, EVM320VC5471 DSP I/O Space

2.3 Oscillator Selection

The TMS320VC5471 evaluation module is equipped with a 25 Megahertz oscillator. When the processor resets the PLL Clock Module defaults to 25 Mhz. The PLL can then be programmed to obtain a variety of clock frequencies. If the PLL frequency is required to change after the programming the part must be returned to the divide mode before the programming of the new PLL frequency. The user should refer to the “PLL Clock Module” section in the TMS320VC5471 User’s guide for valid clock configurations.

There is an option to supply an alternate oscillator for the ARM CPU (ethernet always requires 25 Mhz.). U50 can be populated and jumper JP22 configured to allow for other frequencies.

2.4 Scan Chain

The scan chain on the TMS320VC547x is made up of three devices; the ARM7 CPU, the C54xx DSP, and an ASIC peripheral module. The default scan length is 20 bits. However there is a jumper option to allow only the ARM7 CPU to be in the scan chain resulting in a 4 bit scan length when the EMU0 and EMU1 bits are 0 at reset. Refer to sections 2.12.16 - 2.12.18 which discuss the EMU0 and EMU1 bits for jumper settings.

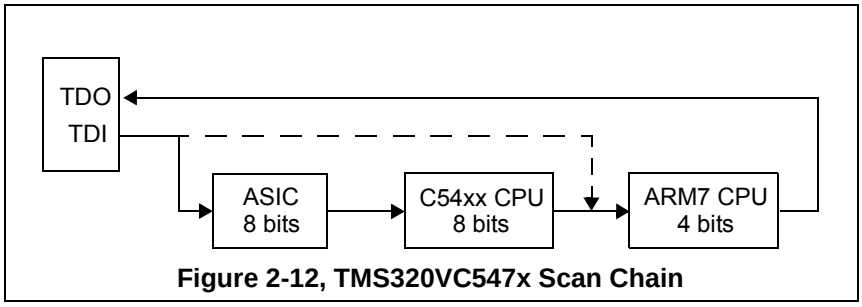

Figure 2-12, TMS320VC547x Scan Chain

2.5 Analog Interface

The VC5471 synchronous serial ports can be used to access either the AIC23 or expansion connectors. Jumpers and DSP configuration latch control these configurations. A block diagram of the codec interface is shown below.

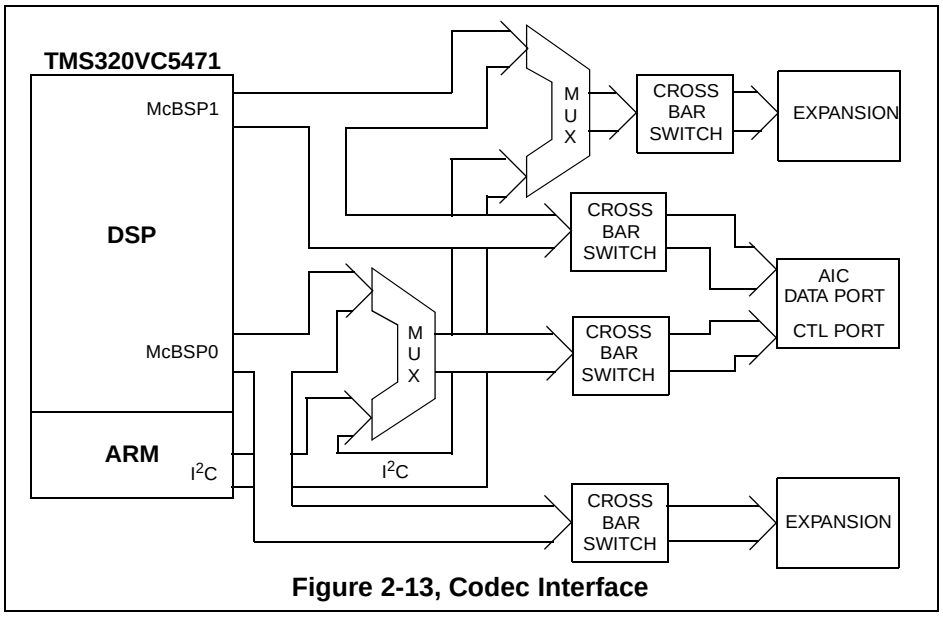

Figure 2-13, Codec Interface

2.5.1 DSP Configuration Latch

The DSP has an 8 bit configuration latch mapped at DSP I/O location 0x0000. This controls McBSP and AIC23 Codec functions. The data bits and their meaning in the Configuration Latch are shown in the table below.

Table 4: DSP Configuration Latch

Data Bit	Function	Reset State
D0	McBSP1 Enable	0
D1	McBSP0 MUX Control	0
D2	McBSP1 Enable	0
D3	AIC23 Analog Power	0
D4	AMP Shutdown	0
D5	Expansion McBSP0 Enable	0
D6	Expansion McBSP1 MUX Control	0
D7	Expansion McBSP1 Enable	0

Example: To configure the latch for on board codec, Latch = 0x1D.

2.5.1.1 DSP Configuration Latch Bit Description

The function of each bit in the DSP Configuration Latch is described below.

D0: McBSP1 Enable
0 = Don't drive McBSP1 to codec data port
1 = Drive McBSP1 to codec data port

D1: McBSP0 Mux Control
0 = Select normal McBSP0 signals on codec control port
1 = Replace McBSP0 signals with I^2C on codec control port

D2: McBSP0 Enable
0 = Don't drive signals to codec control port
1 = Drive signals (McBSP0 or I^2C) to codec control port

D3: AIC23 Analog Power
0 = Turn off power to the codec
1 = Turn on power to the codec

D4: AMP Shutdown
0 = Turn analog amplifier off
1 = Turn analog amplifier on

D5: Expansion McBSP0 Enable
0 = Don't drive McBSP0 to the expansion slot
1 = Drive McBSP0 to the expansion slot

D6: Expansion McBSP1 Mux Control
0 = Select normal McBSP1 signals on expansion slot
1 = Replace McBSP1 signals with I2C on expansion slot

D7: Expansion McBSP1 Enable
0 = Don't drive McBSP1 signals to expansion slot
1 = Drive McBSP1 to expansion slot

2.6 Connectors

The EVM320VC5471 has 12 connectors. These connectors are described in the table below. The following sections will identify the signals on each pin of the connector.

Table 5: EVM320VC5471 Connectors

Connector	Function	# of pins	Layout	Mating Connector Type
P1	DSP Expansion	80	2 x 40	
P2	DSP Expansion	80	2 x 40	
P3	RS-232	9	5, 4	Male DB-9
P4	LCD Interface	16	2 x 8	2 mm.
P5	Keypad Interface	14	2 x 7	2 mm.
P6	TI JTAG	14	2 x 7	0.1 inch
P7	ARM JTAG	40	2 x 20	0.1 inch
P8	ARM Expansion	40	2 x 20	
P9	MII Connector	40	2 x 20	
P11	ARM Expansion	40	2 x20	
P12	Parallel Port JTAG Interface	25	13, 12	Male DB-25

The position of the connectors on the EVM320VC5471 are shown in the figure below.

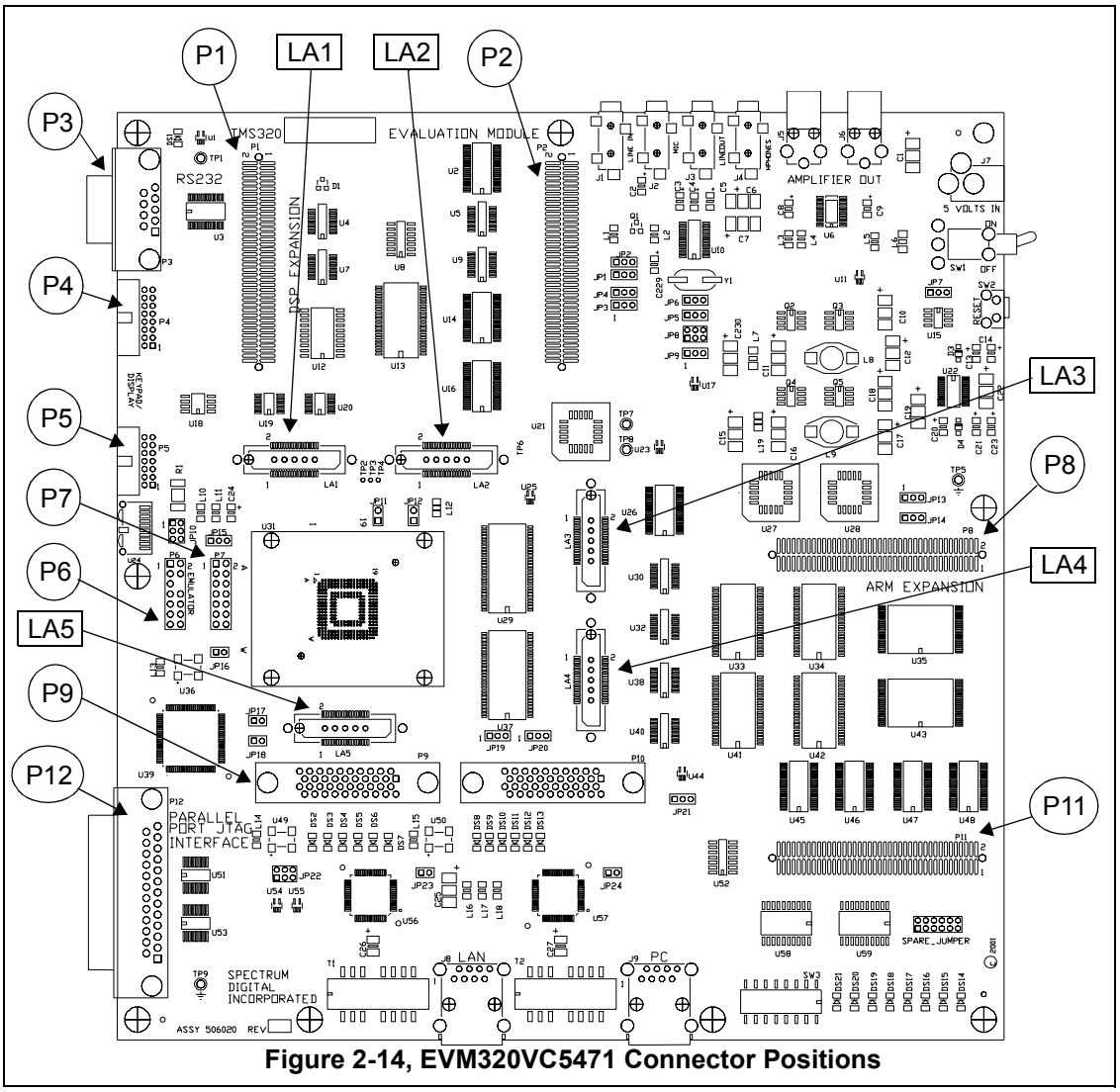

Figure 2-14, EVM320VC5471 Connector Positions

2.6.1 P1, P2, DSP Expansion Bus

The DSP portion of the TMS320VC5471 has two expansion connectors which bring out all of the signals for expansion purposes and custom user logic.

The P1 and P2 expansion connectors are 2 x 40 double row surface mount connectors. All odd numbered pins (1,3,5, ...) are on one side and and the even numbered pins (2,4,6, ...) are on the other. Pin 1 and Pin 2 are indicated in the silkscreen lettering. The signals on these pins are shown in the next table.

Table 6: P1, DSP Expansion Connectors

Pin #	Signal Name	Pin #	Signal Name
1	NC	2	NC
3	Ground	4	Ground
5	+5 Volts	6	+5 Volts
7	Ground	8	Ground
9	+5 Volts	10	+5 Volts
11	AIC23 CLK/IN/OUT	12	NC
13	KBD GPIO8	14	GPIO6
15	I^2C_DATA	16	GPIO9
17	NC	18	I^2C_CLK
19	+3.3 Volts	20	+3.3 Volts
21	BCLKX0	22	NC
23	BFSX0	24	BDX0
25	Ground	26	Ground
27	BCLKR0	28	NC
29	BFSR0	30	BDR0
31	Ground	32	Ground
33	BCLKX1	34	NC
35	BFSX1	36	BDX1
37	Ground	38	Ground
39	BCLKR1	40	NC
41	BFSR1	42	BDX1
43	Ground	44	NC
45	TOUT	46	NC
47	NC	48	NC
49	XF	50	NC
51	Ground	52	Ground
53	INT0-	54	NC
55	NC	56	IOSTRB-
57	NC	58	NC
59	RESET OUT-	60	NC
61	Ground	62	Ground
63	NC	64	NC
65	NC	66	NC
67	PS-	68	NC
69	NC	70	IS-
71	NC	71	NC
73	NC	74	NC
75	Ground	76	Ground
77	Ground	78	DSP CLKOUT
79	Ground	80	Ground

Table 7: P2, DSP Expansion Connectors

Pin #	Signal Name	Pin #	Signal Name
1	+5 Volts	2	+5 volts
3	A19	4	A18
5	A17	6	A16
7	A15	8	A14
9	A13	10	A12
11	Ground	12	Ground
13	A11	14	A10
15	A9	16	A8
17	A7	18	A6
19	A5	20	A4
21	+5 Volts	22	+5 Volts
23	A3	24	A2
25	A1	26	A0
27	Ground	28	Ground
29	Ground	30	Ground
31	Ground	32	Ground
33	NC	34	NC
35	NC	36	NC
37	NC	38	NC
39	NC	40	NC
41	+3.3 Volts	42	+3.3 Volts
43	NC	44	NC
45	NC	46	NC
47	NC	48	NC
49	NC	50	NC
51	Ground	52	Ground
53	D15	54	D14
55	D13	56	D12
57	D11	58	D10
59	D9	60	D8
61	Ground	62	Ground
63	D7	64	D6
65	D5	66	D4
67	D3	68	D2
69	D1	70	D0
71	Ground	71	Ground
73	MEMRD-	74	MEMWE-
75	MEMOE-	76	RDY
77	MSTRB-	78	DS-
79	Ground	80	Ground

2.6.2 P3, RS-232 Connector

The EVM320VC5471 has an internal UART which provides a an additional serial interface. This device allows users to use this resource for data logging, code debugging and other applications.

This UART is brought out to connector P3 on the EVM320VC5471. Connector P3 is a DB9 female connector. The pin positions for the P3 connector as viewed from the edge of the EVM320VC5471.

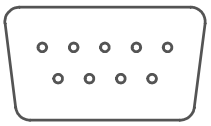

Figure 2-15, P3, DB9 Female Connector

The pin numbers and their corresponding signals are shown in the table below:

Table 8: P3, RS-232 Pinout

Pin #	PC (female)	SD EVM, P3
1	Input	DCD, Output
2	Rx, input	Tx, output
3	Tx, output	Rx, input
4	DTR, output	NC
5	GND	GND
6	NC	NC
7	RTS, output	CTS, input
8	CTS, input	RTS, output
9	NC	NC

2.6.3 P4, LCD Interface Connector

P4, a 2 x 8 double row header, has the signals for an LCD display to be attached to the ARM processor on the EVM320VC5471. The table below identifies the signals on each pin of the connector.

Table 9: P4, LCD Interface Connector

Pin #	Signal Name	Pin #	Signal Name
1	+3.3 Volts	2	+3.3 Volts
3	Reserved	4	Reserved
5	LCD_DATA	6	LCD_A0
7	LCD_RESET	8	LCD_CLK
9	Ground	10	Ground
11	I^2C_DATA	12	Ground
13	I^2C_CLK	14	Ground
15	+3.3 Volts	16	+3.3 Volts

The signals LCD_DATA, LCD_A0, and LCD_CLK implement an 8 bit serial interface which directly interfaces to the LCD display.

The I^2C_DATA and I^2C_CLK signals interface to the three I^2C Analog-to-Digital converters (A/Ds) on the Universal Keypad/Display module. Two of the A/Ds interface to the 2 user potentiometers. The 2 devices and their address on the I^2C bus are shown in the table below.

Table 10: I^2C Device Addressing

Device	I^2C Address
POT1	0x4A
POT2	0x49

2.6.4 P5, Keypad Interface Connector

P5, a 2 x 7 double row header, has the signals for a keyboard to be attached to the ARM processor on the EVM320VC5471. The table below identifies the signals on each pin of the connector.

Table 11: P5, Keypad Interface Connector

Pin #	Signal Name	Pin #	Signal Name
1	+3.3 Volts	2	+3.3 Volts
3	KB_COL0	4	KB_ROW2
5	KB_COL1	6	KB_ROW1
7	KB_COL2	8	KB_ROW0
9	KB_COL3	10	Reserved
11	Reserved	12	Reserved
13	Ground	14	Ground

The table below shows the row-column key mapping for the keypad on the Universal keypad/display unit.

Table 12: Row-Column Key Mapping

Row Signal	KB_COL0	KB_COL1	KB_COL2	KB_COL3
KB_ROW0	SW1	Not Used	SW7	SW4
KB_ROW1	SW5	SW2	Not Used	SW8
KB_ROW2	SW9	SW6	SW3	Not Used

2.6.5 P6, TI JTAG Emulator Connector

The TMS320VC5471 evaluation module is supplied with a 14 pin header interface, P6. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown figure 2-15 below.

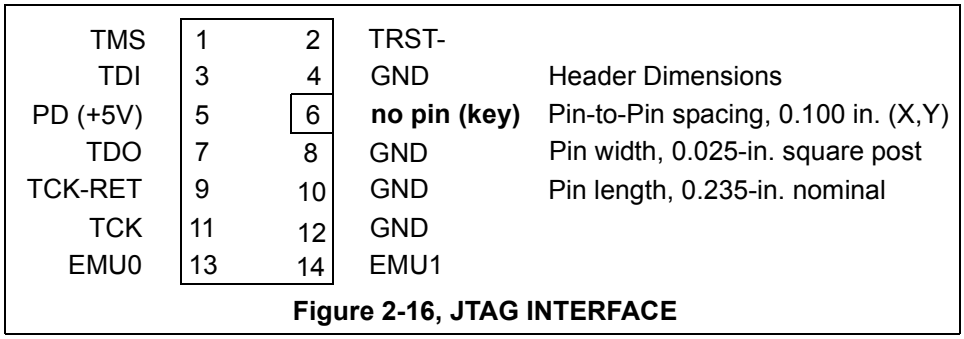

Figure 2-16, JTAG INTERFACE

The table below identifies the signals on each pin of the connector.

Table 13: P6, JTAG Emulator Connector

Pin #	Signal Name	Pin #	Signal Name
1	TMS	2	TRST-
3	TDI	4	GND
5	PD (+5V or +3.3V)	6	**no pin (key)**
7	TDO	8	GND
9	TCK-RET	10	GND
11	TCK	12	GND
13	EMU0 *	14	EMU1 *

* See section on EMU jumpers for changing the number of devices in the scan chain. By jumpering these pins to 0 at reset only the ARM7 CPU will be in the JTAG scan chain. Refer to section x.y

2.6.6 P7, ARM 3rd Party Compatible JTAG Emulation Connector

P7, a 2 x 7 double row header, has the signals for ARM 3rd party compatible emulators. The table below identifies the signals on each pin of the connector.

Table 14: P7, ARM 3rd Party Compatible JTAG Emulator Connector

Pin #	Signal Name	Pin #	Signal Name
1	+3.3 Volt	2	Ground
3	TRST	4	Ground
5	TDI	6	Ground
7	TMS	8	EMU OFF
9	TCK	10	Ground
11	TDO	12	Ground
13	+3.3 Volt	14	Ground

2.6.7 P8, P11, ARM Expansion Bus

The ARM portion of the TMS320VC5471 has two expansion connectors which bring out all of the signals for expansion purposes and custom user logic.

The P8 and P11expansion connectors are 2 x 40 double row surface mount connectors. All odd numbered pins (1,3,5, ...) are on one side and the even numbered pins (2,4,6, ...) are on the other. Pin 1 and Pin 2 are indicated in the silk screen lettering. The signals on these pins are shown in the next table.

Table 15: P8, ARM Expansion Connectors

Pin #	Signal Name	Pin #	Signal Name
1	NC	2	NC
3	Ground	4	Ground
5	NC	6	NC
7	Ground	8	Ground
9	+5 Volts	10	+5 Volts
11	NC	12	NC
13	NC	14	NC
15	NC	16	NC
17	NC	18	NC
19	+3.3 Volts	20	+3.3 Volts
21	NC	22	NC
23	NC	24	NC
25	Ground	26	Ground
27	NC	28	I^2C_CLK
29	NC	30	I^2C_DATA
31	Ground	32	Ground
33	CLKX_SP1	34	NC
35	MCUEN0	36	MCUD0
37	NC	38	NC
39	NC	40	NC
41	NC	42	MCUD1
43	Ground	44	Ground
45	NC	46	NC
47	NC	48	IRQ-
49	NC	50	NC
51	Ground	52	Ground
53	FIQ-	54	NC
55	NC	56	NC
57	NC	58	NC
59	RESET OUT-	60	NC
61	Ground	62	Ground
63	NC	64	NC
65	NC	66	NC
67	NC	68	NC
69	nCS3	70	NC
71	NC	71	NC
73	NC	74	NC
75	Ground	76	Ground
77	Ground	78	ARM MCLK
79	Ground	80	Ground

Table 16: P11, ARM Expansion Connectors

Pin #	Signal Name	Pin #	Signal Name
1	+5 Volts	2	+5 Volts
3	A21	4	A20
5	A19	6	A18
7	A17	8	A16
9	A15	10	A14
11	Ground	12	Ground
13	A13	14	A12
15	A11	16	A10
17	A9	18	A8
19	A7	20	A6
21	+5 Volts	22	+5 Volts
23	A5	24	A4
25	A3	26	A2
27	nBE3	28	nBE2
29	nBE1	30	nBE0
31	Ground	32	Ground
33	D31	34	D30
35	D29	36	D28
37	D27	38	D26
39	D25	40	D24
41	+3.3 Volts	42	+3.3 Volts
43	D23	44	D22
45	D21	46	D20
47	D19	48	D18
49	D17	50	D16
51	Ground	52	Ground
53	D15	54	D14
55	D13	56	D12
57	D11	58	D10
59	D9	60	D8
61	Ground	62	Ground
63	D7	64	D6
65	D5	66	D4
67	D3	68	D2
69	D1	70	D0
71	Ground	71	Ground
73	ARM_READ-	74	ARM_WE-
75	ARM_OE-	76	WAIT
77	ARM_USER *	78	ARM_MEM-
79	Ground	80	Ground

***** ARM_USER is either Interrupt Input or CS3 Output.

2.6.8 P9, MII Connectors

Connectors P9 is a MII connector. This connector allows debug or interfacing between the internal ethernet MAC and the ethernet PHY interface. The layout of these connectors is shown in the drawing below.

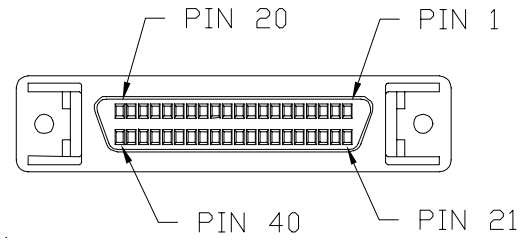

Figure 2-17, Connector P9, Layout

The signals on the pins of this connector, P9 are shown in the following table.

Table 17: P9, MII Connector

Pin #	Signal	Pin #	Signal
1	+3.3/+5 Volts	21	+3.3/+5 Volts
2	MDIO	22	Ground
3	MDCLK	23	Ground
4	RX1D3	24	Ground
5	RX1D2	25	Ground
6	RX1D1	26	Ground
7	RX1D0	27	Ground
8	RXDV0	28	Ground
9	RCLK0	29	Ground
10	RXER0	30	Ground
11	TXER0	31	Ground
12	TCLK0	32	Ground
13	TXEN0	33	Ground
14	TX1D0	34	Ground
15	TX1D1	35	Ground
16	TX1D2	36	Ground
17	TX1D3	37	Ground
18	COL0	38	Ground
19	CRS0	39	Ground
20	+3.3/+5 Volts	40	+3.3/+5 Volts

2.6.9 P12, On Board Parallel Port JTAG Interface

Connector P12 directly interfaces between the bi-directional port on a personal computer and the EVM320VC5471. This connector allows for the on board JTAG logic to operate with debug tools such as Code Composer Studio.

2.7 Logic Analyzer Connectors

The TMS320VC5471 evaluation module has 5 connectors to allow a logic analyzer to be connected to the EVM. These four (2 x 22 pin) connectors are surface mounted to the printed circuit board. Their signals are defined in the following 4 tables.

The signals on connector LA1 are shown in the table below.

Table 18: LA1, Logic Analyzer Connector

Pin #	Signal	Pin #	Signal
1	Reserved	2	Reserved
3	Ground	4	Reserved
5	BCLKX0	6	BCLKX1
7	BDR0	8	DSP D15
9	BFSR0	10	DSP D14
11	BDX0	12	DSP D13
13	BFSX0	14	DSP D12
15	BCLKR1	16	DSP D11
17	BDR1	18	DSP D10
19	BFSR1	20	DSP D9
21	BDX1	22	DSP D8
23	BFSX1	24	DSP D7
25	I^2C CLK	26	DSP D6
27	I^2C DATA	28	DSP D5
29	DSP_RW	30	DSP D4
31	DSP_nCS	32	DSP D3
33	Test Point #2	34	DSP D2
35	Test Point #3	36	DSP D1
37	Test Point #4	38	DSP D0
39	Ground	40	Ground
41	Ground	42	Ground
43	Ground		

The signals on connector LA2 are shown in the table below.

Table 19: LA2, Logic Analyzer Connector

Pin #	Signal	Pin #	Signal
1	Reserved	2	Reserved
3	Ground	4	Reserved
5	Reserved	6	Reserved
7	UART RTS	8	DSP A15
9	UART CTS	10	DSP A14
11	UART RXD	12	DSP A13
13	UART TXD	14	DSP A12
15	UART_DCD	16	DSP A11
17	RX_IRDA	18	DSP A10
19	TX_IRDA	20	DSP A9
21	+3.3 Volts	22	DSP A8
23	Test Point #6	24	DSP A7
25	nRESET	26	DSP A6
27	nRESET_OUT	28	DSP A5
29	AUDIOCLK	30	DSP A4
31	DSP A19	32	DSP A3
33	DSP A18	34	DSP A2
35	DSP A17	36	DSP A1
37	DSP A16	38	DSP A0
39	Ground	40	Ground
41	Ground	42	Ground
43	Ground		

The signals on connector LA3 are shown in the table below.

Table 20: LA3, Logic Analyzer Connector

Pin #	Signal	Pin #	Signal
1	NC	2	NC
3	NC	4	NC
5	SDRAM CLK	6	NC
7	nCS0	8	ARM A15
9	nCS1	10	ARM A14
11	nCS2	12	ARM A13
13	SDRAMnCS	14	ARM A12
15	NOE	16	ARM A11
17	R/W	18	ARM A10
19	SRAM CKE	20	ARM A9
21	Test Point #8	22	ARM A8
23	Test Point #7	24	ARM A7
25	ARM A22	26	ARM A6
27	ARM A21	28	ARM A5
29	ARM A20	30	ARM A4
31	ARM A19	32	ARM A3
33	ARM A18	34	ARM A2
35	ARM A17	36	ARM A1
37	ARM A16	38	ARM A0
39	Ground	40	Ground
41	Ground	42	Ground
43	Ground		

The signals on connector LA4 are shown in the table below.

Table 21: LA4, Logic Analyzer Connector

Pin #	Signal	Pin #	Signal
1	Reserved	2	Reserved
3	Ground	4	Reserved
5	MCLK	6	Reserved
7	ARM D31	8	ARM D15
9	ARM D30	10	ARM D14
11	ARM D29	12	ARM D13
13	ARM D28	14	ARM D12
15	ARM D27	16	ARM D11
17	ARM D26	18	ARM D10
19	ARM D25	20	ARM D9
21	ARM D24	22	ARM D8
23	ARM D23	24	ARM D7
25	ARM D22	26	ARM D6
27	ARM D21	28	ARM D5
29	ARM D20	30	ARM D4
31	ARM D19	32	ARM D3
33	ARM D18	34	ARM D2
35	ARM D17	36	ARM D1
37	ARM D16	38	ARM D0
39	Ground	40	Ground
41	Ground	42	Ground
43	Ground		

The signals on connector LA5 are shown in the table below.

Table 22: LA5, Logic Analyzer Connector

Pin #	Signal	Pin #	Signal
1	No Connect	2	No Connect
3	Ground	4	No Connect
5	RCLK1	6	RCLK0
7	TCLK1	8	TCLK0
9	MDCLK	10	MDIO
11	COL1	12	COL0
13	CRS1	14	CRS0
15	TXEN1	16	TXEN0
17	TXER1	18	TXER0
19	RXDV1	20	RXDV0
21	RXER1	22	RXER0
23	TX1D3	24	TX0D3
25	TX1D2	26	TX0D2
27	TX1D1	28	TX0D1
29	TX1D0	30	TX0D0
31	RX1D3	32	RX0D3
33	RX1D2	34	RX0D2
35	RX1D1	36	RX0D1
37	RX1D0	38	RX0D0
39	Ground	40	Ground
41	Ground	42	Ground
43	Ground		

2.8 Peripheral Connectors

The TMS320VC5471 evaluation module has 9 connectors which allow various peripherals to be attached to the EVM for debug purposes. The connectors are shown in the table below.

Table 23: Peripheral Connectors

Connector #	Peripheral
J1	Audio Line In
J2	Microphone In
J3	Audio Line Out
J4	Headphone Out
J5	Right Amplifier Out
J6	Left Amplifier Out
J7	+5 Volts
J8	Ethernet Interface

The position of the peripheral connectors, test points, switches, and LEDs, on the EVM320VC5471 are shown in the figure below.

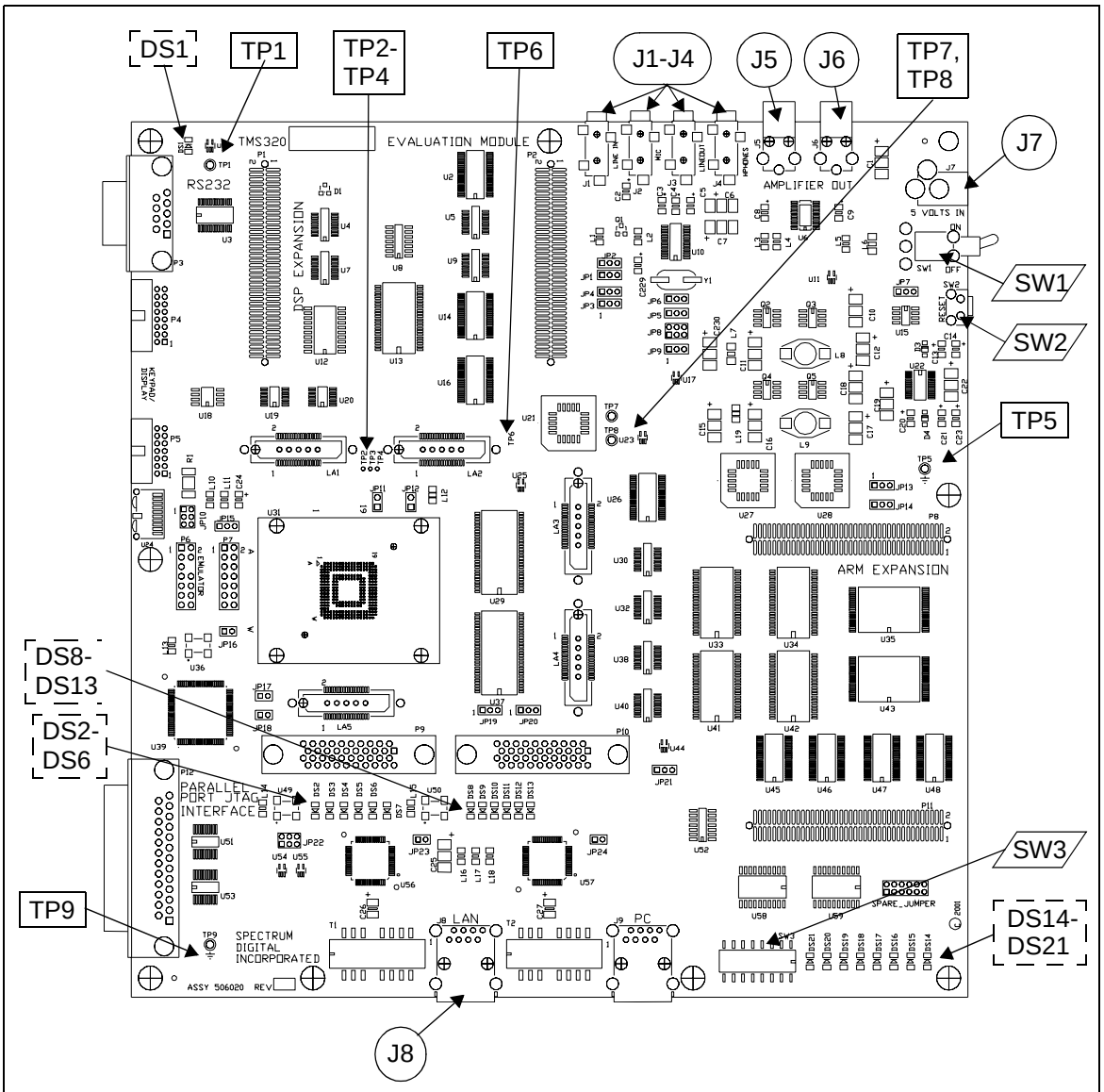

Figure 2-18, EVM320VC5471 Peripheral Connector, Test Point, Switch, and LED Locations

2.8.1 J1, Audio Line In

The audio line in is a stereo input. This input interfaces directly to the TLV320AIC23. The connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

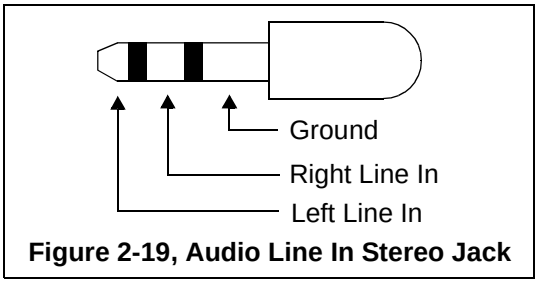

Figure 2-19, Audio Line In Stereo Jack

2.8.2 J2, Microphone Line In

The microphone interfaces directly to the TLV320AIC23. It is a 3.5 mm. stereo jack. Both inputs are connected to the microphone so it is monaural. The signals on the plug are shown in the figure below.

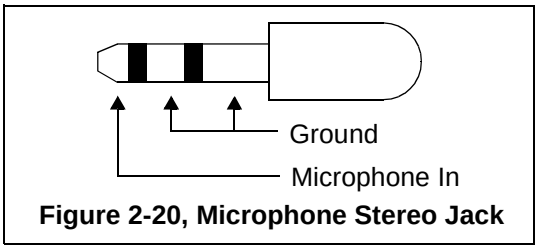

Figure 2-20, Microphone Stereo Jack

2.8.3 J3, Audio Line Out

The audio line out is a stereo output. This output is driven directly by the TLV320AIC23. The connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

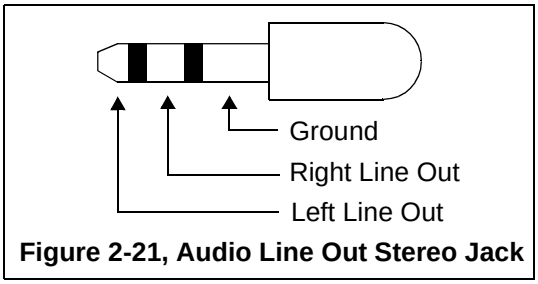

Figure 2-21, Audio Line Out Stereo Jack

2.8.4 J4, Headphone Out

The AIC23 has a low power headphone amplifier. This output is driven directly by the TLV320AIC23. The connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

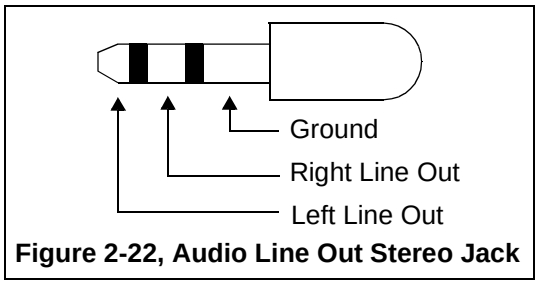

Figure 2-22, Audio Line Out Stereo Jack

2.8.5 J5, J6, Amplifier Out

The TMS320VC5471 EVM is equipped with a medium power single chip amplifier which is driven by the AIC23 line outputs. The amplifier is strapped for 2x amplification and is configured in the BTL mode of operation. J5 is the right channel and J6 is the left channel. The connectors are the standard phono jacks.

2.8.6 J7, +5 Volts

Power (5 volts) is brought onto the TMS320VC5471EVM via the J7 connector. The connector has an outside diameter of 5.5 mm. and an inside diameter of 2 mm. The position of the J7 connector is shown below.

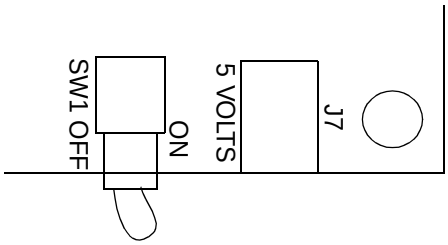

Figure 2-23, Power Connector Location

The diagram of J7, which has the input power is shown below.

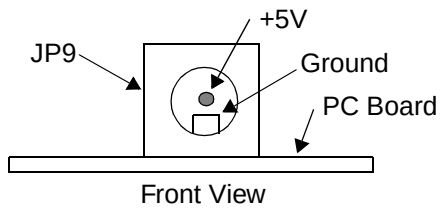

Figure 2-24, TMS320VC5471 EVM Power Connector

2.8.7 J8, Ethernet Interface

Connector J8 is a standard RJ45 connector which directly interfaces to a 10 or 100Mbit ethernet cable. The pin out of the connector is shown below.

Table 24: J8,J9 Ethernet Interface

Pin #	Signal
1	TX+
2	TX-
3	RX+
4	
5	
6	RX-
7	
8	

2.9 Test Points

The EVM320VC5471 has 9 test points to aid in debug. Most of these test points go to the logic analyzer connectors to allow the user to view the signals at a test point. The signals on each test point are shown in the table below.

Table 25: Test Points

Test Point #	Logic Analyzer Connection
TP1	DSP XF Bit
TP2	LA1 Pin 33
TP3	LA1 Pin 35
TP4	LA1 Pin 37
TP5	Ground
TP6	LA2 Pin 23
TP7	LA3 Pin 23
TP8	LA3 Pin 21
TP9	Ground

2.10 Switches

The EVM320VC5471 has 3 switches. Each of the functions are described in the table below..

Table 26: Switches

Switch #	Function
SW1	Power On/Off
SW2	Reset
SW3	8 Position User DIP Switch

2.10.1 SW3, 8 Position User DIP Switch

The TMS320VC547x EVM has an 8 position DIP switch, SW3, mapped into ARM memory location 0x01000000. This switch is mapped to data lines D0-D7 as shown in the table below.

Table 27: SW3, 8 Position DIP Switch

SW3 Switch Position	Data Line
1	D0
2	D1
3	D2
4	D3
5	D4
6	D5
7	D6
8	D7

2.11 LEDs

The EVM320VC5471 has 14 red Light Emitting Diodes (LEDs). The signal tied to each led is shown in the table below.

Table 28: LED Signals

LED #	Signal Name
DS1	DSP XF
DS2	PHY0 LINK
DS3	PHY0 FULLST0
DS4	PHY0 COL
DS5	PHY0 TX
DS6	PHY0 RX
DS7	PHY0 SPEED

Table 29: LED Signals

LED #	Signal Name
DS14	LATCH D0
DS15	LATCH D1
DS16	LATCH D2
DS17	LATCH D3
DS18	LATCH D4
DS19	LATCH D5
DS20	LATCH D6
DS21	LATCH D7

The latch is located in the ARM memory space at location 0x01000000. Note that nCS3 must be programmed first to access this location.

2.12 Jumpers

The TMS320VC5471 evaluation module has 24 jumpers. These jumpers allow the various functions on the EVM to be configured. The function of each jumper is shown in the table below.

Table 30: Jumpers Signals

Jumper #	Size	Function
JP1	1 x 2	AIC23 Mode Select
JP2	1 x 2	AIC23 Chip Select
JP3	1 x 2	AIC23 Left/Right Sync Out Select
JP4	1 x 3	AIC23 Left/Right Sync In Select
JP5	1 x 3	AIC23 Clock Out Select
JP6	1 x 3	AIC23 Clock In Select
JP7	1 x 3	WDOG Select
JP8	3 x 2	AIC23 Clock In Configuration
JP9	1 x 3	Expansion AIC23 Clock Select
JP10	3 x 2	IR Configuration
JP11	1 x 2	CPU +3.3 Volt Power
JP12	1 x 2	CPU +1.8 Volt Power
JP13	1 x 3	User Mode Select
JP14	1 x 3	FLASH Write Protect
JP15	1 x 3	TRST Pull Up/Pull Down Select
JP16	1 x 3	EMUOFF 1 Select
JP17	1 x 2	EMU0 Select
JP18	1 x 2	EMU1 Select
JP19	1 x 3	Endian Select
JP20	1 x 3	ROM Size Select
JP21	3 x 2	MII Power Select
JP22	1 x 3	ARM Oscillator Select
JP23	1 x 3	Phy I Address Select

Each jumper on the EVM320VC5471 is a 1x3 or 1x2 jumper. Each 1x3 jumper must have the selection 1-2 or 2-3. The #2 pin is the center pin. The #1 pin has a square solder pad and can be seen from the solder side of the printed circuit board. This pin is usually marked with a '1' on the boards silk screen. A top view of both types of jumpers is shown below:

Figure 2-25, 1x2 Jumper Layout

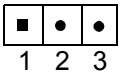

Figure 2-26, 1x3 Jumper Layout

WARNING!
Unless noted otherwise, all 1x3 jumpers must be installed in either the 1-2 or 2-3 position

The position of each jumper on the EVM320VC5471 is shown in the figure below.

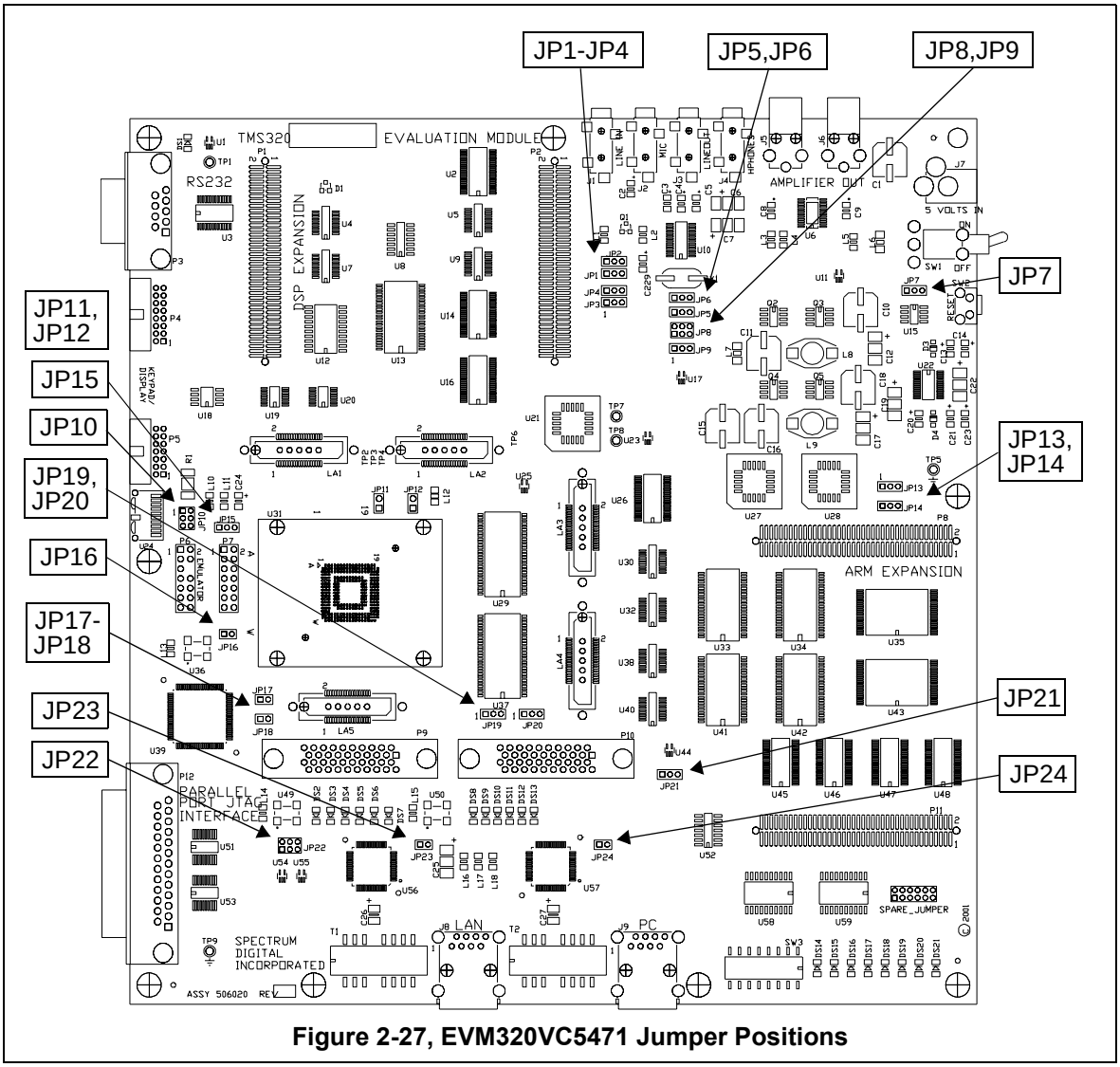

Figure 2-27, EVM320VC5471 Jumper Positions

2.12.1 JP1, AIC23 Mode Select

Jumper JP1 is used to select whether the AIC23 is in SPI mode or I^2C mode. When the jumper is installed between pins 1 and 2 the SPI mode is selected. The 2-3 selection will select the I^2C mode. The default configuration is the SPI mode. The table below shows the positions and their functions.

Table 31: JP1, AIC23 Mode Select

Position	Function
1-2	SPI Mode
2-3	I^2C Mode

2.12.2 JP2, AIC23 Chip Select

Jumper JP2 is used to determine if the AIC23 CS pin is connected to FSX0 for SPI mode or to Ground for the I^2C mode. When the jumper is installed between pins 1 and 2, the FSX0 is connected to the CS pin for the SPI mode. The 2-3 selection will connect the CS pin to Ground for the I^2C mode. The table below shows the positions and their functions.

Table 32: JP2, AIC23 Chip Select

Position	Function
1-2	Connect CS to FSX0 for SPI mode
2-3	Connect CS to Ground for I^2C mode

2.12.3 JP3, AIC23 Left/Right Sync Out Select

Jumper JP3 is used to determine if the data port sync output is connected to McBSP1 FSR1 or FSX1. This jumper is used when the AIC23 is in the master mode. When the jumper is installed between pins 1 and 2, data port sync output is connected to FSR1 on McBSP1. In the 2-3 position the data sync port output is connected to FSX1 on McBSP1. The table below shows the positions and their functions.

Table 33: JP3, AIC23 Left/Right Sync Out Select

Position	Function
1-2	Data port sync output connected to FSR1 on McBSP1
2-3	Data port sync output connected to FSX1 on McBSP1

2.12.4 JP4, AIC23 Left/Right Sync In Select

Jumper JP4 is used to determine if AIC23 data port sync input is connected to McBSP1 FSR1 or FSX1. This jumper is used when the AIC23 is in the slave mode. When the jumper is installed between pins 1 and 2, data port sync input is connected to FSX1 on McBSP1. In the 2-3 position the data sync port input is connected to FSR1 on McBSP1. The table below shows the positions and their functions.

Table 34: JP4, AIC23 Left/Right Sync In Select

Position	Function
1-2	Data port sync input connected to FSX1 on McBSP1
2-3	Data port sync input connected to FSR1 on McBSP1

2.12.5 JP5, AIC23 CLKOUT Select

The AIC23 CLKOUT signal can be used as an input to the VC5471 DSP. There are multiple sources for this output. When the 1-2 position on jumper JP5 is used the AIC23 CLKOUT is driven from AIC23 CLKIN JP8 output. When position 2-3 is selected the AIC23 CLKOUT signal is driven from the AIC23. The table below shows the positions and their functions.

Table 35: JP5, AIC23 Clock Out Select

Position	Function
1-2	AIC23 CLKOUT driven from AIC23 CLKIN JP8 output
2-3	AIC23 CLKOUT driven from AIC23

2.12.6 JP6, AIC23 Clock In Select

Jumper JP6 determines the input source clock for the AIC23. When position 1-2 is selected the output of JP8 drives the Codec input clock. If position 2-3 is used the onboard crystal is selected as the source. The table below shows the positions and their functions.

Table 36: JP6, AIC23 Clock In Select

Position	Function
1-2	JP8 output drives AIC23 clock
2-3	Onboard 12 Mhz crystal drives AIC23 clock

2.12.7 JP7, WDOG Select

Jumper JP7 is used to select if the watchdog monitor in chip U15 is driven by hardware or software. When position 1-2 is selected the clock drives WDOG (WDOG disabled). If position 2-3 is selected software GPIO4 drives the WDOG chip. If neither position is selected the WDOG is disabled. The table below shows the positions and their functions.

Table 37: JP7, WDOG Select

Position	Function
1-2	Clock drives WDOG (WDOG disabled
2-3	GPIO4 drives WDOG chip(software)
None	WDOG disabled

2.12.8 JP8, AIC23 Clock In Configuration

Jumper JP8 is used to select one of three sources for the AIC23 clock. When position 1-2 is used the AIC23 clock is sourced from P1-11. The 3-4 position allows the VC5471 AUDIOCLK GPIO8 to be the source. The 5-6 selection uses CPU CLK JP22 output as the source. The table below shows the positions and their functions.

Table 38: JP8, AIC23 Clock In Configuration

Position	Function
1-2	P1-11 provides AIC23 clock
3-4	VC5471 AUDIOCLK GPIO8 provides AIC23 clock
5-6	CPU CLK JP22 output provides AIC23 clock

2.12.9 JP9, Expansion AIC23 Clock Select

Jumper JP9 is used to select the AIC23 clock source from the expansion connector. When position 1-2 is selected P1-11 drives the expansion AIC23 CLKOUT. If position 2-3 is selected P1-11 is connected to the AIC23 CLKOUT. The table below shows the positions and their functions.

Table 39: JP9, Expansion AIC23 Clock Select

Position	Direction	Function
1-2	Input	P1-11 drives expansion AIC23 CLKOUT
2-3	Output	P1-11 is connected to AIC23 CLKOUT

2.12.10 JP10, IR Configuration

The IR interface has 3 options which are controlled by jumper JP10. The options are shown in the table below.

Table 40: JP10, IR Configuration

Position	Option	Function
1-2	Open	MDO pin high
1-2	Installed	MDO pin low
3-4	Open	MDI pin high
3-4	Installed	MDI pin low
5-6	Open	FIR_SEL pin high
5-6	Installed	FIT_SEL pin low

2.12.11 JP11, 3.3 Volt Core Power

Jumper JP11 is used to allow the measuring of the 3.3 volt power supply current to the TMS320VC5471. The table below shows the positions and their functions.

Table 41: JP11, 3.3 Volt Core Power

Position	Function
1-2	Normal Operation, 3.3 volts

2.12.12 JP12, 1.8 Volt Core Power

Jumper JP12 is used to allow the measuring of the 1.8 volt power supply current to the TMS320VC5471. The table below shows the positions and their functions.

Table 42: JP12, 1.8 Volt Core Power

Position	Function
1-2	Normal Operation, 1.8 volts

2.12.13 JP13, User Mode Select

Jumper JP13 is used to select if the expansion connector P11, pin 77 is used as CS output or interrupt input. When position 1-2 is selected P11-77 is used as CS output. If position 2-3 is selected P11-77 is used as an interrupt input. The table below shows the positions and their functions.

Table 43: JP13, User Mode Select

Position	Function
1-2	P11-77 is used as CS output
2-3	P11-77 is used as an interrupt input

2.12.14 JP14, FLASH Write Protect

Jumper JP14 is used to disable the writing to FLASH memory. When position 1-2 is selected the FLASH Write Protect signal is disabled allowing the FLASH to be programmed. If position 2-3 is selected FLASH Write Protect is enabled so the contents cannot be changed. The table below shows the positions and their functions.

Table 44: JP14, FLASH Write Protect

Position	Function
1-2	FLASH Write Protect Disabled, Unlock lockable FLASH parameter blocks
2-3	FLASH Write Protect Enabled, Lock lockable FLASH parameter blocks

2.12.15 JP15, JTAG TRST Pull Up/Down Select

Jumper JP15 gives external emulators the ability to pull up or pull down the TRST line. This is used to allow the use of open collector type emulators. When position 1-2 is selected the TRST line is pulled up. Selecting the 2-3 position will pull the TRST line down. The table below shows the positions and their functions.

Table 45: JP15, JTAG TRST Pull Up/Down Select

Position	Function
1-2	TRST pulled up
2-3	TRST pulled down

2.12.16 JP16, EMUOFF1 Select

Jumper JP16 is used to force the scan gate array into slave mode so external emulators can supply the emulator clock. This is typical of non-TI type ARM emulators. If the jumper is installed the scan gate array is forced into the slave mode. With no jumper installed the scan gate array is forced into the master mode. The table below shows the positions and their functions.

Table 46: JP16, EMUOFF1 Select

Position	Function
Open	Slave Mode
Installed	Master Mode

2.12.17 JP17,JP18, EMU0/EMU1 Select

These two jumpers allow the user to configure the scan chain at reset. The table below shows the positions and their functions.

Table 47: JP17, EMU0/EMU1 Select

JP18	JP17	Scan Chain
Installed	Installed	ARM Only
Installed	Open	C54xx Only
Open	Installed	Reserved
Open	Open	Normal Operation (ARM and C54xx)

2.12.18 JP19, Big/Little Endian Select

Jumper JP19 is used to select endianess mode of the ARM processor. When position 1-2 is selected the ARM processor will operate in the big endian mode. If position 2-3 is selected the ARM processor will operate in the little endian mode. The table below shows the positions and their functions.

Table 48: JP19, Big/Little Endian Select

Position	Function
1-2	ARM in big endian mode
2-3	ARM in little endian mode

2.12.19 JP20, ROM Size Select

Jumper JP20 is used to determine if the ROM size is 16 or 32 bits. When position 1-2 is selected the ROM size is 32 bits. If position 2-3 is selected the ROM size is 16 bits. The TMS320VC5471 EVM only supports 32 bit ROM sizes. The table below shows the positions for this jumper and their functions.

Table 49: JP20, ROM Size Select

Position	Function
1-2	32 bit ROM size
2-3	16 bit ROM size

2.12.20 JP21, MII Power Select

Jumper JP21 is used to select if +3.3 volts or +5 volts is present on the MII connectors power pins. When position 1-2 is selected +5 volts is present on the MII power pins. If position 2-3 is used +3.3 volts is present on the MII power pins. The table below shows the positions and their functions.

Table 50: JP21, MII Power Select

Position	Function
1-2	+5 Volts present on MII connector power pins
2-3	+3.3 Volts present on MII connector power pins

2.12.21 JP22, ARM Oscillator Select

Jumper JP22 is used to select an input clock source for the VC547x. There are 3 options for this input. The table below shows these options.

Table 51: JP22, ARM Oscillator Select

Position	Function
1-2	25 Mhz Clock
2-4	AIC23 CLKOUT Output
3-6	U50 User Oscillator

2.12.22 JP23, PHY I Address Select

Jumper JP23 is used to select the address of the PHY I. When the jumper is installed the PHY I can be addressed at location 00 binary. If the jumper is removed the PHY I can be addresses at location 10 binary. The table below shows the positions and their functions.

Table 52: JP23, PHY I Address Select

Position	Function
Open	10 Binary
Installed	00 Binary

2.13 Resets

There are multiple resets for the TMS320VC5471 evaluation module. The first reset is the power on reset. This circuit waits until power is within the specified range before releasing the power on reset pin to the TMS320VC5471.

External sources such as push button (SW1), and parallel port JTAG interface also affect reset.

[redacted]

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