

# ***TMS320C54XX***

## ***Evaluation Module***

***Technical  
Reference***

**TMS320C54XX  
Evaluation Module  
Technical Reference**

**503482-0001 Rev. H  
August 2000**

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## About This Manual

This document describes the board level operations of the TMS320C54XX evaluation module (EVM). The EVM is based on the Texas Instruments TMS320C54XX Digital Signal Processor.

The TMS320C54XX EVM is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320C54XX DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

## Notational Conventions

This document uses the following conventions.

The TMS320C54XX will sometimes be referred to as the C54XX.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

*equations*

*!rd = !strobe&rw;*

## Information About Cautions

This book may contain cautions.

***This is an example of a caution statement.***

A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

## Related Documents

Texas Instruments TMS320C54X Users Guide

Texas Instruments TMS320C54X Fixed Point Assembly Language Users Guide

Texas Instruments TMS320C54X Fixed Point C Language Users Guide

Texas Instruments TMS320C54X Fixed Point C Source Debugger Users Guide

# Chapter 1

## Introduction to the TMS320C54XX Evaluation Module

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Chapter One provides a description of the TMS320C54XX Evaluation Module along with the key features and a block diagram of the circuit board.

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## **1.0 Overview of the TMS320C54XX EVM**

The TMS320C54XX evaluation module(EVM) is a stand-alone card. It allows evaluators to examine certain characteristics of the C54XX digital signal processor (DSP) to determine if it meets their application requirements. Furthermore, the module is an excellent platform to develop and run software on the C54XX family of processors.

The C54XX EVM is shipped with a member of the C54xx family. The EVM allows full speed verification of C54XX code. With 32K words of on-chip memory, 256K words of onboard memory, Flash ROM, onboard UART, and a TLC320AD50 Sigma Delta codec, the board can solve a variety of problems as shipped. Five expansion connectors are provided for any necessary evaluation circuitry not provided on the as shipped configuration.

To simplify code development and shorten debugging time, a number of user interfaces are provided. Debuggers providing assembly language and 'C' high level language debug are available with JTAG emulators.

### **1.1 Key Features of the TMS320C54XX EVM**

The C54XX EVM has the following features:

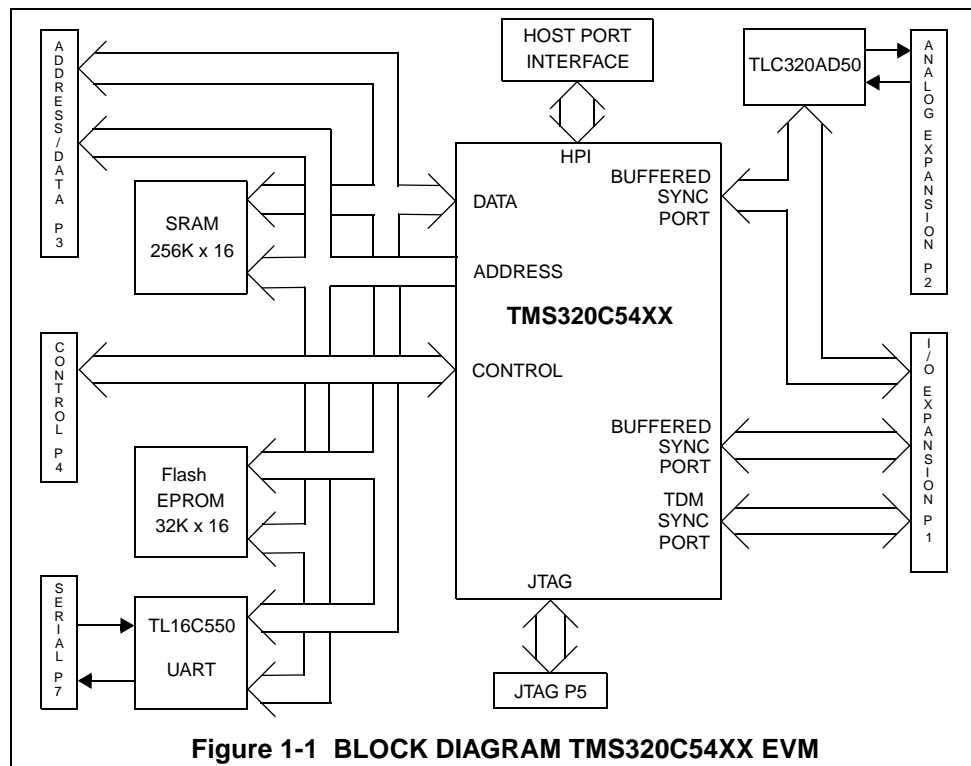
- LC548 operating at 66 MHz with 256K words of one (1) wait state memory
- LC549 operating at 80 MHz with 256K words of one (1) wait state memory
- VC549/VC5409 operating at 100 MHz with 256K words of two (2) wait state memory
- VC5410 operating at 100 MHz with 256K words of one-two (1-2) wait state memory
- VC5416 operating at 100-150 MHz with 256 words of 2 wait state memory
- VC5402 operating at 80-100 MHz with 256 words of 2 wait state memory
- TLC320AD50 Sigma Delta Codec with RCA Jack input and output
- On board UART
- 32K Words of onboard Flash ROM
- 5 Expansion Connectors (data, address, I/O, control, and Host Port Interface)
- On board IEEE 1149.1 JTAG Connection for Optional Emulation
- 5-Volt Only Operation



## 1.2 Functional Overview of the TMS320C54XX EVM

Figure 1-1 shows a block diagram of the basic configuration for the C54XX EVM. The major interfaces of the EVM include the target RAM and ROM interface, target UART and sigma delta codec, and expansion interface.

The C54XX interfaces to 256K Words of onboard static memory. An external I/O interface supports 65,000 parallel I/O ports and optional high speed synchronous serial port. A Flash Boot ROM is mapped into the data and I/O memory space. RCA jacks provide input and outputs to and from the AD50 sigma delta codec.





# Chapter 2

## Operation of the TMS320C54XX Evaluation Module

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This chapter describes the operation of the TMS320C54XX Evaluation Module, the key interfaces and an outline of the circuit board.

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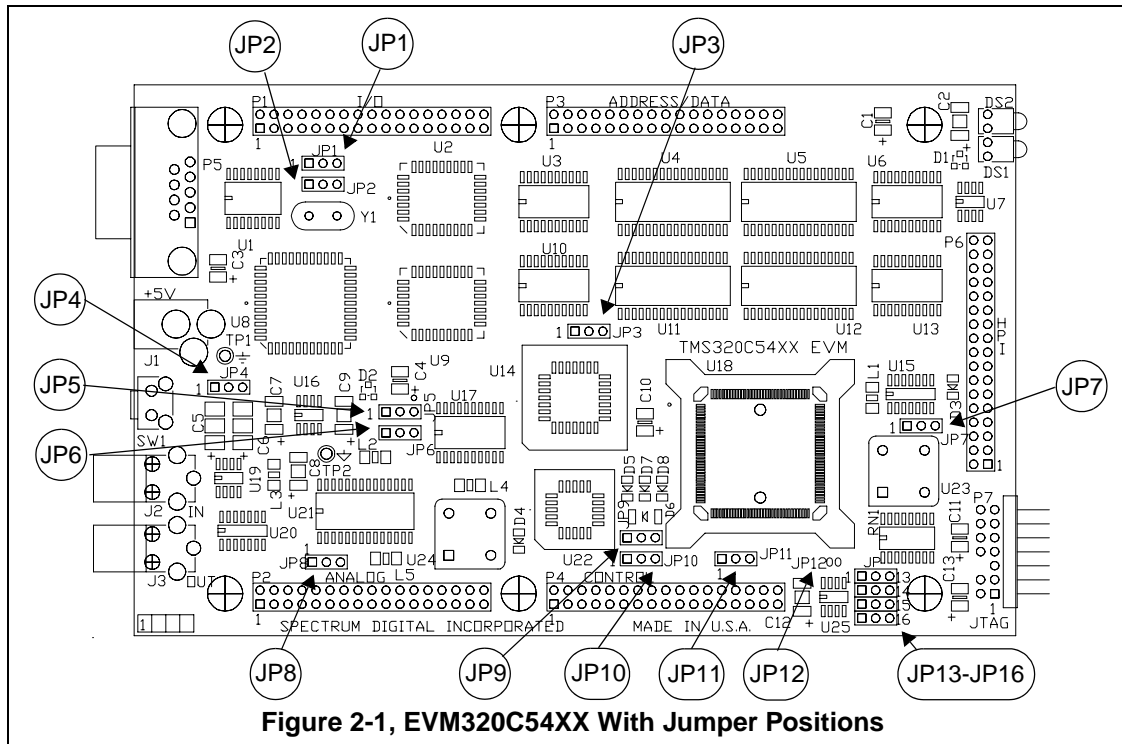
## 2.0 The TMS320C54XX EVM Operation

This chapter describes the C54XX Evaluation module, key components, and how they operate. It also provides information on the EVM's various interfaces. The C54XX EVM consists of five major blocks of logic.

- C54XX external memory
- Analog Interface
- On board Serial I/O interface
- Expansion interface
- JTAG Interface

### 2.1 The TMS320C54XX EVM Board

The C54XX EVM is a 3U sized board which is powered by an external 5 Volt only power supply. Figure 2-1 shows the layout of the C54XX EVM.



### **2.1.1 Power Connector**

The C54XX is powered by a 5 Volt only power supply which is available with the module. The board requires 1 amp. The power is supplied via 2 millimeter jack J1. If expansion boards are connected to the module a higher amperage power supply may be necessary. The board also has a 3.3 and 2.5 volt regulator to provide power to the lower voltage components.

### **2.2 TMS320C54XX Memory Interface**

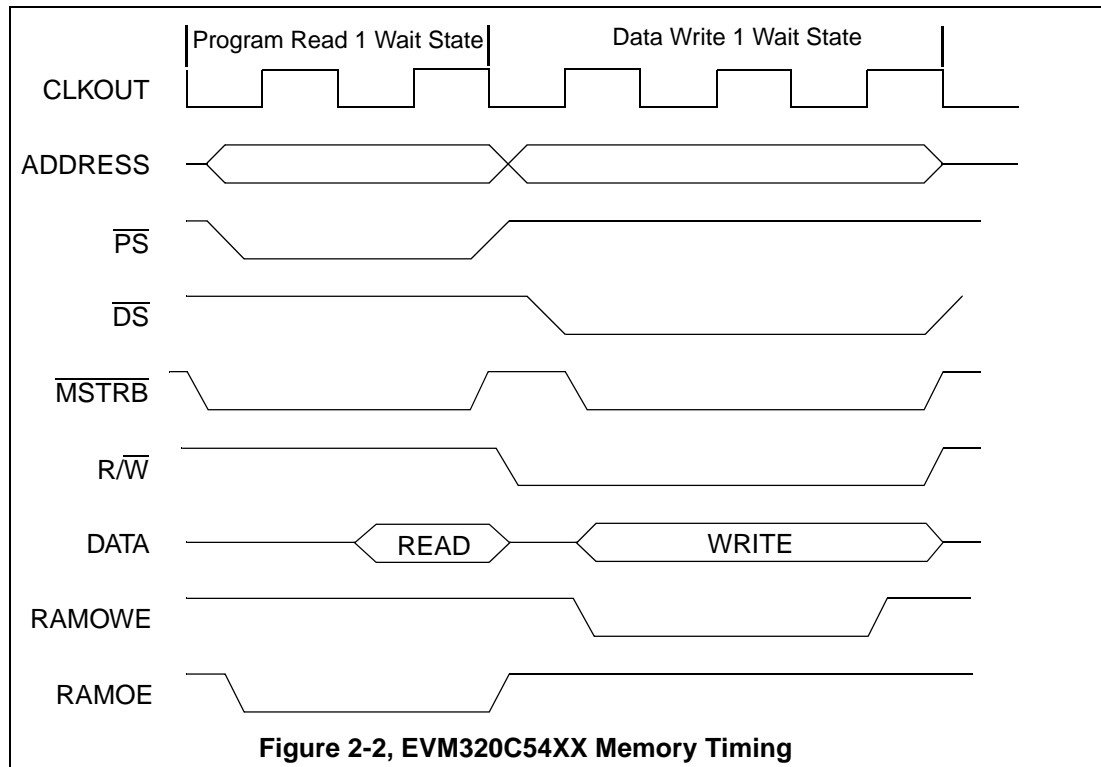
The EVM includes 192k Words of on board program ram memory and 64k words of on board data ram memory, providing a total of 256k words of off chip static ram. The board also features two 32k flash ROMs for boot loading.

It is important to remember that internal memory has a higher precedence than the external memory. For more information on the memory in the device populated in your EVM card please refer to Texas Instruments TMS320C54XX Users Guide. Furthermore, it is important to take into account that external memory is affected by wait-states. Wait state generation for off-chip memory space (data, program, or I/O) is done with the Software Wait State Generation Register(SWWSR). To obtain one waitstate off-chip memory bits in the SWWSR must be appropriately programmed. The board powers up with 7 wait-states. The EVM board does not generate wait states via the ready signal for external program and data memory accesses, only I/O accesses use the ready signal.

External memory decode is done via U14 a GAL20V8. The generic array device selects the RAM, FLASH ROM, or on board peripherals. The equations for the GAL are included in Appendix A. The figure below shows a one wait state program space memory read followed by a data space memory write.

The external Flash ROM is mapped into the upper 32K words of data and I/O space for boot loading. Note that this memory requires multiple wait states. The main purpose of this memory is to allow for the boot loading of programs via the C54XX's internal boot loader.

The figure below shows the memory timing for the EVM320C54XX Evaluation Module.



### 2.2.1 Program Memory

There are two configurations for program memory. The selection of these configurations is done by the 54X's OVLY bit. When in OVLY mode, addresses 0x0000 - 0x8000 are internal for every page. In this mode, there are five (5) 32K word pages of external program RAM and one (1) 32K word page of internal RAM. When in linear mode program memory is mapped to external RAM. Shown below are the two program memory configurations. The following three figures are for the C548 and C549 processors, C5410 processor, and the C5402 respectively.

Linear Mode, OVLY = 0		Overlay Mode, OVLY = 1			
Hex		Hex			
0x000000	External RAM	0x000000	Reserved		
0x00007F		0x00007F			
0x000080	External RAM	0x000080	DARAM		
0x001FFF		0x001FFF			
0x002000	External RAM	0x002000	SARAM		
0x007FFF		0x007FFF			
0x008000	External RAM	0x008000	Page 0		
0x00FF7F		0x00FF7F	External RAM		
0x00FF80	Interrupts External RAM	0x00FF80	Page 0 Interrupts		
0x00FFFF		0x00FFFF	External RAM		
0x010000	External RAM	0x018000	Page 1		
0x027FFF		0x01FFFF	External RAM		
0x028000	RAM Images	0x028000	Page 2		
0x05FFFF		0x02FFFF	External RAM		
0x060000	External	0x038000	Page 3		
0x37FFFF		0x03FFFF	External RAM		
* Jumper JP13 in 2-3 position		0x048000	Page 4		
		0x04FFFF	External RAM		
		0x058000	RAM Images		
		0x05FFFF			
		0x060000	External Page		
		0x37FFFF			
		† Jumper JP13 in 1-2 position			
		<b>Figure 2-3A, EVM320C548/549/5409 Program Space</b>			



Linear Mode, OVLY = 0		Overlay Mode, OVLY = 1	
Hex		Hex	
0x000000	External RAM	0x000000	Reserved
0x00007F		0x00007F	
0x000080	External RAM	0x000080	Internal DARAM
0x001FFF		0x001FFF	
0x002000	External RAM	0x002000	Internal SARAM
0x007FFF		0x007FFF	
0x008000	External RAM	0x008000	Page 0
0x00FF7F		0x00FF7F	
0x00FF80	Interrupts External RAM	0x00FF80	Page 0 Interrupts External RAM
0x00FFFF		0x00FFFF	
0x010000	External RAM	0x018000	Page 1
0x027FFF		0x01FFFF	
0x028000	RAM Images	0x028000	Page 2
0x05FFFF		0x02FFFF	
0x060000	External	0x038000	Page 3
0x37FFFF		0x03FFFF	
		0x048000	Page 4
		0x04FFFF	
		0x058000	RAM Images
		0x05FFFF	
		0x060000	External
		0x37FFFF	

\* Jumper JP13 in 2-3 position

Note: JP13 maps A15 or A15 RAM's A17 is default.

† Jumper JP13 in 1-2 position

**Figure 2-3B, EVM320VC5410 Program Space**

Note that in Microcontroller Mode,  $\overline{MP/MC}$  pin=0, the on chip boot loader resides in high page 0 address space. These addresses are 0xC000 to 0xFFFF on the C549 and C5410, from 0xF000 to 0xFFFF on the C5402 processor, and from 0xF800 to 0xFFFF on the C548.

Linear Mode, OVLY = 0		Overlay Mode, OVLY = 1	
Hex		Hex	
0x000000	External RAM	0x000000	Reserved
0x00007F		0x00007F	
0x000080	External RAM	0x000080	Internal DARAM
0x001FFF		0x003FFF	
0x002000	External RAM	0x004000	External
0x007FFF		0x007FFF	
0x008000	External RAM	0x008000	Page 0
0x00FF7F		0x00FF7F	External RAM
0x00FF80	Interrupts External RAM	0x00FF80	Page 0 Interrupts External RAM
0x00FFFF		0x00FFFF	
0x010000	External RAM	0x018000	Page 1
0x027FFF		0x01FFFF	Internal SARAM2
0x028000	RAM Images	0x028000	Page 2
0x05FFFF		0x02FFFF	External RAM
0x060000	External	0x038000	Page 3
0x37FFFF		0x03FFFF	External RAM
		0x048000	Page 4
		0x04FFFF	External RAM
		0x058000	RAM Images
		0x05FFFF	
		0x060000	External
		0x37FFFF	

\* Jumper JP13 in 2-3 position

Note: JP13 maps A15 or A15 RAM's A17 is default.

† Jumper JP13 in 1-2 position

**Figure 2-3C, EVM320VC5402 Program Space**

In Microcontroller Mode,  $\overline{MP}/\overline{MC}$  pin=0, the on chip boot loader resides in high page 0 address space. These addresses are 0xC000 to 0xFFFF on the C549 and C5410, from 0xF000 to 0xFFFF on the C5402 processor, and from 0xF800 to 0xFFFF on the C548.

Linear Mode, OVLY = 0		Overlay Mode, OVLY = 1	
Hex		Hex	
0x000000	External	0x000000	Reserved
0x00007F	Reserved	0x00007F	
0x000080	External	0x000080	Internal
0x007FFF		0x007FFF	DARAM
0x008000	Page 0	0x008000	Page 0
0x00FF7F	External RAM	0x00BFFF	* External RAM †† Image of page 4
0x00FF80	Page 0	0x00C000	Page 0
0x00FFFF	Interrupts External RAM	0x00FFFF	* External MP/MC=1 Internal ROM MP/MC=0
0x010000	Page 1	0x018000	Page 1
0x017FFF	External	0x01FFFF	* External MP/MC=1 Internal DARAM MP/MC=0
0x018000	Page 1	0x028000	Page 2
0x01FFFF	External MP/MC=1 Internal MP/MC=0	0x02FFFF	* External MP/MC=1 Internal DARAM MP/MC=0
0x020000	Page 2	0x038000	Page 3
0x027FFF	External	0x03FFFF	* External MP/MC=1 Internal DARAM MP/MC=0
0x028000	Page 2	0x048000	Page 4
0x02FFFF	External MP/MC=1 Internal SRAM MP/MC=0	0x04FFFF	Image External RAM
0x030000	Page 3	0x058000	Page 5
0x037FFF	Image	0x05FFFF	Image External RAM
0x038000	Page 3	0x068000	Page 6
0x03FFFF	Internal MP/MC=1 External RAM MP/MC=0	0x06FFFF	Image External RAM
0x048000	Page 4	0x078000	Page 7
0x04FFFF	Image External RAM	0x07FFFF	Image External RAM
0x058000	Page 5	0x080000	External
0x05FFFF	Image External RAM	0x3FFFFF	
0x068000	Page 6		
0x06FFFF	Image External RAM		
0x078000	Page 7		
0x07FFFF	Image External RAM		
0x080000	External		
0x3FFFFF			

† Jumper JP13 in 1-2 position

If MP/MC=1, pages 4-7 are images of pages 0-3

†† Page 4 is mirror image of page 0 when MP/MC=0

**Figure 2-3D, EVM320VC5416 Program Space**

### 2.2.2 Data Memory

The data memory configuration is shown below. The external data memory is mapped from 0x8000 to 0xFFFF for the C548 and C549 processors, and either internal or external for the C5410.

Flash memory is also mapped in data space from 0x8000 to 0xFFFF when the UART OUT3 (DTR bit in MCR Register) bit is set to 0. This allows for boot loading. The memory space can be recovered for RAM memory by setting the OUT3 bit to 1.

**Note:** The logic state of OUT3 is inverted of bit state in the UART register.

Figure 2-4A shows the data space memory map for the C548 and C549 processors.

Hex	
0x0000 0x005F	Memory-Mapped Registers
0x0060 0x007F	Scratch Pad RAM
0x0080 0x1FFF	8K Dual Access RAM (DARAM)
0x2000 0x7FFF	Single Access RAM (SARAM)
0x8000 0xFFFF	External RAM (OUT3=1) FLASH ROM (OUT3=0)

**Figure 2-4A, EVM320C548/C549 Data Space**

Figure 2-4B shows the data space memory map for the VC5410 and VC5416 DSP.

Hex	
0x0000 0x005F	Memory-Mapped Registers
0x0060 0x007F	Scratch Pad RAM
0x0080 0x1FFF	8K Dual Access RAM (DARAM)
0x2000 0x7FFF	Single Access RAM (SARAM)
0x8000 0xFFFF	External RAM (OUT3=1, DROM=0) FLASH ROM (OUT3=0, DROM=0) Internal SARAM2 (OUT3=X, DROM=1)

**Figure 2-4B, EVM320VC5410, VC5416 Data Space**

Figure 2-4C shows the data space memory map for the VC5402 DSP.

Hex	
0x0000 0x005F	Memory-Mapped Registers
0x0060 0x007F	Scratch Pad RAM
0x0080 0x3FFF	8K Dual Access RAM (DARAM)
0x4000 0x7FFF	External RAM
0x8000 0xFFFF	External RAM (OUT3=1, DROM=0) FLASH ROM (OUT3=0, DROM=0) Internal SARAM2 (OUT3=X, DROM=1)

**Figure 2-4C, EVM320VC5402 Data Space**

### 2.2.3 I/O Space

The I/O map for the TMS320C54XX EVM is shown below:

Hex	
0x0000	Off-Chip UART
0x0FFF	
0x1000	Expansion
0x7FFF	
0x8000	FLASH ROM if OUT3 = 0
0xFFFF	Expansion if OUT3 = 1

**Figure 2-5, EVM320C54XX I/O Space**

### 2.3 Onboard UART

The TMS320C54XX EVM has a TL16C550 UART mapped into the I/O space of the C54XX at locations 0x0000 - 0x0008. The UART allows users to use this resource for data logging, code debugging or other application features. Appendix C contains the programming information for the TL16C550 device.

### 2.4 Oscillator Selection

The TMS320C54XX EVM is equipped with a 10 Megahertz oscillator. When the processor resets the PLL Clock Module defaults to 10 Mhz CLKOUT in divide mode. The PLL can then be programmed to obtain a variety of clock frequencies. If the PLL frequency is required to change after the programming the part must be returned to the divide mode before the programming of the new PLL frequency. The user should refer to the "PLL Clock Module" section in the TMS320C54XX User's guide for valid clock configurations.

## 2.5 Analog Interface

The C54XX synchronous serial port can be used to access either the onboard TLC320AD50 sigma delta codec or be jumpered to the expansion connector. Jumper JP5 (1-2) is used to interconnect the serial port to the AD50. If the serial port is to be used from the expansion connector the plug should be in the 2-3 position.

**Table 1: AIC Signal Source**

JP5 Position	Signal Source
1-2	TLC320AD50
2-3	Expansion Connector P4

Programming information for the TLC320AD50 is contained in appendix D.

### 2.5.1 J2, Analog Input

The analog input is driven from either RCA Jack J2 or expansion connector P2. The analog input can be either AC or DC coupled. Jumper JP4 determines if the input is AC or DC coupled.

**Table 2: JP4, Coupling**

JP4 Position	Input Coupling
1-2	DC Coupled
2-3	AC Coupled

### 2.5.2 J3, Analog Output

The analog output is driven to RCA Jack J3 and expansion connector P2.

## **2.6 Expansion Bus**

The TMS320C54XX EVM has an expansion bus which brings out all of the signals from the DSP. This expansion bus allows the user to design custom circuitry to be used with his application without having to design a CPU card. In addition this interface is used by Spectrum Digital for all of its add-on modules.

This expansion bus is divided into 5 double row header connectors. This section contains the signal definitions and pin numbers for each of the connectors.

**Table 3: Expansion Bus Connectors**

Connector	Function
P1	I/O Expansion
P2	Analog Expansion
P3	Address/Data
P4	Control
P6	Host Port Interface



## 2.6.1 P1, I/O Expansion Connector

Because different processors can be used to populate this evaluation module, different signals will be present on P1 depending on the processor used. The next 3 tables show these signals for the respective processors.

### 2.6.1.1 P1, I/O Expansion Connector for LC548, LC549, VC549

The definition of P1, which has the I/O signals for the LC548, LC549, VC549 are shown below.

**Table 4: P1, I/O Expansion Connector (LC548, LC549, VC549)**

Pin #	Signal	Pin #	Signal
1	VCC, +5 Volts	2	VCC, +5 Volts
3	TOUT	4	A16
5	TDR	6	A17
7	TDX	8	A18
9	TFSR	10	A19
11	TFSX	12	A20
13	TCLKR	14	A21
15	TCLKX	16	A22
17	GND	18	GND
19	XF	20	BIO
21	RESERVED	22	RESERVED
23	UARTOUT1	24	UARTOUT3
25	UARTOUT2	26	RESERVED
27	RESERVED	28	RESERVED
29	UARTIN1	30	UARTIN3
31	UARTIN2	32	RESERVED
33	GND	34	GND

**2.6.1.2 P1, I/O Expansion Connector for VC5402**

The definition of P1, which has the I/O signals for the VC5402 is shown below.

**Table 5: P1, I/O Expansion Connector (VC5402)**

Pin #	Signal	Pin #	Signal
1	VCC, +5 Volts	2	VCC, +5 Volts
3	TOUT	4	A16
5	BDR1	6	A17
7	BDX1	8	A18
9	BFSR1	10	A19
11	BFSX1	12	RESERVED
13	BCLKR1	14	RESERVED
15	BCLKX1	16	RESERVED
17	GND	18	GND
19	XF	20	BIO
21	RESERVED	22	RESERVED
23	UARTOUT1	24	UARTOUT3
25	UARTOUT2	26	RESERVED
27	RESERVED	28	RESERVED
29	UARTIN1	30	UARTIN3
31	UARTIN2	32	RESERVED
33	GND	34	GND

**2.6.1.3 P1, I/O Expansion Connector for VC5409/VC5410, VC5416**

The definition of P1, which has the I/O signals for the VC5409, VC5410, and VC5416 are shown below.

**Table 6: P1, I/O Expansion Connector (VC5409/VC5410/VC5416)**

Pin #	Signal	Pin #	Signal
1	VCC, +5 Volts	2	VCC, +5 Volts
3	TOUT	4	A16
5	BDR2	6	A17
7	BDX2	8	A18
9	BFSR1(10)/2(09)	10	A19
11	BFSX1(10)/2(09)	12	A20
13	BCLKR2	14	A21
15	BCLKX2	16	A22
17	GND	18	GND
19	XF	20	BIO
21	RESERVED	22	RESERVED
23	UARTOUT1	24	UARTOUT3
25	UARTOUT2	26	RESERVED
27	RESERVED	28	RESERVED
29	UARTIN1	30	UARTIN3
31	UARTIN2	32	RESERVED
33	GND	34	GND

### 2.6.2 P2, Analog Expansion Connector

The definition of P2, which has the analog signals is shown below.

**Table 7: P2, Analog Expansion Connector**

Pin #	Signal	Pin #	Signal
1	VCCA, +5V Analog	2	VCCA, +5V Analog
3	ADCIN0	4	RESERVED
5	RESERVED	6	RESERVED
7	RESERVED	8	RESERVED
9	RESERVED	10	RESERVED
11	FLAG0	12	RESERVED
13	RESERVED	14	RESERVED
15	RESERVED	16	RESERVED
17	AGND	18	AGND
19	RESERVED	20	RESERVED
21	RESERVED	22	-5V
23	AGND	24	AGND
25	DACOUT0	26	RESERVED
27	RESERVED	28	RESERVED
29	RESERVED	30	RESERVED
31	RESERVED	32	RESERVED
33	AGND	34	AGND

### 2.6.3 P3, Address/data Expansion Connector

The definition of P3, which has the address and data signals is shown below.

**Table 8: P3, Address/Data Expansion Connector**

Pin #	Signal	Pin #	Signal
1	A0	2	A1
3	A2	4	A3
5	A4	6	A5
7	A6	8	A7
9	A8	10	A9
11	A10	12	A11
13	A12	14	A13
15	A14	16	A15
17	GND	18	GND
19	D0	20	D1
21	D2	22	D3
23	D4	24	D5
25	D6	26	D7
27	D8	28	D9
29	D10	30	D11
31	D12	32	D13
33	D14	34	D15

## 2.6.4 P4, Control Expansion Connector

Because different processors can be used to populate this evaluation module, different signals will be present on P4 depending on the processor used. The next 2 tables show these signals for the respective processors.

### 2.6.4.1 P4, Control Expansion Connector for LC548, LC549, VC549, VC5409, VC5410, VC5416

The definition of P4, which has the control signals for the LC548, LC549, VC549, and VC5410 are shown below.

**Table 9: P4, Control Expansion Connector (LC548, LC549, VC549, VC5409, VC5410, VC5416)**

Pin #	Signal	Pin #	Signal
1	VCC, +5 Volts	2	VCC, +5 Volts
3	DS-	4	PS-
5	IS-	6	RESERVED
7	WE-	8	RD-
9	MSTRB-	10	R/W
11	READY	12	IOSTRB-
13	RS-	14	TRGRESET-
15	NMI-	16	XINT1-
17	GND	18	GND
19	XINT2	20	XINT3-
21	BDR0	22	BDR1
23	BDX0	24	BDX1
25	BFSR0	26	BFSR1
27	BFSX0	28	BFSX1
29	BCLKR0	30	BCLKR1
31	RESERVED	32	CLKOUT
33	GND	34	GND

**2.6.4.2 P4, Control Expansion Connector for VC5402**

The definition of P4, which has the control signals for the VC5402 is shown below.

**Table 10: P4, Control Expansion Connector (VC5402)**

Pin #	Signal	Pin #	Signal
1	VCC, +5 Volts	2	VCC, +5 Volts
3	DS-	4	PS-
5	IS-	6	RESERVED
7	WE-	8	RD-
9	MSTRB-	10	R/W
11	READY	12	IOSTRB-
13	RS-	14	TRGRESET-
15	NMI-	16	XINT1-
17	GND	18	GND
19	XINT2	20	XINT3-
21	BDR0	22	RESERVED
23	BDX0	24	RESERVED
25	BFSR0	26	RESERVED
27	BFSX0	28	RESERVED
29	BCLKR0	30	RESERVED
31	RESERVED	32	CLKOUT
33	GND	34	GND

### 2.6.5 P6, Host Port Interface Expansion Connector

The definition of P6, which has the Host Port Interface signals is shown below.

**Table 11: P6, Host Port Interface**

Pin #	Signal	Pin #	Signal
1	HD0	2	HD1
3	HD2	4	HD3
5	HD4	6	HD5
7	HD6	8	HD7
9	RESERVED	10	RESERVED
11	RESERVED	12	RESERVED
13	RESERVED	14	RESERVED
15	RESERVED	16	RESERVED
17	GND	18	GND
19	HCS	20	HDCNTL0
21	RESERVED	22	HDCNTL1
23	HRW	24	HDS2
25	HRDY	26	HDS1
27	HINT	28	HAS
29	HBIL	30	RESERVED
31	RESERVED	32	RESERVED
33	GND	34	GND



## 2.7 P7, JTAG Interface.

The TMS320C54XX Evaluation Module is supplied with a 14 pin header interface, P7. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown figure 2-6 below:

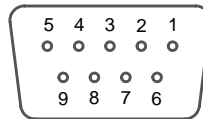
TMS	1	2	TRST-	
TDI	3	4	GND	Header Dimensions
PD (+5V)	5	6	<b>no pin (key)</b>	Pin-to-Pin spacing, 0.100 in. (X,Y)
TDO	7	8	GND	Pin width, 0.025-in. square post
TCK-RET	9	10	GND	Pin length, 0.235-in. nominal
TCK	11	12	GND	
EMU0	13	14	EMU1	

**Figure 2-6, JTAG INTERFACE**

## 2.8 Onboard Serial Interface

The EVM320C54XX has a TL16C550 UART (U8) which provides a an additional serial interface. This UART is mapped into I/O space at locations 0x0000 to 0x0008. This device allows users to use this resource for data logging, code debugging and other applications. The software wait state generator should be set to 3-7 wait states before accessing the UART. The UART interface GAL, U22, generates the necessary wait states to complete the interface cycle.

This UART is brought out to connector P5 on the EVM320C54XX. Connector P5 is a DB9 female connector. The pin positions for the P5 connector as viewed from the edge of the EVM320C54XX.



**Figure 2-7, P5, DB9 Female Connector**

The pin numbers and their corresponding signals are shown in the table below:

**Table 12: P5, RS232 Pinout**

Pin #	PC (female)	SD EVM
2	Rx, input	Tx, output
3	Tx, output	Rx, input
4	DTR, output	Reset/CTS, input*
5	GND	GND
8	CTS, input	RTS, output

\* Jumper JP2 can be used to configure pin 4 to pin 7 on P5. This allows for normal handshaking. The jumper settings are shown in the table below:

**Table 13: JP2 Settings**

JP2 Position	CTS Routing
1-2	P5 pin 4 used on CTS input
2-3	P5 pin 7 used on CTS input

The UART can be jumpered via JP11 to generate different interrupt levels. The type of interrupt is shown in the table below:

**Table 14: Onboard UART Interrupt Selection**

JP11 Position	Interrupt Level
1-2	NMI
2-3	INT1

## 2.9 Boot Loading

The EVM320C54xx is equipped with 32K words of flash ROM for parallel boot loading. This feature does not disallow the ability to boot from the HPI or serial port, but is intended to allow a convenient method of implementing embedded code on the C54XX evaluation module.

The flash ROM on the evaluation module is mapped in data space and I/O space from 0x8000 to 0xFFFF when the module is reset. If the module is in microcomputer mode ( $\overline{\text{MP}}/\overline{\text{MC}}$  pin = 0) the boot loader will be executed.

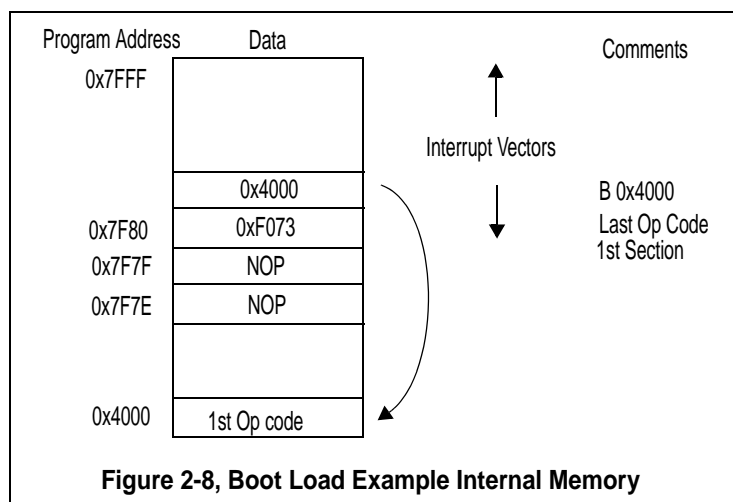
To boot load from flash memory the data must be built in the proper format for the boot loader. Upon execution of the boot loader in parallel mode the on chip boot loader reads the I/O space and/or the data space at 0xFFFF to find the boot loader source address. The appropriate value for the source address boot loading is 0x8000, the flash ROM base address in data space. Since the flash on the evaluation module is word wide we will use the 16 bit parallel load mode in our example.

After the boot loader extracts the source address from the location specified (0xFFFF). The boot loader recognition word (0x10AA) must be located at this address (0x8000 in our example) as shown in table 12.

In our example one section of 0x4000 words will be loaded via the boot loader. Since the part will be in overlay mode on booting our target program space map will be one shown in figure 2-7 in internal C54XX memory.

**Table 15: Sample Boot Load Format Stored In Flash ROM**

Data Space Address	Data Space Data	Function
0xFFFF	0x8000	Source Address
...	0x0000	Zero Fill
0xC009	0x0000	...
0xC008	0xF495(NOP)	Last Op Code, 1st Section
	0xF495(NOP)	
0x8009		1st Op Code, 1st Section
0x8007	0x4000	Destination Address
0x8006	0x0000	Destination of 1st XPC
0x8005	0x4000	Size of 1st Section
0x8004	0x7F80	Entry Point
0x8003	0x0000	Entry XPC
0x8002	0x8802	BSCR Value
0x8001	0x7FFF	SWWR Value
0x8000	0x10AA	Recognition byte 16 bit mode



In our example one section is loaded. However, if multiple sections are used they are tacked onto the first section in the same format as the first section (0x8005 to 0xc008). Of course, the size of each section is independent, as long as the total size of all the sections is less than 32K words. For more information on boot loading options please refer to the C548/C549 boot loading document available from Texas Instruments

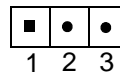
## 2.10 EVM320C54X Jumpers

The EVM320C54X has 14 jumpers which determine how features on the EVM are utilized. The table below lists the jumpers and their function. The following sections describe the use of each jumper.

**Table 16: EVM320C54X Jumpers**

Jumper #	Size	Function
JP1	1 x 3	UART Reset
JP2	1 x 3	UART CTS Routing
JP3	1 x 3	A15/A17 Select
JP4	1 x 3	AD50 AC/DC Coupling
JP5	1 x 3	Synchronous Port Routing
JP6	1 x 3	AD50 Reset
JP7	1 x 3	SYSCLK Option
JP8	1 x 3	AD50 Reference Voltage
JP9	1 x 3	DSP Core Voltage Select
JP10	1 x 3	READY Option
JP11	1 x 3	Onboard UART Interrupt Select
JP12	1 x 2	Voltage select (1.8v/2.5v/3.3v) Default = 1.8 volt, factory installed
JP13	1 x 3	Bootloader Enable
JP14, JP15, JP16	1 x 3	Oscillator Mode Select

Each jumper on the TMS320C54XX EVM is a 1x3 jumper except for jumper. Each 1x3 jumper must have the selection 1-2 or 2-3. The #2 pin is the center pin. The #1 pin has a square solder pad and can be seen from the solder side of the printed circuit board. This pin is usually marked with a '1' on the boards silkscreen. A top view of both types of jumpers is shown below:



**Figure 2-9 1x3 Jumper Layout**

**WARNING!**  
Unless noted otherwise, all 1x3 jumpers must be installed in either the 1-2 or 2-3 position

### 2.10.1 Jumper Positions

The figure 2-1 shows the locations of the jumpers on the EVM320C54XX EVM.

### 2.10.2 JP1, UART Reset

Jumper JP1 is used to select either a system reset from P5, pin4 DTR line or to connect the DTR line to the UART's CTS pin. When position 1-2 is selected the DTR activates the reset. The 2-3 position connects DTR to CTS. The table below shows the positions and their functions:

**Table 17: JP1, UART Reset**

Position	Function
1-2	DTR Activates Reset
2-3	Connects DTR to CTS

### 2.10.3 JP2, Onboard UART CTS Routing

Jumper JP2 can be used to configure the source of the CTS signal on the onboard UART. When position 1-2 is used the pin 4 in P5 is used as the CTS input. If position 2-3 is selected pin 7 on P5 is used as the CTS input. The jumper settings are shown in the table below:

**Table 18: JP2, CTS Routing**

JP13 Position	CTS Routing
1-2	P5 pin 4 used on CTS input
2-3	P5 pin 7 used on CTS input

### 2.10.4 JP3, A15/A17 Select

Jumper JP3 allows the selection of memory address MA15 with either processor address A15 or A17. The table below shows the two positions and their functions:

**Table 19: JP3, A15/A17 Select**

Position	Function
1-2	Use A17 for RAM memory address MA15
2-3	Use A15 for RAM memory address MA15

### 2.10.5 JP4, AD50 AC/DC Coupling

Jumper JP4 is used to select the coupling for the analog input. If position 1-2 is selected the coupling is DC. The 2-3 selection will provide AC coupling.

**Table 20: JP4, AC/DC Coupling**

Position	Function
1-2	DC Coupled
2-3	AC Coupled

### 2.10.6 JP5, Synchronous Port Routing

Jumper JP5 is used to connect the source of data for the synchronous serial port on the C54XX. By selecting position 1-2 the synchronous serial port is connected to the TLC320AD50 AIC. Position 2-3 connects the serial port to the expansion connector P4. The table below shows the positions and their functions:

**Table 21: JP5, Synchronous Port Routing**

Position	Function
1-2	TLC320AD50
2-3	Expansion Connector P4

### 2.10.7 JP6, AD50 Reset

The AD50 Codec can be reset either by the system reset or a user option. Position 1-2 allows the AD50 to be reset by the system reset. In position 2-3 the AD50 is reset from a user defined pin on the DSP. The table below shows the positions and their functions:

**Table 22: JP6, AD50 Reset**

Position	Function
1-2	System Reset Activates AD50 Reset
2-3	User option

### 2.10.8 JP7, SYSCLK Option

Jumper JP7 allows the selection of either the rising edge or falling edge of CLKOUT to generate READY for UART operations. As processor frequencies increase it will be necessary to pipeline the READY signal. This jumper provides for these requirements. The table below shows the two positions and their functions:

**Table 23: JP7, SYSCLK Option**

Position	Function
1-2	Use Inverted CLKOUT for U20 GAL Clock
2-3	Use CLKOUT for U20 GAL Clock

### 2.10.9 JP8, AD50 Reference Voltage

The AD50 AIC can supply an internal reference voltage, however for compatibility with previous versions of the C54xx with the AD50, an external voltage reference is supplied. Jumper JP8 allows the selection of using the external reference or internal reference. When position 1-2 is selected the external reference is used. If the 2-3 position is selected the internal reference is used. These selections are shown in the table below.

**Table 24: JP8, AD50 Reference Voltage**

Position	Function
1-2	External reference
2-3	Internal reference



### 2.10.10 JP9, DSP Core Voltage Select

Jumper JP9 is used to control the voltage to the core of the C54x DSP. If you are not sure of the core voltage refer to a data sheet prior to changing this jumper. The table below shows the setting and the corresponding voltages.

This jumper is set to the appropriate position before shipment.

**Table 25: JP9, DSP Core Voltage Select**

Position	Core Voltage	Device	JP12
1-2	3.3 Volts	LC548, LC549	Not installed
2-3	2.5 Volts	VC549, VC5410	Not installed
2-3	1.8 Volts	VC5402, VC5409, VC5416	Installed
2-3*	1.5 Volts	VC5416	Not Installed

\* resistor values set differently at factory for VC5416.

**WARNING!**  
Setting this jumper incorrectly  
can damage to the DSP device

### 2.10.11 JP10, Ready Routing

READY to the C54XX device from the GAL U20 can be deactivated if necessary. Of course this prevents use of the onboard UART. In normal mode (position 1-2) external READY from the I/O connector is routed through GAL U20. When JP10 is in the 2-3 position the READY signal is routed directly from the expansion connector to the C54XX device. The table below shows the positions and their functions:

**Table 26: JP10, READY Routing**

JP5 Position	Function
1-2	READY from GAL U20
2-3	READY directly from I/O expansion connector

#### 2.10.12 JP11, Onboard UART Interrupt Select

The jumper JP11 is used to select which interrupt the onboard UART will use. Position 1-2 will cause an NMI interrupt. Position 2-3 will cause INT0.

**Table 27: JP11, Onboard UART Interrupt Selection**

JP6 Position	Signal
1-2	NMI
2-3	INT0

This option is used to allow a debug monitor to be placed in ROM or for the serial port to be used with application software which requires interrupt masking.

#### 2.10.13 JP12, Voltage select

Jumper JP12 is a factory installed jumper. This jumper is not to be modified by the user.

#### 2.10.14 JP13, Bootloader Enable/Disable

Jumper JP13 is used to enable or disable the bootloader on the TMS320C54XX. The table below shows the two positions and their functions:

**Table 28: JP13, Bootload Enable/Disabled**

Position	Function
1-2	Boot Loader Enabled
2-3	Boot Loader Disabled

### 2.10.15 JP14, JP15, JP16, Oscillator Selection

Jumpers JP14, JP15, and JP16 are used together to select different clock modes and speeds for the C54XX DSP. The EVM320C54XX is equipped with a 10 megahertz oscillator.

The C54XX PLL can be configured in one of the two provided clock modes:

- The input clock (CLKIN) is divided by 2 or 4; this is called DIV mode
- The input clock (VLKIN) is multiplied by one of 31 possible ratios which range from 0.25 to 15. These ratios are achieved with the Analog Voltage controlled Oscillator (VCO).; this mode is called PLL mode.

When the PLL clock mode is not used, VCO and all the analog parts are disabled in order to minimize the power dissipation

The PLL clock mode can be determined by setting 3 external clock mode pins during reset or by software. In software, a 16 bit register (CLKMD) controls the behavior of the PLL and sets the mode.

At start-up the clock mode is selected with the values on input pins CLKMD1, CLKMD2, and CLKMD3. These these pins are tied to jumpers JP14, JP15, and JP16 respectively. The configuration is shown in the table below.

**Table 29: JP14, JP15, JP16, Clock Mode Table**

<b>JP14, CLKMD1</b>	<b>JP15, CLKMD2</b>	<b>JP16, CLKMD3</b>	<b>Clock Mode/CLKMD Value Upon Reset</b>
2-3	1-2	2-3	1/2 with external source, CLKMD = 0000h
1-2	2-3	2-3	1/2 with external source, CLKMD = 6000h
1-2	1-2	2-3	1/2 with external source, CLKMD = 4000h
2-3	2-3	2-3	1/2 with external source, CLKMD = 2000h
2-3	1-2	1-2	1/2 with external source, CLKMD = 1000h
2-3	2-3	1-2	Stop mode, CLKMD = na
1-2	1-2	1-2	PLL * 1 with external source, CLKMD = 7000h
1-2	2-3	1-2	1/2 with external source, CLKMD = 7000h

## 2.11 LEDs

The EVM320C54X EVM has two light emitting diodes. DS1 indicates the presence of +5 volts and is normally 'on' when power is applied to the board. DS2 is under software control. It is tied to the XF pin on the DSP. These are shown in the table below:

**Table 30: LEDs**

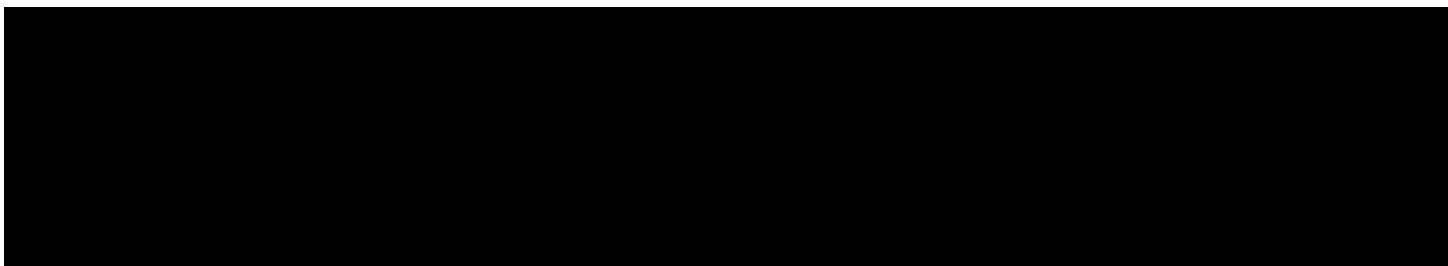
LED #	Color	Controlling Signal	On Signal State
DS1	Green	+5 Volts	1
DS2	Red	XF on DSP	1

## 2.12 Resets

There are multiple resets for the TMS320C54XX EVM. The first reset is the power on reset. This circuit waits until power is within the specified range before releasing the power on reset pin to the TMS320C54XX.

External sources such as push button (SW1), PC Host reset pin 4 on P5 UART interface, and pin 13 on the Control Expansion connector can generate a reset condition.

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