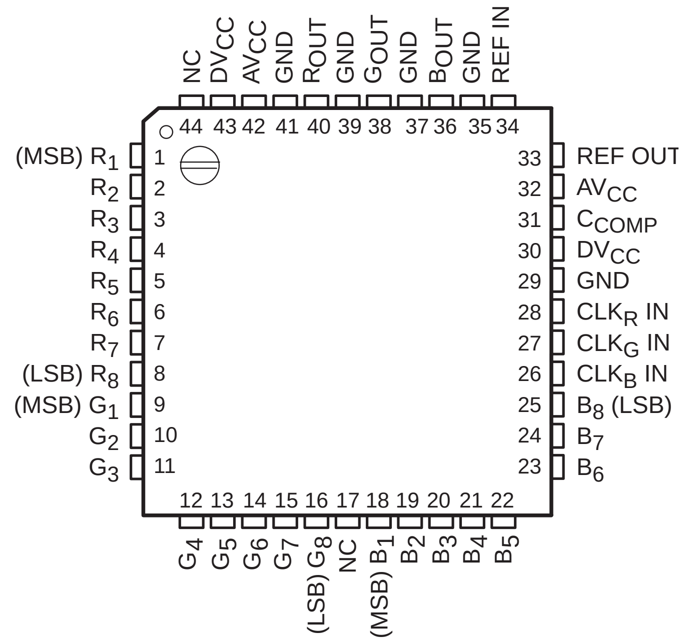
- **8-Bit Resolution**
- **Linearity . . . ±1/2 LSB Maximum**
- **Differential Nonlinearity . . . ±1/2 LSB Maximum**
- **Conversion Rate . . . 60 MHz Min**
- **Nominal Output Signal Operating Range V_{CC} to V_{CC} – 1 V**
- **TTL Digital Input Voltage**
- **5-V Single Power Supply Operation**
- **Low Power Consumption . . . 350 mW Typ**

FR PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL5632C is a low-power ultra-high-speed video digital-to-analog converter that uses the Advanced Low-Power Schottky (ALS) process. The device has a three channel I/O; the red, the blue, and the green channel. The red, blue, and green signals are referred to collectively as the RGB signal. An internally generated reference is also provided for the standard video output voltage range. Conversion of digital signals to analog signals can be at a sampling rate of dc to 60 MHz. The high conversion rate makes the TL5632C suitable for digital television, computer digital video processing, and high-speed data conversion.

The TL5632C is characterized for operation from 0°C to 70°C.

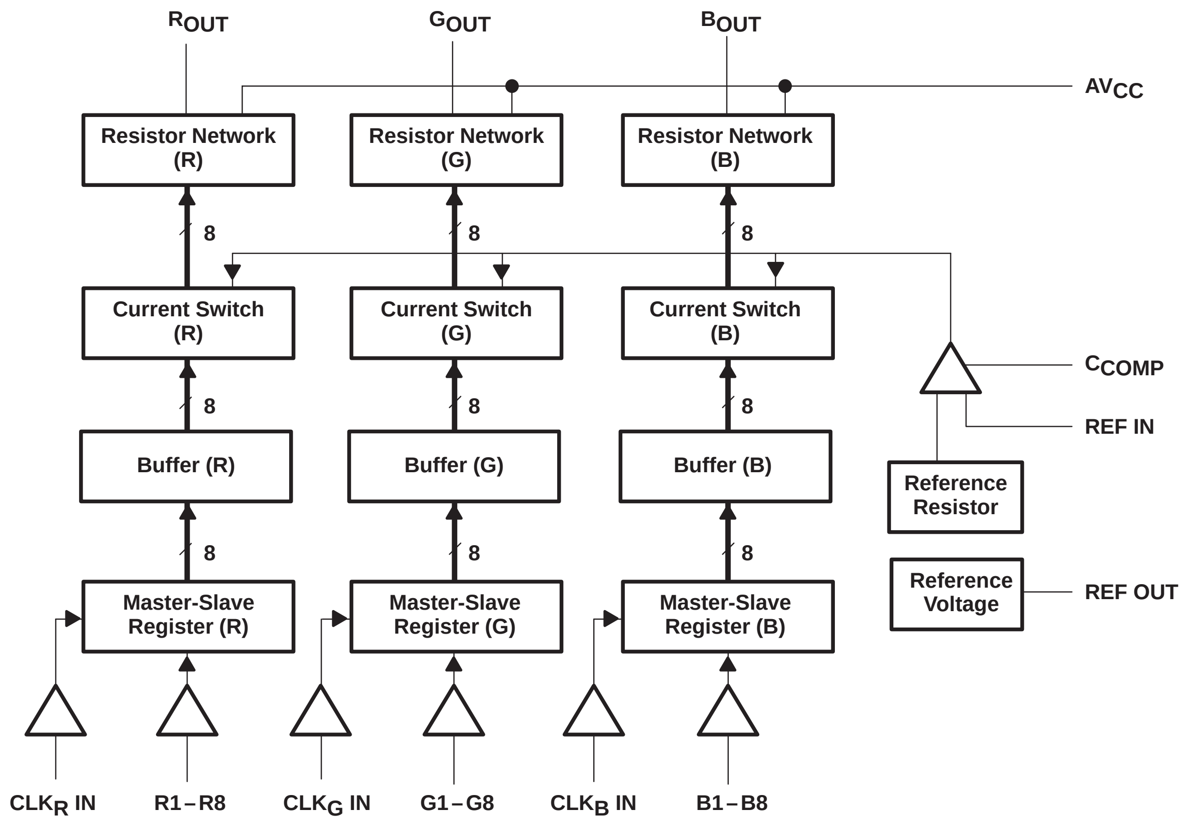
FUNCTION TABLE

STEP	DIGITAL INPUT	OUTPUT VOLTAGE
0	L L L L L L L L	3.980 V
1	L L L L L L L H	3.984 V
•	•	•
•	•	•
•	•	•
127	L H H H H H H H	4.488 V
128	H L L L L L L L	4.492 V
129	H L L L L L L H	4.996 V
•	•	•
•	•	•
•	•	•
254	H H H H H H H L	4.996 V
255	H H H H H H H H	5.000 V

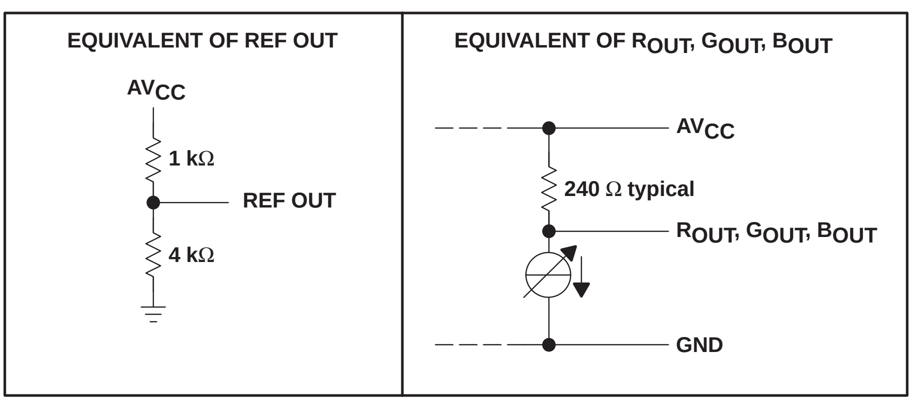
AVAILABLE OPTIONS

T_A	PACKAGE
0°C to 70°C	TL5632CFR

functional block diagram



schematics of outputs



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
$B_1 – B_8$	18 – 25	I	B-channel digital input (B_1= MSB)
B_{OUT}	36	O	B-channel analog output
C_{COMP}	31		Phase compensation capacitance. A 1 μF capacitor is connected from C_{COMP} to GND.
CLK_B IN	26	I	B-channel clock input
CLK_G IN	27	I	G-channel clock input
CLK_R IN	28	I	R-channel clock input
$G_1 – G_8$	9 – 16	I	G-Channel digital input (G_1= MSB)
GND	29, 35, 37, 39, 41		Ground. All GND terminals are connected internally; however, all GND terminals should be connected externally to a ground plane or equivalent low impedance ground return.
G_{OUT}	38	O	G-channel analog output
NC	17, 44		No connection internally
$R_1 – R_8$	1 – 8	I	R-channel digital input (R_1= MSB)
R_{OUT}	40	O	R-channel analog output
AV_{CC}	32, 42		Analog power supply voltage
DV_{CC}	30, 43		Digital power supply voltage
REF IN	34	I	Reference voltage input. REF IN accepts the reference voltage on REF OUT. An external reference can also be applied consistent with Note 1.
REF OUT	33	O	Reference voltage output. An internal voltage divider generates the voltage level (see schematics of outputs, page 2).

NOTE 1: $V_{CC} – V_{ref} \le 1.2$ V

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Power supply voltage range, AV_{CC}, DV_{CC} (see Note 2) . . . . –0.3 V to 7 V
Digital input voltage range, V_I . . . . –0.3 V to DV_{CC}
Analog output voltage range, R_{OUT}, G_{OUT}, B_{OUT}, C_{COMP} (externally applied) . . . . –0.3 V to AV_{CC} + 0.3 V
Reference input range, REF IN . . . . –0.3 V to AV_{CC} + 0.3 V
Reference output range, REF OUT . . . . –0.3 V to AV_{CC} + 0.3 V
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: All voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, AV_{CC}, DV_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Reference voltage, V_{ref} (see Note 1)	3.8	4	4.2	V
Setup time, data before CLK↑, t_{su1}	10			ns
Hold time, data after CLK↑, t_{h1}	3			ns
Pulse duration at high level, t_{w1}	8.3			ns
Pulse duration at low level, t_{w2}	8.3			ns
External phase compensation capacitance, C_{COMP}	1			µF
Operating free-air temperature, T_A	0		70	°C

NOTE 1: $V_{CC} – V_{ref} \leq 1.2$ V

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

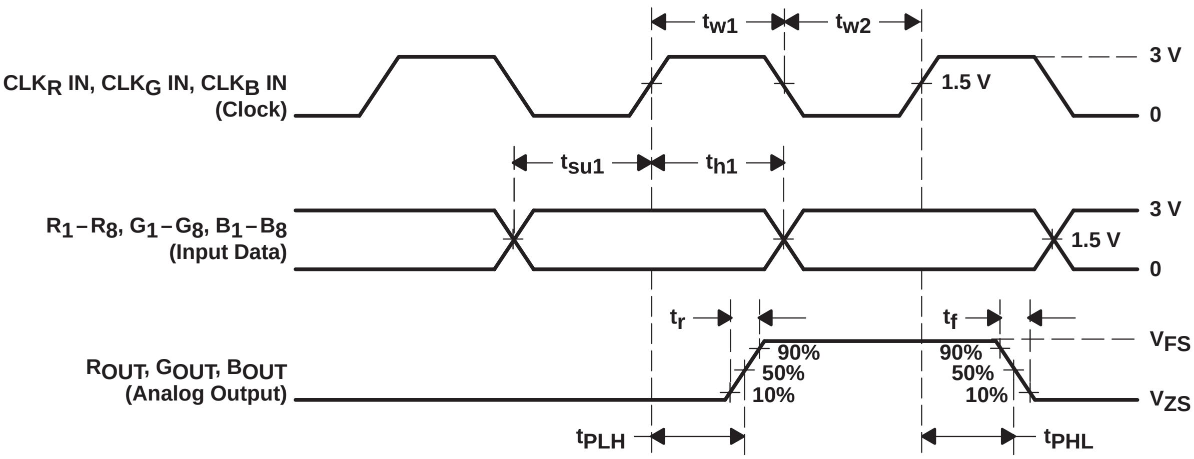
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
	Resolution					8	Bit
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_{IH} = 2.7 V			20	µA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_{IH} = 2.7 V	–400			µA
I_{ref}	Reference input current	REF IN = 4 V				10	µA
V_{ref}	Reference output voltage	V_{CC} = 5 V,	With internal reference	3.8	4	4.2	V
V_{FS}	Full-scale analog output voltage	V_{IH} = 2 V,	REF IN = 4 V	AV_{CC}–15	AV_{CC}	AV_{CC}+15	mV
V_{ZS}	Zero-scale analog output voltage	V_{IL} = 0.8 V,	REF IN = 4 V	3.9	3.98	4.05	V
	RGB full-scale ratio			0%	4%	8%	
z_o	Output impedance			200	240	280	W
I_{CC}	Supply current				70	90	mA

operating characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error	End point, REF IN = 4 V			±0.5	LSB
E_D	Differential linearity error	REF IN = 4 V			±0.5	LSB
f_c	Maximum conversion rate		60			MHz
t_{PLH}	Propagation delay time, low-to-high level	T_A = 25°C, $C_L \leq 5$ pF‡		10		ns
t_{PHL}	Propagation delay time, high-to-low level			10		
t_r	Rise time			5		ns
t_f	Fall time			5		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ C_L includes probe and jig capacitances.

PARAMETER MEASUREMENT INFORMATION



TYPICAL CHARACTERISTICS

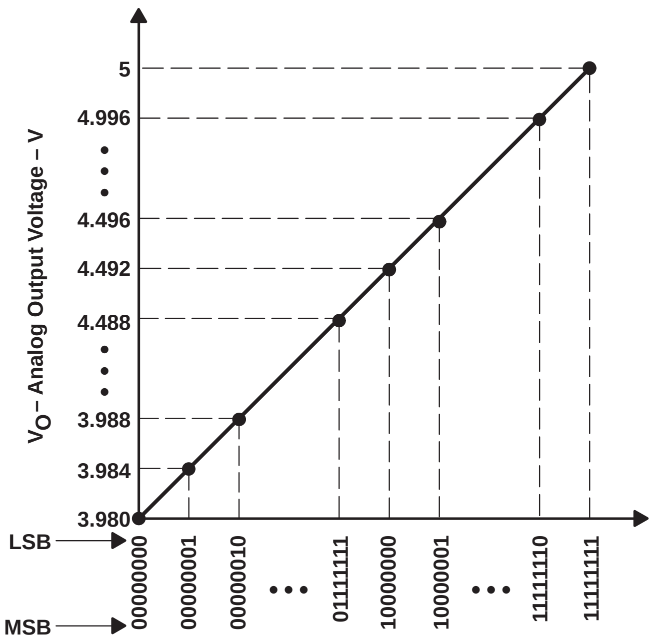


Figure 1. Ideal Conversion Characteristics

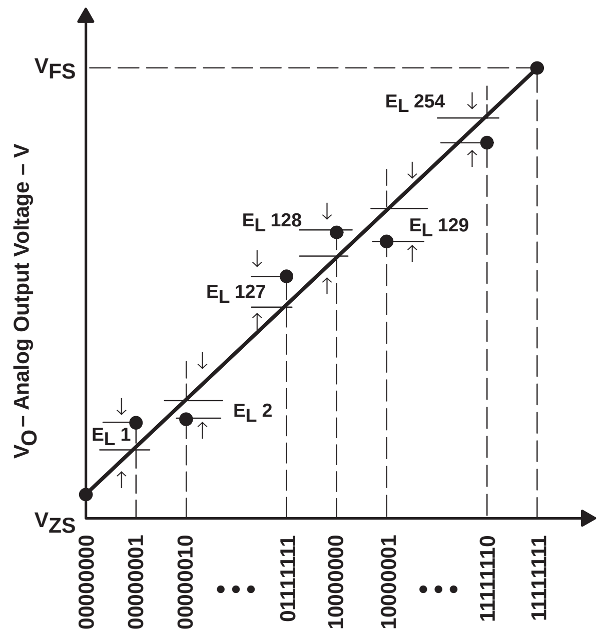


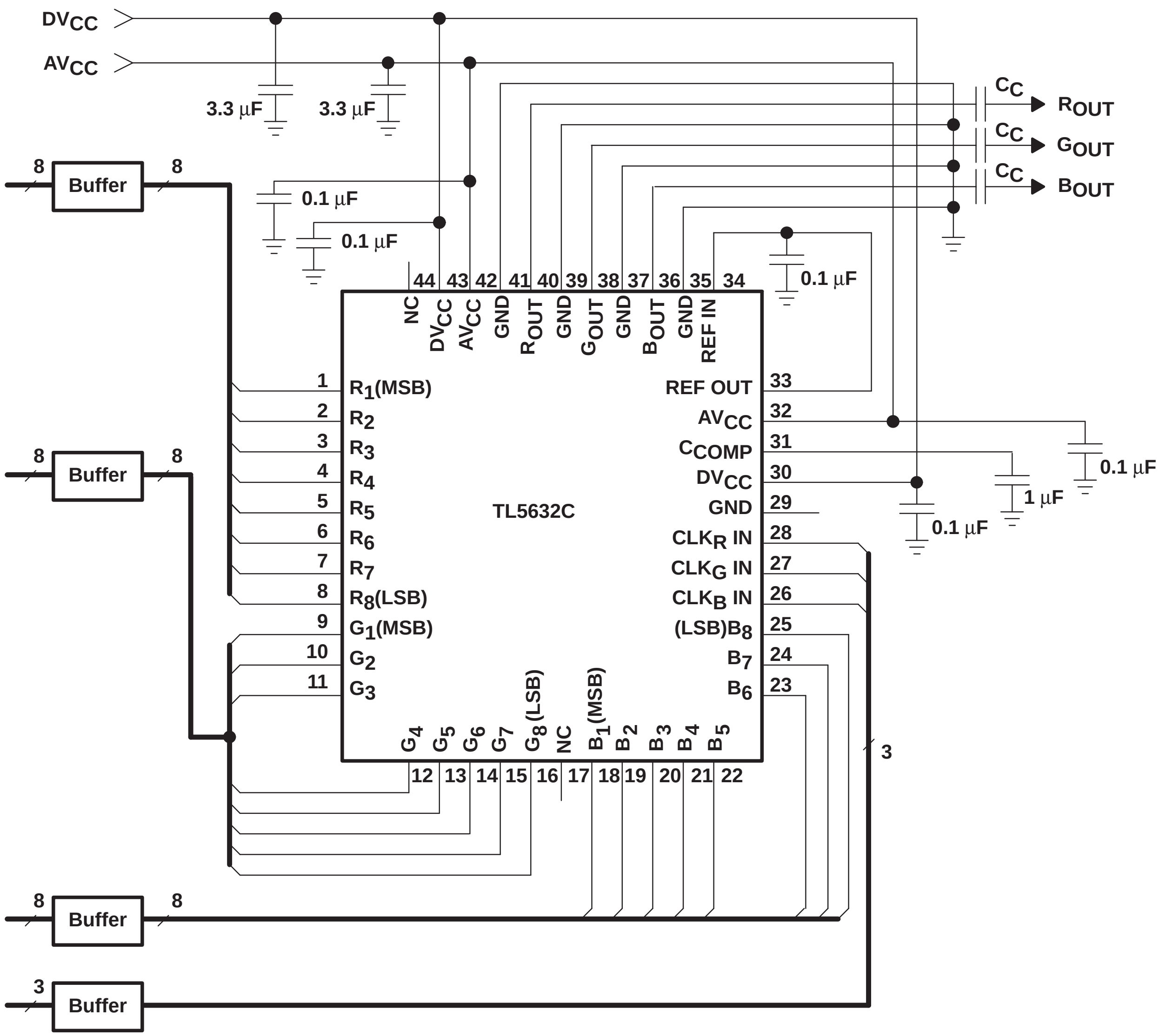
Figure 2. End-Point Linearity Error

APPLICATION INFORMATION

The following design procedures should be used for optimum operation.

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or RF printed-circuit-board (PCB) techniques should be used throughout the evaluation and production process.
- Wide ground leads or a ground plane should be used on the PCB layouts to minimize parasitic inductance and resistance. A ground plane is the better choice for noise reduction.
- AV_{CC} and DV_{CC} are also separate internally, so they must be connected externally. These external PCB leads should also be made as wide as possible. A ferrite bead or equivalent inductance should be placed in series with AV_{CC} and the decoupling capacitor before the AV_{CC} and DV_{CC} leads are connected together on the board. It is critical that the supply voltage applied to AV_{CC} be as noise free and ripple free as possible. Ripple and noise rejection should be a minimum of 60 dB below the full-scale output range of 1 V peak-to-peak.
- AV_{CC} to GND and DV_{CC} to GND should be decoupled with 3.3-µF and 0.1-µF capacitors, respectively, as close as possible to the appropriate device terminals. A ceramic chip capacitor is recommended for the 0.1-µF capacitor.
- The phase compensation capacitor should be connected between C_{COMP} and GND with as short a lead-in as possible.
- The no-connection (NC) terminals on the small-outline package should be connected to GND.
- AV_{CC}, DV_{CC}, and R_{OUT}, G_{OUT}, and B_{OUT} should be shielded from the high-frequency terminals CLK_R IN, CLK_G IN ,and CLK_B IN and the input data terminals. GND traces should be placed on both sides of the R_{OUT}, G_{OUT}, and B_{OUT} traces on the PCB to the following signal processing stage. These output traces should be as short as possible.

APPLICATION INFORMATION

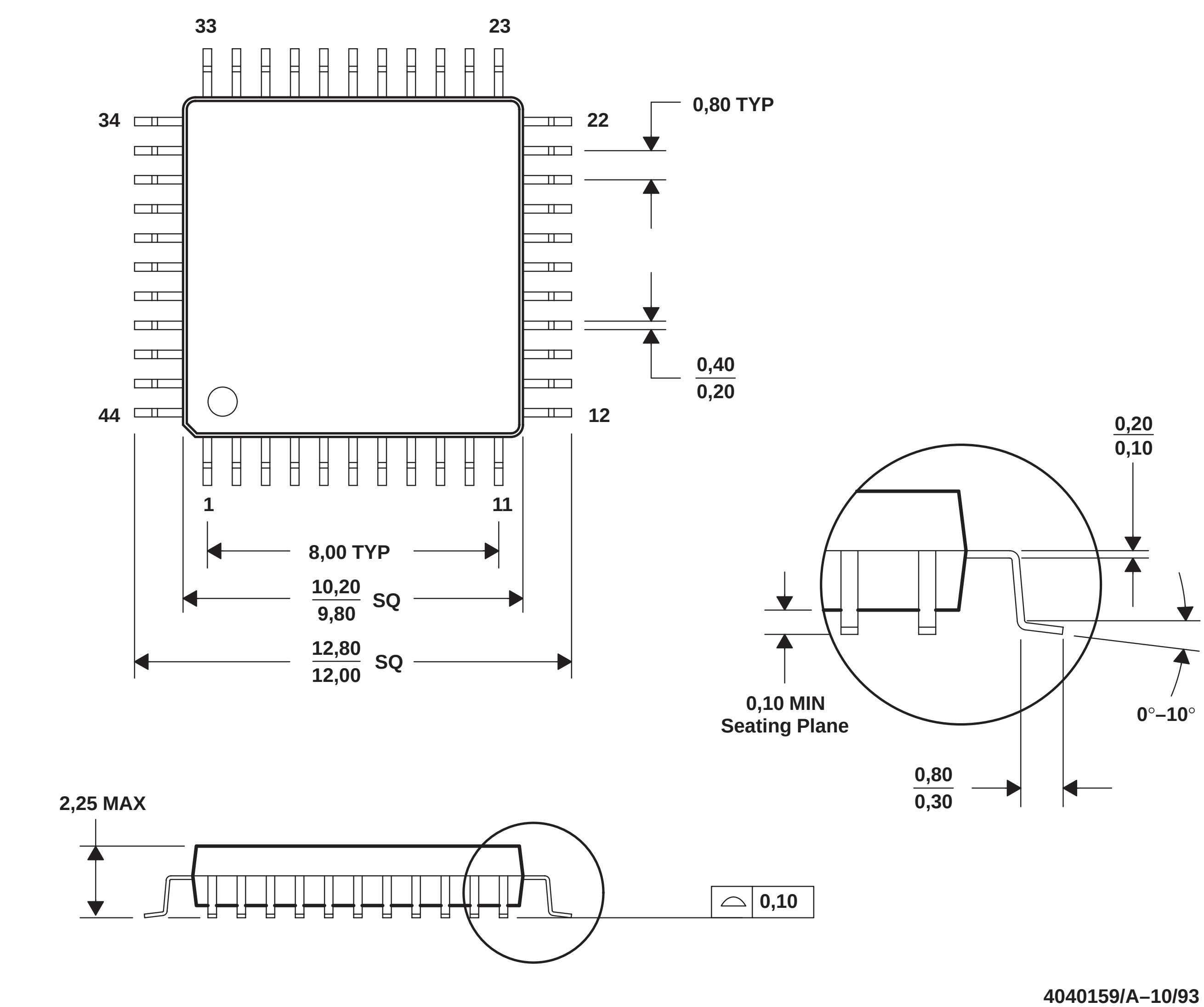


NOTES: A. Buffers are SN74AS244 or equivalent.
B. 0.1 µF capacitors should be placed as close to the device terminals as possible.
C. The coupling capacitor (C_C) value is application specific and selectable by the user.

Figure 3. Typical Bypass, Buffer, and Output Configuration

MECHANICAL DATA

FR/S-PQFP-G44 **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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