- **High-Performance Digital Media Processor (TMS320DM642)**
  - **2-, 1.67-ns Instruction Cycle Time**
  - **500-, 600-MHz Clock Rate**
  - **Eight 32-Bit Instructions/Cycle**
  - **4000, 4800 MIPS**
  - **Fully Software-Compatible With C64x™**
- **VelociTI.2™ Extensions to VelociTI™ Advanced Very-Long-Instruction-Word (VLIW) TMS320C64x™ DSP Core**
  - **Eight Highly Independent Functional Units With VelociTI.2™ Extensions:**
    - **Six ALUs (32-/40-Bit), Each Supports Single 32-Bit, Dual 16-Bit, or Quad 8-Bit Arithmetic per Clock Cycle**
    - **Two Multipliers Support Four 16 x 16-Bit Multiplies (32-Bit Results) per Clock Cycle or Eight 8 x 8-Bit Multiplies (16-Bit Results) per Clock Cycle**
  - **Load-Store Architecture With Non-Aligned Support**
  - **64 32-Bit General-Purpose Registers**
  - **Instruction Packing Reduces Code Size**
  - **All Instructions Conditional**
- **Instruction Set Features**
  - **Byte-Addressable (8-/16-/32-/64-Bit Data)**
  - **8-Bit Overflow Protection**
  - **Bit-Field Extract, Set, Clear**
  - **Normalization, Saturation, Bit-Counting**
  - **VelociTI.2™ Increased Orthogonality**
- **L1/L2 Memory Architecture**
  - **128K-Bit (16K-Byte) L1P Program Cache (Direct Mapped)**
  - **128K-Bit (16K-Byte) L1D Data Cache (2-Way Set-Associative)**
  - **2M-Bit (256K-Byte) L2 Unified Mapped RAM/Cache (Flexible RAM/Cache Allocation)**
- **Endianess: Little Endian, Big Endian**
- **64-Bit External Memory Interface (EMIF)**
  - **Glueless Interface to Asynchronous Memories (SRAM and EPROM) and Synchronous Memories (SDRAM, SBSRAM, ZBT SRAM, and FIFO)**
  - **1024M-Byte Total Addressable External Memory Space**
- **Enhanced Direct-Memory-Access (EDMA) Controller (64 Independent Channels)**
- **10/100 Mb/s Ethernet MAC (EMAC)**
  - **IEEE 802.3 Compliant**
  - **Media Independent Interface (MII)**
  - **8 Independent Transmit (TX) and 8 Independent Receive (RX) Channels**
- **Management Data Input/Output (MDIO)**
- **Three Configurable Video Ports**
  - **Providing a Glueless I/F to Common Video Decoder and Encoder Devices**
  - **Supports Multiple Resolutions and Video Standards (CCIR601, ITU–BT.656, BT.1120, SMPTE 125M, 260M, 274M, and 296M)**
  - **Supports RAW Video I/O**
  - **Transport Stream Interface Mode**
- **VCXO Interpolated Control Port (VIC)**
  - **Supports Audio/Video Synchronization**
- **Host-Port Interface (HPI)**
  - **User-Configurable Bus Width (32-/16-Bit)**
- **32-Bit/66-MHz, 3.3-V Peripheral Component Interconnect (PCI) Master/Slave Interface Conforms to PCI Specification 2.2**
- **Multichannel Audio Serial Port (McASP)**
  - **Eight Serial Data Pins**
  - **Wide Variety of I2S and Similar Bit Stream Format**
  - **Integrated Digital Audio I/F Transmitter Supports S/PDIF, IEC60958-1, AES-3, CP-430 Formats**
- **Inter-Integrated Circuit (I^2C) Bus**
- **Two Multichannel Buffered Serial Ports**
- **Three 32-Bit General-Purpose Timers**
- **Sixteen General-Purpose I/O (GPIO) Pins**
  - **Programmable Interrupt/Event Generation Modes**
- **Flexible PLL Clock Generator**
- **IEEE-1149.1 (JTAG†) Boundary-Scan-Compatible**
- **548-Pin Ball Grid Array (BGA) Package (GDK Suffix), 0.8-mm Ball Pitch**
- **0.12-μm/4-Level Copper Metal Process**
  - **CMOS Technology**
- **3.3-V I/Os, 1.2-V Internal (-500)**
- **3.3-V I/Os, 1.4-V Internal (-600)**

PRODUCT PREVIEW

C64x, VelociTI.2, VelociTI, and TMS320C64x are trademarks of Texas Instruments.
Motorola is a trademark of Motorola, Inc.
† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

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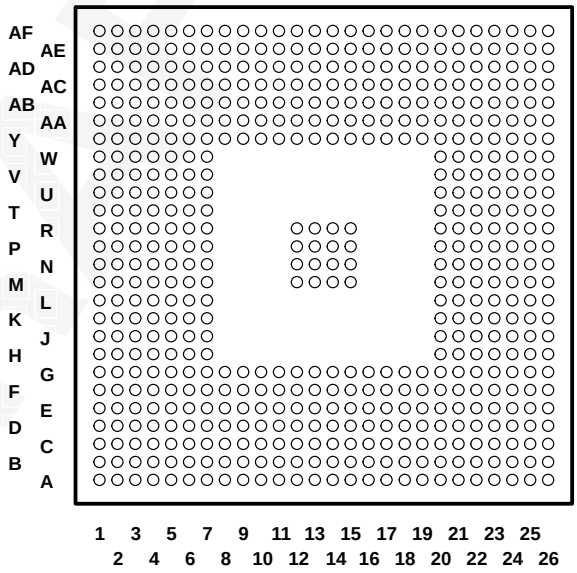
GDK BGA package (bottom view)

**GDK 548-PIN BALL GRID ARRAY (BGA) PACKAGE
(BOTTOM VIEW)**



description

The TMS320C64x™ DSPs (including the TMS320DM642 device) are the highest-performance fixed-point DSP generation in the TMS320C6000™ DSP platform. The TMS320DM642 (DM642) device is based on the second-generation high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture (VelociTI.2™) developed by Texas Instruments (TI), making these DSPs an excellent choice for digital media applications. The C64x™ is a code-compatible member of the C6000™ DSP platform.

With performance of up to 4800 million instructions per second (MIPS) at a clock rate of 600 MHz, the DM642 device offers cost-effective solutions to high-performance DSP programming challenges. The DM642 DSP possesses the operational flexibility of high-speed controllers and the numerical capability of array processors. The C64x™ DSP core processor has 64 general-purpose registers of 32-bit word length and eight highly independent functional units—two multipliers for a 32-bit result and six arithmetic logic units (ALUs)— with VelociTI.2™ extensions. The VelociTI.2™ extensions in the eight functional units include new instructions to accelerate the performance in video and imaging applications and extend the parallelism of the VelociTI™ architecture. The DM642 can produce four 32-bit multiply-accumulates (MACs) per cycle for a total of 2400 million MACs per second (MMACS), or eight 8-bit MACs per cycle for a total of 4800 MMACS. The DM642 DSP also has application-specific hardware logic, on-chip memory, and additional on-chip peripherals similar to the other C6000™ DSP platform devices.

The DM642 uses a two-level cache-based architecture and has a powerful and diverse set of peripherals. The Level 1 program cache (L1P) is a 128-Kbit direct mapped cache and the Level 1 data cache (L1D) is a 128-Kbit 2-way set-associative cache. The Level 2 memory/cache (L2) consists of an 2-Mbit memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or combinations of the two. The peripheral set includes: three configurable video ports; a 10/100 Mb/s Ethernet MAC (EMAC); a management data input/output (MDIO) module; a VCXO interpolated control port (VIC); one multichannel buffered audio serial port (McASP0); an inter-integrated circuit (I2C) Bus module; two multichannel buffered serial ports (McBSPs); three 32-bit general-purpose timers; a user-configurable 16-bit or 32-bit host-port interface (HPI16/HPI32); a peripheral component interconnect (PCI); a general-purpose input/output port (GP0) with 16 GPIO pins; and a 64-bit glueless external memory interface (EMIFA), which is capable of interfacing to synchronous and asynchronous memories and peripherals.

The DM642 device has three configurable video port peripherals (VP0, VP1, and VP2). These video port peripherals provide a glueless interface to common video decoder and encoder devices. All three Video Port peripherals have the capability to operate as a video-capture port, a video-display port, or a transport stream interface (TSI) capture port. The DM642 video port peripherals support multiple resolutions and video standards (e. g., CCIR601, ITU–BT.656, BT.1120, SMPTE 125M, 260M, 274M, and 296M).

These three video port peripherals are configurable and can support either video capture and video display modes. Each video port consists of two channels — A and B with a 5120-byte capture/display buffer that is splittable between the two channels.

For capture operation, the video port can operate as two 8/10-bit channels of BT.656 or two 8/10-bit channel of raw video capture; *or* as a single channel of 8/10-bit BT.656, 8/10-bit raw video, 16/20-bit Y/C video, 16/20-bit raw video, or 8-bit TSI.

For display operation, the video port can operate as a single channel (using only channel A) of 8/10-bit BT.656 display, 8/10-bit raw video display, 16/20-bit Y/C video display, or 16/20-bit raw video display. Also, in the display mode of operation, the video port is capable of operating in a two-channel 8/10-bit raw mode in which two channels are locked to the same timing.

For more details on the Video Port peripherals, see the *TMS320DM642 Technical Overview* (literature number – TBD).

PRODUCT PREVIEW

description (continued)

The McASP0 port supports one transmit and one receive clock zone, with eight serial data pins which can be individually allocated to any of the two zones. The serial port supports time-division multiplexing on each pin from 2 to 32 time slots. The DM642 has sufficient bandwidth to support all 8 serial data pins transmitting a 192-kHz stereo signal. Serial data in each zone may be transmitted and received on multiple serial data pins simultaneously and formatted in a multitude of variations on the Philips Inter-IC Sound (I^2S) format.

In addition, the McASP0 transmitter may be programmed to output multiple S/PDIF, IEC60958, AES-3, CP-430 encoded data channels simultaneously, with a single RAM containing the full implementation of user data and channel status fields.

McASP0 also provides extensive error-checking and recovery features, such as the bad clock detection circuit for each high-frequency master clock which verifies that the master clock is within a programmed frequency range.

VXCO interpolated control port (VIC) – **TBD**

Ethernet MAC (EMAC) – **TBD**

Management data input/output (MDIO) – **TBD**

The I2C0 port on the TMS320DM642 allows the DSP to easily control peripheral devices, boot from a serial EEPROM, and communicate with a host processor. In addition, the standard multichannel buffered serial port (McBSP) may be used to communicate with serial peripheral interface (SPI) mode peripheral devices.

The DM642 has a complete set of development tools which includes: a new C compiler, an assembly optimizer to simplify programming and scheduling, and a Windows™ debugger interface for visibility into source code execution.

Windows is a registered trademark of the Microsoft Corporation.

device characteristics

Table 1 provides an overview of the DM642 DSP. The table shows significant features of the DM642 device, including the capacity of on-chip RAM, the peripherals, the CPU frequency, and the package type with pin count.

Table 1. Characteristics of the DM642 Processor

HARDWARE FEATURES		DM642
Peripherals Not all peripherals pins are available at the same time (For more detail, see the Device Configuration section).	EMIFA (64-bit bus width) (clock source = AECLKIN)	1
	EDMA (64 independent channels)	1
	McASP0 (uses AUXCLK or SYSCLK2)	1
	I2C0 (uses SYSCLK2)	1
	HPI (32- or 16-bit user selectable)	1 (HPI16 or HPI32)
	PCI (32-bit), 66-MHz	1
	McBSPs (internal clock source = CPU/4 clock frequency)	2
	Configurable Video Ports (VP0, VP1, VP2)	3
	10/100 Ehternet MAC (EMAC)	1
	Management Data Input/Output (MDIO)	1
	VXCO Interpolated Control Port (VIC)	1
	32-Bit Timers (internal clock source = CPU/8 clock frequency)	3
	General-Purpose Input/Output Port (GP0)	16
On-Chip Memory	Size (Bytes)	288K
	Organization	16K-Byte (16KB) L1 Program (L1P) Cache 16KB L1 Data (L1D) Cache 256KB Unified Mapped RAM/Cache (L2)
CPU ID + CPU Rev ID	Control Status Register (CSR.[31:16])	0x0C01
JTAG BSDL_ID	JTAGID register (address location: 0x01B3F008)	0x0007902F
Frequency	MHz	500, 600
Cycle Time	ns	2 ns (DM642-500 [500 MHz CPU, 100 MHz EMIF]) 1.67 ns (DM642-600 [600 MHz CPU, 100 MHz EMIF]) 1.67 ns (DM642-603 [600 MHz CPU, 133 MHz EMIF])
Voltage	Core (V)	1.2 V (-500) 1.4 V (-600, -603)
	I/O (V)	3.3 V
PLL Options	CLKIN frequency multiplier	Bypass (x1), x6, x12
BGA Package	23 x 23 mm	548-Pin BGA (GDK)
Process Technology	µm	0.12 µm
Product Status‡	Product Preview (PP) Advance Information (AI) Production Data (PD)	PP
Device Part Numbers	(For more details on the C6000™ DSP part numbering, see Figure 4)	TMX320DM642GDK

† On this DM64x™ device, the rated EMIF speed affects only the SDRAM interface on the EMIF. For more detailed information, see the EMIF device speed portion of this data sheet.

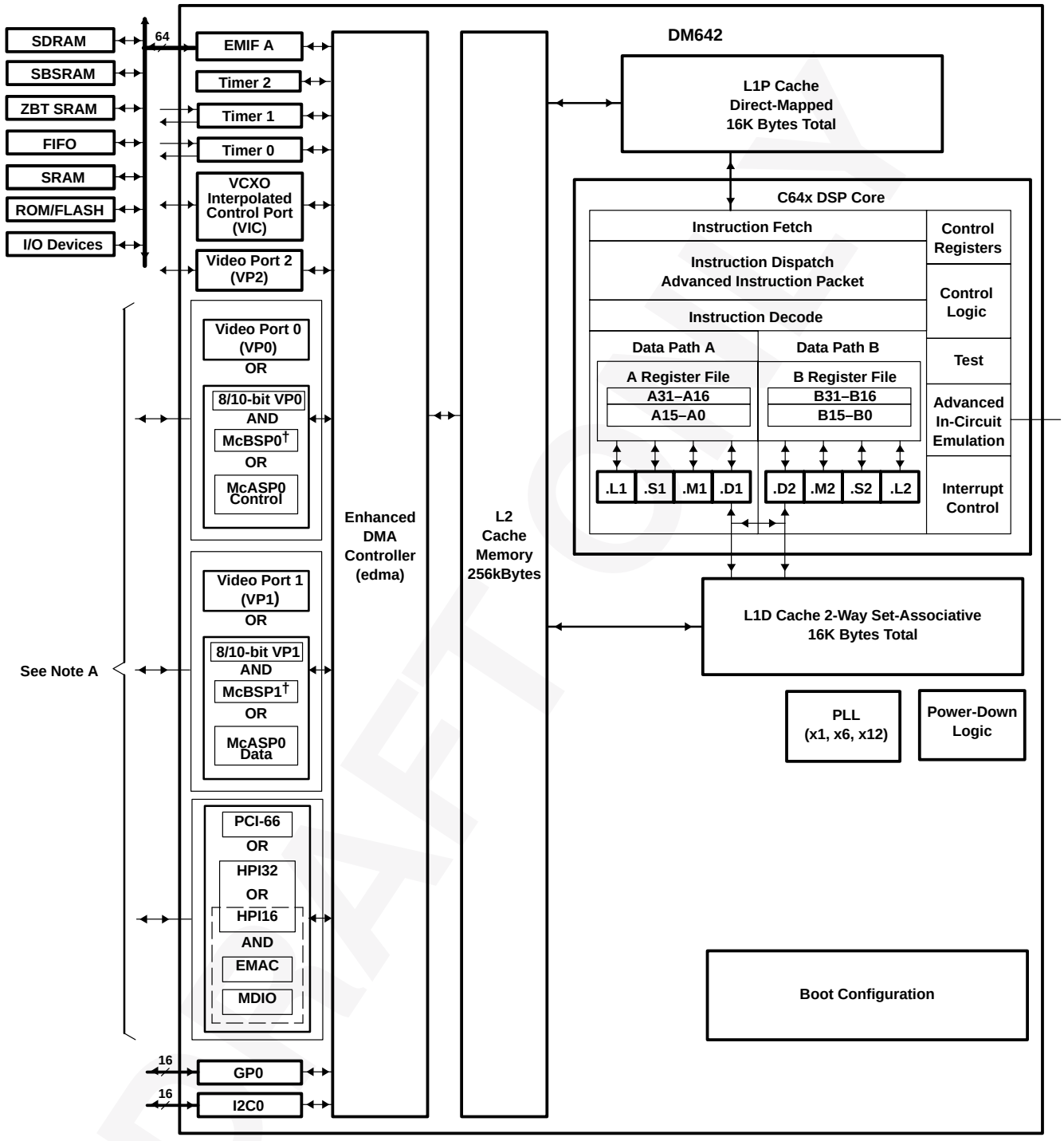
‡ PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.
ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

device compatibility

The DM642 device is a code-compatible member of the C6000™ DSP platform.

TBD

functional block and CPU (DSP core) diagram



† McBSPs: Framing Chips – H.100, MVIP, SCSA, T1, E1; AC97 Devices; SPI Devices; Codecs

NOTE A: The Video Port 0 (VP0) peripheral is muxed with the McBSP0 peripheral and the McASP0 control pins. The Video Port 1 (VP1) peripheral is muxed with the McBSP1 peripheral and the McASP0 data pins. The PCI peripheral is muxed with the HPI(32/16), EMAC, and MDIO peripherals. For more details on the multiplexed pins of these peripherals, see the Device Configurations section of this data sheet.

CPU (DSP core) description

The CPU fetches VelociTI™ advanced very-long instruction words (VLIWs) (256 bits wide) to supply up to eight 32-bit instructions to the eight functional units during every clock cycle. The VelociTI™ VLIW architecture features controls by which all eight units do not have to be supplied with instructions if they are not ready to execute. The first bit of every 32-bit instruction determines if the next instruction belongs to the same execute packet as the previous instruction, or whether it should be executed in the following clock as a part of the next execute packet. Fetch packets are always 256 bits wide; however, the execute packets can vary in size. The variable-length execute packets are a key memory-saving feature, distinguishing the C64x CPUs from other VLIW architectures. The C64x™ VelociTI.2™ extensions add enhancements to the TMS320C62x™ DSP VelociTI™ architecture. These enhancements include:

- Register file enhancements
- Data path extensions
- Quad 8-bit and dual 16-bit extensions with data flow enhancements
- Additional functional unit hardware
- Increased orthogonality of the instruction set
- Additional instructions that reduce code size and increase register flexibility

The CPU features two sets of functional units. Each set contains four units and a register file. One set contains functional units .L1, .S1, .M1, and .D1; the other set contains units .D2, .M2, .S2, and .L2. The two register files each contain 32 32-bit registers for a total of 64 general-purpose registers. In addition to supporting the packed 16-bit and 32-/40-bit fixed-point data types found in the C62x™ VelociTI™ VLIW architecture, the C64x™ register files also support packed 8-bit data and 64-bit fixed-point data types. The two sets of functional units, along with two register files, compose sides A and B of the CPU [see the functional block and CPU (DSP core) diagram, and Figure 1]. The four functional units on each side of the CPU can freely share the 32 registers belonging to that side. Additionally, each side features a “data cross path”—a single data bus connected to all the registers on the other side, by which the two sets of functional units can access data from the register files on the opposite side. The C64x CPU pipelines data-cross-path accesses over multiple clock cycles. This allows the same register to be used as a data-cross-path operand by multiple functional units in the same execute packet. All functional units in the C64x CPU can access operands via the data cross path. Register access by functional units on the same side of the CPU as the register file can service all the units in a single clock cycle. On the C64x CPU, a delay clock is introduced whenever an instruction attempts to read a register via a data cross path if that register was updated in the previous clock cycle.

In addition to the C62x™ DSP fixed-point instructions, the C64x™ DSP includes a comprehensive collection of quad 8-bit and dual 16-bit instruction set extensions. These VelociTI.2™ extensions allow the C64x CPU to operate directly on packed data to streamline data flow and increase instruction set efficiency. This is a key factor for video and imaging applications.

Another key feature of the C64x CPU is the load/store architecture, where all instructions operate on registers (as opposed to data in memory). Two sets of data-addressing units (.D1 and .D2) are responsible for all data transfers between the register files and the memory. The data address driven by the .D units allows data addresses generated from one register file to be used to load or store data to or from the other register file. The C64x .D units can load and store bytes (8 bits), half-words (16 bits), and words (32 bits) with a single instruction. And with the new data path extensions, the C64x .D unit can load and store doublewords (64 bits) with a single instruction. Furthermore, the non-aligned load and store instructions allow the .D units to access words and doublewords on any byte boundary. The C64x CPU supports a variety of indirect addressing modes using either linear- or circular-addressing with 5- or 15-bit offsets. All instructions are conditional, and most can access any one of the 64 registers. Some registers, however, are singled out to support specific addressing modes or to hold the condition for conditional instructions (if the condition is not automatically “true”).

TMS320C62x is a trademark of Texas Instruments.

CPU (DSP core) description (continued)

The two .M functional units perform all multiplication operations. Each of the C64x .M units can perform two 16 × 16-bit multiplies or four 8 × 8-bit multiplies per clock cycle. The .M unit can also perform 16 × 32-bit multiply operations, dual 16 × 16-bit multiplies with add/subtract operations, and quad 8 × 8-bit multiplies with add operations. In addition to standard multiplies, the C64x .M units include bit-count, rotate, Galois field multiplies, and bidirectional variable shift hardware.

The two .S and .L functional units perform a general set of arithmetic, logical, and branch functions with results available every clock cycle. The arithmetic and logical functions on the C64x CPU include single 32-bit, dual 16-bit, and quad 8-bit operations.

The processing flow begins when a 256-bit-wide instruction fetch packet is fetched from a program memory. The 32-bit instructions destined for the individual functional units are “linked” together by “1” bits in the least significant bit (LSB) position of the instructions. The instructions that are “chained” together for simultaneous execution (up to eight in total) compose an execute packet. A “0” in the LSB of an instruction breaks the chain, effectively placing the instructions that follow it in the next execute packet. A C64x™ DSP device enhancement now allows execute packets to cross fetch-packet boundaries. In the TMS320C62x™/TMS320C67x™ DSP devices, if an execute packet crosses the fetch-packet boundary (256 bits wide), the assembler places it in the next fetch packet, while the remainder of the current fetch packet is padded with NOP instructions. In the C64x™ DSP device, the execute boundary restrictions have been removed, thereby, eliminating all of the NOPs added to pad the fetch packet, and thus, decreasing the overall code size. The number of execute packets within a fetch packet can vary from one to eight. Execute packets are dispatched to their respective functional units at the rate of one per clock cycle and the next 256-bit fetch packet is not fetched until all the execute packets from the current fetch packet have been dispatched. After decoding, the instructions simultaneously drive all active functional units for a maximum execution rate of eight instructions every clock cycle. While most results are stored in 32-bit registers, they can be subsequently moved to memory as bytes, half-words, or doublewords. All load and store instructions are byte-, half-word-, word-, or doubleword-addressable.

For more details on the C64x CPU functional units enhancements, see the following documents:

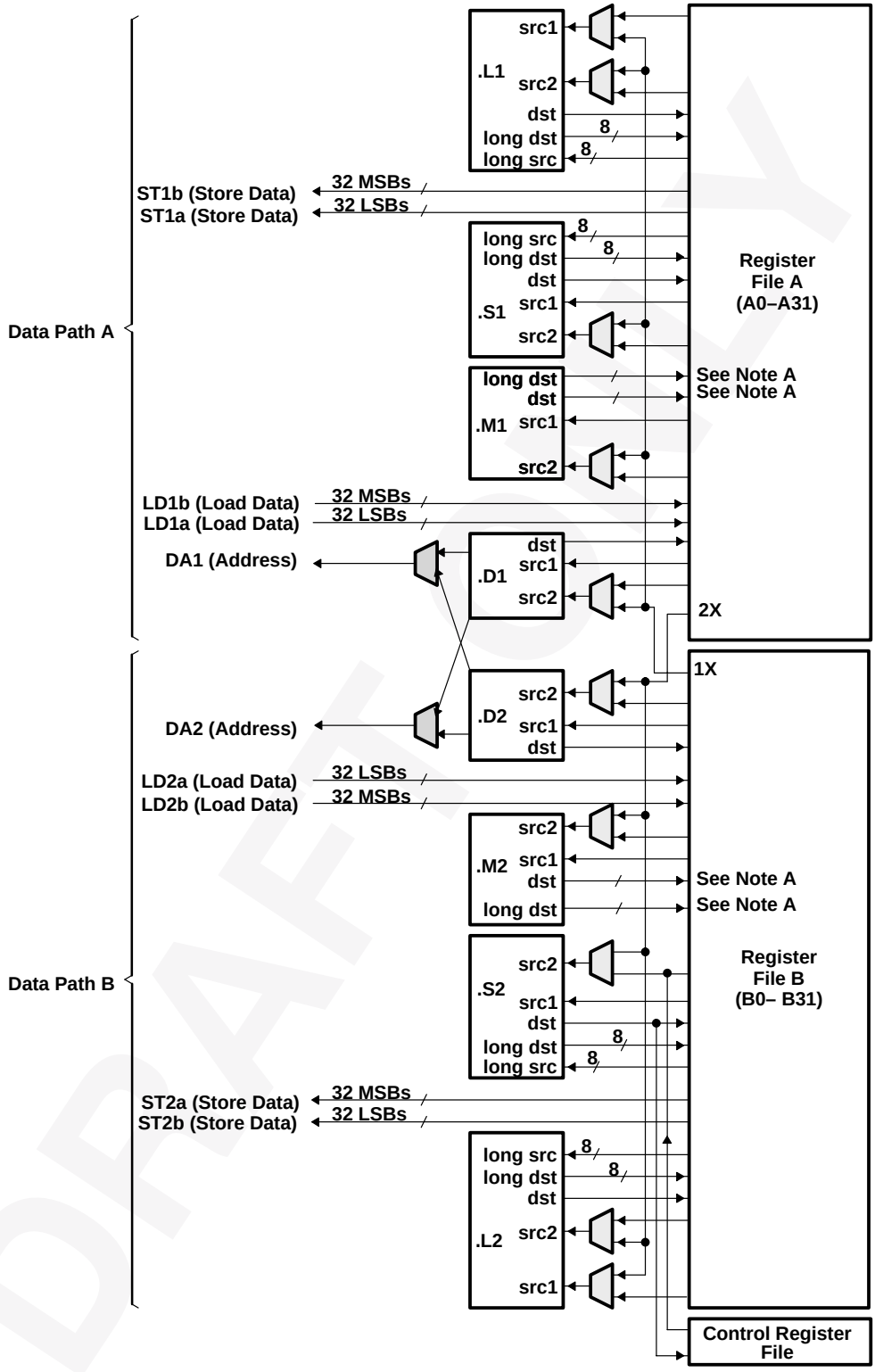
The *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189)

TMS320C64x Technical Overview (literature number SPRU395)

TMS320DM642 Technical Brief (literature number **TBD**)

TMS320C67x is a trademark of Texas Instruments.

CPU (DSP core) description (continued)



NOTE B: For the .M functional units, the long dst is 32 MSBs and the dst is 32 LSBs.

Figure 1. TMS320C64x™ CPU (DSP Core) Data Paths

memory map summary

Table 2 shows the memory map address ranges of the DM642 device. Internal memory is always located at address 0 and can be used as both program and data memory. The external memory address ranges in the DM642 device begin at the hex address location 0x8000 0000 for EMIFA.

Table 2. TMS320DM642 Memory Map Summary

MEMORY BLOCK DESCRIPTION	BLOCK SIZE (BYTES)	HEX ADDRESS RANGE
Internal RAM (L2)	256K	0000 0000 – 0003 FFFF
Reserved	768K	0004 0000 – 000F FFFF
Reserved	23M	0010 0000 – 017F FFFF
External Memory Interface A (EMIFA) Registers	256K	0180 0000 – 0183 FFFF
L2 Registers	256K	0184 0000 – 0187 FFFF
HPI Registers	256K	0188 0000 – 018B FFFF
McBSP 0 Registers	256K	018C 0000 – 018F FFFF
McBSP 1 Registers	256K	0190 0000 – 0193 FFFF
Timer 0 Registers	256K	0194 0000 – 0197 FFFF
Timer 1 Registers	256K	0198 0000 – 019B FFFF
Interrupt Selector Registers	256K	019C 0000 – 019F FFFF
EDMA RAM and EDMA Registers	256K	01A0 0000 – 01A3 FFFF
Reserved	512K	01A4 0000 – 01AB FFFF
Timer 2 Registers	256K	01AC 0000 – 01AF FFFF
GP0 Registers	256K – 4K	01B0 0000 – 01B3 EFFF
Device Configuration Registers	4K	01B3 F000 – 01B3 FFFF
I2C0 Data and Control Registers	16K	01B4 0000 – 01B4 3FFF
Reserved	32K	01B4 4000 – 01B4 BFFF
McASP0 Control Registers	16K	01B4 C000 – 01B4 FFFF
Reserved	192K	01B5 0000 – 01B7 FFFF
Reserved	256K	01B8 0000 – 01BB FFFF
Emulation	256K	01BC 0000 – 01BF FFFF
PCI Registers	256K	01C0 0000 – 01C3 FFFF
VP0 Control	16K	01C4 0000 – 01C4 3FFF
VP1 Control	16K	01C4 4000 – 01C4 7FFF
VP2 Control	16K	01C4 8000 – 01C4 BFFF
VIC Control	16K	01C4 C000 – 01C4 FFFF
Reserved	192K	01C5 0000 – 01C7 FFFF
EMAC Control	4K	01C8 0000 – 01C8 0FFF
EMAC Wrapper	8K	01C8 1000 – 01C8 2FFF
EWRAP Registers	2K	01C8 3000 – 01C8 37FF
MDIO Control Registers	2K	01C8 3800 – 01C8 3FFF
Reserved	3.5M	01C8 4000 – 01FF FFFF
QDMA Registers	52	0200 0000 – 0200 0033
Reserved	928M – 52	0200 0034 – 2FFF FFFF
McBSP 0 Data	64M	3000 0000 – 33FF FFFF
McBSP 1 Data	64M	3400 0000 – 37FF FFFF
Reserved	64M	3800 0000 – 3BFF FFFF

McASP0 Data	1M	**3C00 0000 – 3C0F FFFF**
Reserved	64M – 1M	**3C10 0000 – 3FFF FFFF**
Reserved	832M	**4000 0000 – 73FF FFFF**
VP0 Channel A Data	32M	**7400 0000 – 75FF FFFF**
VP0 Channel B Data	32M	**7600 0000 – 77FF FFFF**
VP1 Channel A Data	32M	**7800 0000 – 79FF FFFF**
VP1 Channel B Data	32M	**7A00 0000 – 7BFF FFFF**
VP2 Channel A Data	32M	**7C00 0000 – 7DFF FFFF**
VP2 Channel B Data	32M	**7E00 0000 – 7FFF FFFF**
EMIFA CE0	256M	**8000 0000 – 8FFF FFFF**
EMIFA CE1	256M	**9000 0000 – 9FFF FFFF**
EMIFA CE2	256M	**A000 0000 – AFFF FFFF**
EMIFA CE3	256M	**B000 0000 – BFFF FFFF**
Reserved	1G	**C000 0000 – FFFF FFFF**

peripheral register descriptions

Table 3 through Table 27 identify the peripheral registers for the DM642 device by their register names, acronyms, and hex address or hex address range. For more detailed information on the register contents, bit names and their descriptions, see the *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190).

Table 3. EMIFA Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0180 0000	GBLCTL	EMIFA global control
0180 0004	CECTL1	EMIFA CE1 space control
0180 0008	CECTL0	EMIFA CE0 space control
0180 000C	–	Reserved
0180 0010	CECTL2	EMIFA CE2 space control
0180 0014	CECTL3	EMIFA CE3 space control
0180 0018	SDCTL	EMIFA SDRAM control
0180 001C	SDTIM	EMIFA SDRAM refresh control
0180 0020	SDEXT	EMIFA SDRAM extension
0180 0024 – 0180 0040	–	Reserved
0180 0044	CESEC1	EMIFA CE1 space secondary control
0180 0048	CESEC0	EMIFA CE0 space secondary control
0180 004C	–	Reserved
0180 0050	CESEC2	EMIFA CE2 space secondary control
0180 0054	CESEC3	EMIFA CE3 space secondary control
0180 0058 – 0183 FFFF	–	Reserved

peripheral register descriptions (continued)

Table 4. L2 Cache Registers (C64x)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0184 0000	CCFG	Cache configuration register	
	–	Reserved	
0184 2000	L2ALLOC0	L2 allocation register 0	
0184 2004	L2ALLOC1	L2 allocation register 1	
0184 2008	L2ALLOC2	L2 allocation register 2	
0184 200C	L2ALLOC3	L2 allocation register 3	
	–	Reserved	
0184 4000	L2FBAR	L2 flush base address register	
0184 4004	L2FWC	L2 flush word count register	
0184 4010	L2CBAR	L2 clean base address register	
0184 4014	L2CWC	L2 clean word count register	
0184 4020	L1PFBAR	L1P flush base address register	
0184 4024	L1PFWC	L1P flush word count register	
0184 4030	L1DFBAR	L1D flush base address register	
0184 4034	L1DFWC	L1D flush word count register	
	–	Reserved	
0184 5000	L2FLUSH	L2 flush register	
0184 5004	L2CLEAN	L2 clean register	
	–	Reserved	
0184 8000 –0184 81FC	MAR0 to MAR127	Reserved	
0184 8200	MAR128	Controls EMIFA CE0 range 8000 0000 – 80FF FFFF	
0184 8204	MAR129	Controls EMIFA CE0 range 8100 0000 – 81FF FFFF	
0184 8208	MAR130	Controls EMIFA CE0 range 8200 0000 – 82FF FFFF	
0184 820C	MAR131	Controls EMIFA CE0 range 8300 0000 – 83FF FFFF	
0184 8210	MAR132	Controls EMIFA CE0 range 8400 0000 – 84FF FFFF	
0184 8214	MAR133	Controls EMIFA CE0 range 8500 0000 – 85FF FFFF	
0184 8218	MAR134	Controls EMIFA CE0 range 8600 0000 – 86FF FFFF	
0184 821C	MAR135	Controls EMIFA CE0 range 8700 0000 – 87FF FFFF	
0184 8220	MAR136	Controls EMIFA CE0 range 8800 0000 – 88FF FFFF	
0184 8224	MAR137	Controls EMIFA CE0 range 8900 0000 – 89FF FFFF	
0184 8228	MAR138	Controls EMIFA CE0 range 8A00 0000 – 8AFF FFFF	
0184 822C	MAR139	Controls EMIFA CE0 range 8B00 0000 – 8BFF FFFF	
0184 8230	MAR140	Controls EMIFA CE0 range 8C00 0000 – 8CFF FFFF	
0184 8234	MAR141	Controls EMIFA CE0 range 8D00 0000 – 8DFF FFFF	
0184 8238	MAR142	Controls EMIFA CE0 range 8E00 0000 – 8EFF FFFF	
0184 823C	MAR143	Controls EMIFA CE0 range 8F00 0000 – 8FFF FFFF	
0184 8240	MAR144	Controls EMIFA CE1 range 9000 0000 – 90FF FFFF	
0184 8244	MAR145	Controls EMIFA CE1 range 9100 0000 – 91FF FFFF	
0184 8248	MAR146	Controls EMIFA CE1 range 9200 0000 – 92FF FFFF	

peripheral register descriptions (continued)

Table 4. L2 Cache Registers (C64x) (Continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0184 824C	MAR147	Controls EMIFA CE1 range 9300 0000 – 93FF FFFF	
0184 8250	MAR148	Controls EMIFA CE1 range 9400 0000 – 94FF FFFF	
0184 8254	MAR149	Controls EMIFA CE1 range 9500 0000 – 95FF FFFF	
0184 8258	MAR150	Controls EMIFA CE1 range 9600 0000 – 96FF FFFF	
0184 825C	MAR151	Controls EMIFA CE1 range 9700 0000 – 97FF FFFF	
0184 8260	MAR152	Controls EMIFA CE1 range 9800 0000 – 98FF FFFF	
0184 8264	MAR153	Controls EMIFA CE1 range 9900 0000 – 99FF FFFF	
0184 8268	MAR154	Controls EMIFA CE1 range 9A00 0000 – 9AFF FFFF	
0184 826C	MAR155	Controls EMIFA CE1 range 9B00 0000 – 9BFF FFFF	
0184 8270	MAR156	Controls EMIFA CE1 range 9C00 0000 – 9CFF FFFF	
0184 8274	MAR157	Controls EMIFA CE1 range 9D00 0000 – 9DFF FFFF	
0184 8278	MAR158	Controls EMIFA CE1 range 9E00 0000 – 9EFF FFFF	
0184 827C	MAR159	Controls EMIFA CE1 range 9F00 0000 – 9FFF FFFF	
0184 8280	MAR160	Controls EMIFA CE2 range A000 0000 – A0FF FFFF	
0184 8284	MAR161	Controls EMIFA CE2 range A100 0000 – A1FF FFFF	
0184 8288	MAR162	Controls EMIFA CE2 range A200 0000 – A2FF FFFF	
0184 828C	MAR163	Controls EMIFA CE2 range A300 0000 – A3FF FFFF	
0184 8290	MAR164	Controls EMIFA CE2 range A400 0000 – A4FF FFFF	
0184 8294	MAR165	Controls EMIFA CE2 range A500 0000 – A5FF FFFF	
0184 8298	MAR166	Controls EMIFA CE2 range A600 0000 – A6FF FFFF	
0184 829C	MAR167	Controls EMIFA CE2 range A700 0000 – A7FF FFFF	
0184 82A0	MAR168	Controls EMIFA CE2 range A800 0000 – A8FF FFFF	
0184 82A4	MAR169	Controls EMIFA CE2 range A900 0000 – A9FF FFFF	
0184 82A8	MAR170	Controls EMIFA CE2 range AA00 0000 – AAFF FFFF	
0184 82AC	MAR171	Controls EMIFA CE2 range AB00 0000 – ABFF FFFF	
0184 82B0	MAR172	Controls EMIFA CE2 range AC00 0000 – ACFF FFFF	
0184 82B4	MAR173	Controls EMIFA CE2 range AD00 0000 – ADFF FFFF	
0184 82B8	MAR174	Controls EMIFA CE2 range AE00 0000 – AEFF FFFF	
0184 82BC	MAR175	Controls EMIFA CE2 range AF00 0000 – AFFF FFFF	
0184 82C0	MAR176	Controls EMIFA CE3 range B000 0000 – B0FF FFFF	
0184 82C4	MAR177	Controls EMIFA CE3 range B100 0000 – B1FF FFFF	
0184 82C8	MAR178	Controls EMIFA CE3 range B200 0000 – B2FF FFFF	
0184 82CC	MAR179	Controls EMIFA CE3 range B300 0000 – B3FF FFFF	
0184 82D0	MAR180	Controls EMIFA CE3 range B400 0000 – B4FF FFFF	
0184 82D4	MAR181	Controls EMIFA CE3 range B500 0000 – B5FF FFFF	
0184 82D8	MAR182	Controls EMIFA CE3 range B600 0000 – B6FF FFFF	
0184 82DC	MAR183	Controls EMIFA CE3 range B700 0000 – B7FF FFFF	
0184 82E0	MAR184	Controls EMIFA CE3 range B800 0000 – B8FF FFFF	
0184 82E4	MAR185	Controls EMIFA CE3 range B900 0000 – B9FF FFFF	
0184 82E8	MAR186	Controls EMIFA CE3 range BA00 0000 – BAFF FFFF	
0184 82EC	MAR187	Controls EMIFA CE3 range BB00 0000 – BBFF FFFF	
0184 82F0	MAR188	Controls EMIFA CE3 range BC00 0000 – BCFF FFFF	

peripheral register descriptions (continued)

Table 4. L2 Cache Registers (C64x) (Continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0184 82F4	MAR189	Controls EMIFA CE3 range BD00 0000 – BDFF FFFF	
0184 82F8	MAR190	Controls EMIFA CE3 range BE00 0000 – BEFF FFFF	
0184 82FC	MAR191	Controls EMIFA CE3 range BF00 0000 – BFFF FFFF	
0184 8300 –0184 83FC	MAR192 to MAR255	Reserved	
0184 8400 –0187 FFFF	–	Reserved	

Table 5. Quick DMA (QDMA) and Pseudo Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0200 0000	QOPT	QDMA options parameter register
0200 0004	QSRC	QDMA source address register
0200 0008	QCNT	QDMA frame count register
0200 000C	QDST	QDMA destination address register
0200 0010	QIDX	QDMA index register
0200 0014 – 0200 001C		Reserved
0200 0020	QSOPT	QDMA pseudo options register
0200 0024	QSSRC	QDMA psuedo source address register
0200 0028	QSCNT	QDMA psuedo frame count register
0200 002C	QSDST	QDMA destination address register
0200 0030	QSIDX	QDMA psuedo index register

peripheral register descriptions (continued)

Table 6. EDMA Registers (C64x)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01A0 0800 – 01A0 FF98	–	Reserved
01A0 FF9C	EPRH	Event polarity high register
01A0 FFA4	CIPRH	Channel interrupt pending high register
01A0 FFA8	CIERH	Channel interrupt enable high register
01A0 FFAC	CCERH	Channel chain enable high register
01A0 FFB0	ERH	Event high register
01A0 FFB4	EERH	Event enable high register
01A0 FFB8	ECRH	Event clear high register
01A0 FFBC	ESRH	Event set high register
01A0 FFC0	PQAR0	Priority queue allocation register 0
01A0 FFC4	PQAR1	Priority queue allocation register 1
01A0 FFC8	PQAR2	Priority queue allocation register 2
01A0 FFCC	PQAR3	Priority queue allocation register 3
01A0 FFDC	EPRL	Event polarity low register
01A0 FFE0	PQSR	Priority queue status register
01A0 FFE4	CIPRL	Channel interrupt pending low register
01A0 FFE8	CIERL	Channel interrupt enable low register
01A0 FFEC	CCERL	Channel chain enable low register
01A0 FFF0	ERL	Event low register
01A0 FFF4	EERL	Event enable low register
01A0 FFF8	ECRL	Event clear low register
01A0 FFFC	ESRL	Event set low register
01A1 0000 – 01A3 FFFF	–	Reserved

peripheral register descriptions (continued)

Table 7. EDMA Parameter RAM (C64x)†

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
01A0 0000 – 01A0 0017	–	Parameters for Event 0 (6 words)	Parameters for Event 0 (6 words) or Reload/Link Parameters for other Event
01A0 0018 – 01A0 002F	–	Parameters for Event 1 (6 words)	
01A0 0030 – 01A0 0047	–	Parameters for Event 2 (6 words)	
01A0 0048 – 01A0 005F	–	Parameters for Event 3 (6 words)	
01A0 0060 – 01A0 0077	–	Parameters for Event 4 (6 words)	
01A0 0078 – 01A0 008F	–	Parameters for Event 5 (6 words)	
01A0 0090 – 01A0 00A7	–	Parameters for Event 6 (6 words)	
01A0 00A8 – 01A0 00BF	–	Parameters for Event 7 (6 words)	
01A0 00C0 – 01A0 00D7	–	Parameters for Event 8 (6 words)	
01A0 00D8 – 01A0 00EF	–	Parameters for Event 9 (6 words)	
01A0 00F0 – 01A0 00107	–	Parameters for Event 10 (6 words)	
01A0 0108 – 01A0 011F	–	Parameters for Event 11 (6 words)	
01A0 0120 – 01A0 0137	–	Parameters for Event 12 (6 words)	
01A0 0138 – 01A0 014F	–	Parameters for Event 13 (6 words)	
01A0 0150 – 01A0 0167	–	Parameters for Event 14 (6 words)	
01A0 0168 – 01A0 017F	–	Parameters for Event 15 (6 words)	
01A0 0150 – 01A0 0167	–	Parameters for Event 16 (6 words)	
01A0 0168 – 01A0 017F	–	Parameters for Event 17 (6 words)	
...		...	
01A0 05D0 – 01A0 05E7	–	Parameters for Event 62 (6 words)	
01A0 05E8 – 01A0 05FF	–	Parameters for Event 63 (6 words)	
01A0 0600 – 01A0 0617	–	Reload/link parameters for Event 0 (6 words)	Reload/Link Parameters for other Event 0–15
01A0 0618 – 01A0 062F	–	Reload/link parameters for Event 1 (6 words)	
...		...	
01A0 07E0 – 01A0 07F7	–	Reload/link parameters for Event 20 (6 words)	
01A0 07F8 – 01A0 07FF	–	Reload/link parameters for Event 21 (6 words)	
01A0 0800 – 01A0 0817	–	Reload/link parameters for Event 22 (6 words)	
...		...	
01A0 13C8 – 01A0 13DF	–	Reload/link parameters for Event 147 (6 words)	
01A0 13E0 – 01A0 13F7	–	Reload/link parameters for Event 148 (6 words)	
01A0 13F8 – 01A0 13FF	–	Scratch pad area (2 words)	
01A0 1400 – 01A3 FFFF	–	Reserved	

† The DM64x device has 213 EDMA parameters total: 64-Event/Reload channels and 149-Reload only parameter sets [six (6) words each] that can be used to reload/link EDMA transfers.

peripheral register descriptions (continued)

Table 8. Interrupt Selector Registers (C64x)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
019C 0000	MUXH	Interrupt multiplexer high	Selects which interrupts drive CPU interrupts 10–15 (INT10–INT15)
019C 0004	MUXL	Interrupt multiplexer low	Selects which interrupts drive CPU interrupts 4–9 (INT04–INT09)
019C 0008	EXTPOL	External interrupt polarity	Sets the polarity of the external interrupts (EXT_INT4–EXT_INT7)
019C 000C – 019C 01FF	–	Reserved	
019C 0200	PDCTL	Peripheral power-down control register (see Table 9)	
019C 0204 – 019F FFFF	–	Reserved	

Table 9. Peripheral Power-Down Control Register

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
019C 0200	PDCTL	Peripheral power-down control register

peripheral register descriptions (continued)

Table 10. Ethernet MAC (EMAC) Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01C4 C000	TX_IdVer	Transmit (TX) identification and version register
01C4 C004	Tx_Control	TX control register
01C4 C008	Tx_Teardown	TX teardown register
01C4 C00C		
01C4 C010	RX_IdVer	Receive (RX) identification and version register
01C4 C014	Rx_Control	RX control register
01C4 C018	Rx_Teardown	RX teardown register
01C4 C01C		
01C4 C020 – 01C4 FFFF	–	
01C4 C00C – 01C4 FFFF	–	Reserved
01C4 C00C – 01C4 FFFF	–	Reserved

Table 11. Device Configuration Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
01B3 F000	PERCFG	Peripheral Configuration Register	Enables or disables specific peripherals. This register is also used for power-down of disabled peripherals.
01B3 F004	DEVSTAT	Device Status Register	Read-only. Provides status of the User's device configuration on reset.
01B3 F008	JTAGID	JTAG Identification Register	Read-only. Provides 32-bit JTAG ID of the device.
01B3 F00C	–	Reserved	
01B3 F010	–	Reserved	
01B3 F014 – 01B3 FFFF	–	Reserved	

peripheral register descriptions (continued)

Table 12. McBSP 0 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
018C 0000	DRR0	McBSP0 data receive register via Configuration Bus	The CPU and EDMA controller can only read this register; they cannot write to it.
0x3000 0000 – 0x33FF FFFF	DRR0	McBSP0 data receive register via Peripheral Bus	
018C 0004	DXR0	McBSP0 data transmit register via Configuration Bus	
0x3000 0000 – 0x33FF FFFF	DXR0	McBSP0 data transmit register via Peripheral Bus	
018C 0008	SPCR0	McBSP0 serial port control register	
018C 000C	RCR0	McBSP0 receive control register	
018C 0010	XCR0	McBSP0 transmit control register	
018C 0014	SRGR0	McBSP0 sample rate generator register	
018C 0018	MCR0	McBSP0 multichannel control register	
018C 001C	RCERE00	McBSP0 enhanced receive channel enable register 0	
018C 0020	XCERE00	McBSP0 enhanced transmit channel enable register 0	
018C 0024	PCR0	McBSP0 pin control register	
018C 0028	RCERE10	McBSP0 enhanced receive channel enable register 1	
018C 002C	XCERE10	McBSP0 enhanced transmit channel enable register 1	
018C 0030	RCERE20	McBSP0 enhanced receive channel enable register 2	
018C 0034	XCERE20	McBSP0 enhanced transmit channel enable register 2	
018C 0038	RCERE30	McBSP0 enhanced receive channel enable register 3	
018C 003C	XCERE30	McBSP0 enhanced transmit channel enable register 3	
018C 0040 – 018F FFFF	–	Reserved	

peripheral register descriptions (continued)

Table 13. McBSP 1 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0190 0000	DRR1	McBSP1 data receive register via Configuration Bus	The CPU and EDMA controller can only read this register; they cannot write to it.
0x3400 0000 – 0x37FF FFFF	DRR1	McBSP1 data receive register via Peripheral Bus	
0190 0004	DXR1	McBSP1 data transmit register via Configuration Bus	
0x3400 0000 – 0x37FF FFFF	DXR1	McBSP1 data transmit register via Peripheral Bus	
0190 0008	SPCR1	McBSP1 serial port control register	
0190 000C	RCR1	McBSP1 receive control register	
0190 0010	XCR1	McBSP1 transmit control register	
0190 0014	SRGR1	McBSP1 sample rate generator register	
0190 0018	MCR1	McBSP1 multichannel control register	
0190 001C	RCERE01	McBSP1 enhanced receive channel enable register 0	
0190 0020	XCERE01	McBSP1 enhanced transmit channel enable register 0	
0190 0024	PCR1	McBSP1 pin control register	
0190 0028	RCERE11	McBSP1 enhanced receive channel enable register 1	
0190 002C	XCERE11	McBSP1 enhanced transmit channel enable register 1	
0190 0030	RCERE21	McBSP1 enhanced receive channel enable register 2	
0190 0034	XCERE21	McBSP1 enhanced transmit channel enable register 2	
0190 0038	RCERE31	McBSP1 enhanced receive channel enable register 3	
0190 003C	XCERE31	McBSP1 enhanced transmit channel enable register 3	
0190 0040 – 0193 FFFF	–	Reserved	

peripheral register descriptions (continued)

Table 14. Timer 0 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0194 0000	CTL0	Timer 0 control register	Determines the operating mode of the timer, monitors the timer status, and controls the function of the TOUT pin.
0194 0004	PRD0	Timer 0 period register	Contains the number of timer input clock cycles to count. This number controls the TSTAT signal frequency.
0194 0008	CNT0	Timer 0 counter register	Contains the current value of the incrementing counter.
0194 000C – 0197 FFFF	–	Reserved	

Table 15. Timer 1 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0198 0000	CTL1	Timer 1 control register	Determines the operating mode of the timer, monitors the timer status, and controls the function of the TOUT pin.
0198 0004	PRD1	Timer 1 period register	Contains the number of timer input clock cycles to count. This number controls the TSTAT signal frequency.
0198 0008	CNT1	Timer 1 counter register	Contains the current value of the incrementing counter.
0198 000C – 019B FFFF	–	Reserved	

Table 16. Timer 2 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
01AC 0000	CTL2	Timer 2 control register	Determines the operating mode of the timer, monitors the timer status.
01AC 0004	PRD2	Timer 2 period register	Contains the number of timer input clock cycles to count. This number controls the TSTAT signal frequency.
01AC 0008	CNT2	Timer 2 counter register	Contains the current value of the incrementing counter.
01AC 000C – 01AF FFFF	–	Reserved	

peripheral register descriptions (continued)

Table 17. HPI Registers (C64x)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
–	HPID	HPI data register	Host read/write access only
0188 0000	HPIC	HPI control register	HPIC has both Host/CPU read/write access
0188 0004	HPIA (HPIAW)†	HPI address register (Write)	HPIA has both Host/CPU read/write access
0188 0008	HPIA (HPIAR)†	HPI address register (Read)	
0188 0001 – 018B FFFF	–	Reserved	

† Host access to the HPIA register updates both the HPIAW and HPIAR registers. The CPU can access HPIAW and HPIAR independently.

Table 18. GP0 Registers (C64x)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01B0 0000	GPEN	GP0 enable register
01B0 0004	GPDIR	GP0 direction register
01B0 0008	GPVAL	GP0 value register
01B0 000C	–	Reserved
01B0 0010	GPDH	GP0 delta high register
01B0 0014	GPHM	GP0 high mask register
01B0 0018	GPDL	GP0 delta low register
01B0 001C	GPLM	GP0 low mask register
01B0 0020	GPGC	GP0 global control register
01B0 0024	GPPOL	GP0 interrupt polarity register
01B0 0028 – 01B3 EFFF	–	Reserved

peripheral register descriptions (continued)

Table 19. PCI Peripheral Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01C0 0000	RSTSRC	DSP Reset source/status register
01C0 0004	PMDCSR	Power management DSP control/status register
01C0 0008	PCIIS	PCI interrupt source register
01C0 000C	PCIIEN	PCI interrupt enable register
01C0 0010	DSPMA	DSP master address register
01C0 0014	PCIMA	PCI master address register
01C0 0018	PCIMC	PCI master control register
01C0 001C	CDSPA	Current DSP address register
01C0 0020	CPCIA	Current PCI address register
01C0 0024	CCNT	Current byte count register
01C0 0028	–	Reserved
01C0 002C – 01C1 FFEF	–	Reserved
0x01C1 FFF0	HSR	Host status register
0x01C1 FFF4	HDCR	Host-to-DSP control register
0x01C1 FFF8	DSPP	DSP page register
0x01C1 FFFC	–	Reserved
01C2 0000	EEADD	EEPROM address register
01C2 0004	EEDAT	EEPROM data register
01C2 0008	EECTL	EEPROM control register
01C2 000C – 01C2 FFFF	–	Reserved
01C3 0000	PCI_TRCNTL	PCI transfer request control register
01C3 0004 – 01C3 FFFF	–	Reserved
TBD	PID	Peripheral device identification register — Register value TBD

Table 20. VXCO Interpolated Control Port (VIC) Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01C8 C000	VIC_CTL	VIC control register
01C8 C004	VIC_IN	VIC input register
01C8 C008	VP_DIV	VIC clock divider register
01C4 C00C – 01C4 FFFF	–	Reserved

peripheral register descriptions (continued)

Table 21. MDIO Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01C8 3800		
01C8 3804		
01C8 3808		
01C8 380C		
01C8 3810 – 01C8 3FFF	–	Reserved

Table 22. Video Port 2 (VP2) Control Registers TBD

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01C4 8000	VP_CTL	VP2 control register
01C4 8004	VP_STAT	VP2 status register
01C4 8008	VP_IE	VP2 interrupt enable register
01C4 800C	VP_IS	VP2 interrupt status register
01C4 8010		
01C4 8014		
TBD – 01C4 BFFF	–	Reserved

Table 23. Video Port 1 (VP1) Control Registers TBD

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01C4 4000	VP_CTL	VP1 control register
01C4 4004	VP_STAT	VP1 status register
01C4 4008	VP_IE	VP1 interrupt enable register
01C4 400C	VP_IS	VP1 interrupt status register
01C4 4010		
01C4 4014		
TBD – 01C4 7FFF	–	Reserved

Table 24. Video Port 0 (VP0) Control Registers TBD

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01C4 0000	VP_CTL	VP0 control register
01C4 0004	VP_STAT	VP0 status register
01C4 0008	VP_IE	VP0 interrupt enable register
01C4 000C	VP_IS	VP0 interrupt status register
01C4 8010		
01C4 8014		
TBD – 01C4 3FFF	–	Reserved

peripheral register descriptions (continued)

Table 25. McASP0 Registers – TBD Need to Split Control and Data

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01B4 C000	PID	Peripheral Identification register [Register value: TBD]
01B4 C004	PWRDEMU	Power down and emulation management register
01B4 C008	–	Reserved
01B4 C00C	–	Reserved
01B4 C010	PFUNC	Pin function register
01B4 C014	PDIR	Pin direction register
01B4 C018	PDOUT	Pin data out register
01B4 C01C	PDIN/PDSET	Pin data in / data set register Read returns: PDIN Writes affect: PDSET
01B4 C020	PDCLR	Pin data clear register
01B4 C024 – 01B4 C040	–	Reserved
01B4 C044	GBLCTL	Global control register
01B4 C048	AMUTE	Mute control register
01B4 C04C	DLBCTL	Digital Loop-back control register
01B4 C050	DITCTL	DIT mode control register
01B4 C054 – 01B4 C05C	–	Reserved
01B4 C060	RGBLCTL	Alias of GBLCTL containing only Receiver Reset bits, allows transmit to be reset independently from receive.
01B4 C064	RMASK	Receiver format unit bit mask register
01B4 C068	RFMT	Receive bit stream format register
01B4 C06C	AFSRCTL	Receive frame sync control register
01B4 C070	ACLKRCTL	Receive clock control register
01B4 C074	AHCLKRCTL	High-frequency receive clock control register
01B4 C078	RTDM	Receive TDM slot 0–31 register
01B4 C07C	RINTCTL	Receiver interrupt control register
01B4 C080	RSTAT	Status register – Receiver
01B4 C084	RSLOT	Current receive TDM slot register
01B4 C088	RCLKCHK	Receiver clock check control register
01B4 C08C – 01B4 C09C	–	Reserved
01B4 C0A0	XGBLCTL	Alias of GBLCTL containing only Transmitter Reset bits, allows transmit to be reset independently from receive.
01B4 C0A4	XMASK	Transmit format unit bit mask register
01B4 C0A8	XFMT	Transmit bit stream format register
01B4 C0AC	AFSXCTL	Transmit frame sync control register
01B4 C0B0	ACLKXCTL	Transmit clock control register
01B4 C0B4	AHCLKXCTL	High-frequency Transmit clock control register
01B4 C0B8	XTDM	Transmit TDM slot 0–31 register
01B4 C0BC	XINTCTL	Transmit interrupt control register
01B4 C0C0	XSTAT	Status register – Transmitter
01B4 C0C4	XSLOT	Current transmit TDM slot
01B4 C0C8	XCLKCHK	Transmit clock check control register

peripheral register descriptions (continued)

Table 25. McASP0 Registers (Continued)– TBD Need to Split Control and Data

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01B4 C0CC	XEVTCTL	Tranmitter DMA control register
01B4 C0D0 – 01B4 C0FC	–	Reserved
01B4 C100	DITCSRA0	Left (even TDM slot) channel status register file
01B4 C104	DITCSRA1	Left (even TDM slot) channel status register file
01B4 C108	DITCSRA2	Left (even TDM slot) channel status register file
01B4 C10C	DITCSRA3	Left (even TDM slot) channel status register file
01B4 C110	DITCSRA4	Left (even TDM slot) channel status register file
01B4 C114	DITCSRA5	Left (even TDM slot) channel status register file
01B4 C118	DITCSRB0	Right (odd TDM slot) channel status register file
01B4 C11C	DITCSRB1	Right (odd TDM slot) channel status register file
01B4 C120	DITCSRB2	Right (odd TDM slot) channel status register file
01B4 C124	DITCSRB3	Right (odd TDM slot) channel status register file
01B4 C128	DITCSRB4	Right (odd TDM slot) channel status register file
01B4 C12C	DITCSRB5	Right (odd TDM slot) channel status register file
01B4 C130	DITUDRA0	Left (even TDM slot) user data register file
01B4 C134	DITUDRA1	Left (even TDM slot) user data register file
01B4 C138	DITUDRA2	Left (even TDM slot) user data register file
01B4 C13C	DITUDRA3	Left (even TDM slot) user data register file
01B4 C140	DITUDRA4	Left (even TDM slot) user data register file
01B4 C144	DITUDRA5	Left (even TDM slot) user data register file
01B4 C148	DITUDRB0	Right (odd TDM slot) user data register file
01B4 C14C	DITUDRB1	Right (odd TDM slot) user data register file
01B4 C150	DITUDRB2	Right (odd TDM slot) user data register file
01B4 C154	DITUDRB3	Right (odd TDM slot) user data register file
01B4 C158	DITUDRB4	Right (odd TDM slot) user data register file
01B4 C15C	DITUDRB5	Right (odd TDM slot) user data register file
01B4 C160 – 01B4 C17C	–	Reserved
01B4 C180	SRCTL0	Serializer 0 control register
01B4 C184	SRCTL1	Serializer 1 control register
01B4 C188	SRCTL2	Serializer 2 control register
01B4 C18C	SRCTL3	Serializer 3 control register
01B4 C190	SRCTL4	Serializer 4 control register
01B4 C194	SRCTL5	Serializer 5 control register
01B4 C198	SRCTL6	Serializer 6 control register
01B4 C19C	SRCTL7	Serializer 7 control register
01B4 C1A0 – 01B4 C1FC	–	Reserved
01B4 C200	XBUF0	Transmit Buffer for Serializer 0
01B4 C204	XBUF1	Transmit Buffer for Serializer 1
01B4 C208	XBUF2	Transmit Buffer for Serializer 2
01B4 C20C	XBUF3	Transmit Buffer for Serializer 3
01B4 C210	XBUF4	Transmit Buffer for Serializer 4
01B4 C214	XBUF5	Transmit Buffer for Serializer 5

peripheral register descriptions (continued)

Table 25. McASP0 Registers (Continued)– TBD Need to Split Control and Data

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01B4 C218	XBUF6	Transmit Buffer for Serializer 6
01B4 C21C	XBUF7	Transmit Buffer for Serializer 7
01B4 C220 – 01B4 C27C	–	Reserved
01B4 C280	RBUF0	Receive Buffer for Serializer 0
01B4 C284	RBUF1	Receive Buffer for Serializer 1
01B4 C288	RBUF2	Receive Buffer for Serializer 2
01B4 C28C	RBUF3	Receive Buffer for Serializer 3
01B4 C290	RBUF4	Receive Buffer for Serializer 4
01B4 C294	RBUF5	Receive Buffer for Serializer 5
01B4 C298	RBUF6	Receive Buffer for Serializer 6
01B4 C29C	RBUF7	Receive Buffer for Serializer 7
01B4 C2A0 – 01B4 FFFF	–	Reserved

Table 26. McASP0 Data Registers TBD

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
3C00 0000		register
3C00 0004		
3C00 0008		
3C00 000C – 3C0F FFFF		

Table 27. I2C0 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
01B4 0000	I2COAR0	I2C0 own address register
01B4 0004	I2CIER0	I2C0 interrupt enable register
01B4 0008	I2CSTR0	I2C0 interrupt status register
01B4 000C	I2CCLKL0	I2C0 clock low-time divider register
01B4 0010	I2CCLKH0	I2C0 clock high-time divider register
01B4 0014	I2CCNT0	I2C0 data count register
01B4 0018	I2CDRR0	I2C0 data receive register
01B4 001C	I2CSAR0	I2C0 slave address register
01B4 0020	I2CDXR0	I2C0 data transmit register
01B4 0024	I2CMDR0	I2C0 mode register
01B4 0028	I2CISRC0	I2C0 interrupt source register
01B4 002C	–	Reserved
01B4 0030	I2CPSC0	I2C0 prescaler register
01B4 0034	I2CPID10	I2C0 Peripheral Identification register 1 [DA610 value: 0x0000 0101]
01B4 0038	I2CPID20	I2C0 Peripheral Identification register 2 [DA610 value: 0x0000 0005]
01B4 003C – 01B4 3FFF	–	Reserved

EDMA channel synchronization events

The C64x EDMA supports up to 64 EDMA channels which service peripheral devices and external memory. Table 28 lists the source of C64x EDMA synchronization events associated with each of the programmable EDMA channels. For the DM642 device, the association of an event to a channel is fixed; each of the EDMA channels has one specific event associated with it. These specific events are captured in the EDMA event registers (ERL, ERH) even if the events are disabled by the EDMA event enable registers (EERL, EERH). The priority of each event can be specified independently in the transfer parameters stored in the EDMA parameter RAM. For more detailed information on the EDMA module and how EDMA events are enabled, captured, processed, linked, chained, and cleared, etc., see the EDMA Controller chapter of the *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190).

Table 28. TMS320DM642 EDMA Channel Synchronization Events† – TBD

EDMA CHANNEL	EVENT NAME	EVENT DESCRIPTION
0	DSP_INT	HPI/PCI-to-DSP interrupt
1	TINT0	Timer 0 interrupt
2	TINT1	Timer 1 interrupt
3	SD_INTA	EMIFA SDRAM timer interrupt
4	GPINT4/EXT_INT4	GP0 event 4/External interrupt pin 4
5	GPINT5/EXT_INT5	GP0 event 5/External interrupt pin 5
6	GPINT6/EXT_INT6	GP0 event 6/External interrupt pin 6
7	GPINT7/EXT_INT7	GP0 event 7/External interrupt pin 7
8	GPINT0	GP0 event 0
9	GPINT1	GP0 event 1
10	GPINT2	GP0 event 2
11	GPINT3	GP0 event 3
12	XEVT0	McBSP0 transmit event
13	REVT0	McBSP0 receive event
14	XEVT1	McBSP1 transmit event
15	REVT1	McBSP1 receive event
16	VP0EVTYA	VP0 Channel A Y event DMA request
17	VP0EVTUA	VP0 Channel A Cb event DMA request
18	VP0EVTVA	VP0 Channel A Cr event DMA request
19	TINT2	Timer 2 interrupt
20–23	–	None
24	VP0EVTYB	VP0 Channel B Y event DMA request
25	VP0EVTUB	VP0 Channel B Cb event DMA request
26	VP0EVTVB	VP0 Channel B Cr event DMA request
27–31	–	None
32	AXEVTE0	McASP0 transmit event —TBD
33	AXEVTO0	McASP0 tranmit event —TBD
34	AXEVT0	McASP0 tranmit event —TBD
35	AREVTE0	McASP0 receive event —TBD
36	AREVTO0	McASP0 receive event —TBD
37	AREVT0	McASP0 receive event —TBD
38	VP1EVTYB	VP1 event YB —TBD
39	VP1EVTUB	VP1 event UB —TBD
40	VP1EVTVB	VP1 event VB —TBD
41	VP2EVTYB	VP2 event YB —TBD
42	VP2EVTUB	VP2 event UB —TBD
43	VP2EVTVB	VP2 event VB —TBD
44	ICREVT0	I2C0 receive event —TBD
45	ICXEVT0	I2C0 tranmit event —TBD

46–47	–	None
48	GPINT8	GP0 event 8
49	GPINT9	GP0 event 9
50	GPINT10	GP0 event 10
51	GPINT11	GP0 event 11
52	GPINT12	GP0 event 12
53	GPINT13	GP0 event 13
54	GPINT14	GP0 event 14
55	GPINT15	GP0 event 15
56	VP1EVTYA	VP1 event YA —TBD
57	VP1EVTUA	VP1 event UA —TBD
58	VP1EVTVA	VP1 event VA —TBD
59	VP2EVTYA	VP2 event YA —TBD
60	VP2EVTUA	VP2 event UA —TBD
61	VP2EVTVA	VP2 event VA —TBD
62–63	–	None

† In addition to the events shown in this table, each of the 64 channels can also be synchronized with the transfer completion or alternate transfer completion events. For more detailed information on EDMA event-transfer chaining, see the EDMA Controller chapter of the *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190).

interrupt sources and interrupt selector

The C64x DSP core supports 16 prioritized interrupts, which are listed in Table 29. The highest-priority interrupt is INT_00 (dedicated to RESET) while the lowest-priority interrupt is INT_15. The first four interrupts (INT_00–INT_03) are non-maskable and fixed. The remaining interrupts (INT_04–INT_15) are maskable and default to the interrupt source specified in Table 29. The interrupt source for interrupts 4–15 can be programmed by modifying the selector value (binary value) in the corresponding fields of the Interrupt Selector Control registers: MUXH (address 0x019C0000) and MUXL (address 0x019C0004).

interrupt sources and interrupt selector (continued)

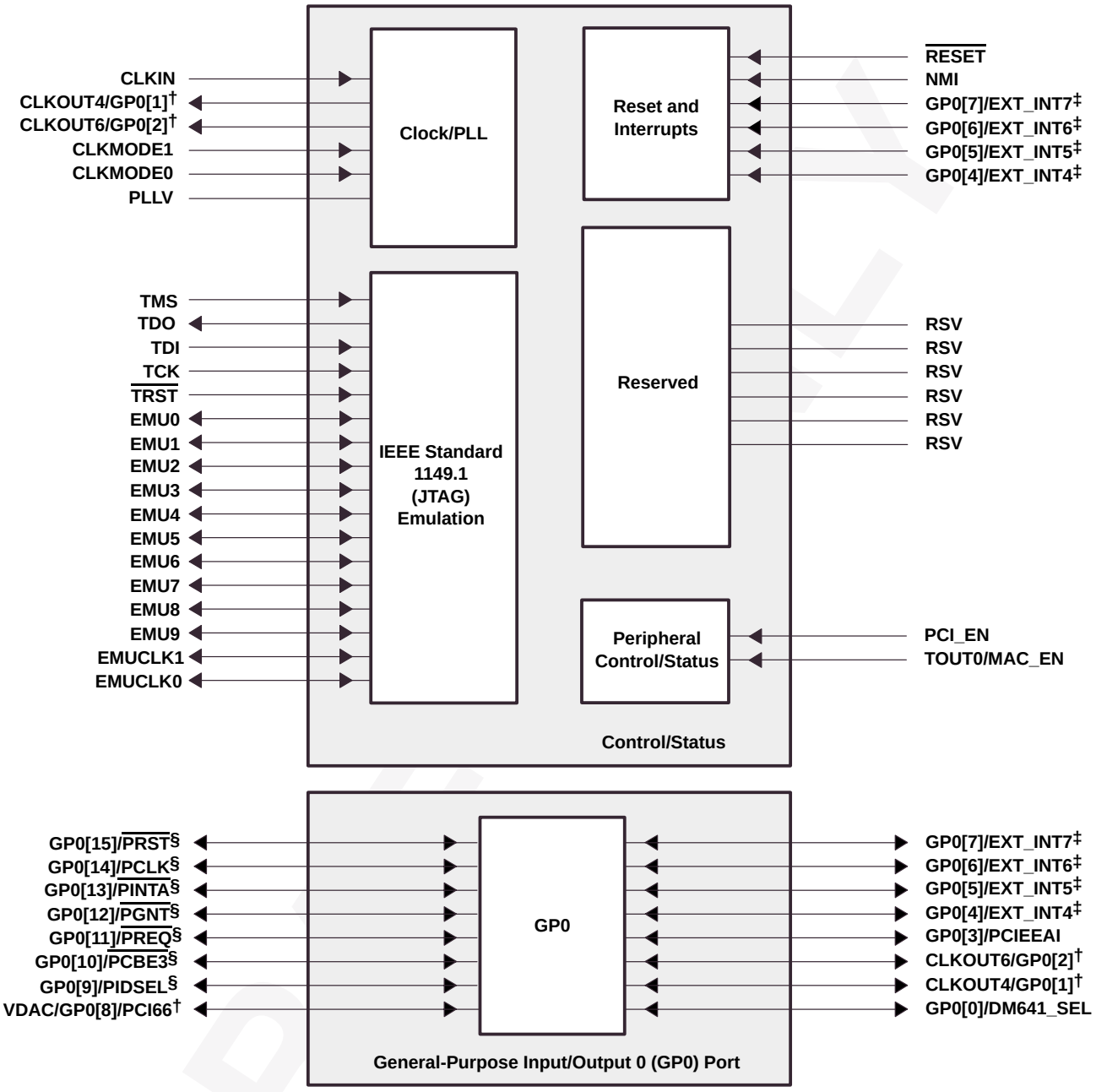
Table 29. DM642 DSP Interrupts – TBD

CPU INTERRUPT NUMBER	INTERRUPT SELECTOR CONTROL REGISTER	SELECTOR VALUE (BINARY)	INTERRUPT EVENT	INTERRUPT SOURCE
INT_00†	–	–	RESET	
INT_01†	–	–	NMI	
INT_02†	–	–	Reserved	Reserved. Do not use.
INT_03†	–	–	Reserved	Reserved. Do not use.
INT_04‡	MUXL[4:0]	00100	GPINT4/EXT_INT4	GP0 interrupt 4/External interrupt pin 4
INT_05‡	MUXL[9:5]	00101	GPINT5/EXT_INT5	GP0 interrupt 5/External interrupt pin 5
INT_06‡	MUXL[14:10]	00110	GPINT6/EXT_INT6	GP0 interrupt 6/External interrupt pin 6
INT_07‡	MUXL[20:16]	00111	GPINT7/EXT_INT7	GP0 interrupt 7/External interrupt pin 7
INT_08‡	MUXL[25:21]	01000	EDMA_INT	EDMA channel (0 through 63) interrupt
INT_09‡	MUXL[30:26]	01001	EMU_DTDMA	EMU DTDMA
INT_10‡	MUXH[4:0]	00011	SD_INTA	EMIFA SDRAM timer interrupt
INT_11‡	MUXH[9:5]	01010	EMU_RTDXRX	EMU real-time data exchange (RTDX) receive
INT_12‡	MUXH[14:10]	01011	EMU_RTDXTX	EMU RTDX transmit
INT_13‡	MUXH[20:16]	00000	DSP_INT	HPI/PCI-to-DSP interrupt
INT_14‡	MUXH[25:21]	00001	TINT0	Timer 0 interrupt
INT_15‡	MUXH[30:26]	00010	TINT1	Timer 1 interrupt
–	–	01100	XINT0	McBSP0 transmit interrupt
–	–	01101	RINT0	McBSP0 receive interrupt
–	–	01110	XINT1	McBSP1 transmit interrupt
–	–	01111	RINT1	McBSP1 receive interrupt
–	–	10000	GPINT0	GP0 interrupt 0
–	–	10001	Reserved	Reserved. Do not use.
–	–	10010	Reserved	Reserved. Do not use.
–	–	10011	TINT2	Timer 2 interrupt
–	–	10100	Reserved	Reserved. Do not use.
–	–	10101	Reserved	Reserved. Do not use.
–	–	10110	ICINT0	I2C0 interrupt — TBD.
–	–	10111	Reserved	Reserved. Do not use.
–	–	11000	EMAC_MDIO_INT	EMAC/MDIO interrupt — TBD.
–	–	11001	VPINT0	VP0 interrupt — TBD.
–	–	11010	VPINT1	VP1 interrupt — TBD.
–	–	11011	VPINT2	VP2 interrupt — TBD.
–	–	11100	AXINT0	McASP0 transmit interrupt — TBD.
–	–	11101	ARINT0	McASP0 receive interrupt — TBD.
–	–	11110 – 11111	Reserved	Reserved. Do not use.

† Interrupts INT_00 through INT_03 are non-maskable and fixed.

‡ Interrupts INT_04 through INT_15 are programmable by modifying the binary selector values in the Interrupt Selector Control registers fields. Table 29 shows the default interrupt sources for Interrupts INT_04 through INT_15. For more detailed information on interrupt sources and selection, see the Interrupt Selector and External Interrupts chapter of the *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190). **TBD**

signal groups description



† These pins are muxed with the GP0 pins and by default these signals function as clocks (CLKOUT4 or CLKOUT6). To use these muxed pins as GPIO signals, the appropriate GPIO register bits (GPxEN and GPxDIR) must be properly enabled and configured. For more details, see the Device Configurations section of this data sheet.

‡ These pins are GP0 pins that can also function as external interrupt sources (EXT_INT[7:4]). Default after reset is EXT_INTx or GPIO as input-only.

§ These GP0 pins are muxed with the PCI peripheral pins and by default these signals are set up to no function with both the GPIO and PCI pin functions *disabled*. For more details on these muxed pins, see the Device Configurations section of this data sheet.

Figure 2. CPU and Peripheral Signals

signal groups description (continued)

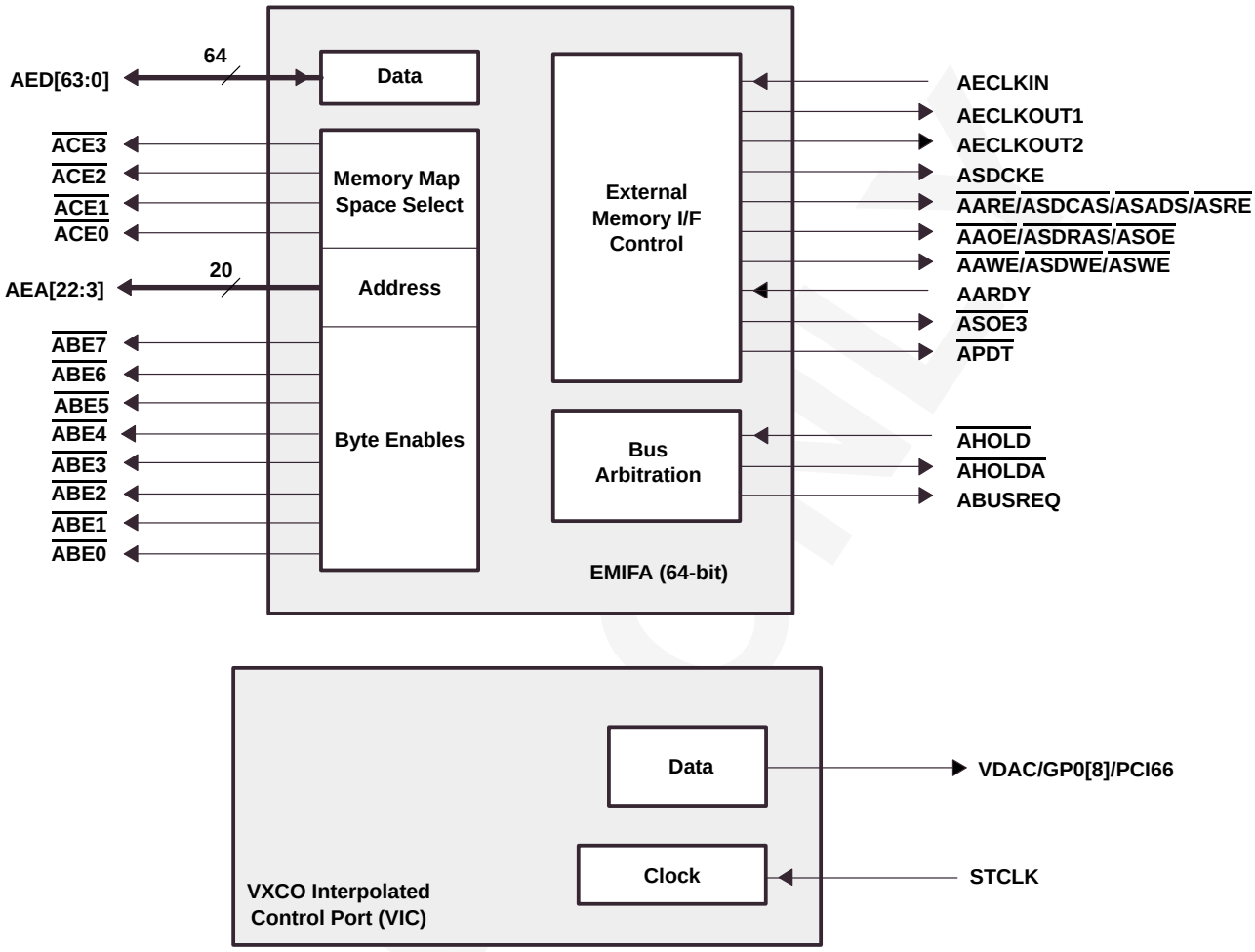
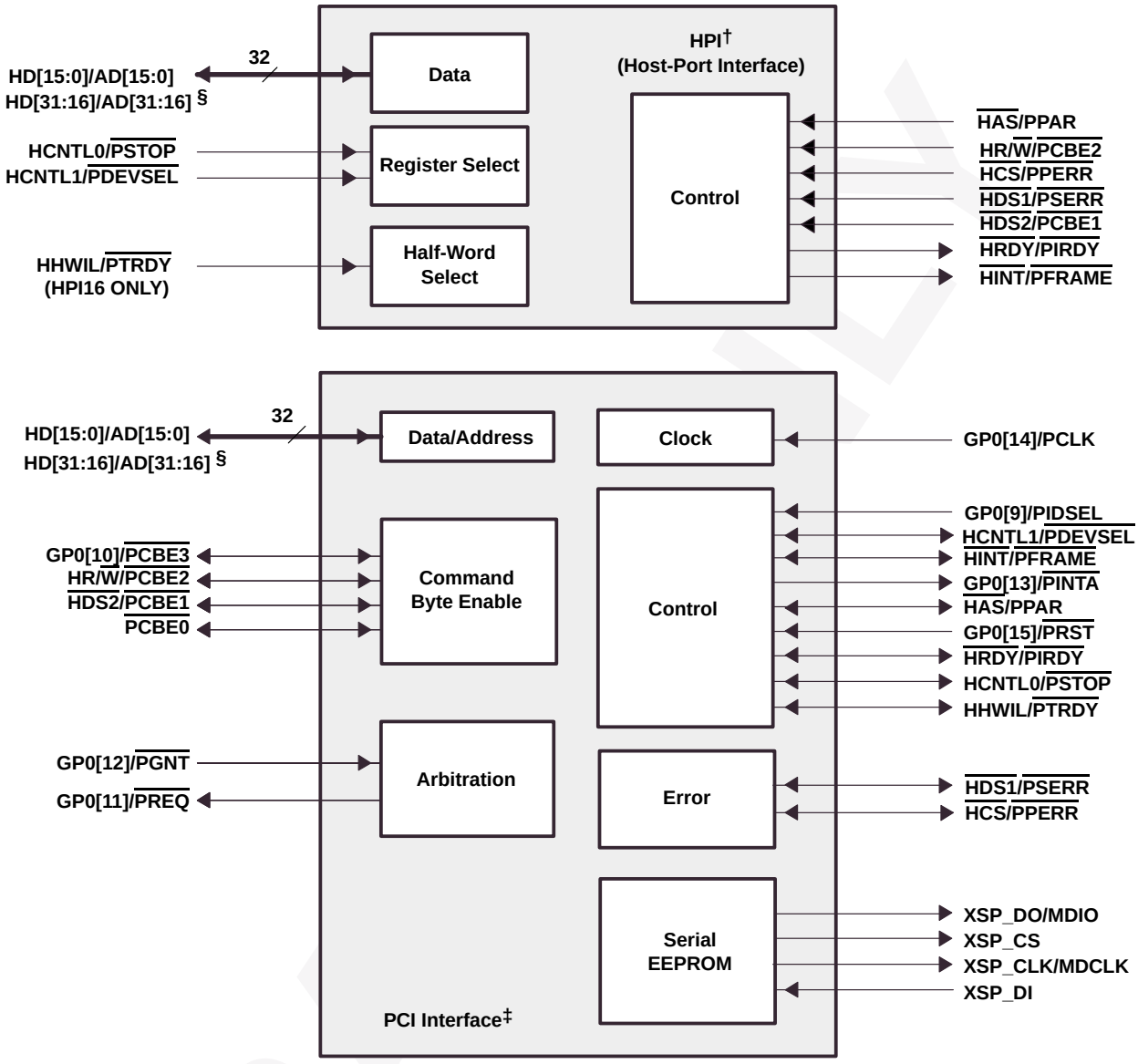


Figure 3. Peripheral Signals

PRODUCT PREVIEW

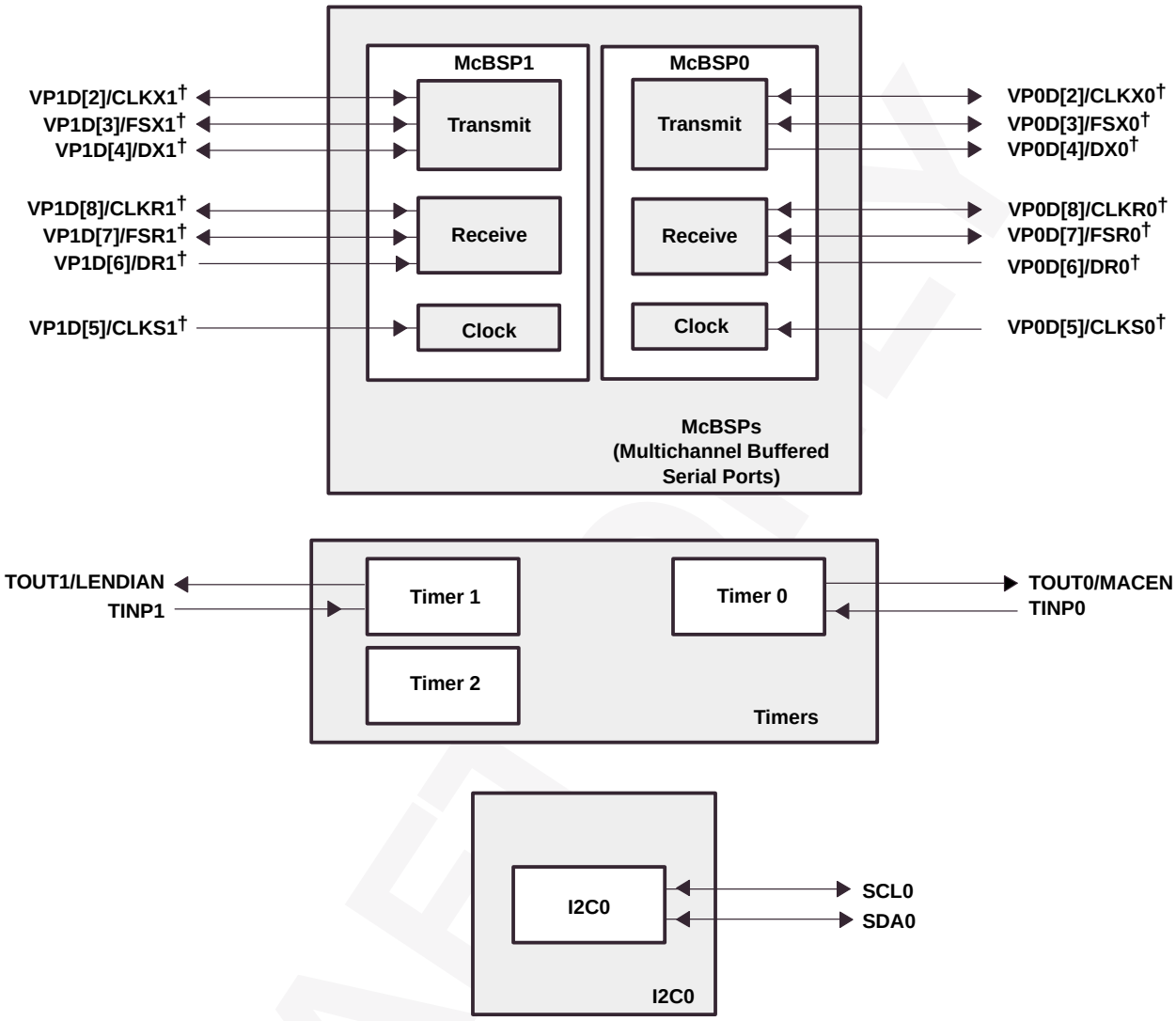
signal groups description (continued)



† These HPI pins are muxed with the PCI peripheral. By default, these signals function as HPI. For more details on these muxed pins, see the Device Configurations section of this data sheet.
‡ These PCI pins (excluding PCBE0 and XSP_CS) are muxed with the HPI or MDIO or GP0 peripherals. By default, these signals function as HPI and no function, respectively. For more details on these muxed pins, see the Device Configurations section of this data sheet.
§ These HPI/PCI data pins (HD[31:16/AD[31:16]) are muxed with the EMAC peripheral. By default, these pins function as HPI. For more details on the EMAC pin functions, see the Ethernet MAC (EMAC) peripheral signals section and the ternminal functions table portions of this data sheet.

Figure 3. Peripheral Signals (Continued)

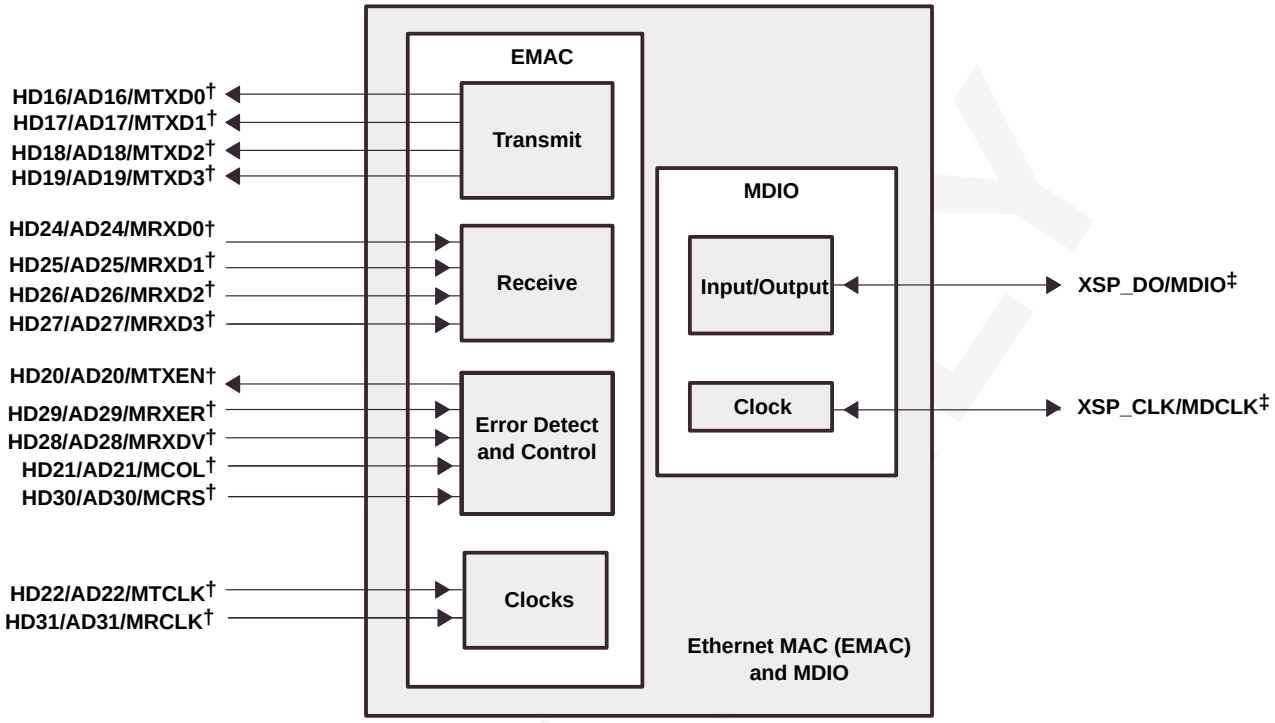
signal groups description (continued)



† These McBSP1 and McBSP0 pins are muxed with the Video Port 1 (VP1) and Video Port 0 (VP0) peripherals, respectively. By default, these signals function as VP1 and VP0, respectively. For more details on these muxed pins, see the Device Configurations section of this data sheet.

Figure 3. Peripheral Signals (Continued)

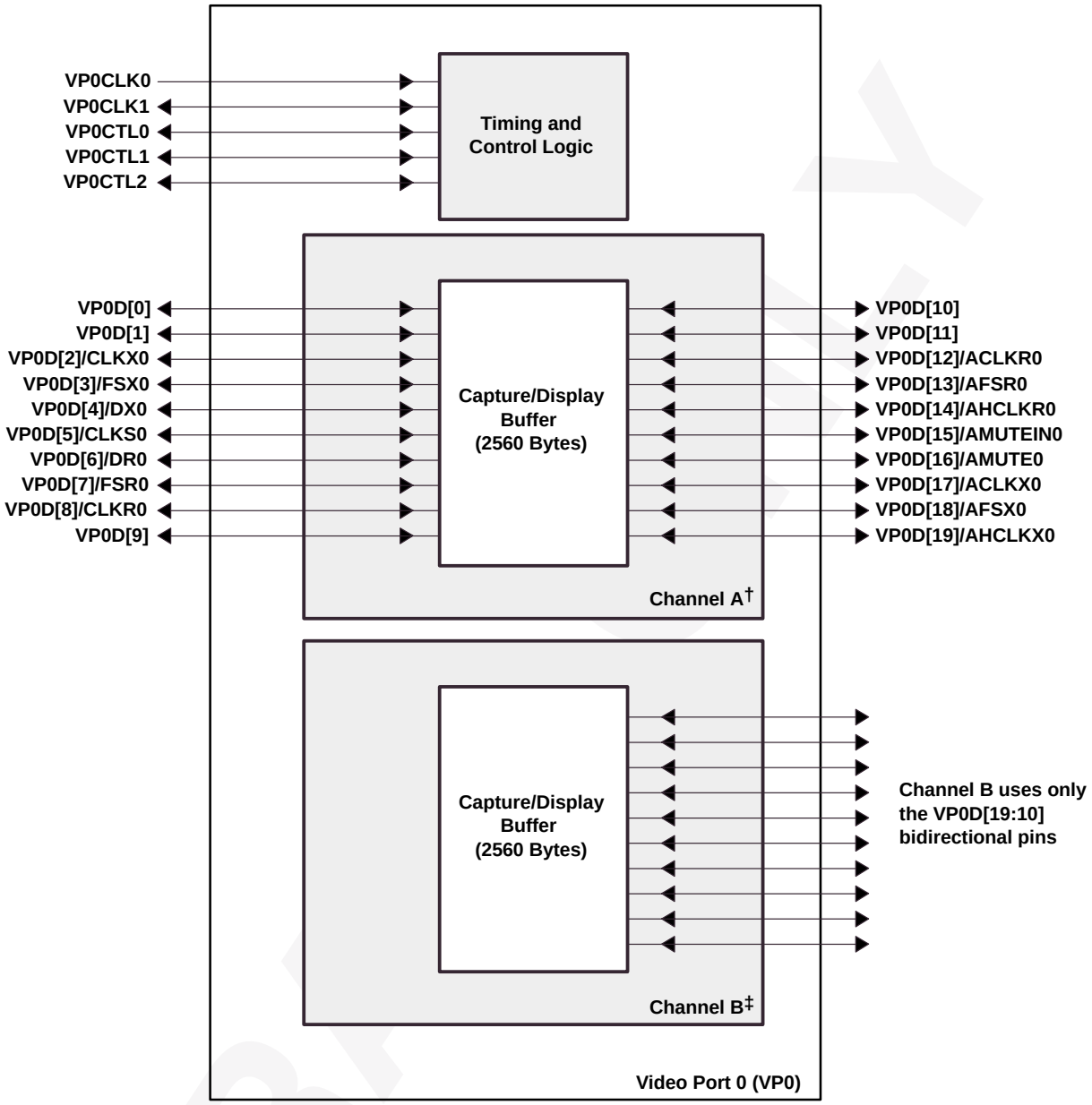
signal groups description (continued)



† These EMAC pins are muxed with the upper data pins of the HPI or PCI peripherals. By default, these signals function as HPI. For more details on these muxed pins, see the Device Configurations section of this data sheet.
‡ These MDIO pins are muxed with the PCI peripherals. By default, these signals function as PCI. For more details on these muxed pins, see the Device Configurations section of this data sheet.

Figure 3. Peripheral Signals (Continued)

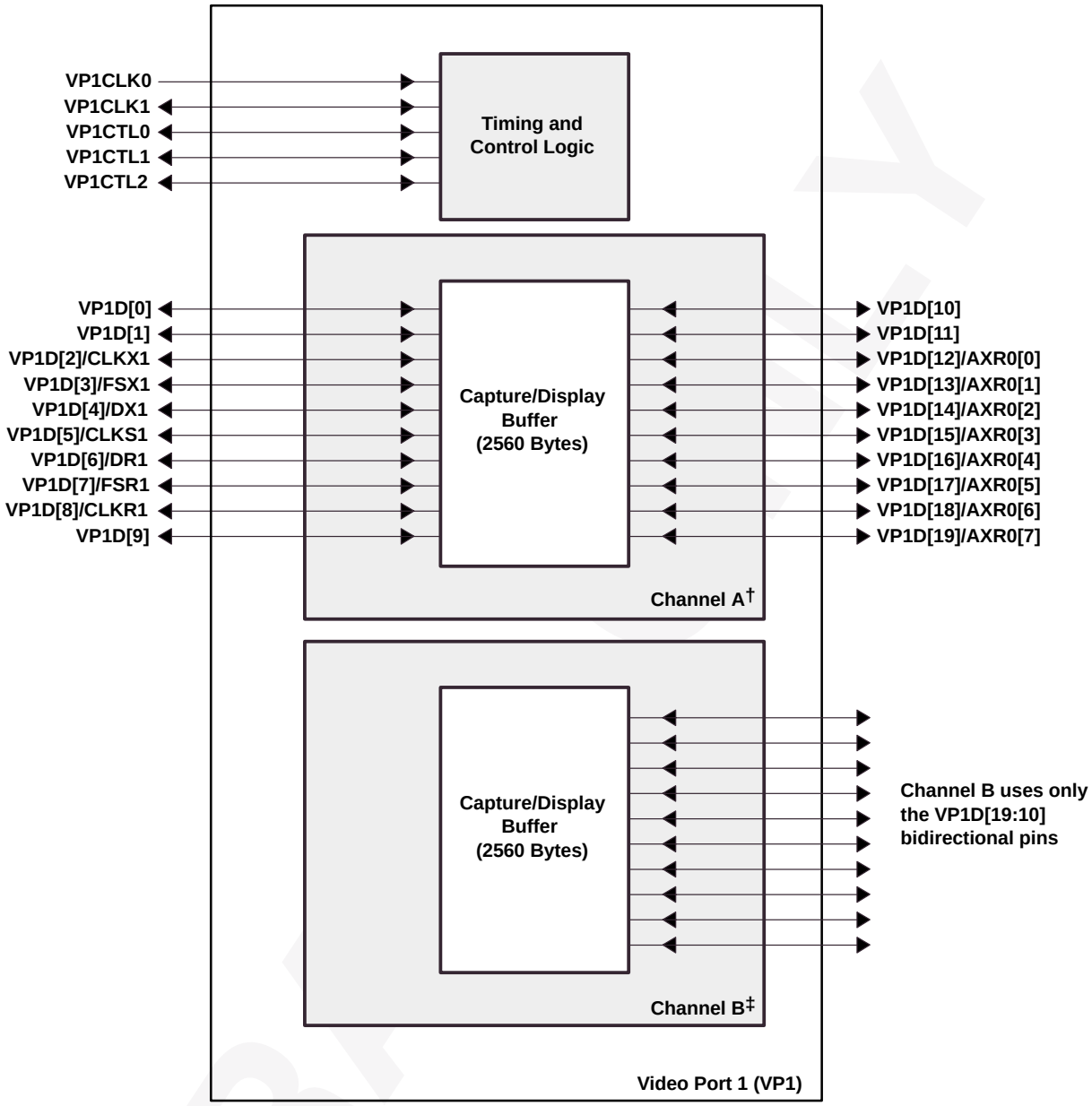
signal groups description (continued)



† Channel A supports: BT.656 (8/10-bit), Y/C Video (16/20-bit), RAW Video (16/20-bit), TSI (8-bit) capture pipeline modes and BT.656 (8/10-bit), Y/C Video (16/20-bit), RAW Video (16/20-bit) display pipeline modes.
‡ Channel B supports: BT.656 (8/10-bit), RAW Video (8/10-bit) capture pipeline modes and can display synchronized RAW Video data with Channel A.

Figure 3. Peripheral Signals (Continued)

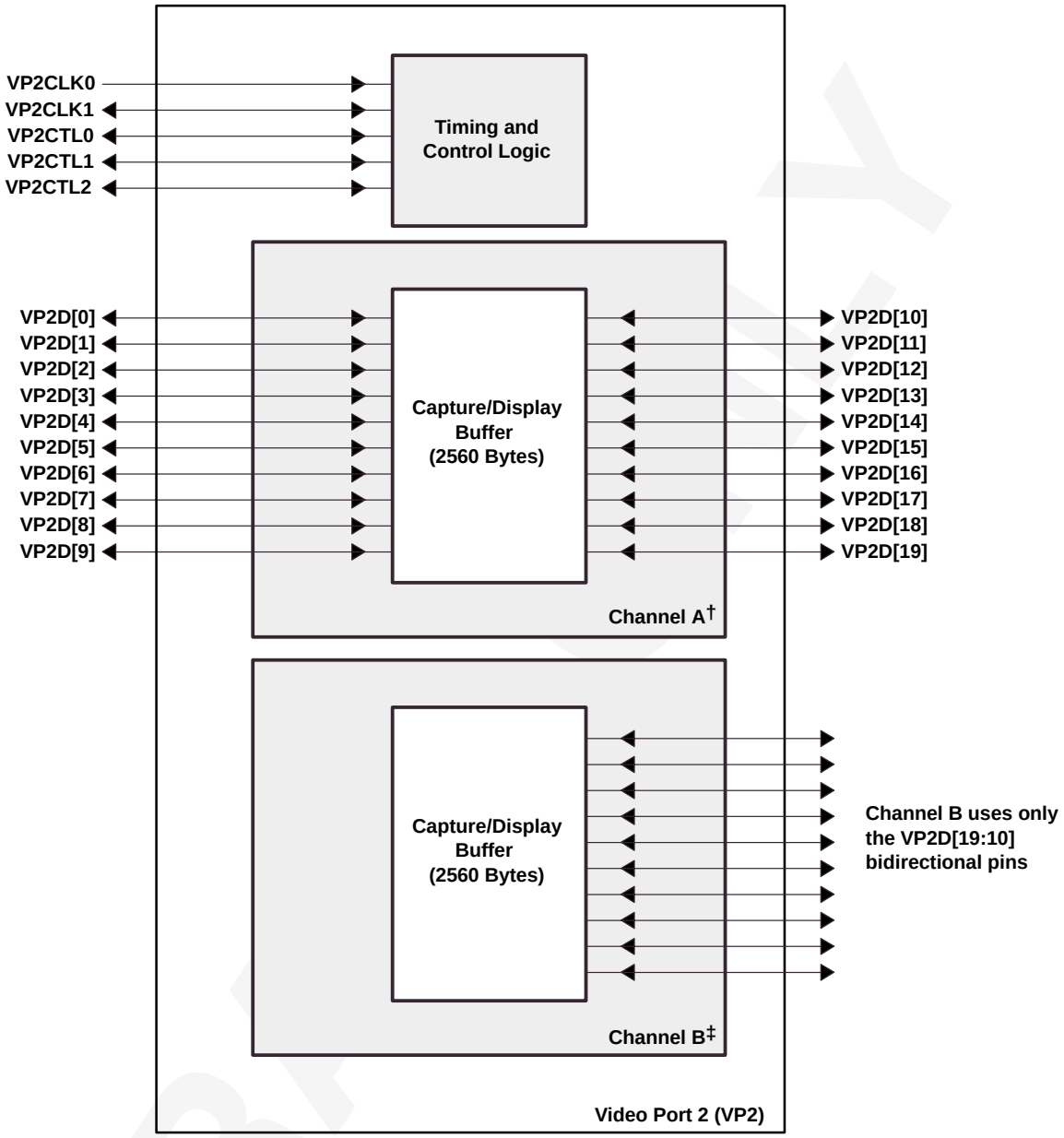
signal groups description (continued)



† Channel A supports: BT.656 (8/10-bit), Y/C Video (16/20-bit), RAW Video (16/20-bit), TSI (8-bit) capture pipeline modes and BT.656 (8/10-bit), Y/C Video (16/20-bit), RAW Video (16/20-bit) display pipeline modes.
‡ Channel B supports: BT.656 (8/10-bit), RAW Video (8/10-bit) capture pipeline modes and can display synchronized RAW Video data with Channel A.

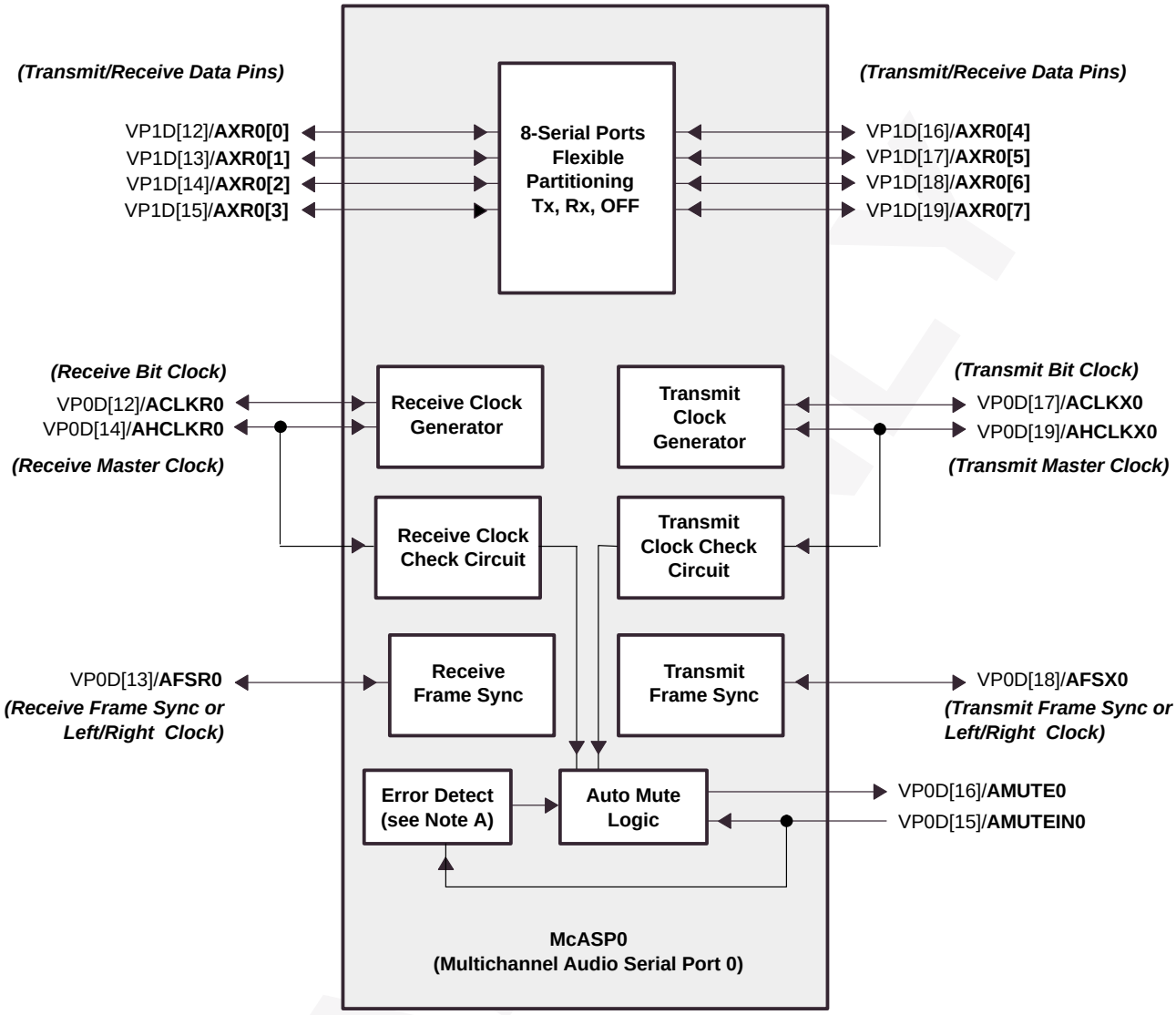
Figure 3. Peripheral Signals (Continued)

signal groups description (continued)



† Channel A supports: BT.656 (8/10-bit), Y/C Video (16/20-bit), RAW Video (16/20-bit), TSI (8-bit) capture pipeline modes and BT.656 (8/10-bit), Y/C Video (16/20-bit), RAW Video (16/20-bit) display pipeline modes.
‡ Channel B supports: BT.656 (8/10-bit), RAW Video (8/10-bit) capture pipeline modes and can display synchronized RAW Video data with Channel A.

Figure 3. Peripheral Signals (Continued)



NOTES: A. The McASPs' Error Detect function detects underruns, overruns, early/late frame syncs, DMA errors, and external mute input.
B. On multiplexed pins, bolded text denotes the active function of the pin for that particular peripheral module.
C. Bolded and italicized text within parentheses denotes the function of the pins in an audio system.

Figure 3. Peripheral Signals (Continued)

DEVICE CONFIGURATIONS

On the DM642 device, bootmode and certain device configurations/peripheral selections are determined at device reset, while other device configurations/peripheral selections are software-configurable via the peripheral configurations register (PERCFG) [address location 0x01B3F000] after device reset.

peripheral selection at device reset

Some DM642 peripherals share the same pins (internally muxed) and are mutually exclusive (i.e., HPI, general-purpose input/output pins GP0[15:9], PCI and its internal EEPROM, EMAC, MDIO, and VIC). Other DM642 peripherals (i.e., the Timers, I2C0, and the GP0[7:0] pins), are always available.

- HPI, GP0[15:9], PCI, EEPROM (internal to PCI), EMAC, and VIC peripherals

  The PCI_EN and MAC_EN pins are latched at reset. They determine specific peripheral selection, summarized in Table 30.

Table 30. PCI_EN, HD5, and MAC_EN Peripheral Selection (HPI, GP0[15:9], PCI, EMAC, MDIO, and VIC)

PERIPHERAL SELECTION†				PERIPHERALS SELECTED					
PCI_EN Pin [AA4]	PCI_EEAI Pin [L5]	HD5 Pin [Y1]	MAC_EN Pin [D6]	HPI Data Lower	HPI Data Upper	32-Bit PCI	EEPROM (Internal to PCI)	EMAC and MDIO	GP0 – GP0[15:9]
0	0	0	0	√	Hi-Z	Disabled	Disabled	Disabled	√
0	0	0	1	√	Hi-Z	Disabled	Disabled	√	√
0	0	1	0	√	√	Disabled	Disabled	Disabled	√
0	0	1	1	Disabled		Disabled	Disabled	√	√
1	1	X	X	Disabled		√	√	Disabled	Disabled

†
‡

  – If the PCI is disabled (PCI_EN = 0), the HPI peripheral is enabled and based on the HD5 and MAC_EN pin configuration at reset, HPI16 mode or EMAC and MDIO can be selected. When the PCI is disabled (PCI_EN = 0), the GP0[15:9] pins can also be programmed as GPIO, provided the GPxEN and GPxDIR bits are properly configured.

    This means all multiplexed HPI/PCI pins function as HPI and all standalone PCI pins ($\overline{\text{PCBE0}}$ and XSP_CS) are tied-off (Hi-Z). Also, the multiplexed GP0/PCI pins can be used as GPIO with the proper software configuration of the GPIO enable and direction registers (for more details, see Table 35).

  – If the PCI is enabled (PCI_EN = 1), the HPI peripheral is disabled.

    This means all multiplexed HPI/PCI pins function as PCI. Also, the multiplexed GP0/PCI pins function as PCI pins (for more details, see Table 35).

  – The MAC_EN pin, in combination with the PCI_EN and HD5 pins, controls the selection of the EMAC and MDIO peripherals (for more details, see Table 31).

  – The PCI_EN pin (= 1) and the PCI_EEAI pin control the whether the PCI initializes its internal registers via external EEPROM (PCI_EEAI = 1) or if the internal default values are used instead (PCI_EEAI = 0).

DEVICE CONFIGURATIONS (CONTINUED)

TBD reference

Table 31. HPI vs. EMAC Peripheral Pin Selection

CONFIGURATION SELECTION†			PERIPHERALS SELECTED	
GP0[0]/ DM641_SEL Pin [AF6]†	HD5 Pin [Y1]	MAC_EN Pin [D6]	HD[15:0]	HD[31:16]
0	0	0	HPI16	Hi-Z
0	0	1	HPI16	used for EMAC
0	1	0	HPI32 (HD[31:0])	
0	1	1	Hi-Z	used for EMAC

† GP0[0]/DM641_SEL = 0 denotes a non-DM41 device.

GP0[0]/DM641_SEL

DEVICE CONFIGURATIONS (CONTINUED)

device configuration at reset

Table 32 describes the DM642 device configuration pins, which are set up via external pullup/pulldown resistors through the specified EMIFA address bus pins (AEA[22:19]), and the TOUT1/LENDIAN, GP0[3]/PCIEEAI, and the HD5 pins (all of which are latched during device reset).

Table 32. DM642 Device Configuration Pins (TOUT1/LENDIAN, AEA[22:19], GP0[3]/PCIEEAI, DM641_SEL, and HD5)

CONFIGURATION PIN	NO.	FUNCTIONAL DESCRIPTION
TOUT1/**LENDIAN**	B5	Device Endian mode (LEND) 0 – System operates in Big Endian mode 1 – System operates in Little Endian mode (default)
AEA[22:21]	[U23, V24]	Bootmode [1:0] 00 – No boot (default mode) 01 – HPI/PCI boot (based on PCI_EN pin) 10 – Reserved 11 – EMIFA boot
AEA[20:19]	[V25, V26]	EMIFA input clock select Clock mode select for EMIFA (AECLKIN_SEL[1:0]) 00 – AECLKIN (default mode) 01 – CPU/4 Clock Rate 10 – CPU/6 Clock Rate 11 – AECLKIN
GP0[3]/**PCIEEAI**	AC6	PCI EEPROM Auto-Initialization (PCIEEAI) PCI auto-initialization via external EEPROM 0 – PCI auto-initialization through EEPROM is disabled; the PCI peripheral uses the specified PCI default values (default). 1 – PCI auto-initialization through EEPROM is enabled; the PCI peripheral is configured through EEPROM provided the PCI peripheral pin is enabled (PCI_EN = 1). Note: If the PCI peripheral is disabled (PCI_EN pin = 0), this pin must ***not*** be pulled up. For more information on the PCI EEPROM default values, see the PCI chapter of the *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190).
HD5/AD5	Y1	HPI peripheral bus width (HPI_WIDTH) 0 – HPI operates as an HPI16. (HPI bus is 16 bits wide. HD[15:0] pins are used and the remaining HD[31:16] pins are reserved pins in the Hi-Z state.) 1 – HPI operates as an HPI32. (HPI bus is 32 bits wide. All HD[31:0] pins are used for host-port operations.) (Also see the PCI_EN; TOUT0/MAC_EN functional description in this table)
GP0[0]/**DM641_SEL**	AF6	Device Select 0 – Non-DM641 device (default) 1 – DM641; EMAC pins are only on HD[15:0]
PCI_EN; TOUT0/**MAC_EN**	[AA4; D6]	Peripheral Selection 00 – HPI (default mode) [HPI32, if HD5 = 1; HPI16 if HD5 = 0 01 – EMAC and MDIO; HPI16, if HD5 = 0; HPI disabled, if HD5 = 1 10 – PCI 11 – Reserved

DEVICE CONFIGURATIONS (CONTINUED)

peripheral selection after device reset

Video Ports, McBSP1, McBSP0, McASP0 and I2C0 – **TBD**

The DM642 device has designated registers for peripheral configuration (PERCFG), device status (DEVSTAT), and JTAG identification (JTAGID). These registers are part of the Device Configuration module and are mapped to a 4K block memory starting at 0x01B3F000. The CPU accesses these registers via the CFGBUS.

The peripheral configuration register (PERCFG), allows the user to control the peripheral selection of the Video Ports (VP0, VP1, VP2) McBSP0, McBSP1, McASP0, and I2C0 peripherals. For more detailed information on the PERCFG register control bits, see Table 33 and Table 34.

Table 33. Peripheral Configuration Register (PERCFG) [Address location: 0x01B3F000 – 0x01B3F003]

31 – 24	23 – 16	15 – 8
Reserved	Reserved	Reserved
R-0	R-0	R-0

7	6	5	4	3	2	1	0
Reserved	VP2EN	VP1EN	VP0EN	I2C0EN	MCBSP1EN	MCBSP0EN	MCASP0EN
R-0	R/W-0	R/W-0	R/W-0	R/W-0	**R/W-1**	**R/W-1**	R/W-0

Legend: R = Read only; R/W = Read/Write; -n = value after reset

DEVICE CONFIGURATIONS (CONTINUED)

Table 34. Peripheral Configuration (PERCFG) Register Selection Bit Descriptions – TBD

BIT #	NAME	DESCRIPTION
31:7	Reserved	Reserved. Read-only, writes have no effect.
6	VP2EN	VP2 Enable bit. Determines whether the VP2 peripheral is enabled or disabled. (This feature allows power savings by disabling the peripheral when not in use.) 0 = VP2 is disabled, and the module is powered down (default). 1 = VP2 is enabled.
5	VP1EN	VP1 Enable bit. Determines whether the VP1 peripheral is enabled or disabled. 0 = VP1 is disabled, and the module is powered down (default). (This feature allows power savings by disabling the peripheral when not in use.) 1 = VP1 is enabled .
4	VP0EN	VP0 Enable bit. Determines whether the VP0 peripheral is enabled or disabled. 0 = VP0 is disabled, and the module is powered down (default). (This feature allows power savings by disabling the peripheral when not in use.) 1 = VP0 is enabled.
3	I2C0EN	Inter-integrated circuit 0 (I2C0) enable bit. Selects whether I2C0 peripheral is enabled or disabled (default). 0 = I2C0 is disabled, and the module is powered down (default). 1 = I2C0 is enabled.
2	MCBSP1EN	Video Port 1 (VP1) lower data pins vs. McBSP1 enable bit. Selects whether VP1 peripheral lower-data pins or the McBSP1 peripheral is enabled. 0 = VP1 lower-data pins are enabled and function (if VP1EN=1), McBSP1 is disabled; the remaining VP1 upper-data pins are dependent on the MCASP0EN bit and the VP1EN bit settings. 1 = McBSP1 is enabled, VP1 lower-data pin functions are disabled (default).
1	MCBSP0EN	Video Port 0 (VP0) lower data pins vs. McBSP0 enable bit. Selects whether VP0 peripheral lower-data pins or the McBSP1 peripheral is enabled. 0 = VP0 lower-data pins are enabled and function (if VP0EN=1), McBSP0 is disabled; the remaining VP0 upper-data pins are dependent on the MCASP0EN bit and the VP1EN bit settings. 1 = McBSP0 is enabled, VP0 lower-data pin functions are disabled (default).
0	MCASP0EN	McASP0 vs. VP0/VP1 upper-data pins select bit. Selects whether the McASP0 peripheral or the VP0 and VP1 upper-data pins are enabled. 0 = McASP0 is disabled; VP0 and VP1 upper-data pins are enabled; and the VP0 and VP1 lower-data pins are dependent on the MCBSP0EN and VP0EN, and MCSBP1EN and VP1EN bits, respectively. 1 = McASP0 is enabled; VP0 and VP1 upper-data pins are disabled; and the VP0 and VP1 lower-data pins are dependent on the MCBSP0EN and VP0EN, and MCSBP1EN and VP1EN bits, respectively.

DEVSTAT register description – **TBD**

JTAG ID register description – **TBD**

DEVICE CONFIGURATIONS (CONTINUED)

multiplexed pins

Multiplexed pins are pins that are shared by more than one peripheral and are internally multiplexed. Some of these pins are configured by software, and the others are configured by external pullup/pulldown resistors only at reset. Those muxed pins that are configured by software can be programmed to switch functionalities at any time. Those muxed pins that are configured by external pullup/pulldown resistors are mutually exclusive; only one peripheral has primary control of the function of these pins after reset. Table 35 identifies the multiplexed pins on the DM642 device; shows the default (primary) function and the default settings after reset; and describes the pins, registers, etc. necessary to configure specific multiplexed functions.

debugging considerations

It is recommended that external connections be provided to device configuration pins, including AEA[22:19], HD5/AD5, GP0[0]/DM641_SEL, PCI_EN, and TOUT0/MAC_EN. Although internal pullup/pulldown resistors exist on these pins, providing external connectivity adds convenience to the user in debugging and flexibility in switching operating modes.

Internal pullup/pulldown resistors also exist on the non-configuration pins on the AEA bus (AEA[18:0]). Do ***not*** oppose the internal pullup/pulldown resistors on these non-configuration pins with external pullup/pulldown resistors. If an external controller provides signals to these non-configuration pins, these signals must be driven to the default state of the pins at reset, or not be driven at all.

For the internal pullup/pulldown resistors for all device pins, see the terminal functions table.

DEVICE CONFIGURATIONS (CONTINUED)

Table 35. DM642 Device Multiplexed Pins† –TBD

MULTIPLEXED PINS NAME	MULTIPLEXED PINS NO.	DEFAULT FUNCTION	DEFAULT SETTING	DESCRIPTION
CLKOUT4/GP0[1]	D6	CLKOUT4	GP1EN = 0 (disabled)	These pins are software-configurable. To use these pins as GPIO pins, the GPxEN bits in the GPIO Enable Register and the GPxDIR bits in the GPIO Direction Register must be properly configured. GPxEN = 1: GPx pin enabled GPxDIR = 0: GPx pin is an input GPxDIR = 1: GPx pin is an output
CLKOUT6/GP0[2]	C6	CLKOUT6	GP2EN = 0 (disabled)	
GP0[0]/DM641_SEL	M5	DM641_SEL	GP0EN = 0 (disabled)	TBD
GP0[3]/PCIEEAI	L5	PCIEEAI	GP3EN = 0 (disabled)	TBD
VDAC/GP0[8]/PCI66	AD1	PCI66	GP8EN = 0 (disabled) MAC_EN = 0 (disabled)	TBD
GP0[9]/PIDSEL	K3	None	GPxEN = 0 (disabled) PCI_EN = 0 (disabled)†	To use GP0[15:9] as GPIO pins, the PCI needs to be disabled (PCI_EN = 0), the GPxEN bits in the GPIO Enable Register and the GPxDIR bits in the GPIO Direction Register must be properly configured. GPxEN = 1: GPx pin enabled GPxDIR = 0: GPx pin is an input GPxDIR = 1: GPx pin is an output
GP0[10]/$\overline{\text{PCBE3}}$	J2			
GP0[11]/$\overline{\text{PREQ}}$	F1			
GP0[12]/$\overline{\text{PGNT}}$	H4			
GP0[13]/$\overline{\text{PINTA}}$	G4			
GP0[14]/PCLK	C1			
GP0[15]/$\overline{\text{PRST}}$	G3			
VP1D[19]/AXR0[7]	AB12	None	VP1EN bit = 0 (disabled) MCASP0EN bit = 0 (disabled)	By default, no function is enabled upon reset. To enable the Video Port 1 data pins, the VP1EN bit in the PERCFG register must be set to a 1. (McASP0 data pins are disabled). To enable the McASP0[7:0] data pins, the MCASP0EN bit in the PERCFG register must be set to a 1. (VP1 upper data pins are disabled).
VP1D[18]/AXR0[6]	AB11			
VP1D[17]/AXR0[5]	AC11			
VP1D[16]/AXR0[4]	AD11			
VP1D[15]/AXR0[3]	AE11			
VP1D[14]/AXR0[2]	AC10			
VP1D[13]/AXR0[1]	AD10			
VP1D[12]/AXR0[0]	AC9			
VP1D[8]/CLKR1	AD8	McBSP1 functions	VP1EN bit = 0 (disabled) MCBSP1EN bit = 1 (enabled)	By default, the McBSP1 peripheral, function is enabled upon reset (MCBSP1EN bit = 1). To enable the Video Port 1 data pins, the VP1EN bit in the PERCFG register must be set to a 1.
VP1D[7]/FSR1	AC7			
VP1D[6]/DR1	AD7			
VP1D[5]/CLKS1	AE7			
VP1D[4]/DX1	AC6			
VP1D[3]/FSX1	AD6			
VP1D[2]/CLKX1	AE6			
VP0D[19]/AHCLKX0	AC12	None	VP0EN bit = 0 (disabled) MCASP0EN bit = 0 (disabled)	By default, no function is enabled upon reset. To enable the Video Port 0 data pins, the VP0EN bit in the PERCFG register must be set to a 1. (McASP0 control pins are disabled). To enable the McASP0 control pins, the MCASP0EN bit in the PERCFG register must be set to a 1. (VP0 upper data pins are disabled).
VP0D[18]/AFSX0	AD12			
VP0D[17]/ACLKX0	AB13			
VP0D[16]/AMUTE0	AC13			
VP0D[15]/AMUTEIN0	AD13			
VP0D[14]/AHCLKR0	AB14			
VP0D[13]/AFSR0	AC14			
VP0D[12]/ACLKR0	AD14			

VP0D[8]/CLKR0	AE15	None	VP0EN bit = 0 (disabled) MCBSP0EN bit = 1 (enabled)	By default, the McBSP0 peripheral function is enabled upon reset (MCBSP0EN bit = 1). To enable the Video Port 0 data pins, the VP0EN bit in the PERCFG register must be set to a 1.
VP0D[7]/FSR0	AB16			
VP0D[6]/DR0	AC16			
VP0D[5]/CLKS0	AD16			
VP0D[4]/DX0	AE16			
VP0D[3]/FSX0	AF16			
VP0D[2]/CLKX0	AF17			
XSP_CLK/MDCLK	R5	None	PCI_EN = 0 (disabled)† MAC_EN = 0 (disabled)†	By default, no functions enabled upon reset (PCI is disabled). To enable the PCI peripheral, an external pullup resistor (1 kΩ) must be provided on the PCI_EN pin (setting PCI_EN = 1 at reset) To enable the MDIO peripheral (which also enables the EMAC peripheral), an external pullup resistor (1 kΩ) must be provided on the MAC_EN pin (setting MAC_EN = 1 at reset)
XSP_DO/MDIO	P5			
$\overline{\text{HAS}}$/PPAR	P3	$\overline{\text{HAS}}$	PCI_EN = 0 (disabled)†	By default, HPI is enabled upon reset (PCI is disabled). To enable the PCI peripheral, an external pullup resistor (1 kΩ) must be provided on the PCI_EN pin (setting PCI_EN = 1 at reset).
HCNTL1/$\overline{\text{PDEVSEL}}$	P1	HCNTL1		
HCNTL0/$\overline{\text{PSTOP}}$	R3	HCNTL0		
$\overline{\text{HDS1}}$/$\overline{\text{PSERR}}$	R2	$\overline{\text{HDS1}}$		
$\overline{\text{HDS2}}$/$\overline{\text{PCBE1}}$	T2	$\overline{\text{HDS2}}$		
HR/$\overline{\text{W}}$/$\overline{\text{PCBE2}}$	M1	HR/$\overline{\text{W}}$		
HHWIL/$\overline{\text{PTRDY}}$	N3	HHWIL (HPI16 only)		
$\overline{\text{HINT}}$/$\overline{\text{PFRAME}}$	N4	$\overline{\text{HINT}}$		
$\overline{\text{HCS}}$/$\overline{\text{PPERR}}$	R1	$\overline{\text{HCS}}$		
$\overline{\text{HRDY}}$/$\overline{\text{PIRDY}}$	N1	$\overline{\text{HRDY}}$		
HD[23,15:0]/AD[23,15:0]	‡	HD[23, 15:0]	PCI_EN = 0 (disabled)†	By default, HPI is enabled upon reset (PCI is disabled). To enable the PCI peripheral, an external pullup resistor (1 kΩ) must be provided on the PCI_EN pin (setting PCI_EN = 1 at reset).
HD31/AD31/MRCLK	G1	HD31	PCI_EN = 0 (disabled)† MAC_EN = 0 (disabled)†	By default, HPI is enabled upon reset (PCI is disabled). To enable the PCI peripheral, an external pullup resistor (1 kΩ) must be provided on the PCI_EN pin (setting PCI_EN = 1 at reset). To enable the EMAC peripheral, an external pullup resistor (1 kΩ) must be provided on the MAC_EN pin (setting MAC_EN = 1 at reset).
HD30/AD30/MCRS	H3	HD30		
HD29/AD29/MRXER	G2	HD29		
HD28/AD28/MRXDV	J4	HD28		
HD27/AD27/MRXD3	H2	HD27		
HD26/AD26/MRXD2	J3	HD26		
HD25/AD25/MRXD1	J1	HD25		
HD24/AD24/MRXD0	K4	HD24		
HD22/AD22/MTCLK	L4	HD22		
HD21/AD21/MCOL	K2	HD21		
HD20/AD20/MTXEN	L3	HD20		
HD19/AD19/MTXD3	L2	HD19		
HD18/AD18/MTXD2	M4	HD18		
HD17/AD17/MTXD1	M2	HD17		
HD16/AD16/MTXD0	M3	HD16		

† All other standalone PCI pins are tied-off internally (pins in Hi-Z) when the peripheral is disabled [PCI_EN = 0].
‡ For the HD[31:0]/AD[31:0] multiplexed pins pin numbers, see the *Terminal Functions* table.

DEVICE CONFIGURATIONS (CONTINUED)

configuration examples TBD

Figure **TBD** through Figure **TBD** illustrate examples of peripheral selections that are configurable on this device.

Terminal Functions

SIGNAL NAME	NO.	TYPE†	IPD/ IPU‡	DESCRIPTION
CLOCK/PLL CONFIGURATION				
CLKIN	AC2	I	IPD	Clock Input. This clock is the input to the on-chip PLL.
CLKOUT4/GP0[1]§	D6	I/O/Z	IPD	Clock output at 1/4 of the device speed (**O/Z**) [default] or this pin can be programmed as a GP0 1 pin (**I/O/Z**).
CLKOUT6/GP0[2]§	C6	I/O/Z	IPD	Clock output at 1/6 of the device speed (**O/Z**) [default] or this pin can be programmed as a GP0 2 pin (**I/O/Z**).
CLKMODE1	AE4	I	IPD	Clock mode select • Selects whether the CPU clock frequency = input clock frequency x1 (Bypass), x6, or x12. For more details on the CLKMODE pins and the PLL multiply factors, see the Clock PLL section of this data sheet.
CLKMODE0	AA2	I	IPD	
PLLV¶	V6	A#		PLL voltage supply
JTAG EMULATION				
TMS	E15	I	IPU	JTAG test-port mode select
TDO	B18	O/Z	IPU	JTAG test-port data out
TDI	A18	I	IPU	JTAG test-port data in
TCK	A16	I	IPU	JTAG test-port clock
$\overline{\text{TRST}}$	D14	I	IPD	JTAG test-port reset. For IEEE 1149.1 JTAG compatibility, see the IEEE 1149.1 JTAG compatibility statement portion of this data sheet.
EMU9	B17	I/O/Z	IPU	Emulation pin 9. Reserved for future use, leave unconnected.
EMU8	D16	I/O/Z	IPU	Emulation pin 8. Reserved for future use, leave unconnected.
EMU7	A17	I/O/Z	IPU	Emulation pin 7. Reserved for future use, leave unconnected.
EMU6	C16	I/O/Z	IPU	Emulation pin 6. Reserved for future use, leave unconnected.
EMU5	B16	I/O/Z	IPU	Emulation pin 5. Reserved for future use, leave unconnected.
EMU4	D15	I/O/Z	IPU	Emulation pin 4. Reserved for future use, leave unconnected.
EMU3	C15	I/O/Z	IPU	Emulation pin 3. Reserved for future use, leave unconnected.
EMU2	B15	I/O/Z	IPU	Emulation pin 2. Reserved for future use, leave unconnected.
EMU1	C14	I/O/Z	IPU	Emulation pin 1‖
EMU0	A15	I/O/Z	IPU	Emulation pin 0‖
EMUCLK1	D17	I/O/Z	IPU	Emulation clock 1. Reserved for future use, leave unconnected.
EMUCLK0	C17	I/O/Z	IPU	Emulation clock 0. Reserved for future use, leave unconnected.
RESETS, INTERRUPTS, AND GENERAL-PURPOSE INPUT/OUTPUTS				
$\overline{\text{RESET}}$	P4	I		Device reset
NMI	B4	I	IPD	Nonmaskable interrupt, edge-driven (rising edge)
GP0[7]/EXT_INT7	E1	I/O/Z	IPU	General-purpose input/output (GPIO) pins (**I/O/Z**) or external interrupts (**input only**). The default after reset setting is GPIO enabled as input-only. • When these pins function as External Interrupts [by selecting the corresponding interrupt enable register bit (IER.[7:4])], they are edge-driven and the polarity can be independently selected via the External Interrupt Polarity Register bits (EXTPOL.[3:0]).
GP0[6]/EXT_INT6	F2			
GP0[5]/EXT_INT5	F3			
GP0[4]/EXT_INT4	F4			

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

§ These pins are multiplexed pins. For more details, see the Device Configurations section of this data sheet.

¶ PLLV is not part of external voltage supply. See the Clock PLL section for information on how to connect this pin.

A = Analog signal (PLL Filter)

‖ The EMU0 and EMU1 pins are internally pulled up with 30-kΩ resistors; therefore, for emulation and normal operation, no external pullup/pulldown resistors are necessary. However, for boundary scan operation, pull down the EMU1 and EMU0 pins with a dedicated 1-kΩ resistor.

Terminal Functions (Continued)

SIGNAL NAME	NO.	TYPE†	IPD/ IPU‡	DESCRIPTION
RESETS, INTERRUPTS, AND GENERAL-PURPOSE INPUT/OUTPUTS (CONTINUED)				
GP0[15]/$\overline{\text{PRST}}$§	G3	I/O/Z		General-purpose input/output (GP0) 15 pin (**I/O/Z**) or PCI reset (**I**). No function at default.
GP0[14]/PCLK§	C1			GP0 14 pin (**I/O/Z**) or PCI clock (**I**). No function at default.
GP0[13]/$\overline{\text{PINTA}}$§	G4			GP0 13 pin (**I/O/Z**) or PCI interrupt A (**O/Z**). No function at default.
GP0[12]/$\overline{\text{PGNT}}$§	H4			GP0 12 pin (**I/O/Z**) or PCI bus grant (**I**). No function at default.
GP0[11]/$\overline{\text{PREQ}}$§	F1			GP0 11 pin (**I/O/Z**) or PCI bus request (**O/Z**). No function at default.
GP0[10]/$\overline{\text{PCBE3}}$§	J2			GP0 10 pin (**I/O/Z**) or PCI command/byte enable 3 (**I/O/Z**). No function at default.
GP0[9]/PIDSEL§	K3			GP0 9 pin (**I/O/Z**) or PCI initialization device select (**I**). No function at default.
GP0[3]/PCIEEAI	L5		IPD	GP0 3 pin (**I/O/Z**) and PCI EEPROM Auto-Initialization (EEAI). If the PCI peripheral is disabled (PCI_EN pin = 0), this pin must ***not*** be pulled up. 0 – PCI auto-initialization through EEPROM is disabled (default). 1 – PCI auto-initialization through EEPROM is enabled.
GP0[0]/ DM641_SEL	M5		IPD	GP0 0 pin (**I/O/Z**) [default] or device selection (**I**) [default] or Device identification select . The general-purpose 0 pin (GP0[0]) (**I/O/Z**) can be programmed as GPIO 0 (**input only**) [default] or as GP0[0] (**output only**) pin or output as a general-purpose interrupt (GP0INT) signal (**output only**). DM641_SEL 0 – Non-DM641 device (default). 1 – Low-cost device.
VDAC/ GP0[8]/PCI66§	AD1	I/O/Z	IPD	VXCO Interpolated Control Port (VIC) single-bit digital-to-analog converter (VDAC) output [**output only**] [default] or this pin can be programmed as a GP0 8 pin (**I/O/Z**) or PCI frequency selection (PCI66). If the PCI peripheral is enabled (PCI_EN pin = 1), then: 0 – PCI operates at 66 MHz (default). 1 – PCI operates at 33 MHz. If the PCI peripheral is disabled (PCI_EN pin = 0), this pin must ***not*** be pulled up. **TBD**
CLKOUT6/ GP0[2]§	C6	I/O/Z	IPD	Clock output at 1/6 of the device speed (**O/Z**) [default] or this pin can be programmed as a GP0 2 pin (**I/O/Z**).
CLKOUT4/ GP0[1]§	D6	I/O/Z	IPD	Clock output at 1/4 of the device speed (**O/Z**) [default] or this pin can be programmed as a GP0 1 pin (**I/O/Z**).
HOST-PORT INTERFACE (HPI) or PERIPHERAL COMPONENT INTERCONNECT (PCI) or EMAC				
PCI_EN	E2	I	IPD	PCI enable pin. This pin and the MAC_EN pin control the selection (enable/disable) of the HPI, EMAC, MDIO, and GP0[15:8], or PCI peripherals. The pins work in conjunction to enable/disable these peripherals (for more details, see the Device Configurations section of this data sheet).
$\overline{\text{HINT}}$/$\overline{\text{PFRAME}}$§	N4	I/O/Z		Host interrupt from DSP to host (**O**) [default] or PCI frame (**I/O/Z**)
$\overline{\text{HCNTL1}}$/ $\overline{\text{PDEVSEL}}$§	P1	I/O/Z		Host control – selects between control, address, or data registers (**I**) [default] or PCI device select (**I/O/Z**).
$\overline{\text{HCNTL0}}$/ $\overline{\text{PSTOP}}$§	R3	I/O/Z		Host control – selects between control, address, or data registers (**I**) [default] or PCI stop (**I/O/Z**)
HHWIL/$\overline{\text{PTRDY}}$§	N3	I/O/Z		Host half-word select – first or second half-word (not necessarily high or low order) [For HPI16 bus width selection only] (**I**) [default] or PCI target ready (**I/O/Z**)
HR/$\overline{\text{W}}$/$\overline{\text{PCBE2}}$§	M1	I/O/Z		Host read or write select (**I**) [default] or PCI command/byte enable 2 (**I/O/Z**)
$\overline{\text{HAS}}$/PPAR§	P3	I/O/Z		Host address strobe (**I**) [default] or PCI parity (**I/O/Z**)

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

§ These pins are multiplexed pins. For more details, see the Device Configurations section of this data sheet.

PRODUCT PREVIEW

Terminal Functions (Continued)

SIGNAL NAME	NO.	TYPE†	IPD/ IPU‡	DESCRIPTION
HOST-PORT INTERFACE (HPI) or PERIPHERAL COMPONENT INTERCONNECT (PCI) or EMAC (CONTINUED)				
$\overline{\text{HCS}}$/$\overline{\text{PPERR}}$§	R1	I/O/Z		Host chip select (**I**) [default] or PCI parity error (**I/O/Z**)
$\overline{\text{HDS1}}$/$\overline{\text{PSERR}}$§	R2	I/O/Z		Host data strobe 1 (**I**) [default] or PCI system error (**I/O/Z**)
$\overline{\text{HDS2}}$/$\overline{\text{PCBE1}}$§	T2	I/O/Z		Host data strobe 2 (**I**) [default] or PCI command/byte enable 1 (**I/O/Z**)
$\overline{\text{HRDY}}$/$\overline{\text{PIRDY}}$§	N1	I/O/Z		Host ready from DSP to host (**O**) [default] or PCI initiator ready (**I/O/Z**).
HD31/AD31/MRCLK§	G1	I/O/Z		Host-port data (**I/O/Z**) [default] or PCI data-address bus (**I/O/Z**) or EMAC transmit/receive or control pins As HPI data bus (PCI_EN pin = 0) • Used for transfer of data, address, and control • Host-Port bus width user-configurable at device reset via a 10-kΩ resistor pullup/ pulldown resistor on the HD5 pin: HD5 pin = 0: HPI operates as an HPI16. (HPI bus is 16 bits wide. HD[15:0] pins are used and the remaining HD[31:16] pins are reserved pins in the high-impedance state.) HD5 pin = 1: HPI operates as an HPI32. (HPI bus is 32 bits wide. All HD[31:0] pins are used for host-port operations.) As PCI data-address bus (PCI_EN pin = 1) • Used for transfer of data and address For superset devices like DM642, the HD31/AD31 through HD16/AD16 pins can also function as EMAC transmit/receive or control pins (when PCI_EN pin = 0; MAC_EN pin = 1). For more details on the EMAC pin functions, see the *Ethernet MAC (EMAC) peripheral* section of this table and for more details on how to configure the EMAC pin, see the device configuration section of this data sheet.
HD30/AD30/MCRS§	H3			
HD29/AD29/MRXER§	G2			
HD28/AD28/MRXDV§	J4			
HD27/AD27/MRXD3§	H2			
HD26/AD26/MRXD2§	J3			
HD25/AD25/MRXD1§	J1			
HD24/AD24/MRXD0§	K4			
HD23/AD23§	K1			
HD22/AD22/MTCLK§	L4			
HD21/AD21/MCOL§	K2			
HD20/AD20/MTXEN§	L3			
HD19/AD19/MTXD3§	L2			
HD18/AD18/MTXD2§	M4			
HD17/AD17/MTXD1§	M2			
HD16/AD16/MTXD0§	M3			
HD15/AD15§	T3			
HD14/AD14§	U1			
HD13/AD13§	U3			
HD12/AD12§	U2			
HD11/AD11§	U4			
HD10/AD10§	V1			
HD9/AD9§	V3			
HD8/AD8§	V2			
HD7/AD7§	W2			
HD6/AD6§	W4			
HD5/AD5§	Y1			
HD4/AD4§	W3			
HD3/AD3§	Y2			
HD2/AD2§	Y4			
HD1/AD1§	AA1			
HD0/AD0§	Y3			
$\overline{\text{PCBE0}}$	V4	I/O/Z		PCI command/byte enable 0 (**I/O/Z**). When PCI is disabled (PCI_EN = 0), this pin is tied-off.
GP0[15]/$\overline{\text{PRST}}$§	G3	I/O/Z		General-purpose input/output (GP0) 15 pin (**I/O/Z**) or PCI reset (**I**). No function at de-fault.

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground
‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)
§ These pins are multiplexed pins. For more details, see the Device Configurations section of this data sheet.

Terminal Functions (Continued)

SIGNAL NAME	NO.	TYPE†	IPD/ IPU‡	DESCRIPTION
HOST-PORT INTERFACE (HPI) or PERIPHERAL COMPONENT INTERCONNECT (PCI) or EMAC (CONTINUED)				
XSP_CS	T4	O	IPD	PCI serial interface chip select (**O**). When PCI is disabled (PCI_EN = 0), this pin is tied-off.
XSP_CLK/ MDCLK§	R5	I/O/Z	IPD	PCI serial interface clock (**O**) [default] or MDIO serial clock input/output (**I/O/Z**).
XSP_DI	R4	I	IPU	PCI serial interface data in (**I**) [default]. In PCI mode, this pin is connected to the output data pin of the serial PROM.
XSP_DO/MDIO§	P5	I/O/Z	IPU	PCI serial interface data out (**O**) [default] or MDIO serial data input/output (**I/O/Z**). In PCI mode, this pin is connected to the input data pin of the serial PROM.
GP0[14]/PCLK§	C1	I/O/Z		GP0 14 pin (**I/O/Z**) or PCI clock (**I**). No function at default.
GP0[13]/$\overline{\text{PINTA}}$§	G4			GP0 13 pin (**I/O/Z**) or PCI interrupt A (**O/Z**). No function at default.
GP0[12]/$\overline{\text{PGNT}}$§	H4			GP0 12 pin (**I/O/Z**) or PCI bus grant (**I**). No function at default.
GP0[11]/$\overline{\text{PREQ}}$§	F1			GP0 11 pin (**I/O/Z**) or PCI bus request (**O/Z**). No function at default.
GP0[10]/$\overline{\text{PCBE3}}$§	J2			GP0 10 pin (**I/O/Z**) or PCI command/byte enable 3 (**I/O/Z**). No function at default.
GP0[9]/PIDSEL§	K3			GP0 9 pin (**I/O/Z**) or PCI initialization device select (**I**). No function at default.
GP0[3]/PCIEEAI	L5	I/O/Z	IPD	GP0 3 pin (**I/O/Z**) and PCI EEPROM Auto-Initialization (EEAI). If the PCI peripheral is disabled (PCI_EN pin = 0), this pin must ***not*** be pulled up. 0 – PCI auto-initialization through EEPROM is disabled (default). 1 – PCI auto-initialization through EEPROM is enabled.
VDAC/ GP0[8]/PCI66§	AD1	I/O/Z	IPD	VXCO Interpolated Control Port (VIC) single-bit digital-to-analog converter (VDAC) output [**output only**] [default] or this pin can be programmed as a GP0 8 pin (**I/O/Z**) or PCI frequency selection (PCI66). If the PCI peripheral is enabled (PCI_EN pin = 1), then: 0 – PCI operates at 66 MHz (default). 1 – PCI operates at 33 MHz. If the PCI peripheral is disabled (PCI_EN pin = 0), this pin must ***not*** be pulled up. **TBD**
EMIFA (64-bit) – CONTROL SIGNALS COMMON TO ALL TYPES OF MEMORY				
$\overline{\text{ACE3}}$	L26	O/Z	IPU	EMIFA memory space enables • Enabled by bits 28 through 31 of the word address • Only one pin is asserted during any external data access
$\overline{\text{ACE2}}$	K23	O/Z	IPU	
$\overline{\text{ACE1}}$	K24	O/Z	IPU	
$\overline{\text{ACE0}}$	K25	O/Z	IPU	
$\overline{\text{ABE7}}$	T22	O/Z	IPU	EMIFA byte-enable control • Decoded from the low-order address bits. The number of address bits or byte enables used depends on the width of external memory. • Byte-write enables for most types of memory • Can be directly connected to SDRAM read and write mask signal (SDQM)
$\overline{\text{ABE6}}$	T23	O/Z	IPU	
$\overline{\text{ABE5}}$	R25	O/Z	IPU	
$\overline{\text{ABE4}}$	R26	O/Z	IPU	
$\overline{\text{ABE3}}$	M25	O/Z	IPU	
$\overline{\text{ABE2}}$	M26	O/Z	IPU	
$\overline{\text{ABE1}}$	L23	O/Z	IPU	
$\overline{\text{ABE0}}$	L24	O/Z	IPU	
$\overline{\text{APDT}}$	M22	O/Z	IPU	EMIFA peripheral data transfer, allows direct transfer between external peripherals
EMIFA (64-BIT) – BUS ARBITRATION☆				
$\overline{\text{AHOLDA}}$	N22	O	IPU	EMIFA hold-request-acknowledge to the host
$\overline{\text{AHOLD}}$	W24	I	IPU	EMIFA hold request from the host
ABUSREQ	P22	O	IPU	EMIFA bus request output

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

§ These pins are multiplexed pins. For more details, see the Device Configurations section of this data sheet.

Terminal Functions (Continued)

SIGNAL NAME	NO.	TYPE†	IPD/ IPU‡	DESCRIPTION
EMIFA (64-BIT) – ASYNCHRONOUS/SYNCHRONOUS MEMORY CONTROL				
AECLKIN	H25	I	IPD	EMIFA external input clock. The EMIFA input clock (AECLKIN, CPU/4 clock, or CPU/6 clock) is selected at reset via the pullup/pulldown resistors on the BEA[17:16] pins. AECLKIN is the default for the EMIFA input clock.
AECLKOUT2	J23	O/Z	IPD	EMIFA output clock 2. Programmable to be EMIFA input clock (AECLKIN, CPU/4 clock, or CPU/6 clock) frequency divided-by-1, -2, or -4.
AECLKOUT1	J26	O/Z	IPD	EMIFA output clock 1 [at EMIFA input clock (AECLKIN, CPU/4 clock, or CPU/6 clock) frequency].
AARE/ ASDCAS/ ASADS/ASRE	J25	O/Z	IPU	EMIFA asynchronous memory read-enable/SDRAM column-address strobe/programmable synchronous interface-address strobe or read-enable • For programmable synchronous interface, the RENEN field in the CE Space Secondary Control Register (CExSEC) selects between ASADS and ASRE: If RENEN = 0, then the ASADS/ASRE signal functions as the ASADS signal. If RENEN = 1, then the ASADS/ASRE signal functions as the ASRE signal.
AAOE/ ASDRAS/ ASOE	J24	O/Z	IPU	EMIFA asynchronous memory output-enable/SDRAM row-address strobe/programmable synchronous interface output-enable
AAWE/ ASDWE/ ASWE	K26	O/Z	IPU	EMIFA asynchronous memory write-enable/SDRAM write-enable/programmable synchronous interface write-enable
ASDCKE	L25	O/Z	IPU	EMIFA SDRAM clock-enable (used for self-refresh mode). [EMIFA module only.] • If SDRAM is not in system, ASDCKE can be used as a general-purpose output.
ASOE3	R22	O/Z	IPU	EMIFA synchronous memory output-enable for ACE3 (for glueless FIFO interface)
AARDY	L22	I	IPU	Asynchronous memory ready input
EMIFA (64-BIT) – ADDRESS				
AEA22	U23	O/Z	IPD	EMIFA external address (doubleword address) • Also controls initialization of DSP modes at reset (**I**) via pullup/pulldown resistors – Boot mode (AEA[22:21]): 00 – No boot 01 – HPI boot 10 – EMIFA 8-bit ROM boot with default timings (default mode) 11 – Reserved – EMIF clock select – AEA[20:19]: Clock mode select for EMIFA (AECLKIN_SEL[1:0]) 00 – AECLKIN (default mode) 01 – CPU/4 Clock Rate 10 – CPU/6 Clock Rate 11 – Reserved For more details, see the Device Configurations section of this data sheet.
AEA21	V24			
AEA20	V25			
AEA19	V26			
AEA18	V23			
AEA17	U24			
AEA16	U25			
AEA15	U26			
AEA14	T24			
AEA13	T25			
AEA12	R23			
AEA11	R24			
AEA10	P23			
AEA9	P24			
AEA8	P26			
AEA7	N23			
AEA6	N24			
AEA5	N26			
AEA4	M23			
AEA3	M24			

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Terminal Functions (Continued)

SIGNAL NAME	SIGNAL NO.	TYPE†	IPD/ IPU‡	DESCRIPTION
EMIFA (64-bit) – DATA				
AED63	AF24	I/O/Z	IPU	EMIFA external data
AED62	AF23			
AED61	AE23			
AED60	AD23			
AED59	AD22			
AED58	AE22			
AED57	AD21			
AED56	AE21			
AED55	AC21			
AED54	AF21			
AED53	AD20			
AED52	AE20			
AED51	AC20			
AED50	AF20			
AED49	AC19			
AED48	AD19			
AED47	W23			
AED46	Y26			
AED45	Y23			
AED44	Y25			
AED43	Y24			
AED42	AA26			
AED41	AA23			
AED40	AA25			
AED39	AA24			
AED38	AB23			
AED37	AB25			
AED36	AB24			
AED35	AC26			
AED34	AC25			
AED33	AD25			
AED32	AD26			
AED31	C26			
AED30	C25			
AED29	D26			
AED28	D25			
AED27	E24			
AED26	E25			

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‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Terminal Functions (Continued)

SIGNAL NAME	NO.	TYPE†	IPD/ IPU‡	DESCRIPTION
EMIFA (64-bit) – DATA (CONTINUED)				
AED25	F24	I/O/Z	IPU	EMIFA external data
AED24	F25			
AED23	F23			
AED22	F26			
AED21	G24			
AED20	G25			
AED19	G23			
AED18	G26			
AED17	H23			
AED16	H24			
AED15	C19			
AED14	D19			
AED13	A20			
AED12	D20			
AED11	B20			
AED10	C20			
AED9	A21			
AED8	D21			
AED7	B21			
AED6	C21			
AED5	A23			
AED4	C22			
AED3	B22			
AED2	B23			
AED1	A24			
AED0	B24			
VCX0 INTERPOLATED CONTROL PORT (VIC)				
VDAC/ GP0[8]/PCI66§	AD1	I/O/Z	IPD	VXCO Interpolated Control Port (VIC) single-bit digital-to-analog converter (VDAC) output [**output only**] [default] or this pin can be programmed as a GP0 8 pin (**I/O/Z**) or PCI frequency selection (PCI66). If the PCI peripheral is enabled (PCI_EN pin = 1), then: 0 – PCI operates at 66 MHz (default). 1 – PCI operates at 33 MHz. If the PCI peripheral is disabled (PCI_EN pin = 0), this pin must ***not*** be pulled up. **TBD**
STCLK	AC1	I	IPD	VIC system time clock (**I**). The STCLK signal drives the hardware counter on the video ports.
MANAGEMENT DATA INPUT/OUTPUT (MDIO)				
XSP_CLK/MDCLK§	R5	I/O/Z	IPD	PCI serial interface clock (**O**) [default] or MDIO serial clock input/output (**I/O/Z**).
XSP_DO/MDIO§	P5	I/O/Z	IPU	PCI serial interface data out (**O**) [default] or MDIO serial data input/output (**I/O/Z**). In PCI mode, this pin is connected to the input data pin of the serial PROM.

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‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)
§ These pins are multiplexed pins. For more details, see the Device Configurations section of this data sheet.

Terminal Functions (Continued)

SIGNAL NAME	NO.	TYPE†	IPD/ IPU‡	DESCRIPTION
VIDEO PORT 2 (VP2)				
VP2D[19]	E13	I/O/Z	IPD	Video port 2 (VP2) data input/output (**I/O/Z**) [default]
VP2D[18]	E12			
VP2D[17]	D12			
VP2D[16]	C12			
VP2D[15]	B12			
VP2D[14]	E11			
VP2D[13]	D11			
VP2D[12]	C11			
VP2D[11]	B11			
VP2D[10]	A11			
VP2D[9]	D10			
VP2D[8]	C10			
VP2D[7]	B10			
VP2D[6]	A10			
VP2D[5]	D9			
VP2D[4]	C9			
VP2D[3]	B9			
VP2D[2]	A9			
VP2D[1]	D8			
VP2D[0]	C8			
VP2CLK1	A13	I/O/Z	IPD	Video port 2 clock 1 (**I/O/Z**) [default]
VP2CLK0	A7	I		VP2 clock 0 (**I**) [default]
VP2CTL2	C7	I/O/Z		VP2 control 2 (**I/O/Z**) [default]
VP2CTL1	D7			VP2 control 1 (**I/O/Z**) [default]
VP2CTL0	B8			VP2 control 0 (**I/O/Z**) [default]
VIDEO PORT 1 (VP1) OR MCASP0 DATA				
VP1D[19]/AXR0[7]§	AB12	I/O/Z	IPD	Video port 1 (VP1) data input/output (**I/O/Z**) [default] or McASP0 data pins (**I/O/Z**) or McBSP1 data input/output (**I/O/Z**) For more details on the McBSP1 pin functions or the McASP0 data pin functions, see *McBSP1* or *McASP0 data* sections of this table.
VP1D[18]/AXR0[6]§	AB11			
VP1D[17]/AXR0[5]§	AC11			
VP1D[16]/AXR0[4]§	AD11			
VP1D[15]/AXR0[3]§	AE11			
VP1D[14]/AXR0[2]§	AC10			
VP1D[13]/AXR0[1]§	AD10			
VP1D[12]/AXR0[0]§	AC9			
VP1D[11]	AD9			
VP1D[10]	AE9			
VP1D[9]	AC8			
VP1D[8]/CLKR1§	AD8			
VP1D[7]/FSR1§	AC7			
VP1D[6]/DR1§	AD7			

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

§ These pins are multiplexed pins. For more details, see the Device Configurations section of this data sheet.

Terminal Functions (Continued)

SIGNAL NAME	NO.	TYPE†	IPD/ IPU‡	DESCRIPTION
VIDEO PORT 1 (VP1) (CONTINUED)				
VP1D[5]/CLKS1§	AE7	I/O/Z	IPD	Video port 1 (VP1) data input/output (**I/O/Z**) [default] or McASP0 data pins (**I/O/Z**) or McBSP1 data input/output (**I/O/Z**) For more details on the McBSP1 pin functions or the McASP0 data pin functions, see *McBSP1* or *McASP0 data* sections of this table.
VP1D[4]/DX1§	AC6			
VP1D[3]/FSX1§	AD6			
VP1D[2]/CLKX1§	AE6			
VP1D[1]	AF6			
VP1D[0]	AF5			
VP1CLK1	AF10	I/O/Z	IPD	VP1 clock 1 (**I/O/Z**) [default]
VP1CLK0	AF8	I		VP1 clock 0 (**I**) [default]
VP1CTL2	AD5	I/O/Z		VP1 control 2 (**I/O/Z**) [default]
VP1CTL1	AE5			VP1 control 1 (**I/O/Z**) [default]
VP1CTL0	AF4			VP1 control 0 (**I/O/Z**) [default]
VIDEO PORT 0 (VP0) OR MCASP0 CONTROL				
VP0D[19]/AHCLKX0§	AC12	I/O/Z	IPD	Video port 0 (VP0) data input/output (**I/O/Z**) [default] or McASP0 control pins (**I/O/Z**) or McBSP0 data input/output (**I/O/Z**) For more details on the McBSP0 pin functions or the McASP0 control pin functions, see *McBSP0* or *McASP0 control* sections of this table.
VP0D[18]/AFSX0§	AD12			
VP0D[17]/ACLKX0§	AB13			
VP0D[16]/AMUTE0§	AC13			
VP0D[15]/AMUTEIN0§	AD13			
VP0D[14]/AHCLKR0§	AB14			
VP0D[13]/AFSR0§	AC14			
VP0D[12]/ACLKR0§	AD14			
VP0D[11]	AB15			
VP0D[10]	AC15			
VP0D[9]	AD15			
VP0D[8]/CLKR0§	AE15			
VP0D[7]/FSR0§	AB16			
VP0D[6]/DR0§	AC16			
VP0D[5]/CLKS0§	AD16			
VP0D[4]/DX0§	AE16			
VP0D[3]/FSX0§	AF16			
VP0D[2]/CLKX0§	AF17			
VP0D[1]	AE18			
VP0D[0]	AF18			
VP0CLK1	AF12	I/O/Z	IPD	VP0 clock 1 (**I/O/Z**) [default]
VP0CLK0	AF14	I		VP0 clock 0 (**I**) [default]
VP0CTL2	AD17	I/O/Z		VP0 control 2 (**I/O/Z**) [default]
VP0CTL1	AC17			VP0 control 1 (**I/O/Z**) [default]
VP0CTL0	AE17			VP0control 0 (**I/O/Z**) [default]

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

§ These pins are multiplexed pins. For more details, see the Device Configurations section of this data sheet.

Terminal Functions (Continued)

SIGNAL NAME	NO.	TYPE†	IPD/ IPU‡	DESCRIPTION
TIMER 2				
	–			No external pins. The timer 2 peripheral pins are ***not*** pinned out as external pins.
TIMER 1				
TOUT1/LENDIAN	B5	O/Z	IPD	Timer 1 output (**O/Z**) or device endian mode (**I**). Also controls initialization of DSP modes at reset via pullup/pulldown resistors – Device Endian mode 0 – Big Endian 1 – Little Endian (default) For more details on LENDIAN, see the Device Configurations section of this data sheet.
TINP1	A5	I	IPD	Timer 1 or general-purpose input
TIMER 0				
TOUT0/MAC_EN	C5	O/Z	IPD	Timer 0 output (**O/Z**) or MAC enable select bit (**I**) MAC enable pin. This pin and the MAC_EN pin control the selection (enable/disable) of the HPI, EMAC, MDIO, and GP0[15:9], or PCI peripherals. The pins work in conjunction to enable/disable these peripherals (for more details, see the Device Configurations section of this data sheet). For more details, see the Device Configurations section of this data sheet.
TINP0	A4	I	IPD	Timer 0 or general-purpose input
INTER-INTEGRATED CIRCUIT 0 (I2C0)				
SCL0	E4	I/O/Z	—	I2C0 clock.
SDA0	D3	I/O/Z	—	I2C0 data.
MULTICHANNEL BUFFERED SERIAL PORT 1 (McBSP1)				
VP1D[8]/CLKR1§	AD8	I/O/Z	IPD	Video Port 1 (VP1) input/output data 8 pin (**I/O/Z**) [default] or McBSP1 receive clock (**I/O/Z**)
VP1D[7]/FSR1§	AC7	I/O/Z	IPD	VP1 input/output data 7 pin (**I/O/Z**) [default] or McBSP1 receive frame sync (**I/O/Z**)
VP1D[6]/DR1§	AD7	I	IPD	VP1 input/output data 6 pin (**I/O/Z**) [default] or McBSP1 receive data (**I**)
VP1D[5]/CLKS1§	AE7	I	IPD	VP1 input/output data 5 pin (**I/O/Z**) [default] or McBSP1 external clock source (**I**) (as opposed to internal)
VP1D[4]/DX1§	AC6	I/O/Z	IPD	VP1 input/output data 4 pin (**I/O/Z**) [default] or McBSP1 transmit data (**O/Z**)
VP1D[3]/FSX1§	AD6	I/O/Z	IPD	VP1 input/output data 3 pin (**I/O/Z**) [default] or McBSP1 transmit frame sync (**I/O/Z**)
VP1D[2]/CLKX1§	AE6	I/O/Z	IPD	VP1 input/output data 2 pin (**I/O/Z**) [default] or McBSP1 transmit clock (**I/O/Z**)
MULTICHANNEL BUFFERED SERIAL PORT 0 (McBSP0)				
VP0D[8]/CLKR0§	AE15	I/O/Z	IPD	Video Port 0 (VP0) input/output data 8 pin (**I/O/Z**) [default] or McBSP0 receive clock (**I/O/Z**)
VP0D[7]/FSR0§	AB16	I/O/Z	IPD	VP0 input/output data 7 pin (**I/O/Z**) [default] or McBSP0 receive frame sync (**I/O/Z**)
VP0D[6]/DR0§	AC16	I	IPU	VP0 input/output data 6 pin (**I/O/Z**) [default] or McBSP0 receive data (**I**)
VP0D[5]/CLKS0§	AD16	I	IPD	VP0 input/output data 5 pin (**I/O/Z**) [default] or McBSP0 external clock source (**I**) (as opposed to internal)
VP0D[4]/DX0§	AE16	O/Z	IPU	VP0 input/output data 4 pin (**I/O/Z**) [default] or McBSP0 transmit data (**O/Z**)
VP0D[3]/FSX0§	AF16	I/O/Z	IPD	VP0 input/output data 3 pin (**I/O/Z**) [default] or McBSP0 transmit frame sync (**I/O/Z**)
VP0D[2]/CLKX0§	AF17	I/O/Z	IPD	VP0 input/output data 2 pin (**I/O/Z**) [default] or McBSP0 transmit clock (**I/O/Z**)

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

§ These pins are multiplexed pins. For more details, see the Device Configurations section of this data sheet.

Terminal Functions (Continued)

SIGNAL NAME	NO.	TYPE†	IPD/ IPU‡	DESCRIPTION
Ethernet MAC (EMAC)				
HD31/AD31/MRCLK§	G1	I		EMAC Media Independent I/F (MII) data, clocks, and control pins for Transmit/Receive. MII transmit clock (MTCLK), Transmit clock source from the attached PHY. MII transmit data (MTXD[3:0]), Transmit data nibble synchronous with transmit clock (MTCLK). MII transmit enable (MTXEN), This signal indicates a valid transmit data on the transmit data pins (MTDX[3:0]). MII collision sense (MCOL) Assertion of this signal during half-duplex operataion indicates network collision. During full-duplex operation, transmission of new frames will not begin if this pin is asserted. MII carrier sense (MCRS) Indicates a frame carrier signal is being received. MII receive data (MRXD[3:0]), Receive data nibble synchronous with receive clock (MRCLK). MII receive clock (MRCLK), Receive clock source from the attached PHY. MII receive data valid (MRXDV), This siganl indicates a valid data nibble on the receive data pins (MRDX[3:0]). and MII receive error (MRXER), Indicates reception of a coding error on the receive data.
HD30/AD30/MCRS§	H3	I		
HD29/AD29/MRXER§	G2	I		
HD28/AD28/MRXDV§	J4	I		
HD27/AD27/MRXD3§	H2	I		
HD26/AD26/MRXD2§	J3	I		
HD25/AD25/MRXD1§	J1	I		
HD24/AD24/MRXD0§	K4	I		
HD22/AD22/MTCLK§	L4	I		
HD21/AD21/MCOL§	K2	I		
HD20/AD20/MTXEN§	L3	O/Z		
HD19/AD19/MTXD3§	L2	O/Z		
HD18/AD18/MTXD2§	M4	O/Z		
HD17/AD17/MTXD1§	M2	O/Z		
HD16/AD16/MTXD0§	M3	O/Z		
MULTICHANNEL AUDIO SERIAL PORT 0 (McASP0) CONTROL				
VP0D[19]/AHCLKX0§	AC12			TBD
VP0D[18]/AFSX0§	AD12			
VP0D[17]/ACLKX0§	AB13			
VP0D[16]/AMUTE0§	AC13			
VP0D[15]/AMUTEIN0§	AD13			
VP0D[14]/AHCLKR0§	AB14			
VP0D[13]/AFSR0§	AC14			
VP0D[12]/ACLKR0§	AD14			
MULTICHANNEL AUDIO SERIAL PORT 0 (McASP0) DATA				
VP1D[19]/AXR0[7]§	AB12			TBD
VP1D[18]/AXR0[6]§	AB11			
VP1D[17]/AXR0[5]§	AC11			
VP1D[16]/AXR0[4]§	AD11			
VP1D[15]/AXR0[3]§	AE11			
VP1D[14]/AXR0[2]§	AC10			
VP1D[13]/AXR0[1]§	AD10			
VP1D[12]/AXR0[0]§	AC9			

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

‡ IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

§ These pins are multiplexed pins. For more details, see the Device Configurations section of this data sheet.

Terminal Functions (Continued)

SIGNAL NAME	SIGNAL NO.	TYPE†	IPD/ IPU‡	DESCRIPTION
RESERVED FOR TEST				
RSV	E14			Reserved (leave unconnected, ***do not*** connect to power or ground)
	AA3			
	AB3			
	AC4			
	AD3			
	AF3			

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

Terminal Functions (Continued)

SIGNAL NAME	SIGNAL NO.	TYPE†	DESCRIPTION
SUPPLY VOLTAGE PINS			
DV_{DD}	A2	S	3.3-V supply voltage
	A25		
	B1		
	B2		
	B14		
	B25		
	B26		
	C3		
	C24		
	D4		
	D23		
	E5		
	E7		
	E8		
	E10		
	E17		
	E19		
	E20		
	E22		
	F9		
	F12		
	F15		
	F18		
	G5		
	G22		
	H5		
	H22		
	J6		
	J21		
	K5		
	K22		
	M6		
	M21		
	N2		
	P25		
	R21		
	U5		
	U22		
	V21		
	W5		

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

Terminal Functions (Continued)

SIGNAL NAME	NO.	TYPE†	DESCRIPTION
SUPPLY VOLTAGE PINS (CONTINUED)			
DV_{DD}	W22	S	3.3-V supply voltage
	W25		
	Y5		
	Y22		
	AA9		
	AA12		
	AA15		
	AA18		
	AB5		
	AB7		
	AB8		
	AB10		
	AB17		
	AB19		
	AB20		
	AB22		
	AC23		
	AD24		
	AE1		
	AE2		
	AE13		
	AE25		
	AE26		
	AF2		
	AF25		
CV_{DD}	F6	S	1.2-V supply voltage (-500 device) 1.4 V supply voltage (-600, -603 devices)
	F7		
	F20		
	F21		
	G6		
	G7		
	G8		
	G10		
	G11		
	G13		
	G14		
	G16		
	G17		
	G19		

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

Terminal Functions (Continued)

SIGNAL NAME	SIGNAL NO.	TYPE†	DESCRIPTION
SUPPLY VOLTAGE PINS (CONTINUED)			
CV_{DD}	G20	S	1.2-V supply voltage (-500 device) 1.4 V supply voltage (-600, -603 devices)
	G21		
	H20		
	K7		
	K20		
	L7		
	L20		
	M12		
	M14		
	N7		
	N13		
	N15		
	N20		
	P7		
	P12		
	P14		
	P20		
	R13		
	R15		
	T7		
	T20		
	U7		
	U20		
	W20		
	Y6		
	Y7		
	Y8		
	Y10		
	Y11		
	Y13		
	Y14		
	Y16		
	Y17		
	Y19		
	Y20		
	Y21		
	AA6		
	AA7		
	AA20		
	AA21		

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

Terminal Functions (Continued)

SIGNAL NAME	NO.	TYPE†	DESCRIPTION
GROUND PINS			
V_{SS}	A1	GND	Ground pins
	A3		
	A6		
	A8		
	A12		
	A14		
	A19		
	A22		
	A26		
	B3		
	B6		
	B7		
	B13		
	B19		
	C2		
	C4		
	C13		
	C18		
	C23		
	D1		
	D2		
	D5		
	D13		
	D18		
	D22		
	D24		
	E3		
	E6		
	E9		
	E16		
	E18		
	E21		
	E23		
	E26		
	F5		
	F8		
	F10		
	F11		
	F13		

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

Terminal Functions (Continued)

SIGNAL NAME	SIGNAL NO.	TYPE†	DESCRIPTION
GROUND PINS (CONTINUED)			
V_{SS}	F14	GND	Ground pins
	F16		
	F17		
	F19		
	F22		
	G9		
	G12		
	G15		
	G18		
	H1		
	H6		
	H21		
	H26		
	J5		
	J7		
	J20		
	J22		
	K6		
	K21		
	L1		
	L6		
	L21		
	M7		
	M13		
	M15		
	M20		
	N5		
	N6		
	N12		
	N14		
	N21		
	N25		
	P2		
	P6		
	P13		
	P15		
	P21		
	R7		
	R12		

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

Terminal Functions (Continued)

SIGNAL NAME	NO.	TYPE†	DESCRIPTION
GROUND PINS (CONTINUED)			
V_{SS}	R14	GND	Ground pins
	R20		
	T1		
	T5		
	T6		
	T21		
	T26		
	U6		
	U21		
	V5		
	V7		
	V20		
	V22		
	W1		
	W6		
	W21		
	W26		
	Y9		
	Y12		
	Y15		
	Y18		
	AA4		
	AA5		
	AA8		
	AA10		
	AA11		
	AA13		
	AA14		
	AA16		
	AA17		
	AA19		
	AA22		
	AB1		
	AB2		
	AB4		
	AB6		
	AB9		
	AB18		
	AB21		
	AB26		

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

Terminal Functions (Continued)

SIGNAL NAME	SIGNAL NO.	TYPE†	DESCRIPTION
GROUND PINS (CONTINUED)			
V_{SS}	AC3	GND	Ground pins
	AC5		
	AC18		
	AC22		
	AC24		
	AD2		
	AD4		
	AD18		
	AE3		
	AE8		
	AE10		
	AE12		
	AE14		
	AE19		
	AE24		
	AF1		
	AF7		
	AF9		
	AF11		
	AF13		
	AF15		
	AF19		
	AF22		
	AF26		

† I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground

development support

TI offers an extensive line of development tools for the TMS320C6000™ DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of C6000™ DSP-based applications:

Software Development Tools:
Code Composer Studio™ Integrated Development Environment (IDE): including Editor
C/C++/Assembly Code Generation, and Debug plus additional development tools
Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any DSP application.

Hardware Development Tools:
Extended Development System (XDS™) Emulator (supports C6000™ DSP multiprocessor system debug)
EVM (Evaluation Module)

For a complete listing of development-support tools for the TMS320C6000™ DSP platform, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

device and development-support tool nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ DSP devices and support tools. Each TMS320™ DSP family member has one of three prefixes: TMX, TMP, or TMS. Texas Instruments recommends two of three possible prefix designators for support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

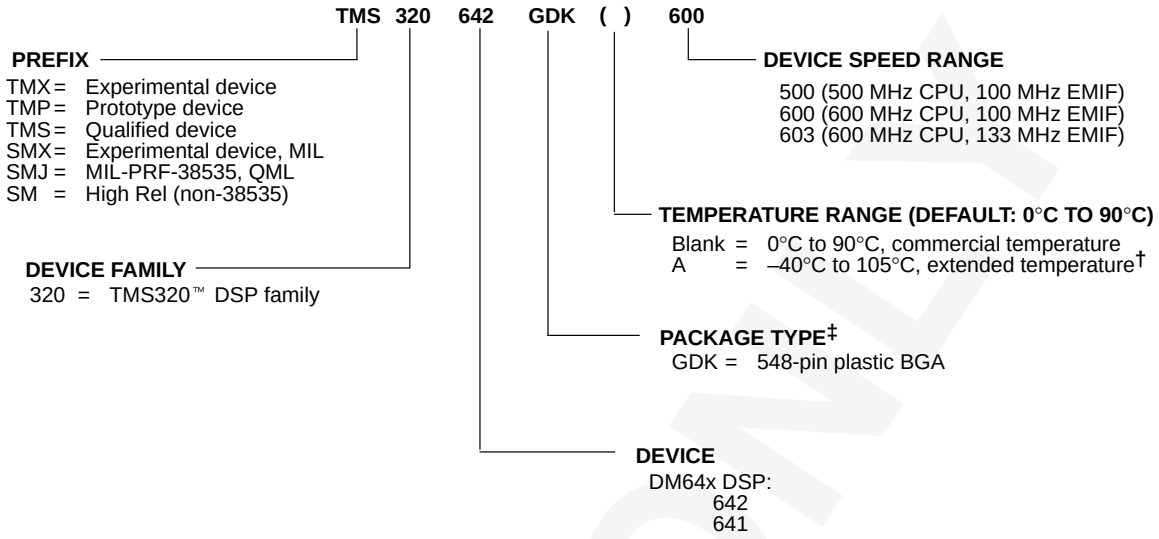
TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ DSP devices and support tools. Each TMS320™ DSP family member has one of three prefixes: TMX, TMP, or TMS. Texas Instruments recommends two of three possible prefix designators for support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, GDK), the temperature range (for example, blank is the default commercial temperature range), and the device speed range in megahertz (for example, -600 is 600 MHz). Figure 4 provides a legend for reading the complete device name for any TMS320C6000™ DSP platform member.

device and development-support tool nomenclature (continued)



† The extended temperature "A version" devices may have different operating conditions than the commercial temperature devices. See the recommended operating conditions portion of this data sheet for more detail.
‡ BGA = Ball Grid Array

Figure 4. TMS320DM64x™ DSP Device Nomenclature (Including the TMS320DM642 Device)

documentation support

Extensive documentation supports all TMS320™ DSP family generations of devices from product announcement through applications development. The types of documentation available include: data sheets, such as this document, with design specifications; complete user's reference guides for all devices and tools; technical briefs; development-support tools; on-line help; and hardware and software applications. The following is a brief, descriptive list of support documentation specific to the C6000™ DSP devices:

The *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189) describes the C6000™ DSP CPU (core) architecture, instruction set, pipeline, and associated interrupts.

The *TMS320C6000 Peripherals Reference Guide* (literature number SPRU190) describes the functionality of the peripherals available on the C6000™ DSP platform of devices, such as the 64-/32-/16-bit external memory interfaces (EMIFs), enhanced direct-memory-access (EDMA) controller, multichannel buffered serial ports (McBSPs), 32-/16-bit host-port interfaces (HPIs), a peripheral component interconnect (PCI), clocking and phase-locked loop (PLL); general-purpose timers, general-purpose input/output port (GP0), and power-down modes. This guide also includes information on internal data and program memories.

The *TMS320C64x Technical Overview* (literature number SPRU395) gives an introduction to the C64x™ digital signal processor, and discusses the application areas that are enhanced by the C64x™ DSP VelociTI.2™ VLIW architecture.

The *TMS320DA6x DSP Multichannel Audio Serial Port (McASP) Peripheral Reference Guide* (literature number **TBD**) describes the functionality of the McASP peripherals.

TMS320C6000 DSP Inter-Integrated Circuit (I2C) Module Peripheral Reference Guide (literature number SPRU175)

TMS320DM642 Technical Overview (literature number **TBD**)

The tools support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE). For a complete listing of C6000™ DSP latest documentation, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL).

clock PLL

Most of the internal C64x™ DSP clocks are generated from a single source through the CLKIN pin. This source clock either drives the PLL, which multiplies the source clock frequency to generate the internal CPU clock, or bypasses the PLL to become the internal CPU clock.

To use the PLL to generate the CPU clock, the external PLL filter circuit must be properly designed. Figure 5 shows the external PLL circuitry for either x1 (PLL bypass) or other PLL multiply modes.

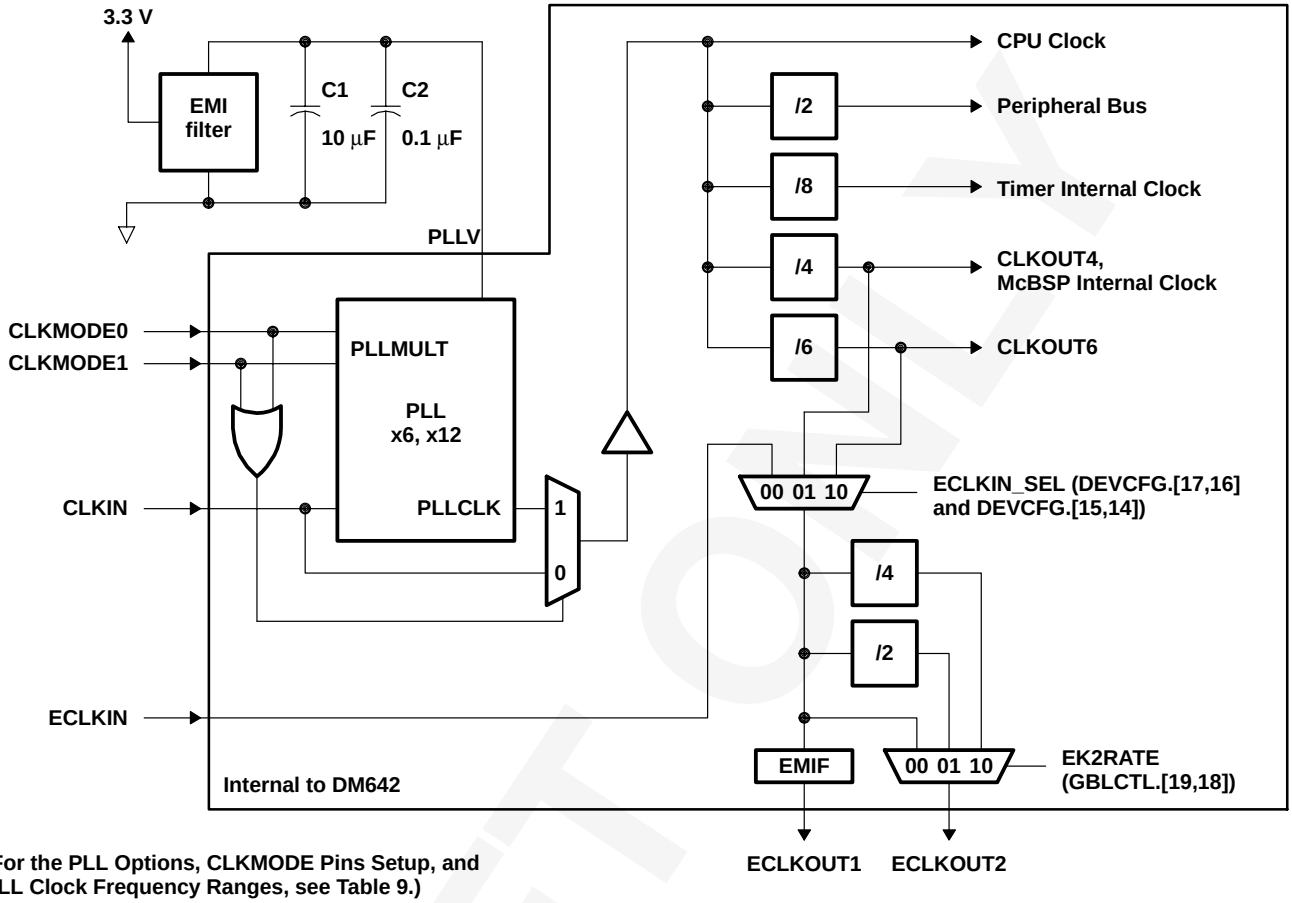
To minimize the clock jitter, a single clean power supply should power both the C64x™ DSP device and the external clock oscillator circuit. The minimum CLKIN rise and fall times should also be observed. For the input clock timing requirements, see the *input and output clocks* electricals section.

Rise/fall times, duty cycles (high/low pulse durations), and the load capacitance of the external clock source must meet the DSP requirements in this data sheet (see the *electrical characteristics over recommended ranges of suppy voltage and operating case temperature* table and the *input and output clocks* electricals section). Table 36 lists some examples of compatible CLKIN external clock sources:

Table 36. Compatible CLKIN External Clock Sources

COMPATIBLE PARTS FOR EXTERNAL CLOCK SOURCES (CLKIN)	PART NUMBER	MANUFACTURER
Oscillators	JITO-2	Fox Electronix
	STA series, ST4100 series	SaRonix Corporation
	SG-636	Epson America
	342	Corning Frequency Control
PLL	MK1711-S, ICS525-02	Integrated Circuit Systems

clock PLL (continued)



(For the PLL Options, CLKMODE Pins Setup, and PLL Clock Frequency Ranges, see Table 9.)

NOTES: A. Place all PLL external components (C1, C2, and the EMI Filter) as close to the C6000™ DSP device as possible. For the best performance, TI recommends that all the PLL external components be on a single side of the board without jumpers, switches, or components other than the ones shown.

B. For reduced PLL jitter, maximize the spacing between switching signals and the PLL external components (C1, C2, and the EMI Filter).

C. The 3.3-V supply for the EMI filter must be from the same 3.3-V power plane supplying the I/O voltage, DV_{DD}.

D. EMI filter manufacturer TDK part number ACF451832-333, -223, -153, -103. Panasonic part number EXCCET103U.

Figure 5. External PLL Circuitry for Either PLL Multiply Modes or x1 (Bypass) Mode

clock PLL (continued)

Table 37. TMS320DM642 PLL Multiply Factor Options, Clock Frequency Ranges, and Typical Lock Time†‡

GDK PACKAGE – 23 x 23 mm BGA							
CLKMODE1	CLKMODE0	CLKMODE (PLL MULTIPLY FACTORS)	CLKIN RANGE (MHz)	CPU CLOCK FREQUENCY RANGE (MHz)	CLKOUT4 RANGE (MHz)	CLKOUT6 RANGE (MHz)	TYPICAL LOCK TIME (μs)§
0	0	Bypass (x1)	30–75	30–75	7.5–18.8	5–12.5	N/A
0	1	x6	30–75	180–450	45–112.5	30–75	75
1	0	x12	30–50	360–600	90–150	60–100	
1	1	Reserved	–	–	–	–	–

† These clock frequency range values are applicable to a DM642–600 speed device. For –500 device speed values, see the CLKIN timing requirements table for the specific device speed.

‡ Use external pullup resistors on the CLKMODE pins (CLKMODE1 and CLKMODE0) to set the DM642 device to one of the valid PLL multiply clock modes (x6 or x12). With internal pulldown resistors on the CLKMODE pins (CLKMODE1, CLKMODE0), the default clock mode is x1 (bypass).

§ Under some operating conditions, the maximum PLL lock time may vary by as much as 150% from the specified typical value. For example, if the typical lock time is specified as 100 μs, the maximum value may be as long as 250 μs.

multichannel audio serial port (McASP0) peripheral – TBD

I2C – TBD

power-supply sequencing

TI DSPs do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to ensure that neither supply is powered up for extended periods of time if the other supply is below the proper operating voltage.

system-level design considerations

System-level design considerations, such as bus contention, may require supply sequencing to be implemented. In this case, the core supply should be powered up at the same time as, or prior to (and powered down after), the I/O buffers. This is to ensure that the I/O buffers receive valid inputs from the core before the output buffers are powered up, thus, preventing bus contention with other chips on the board.

power-supply design considerations

A dual-power supply with simultaneous sequencing can be used to eliminate the delay between core and I/O power up. A Schottky diode can also be used to tie the core rail to the I/O rail.

Core and I/O supply voltage regulators should be located close to the DSP (or DSP array) to minimize inductance and resistance in the power delivery path. Additionally, when designing for high-performance applications utilizing the C6000™ platform of DSPs, the PC board should include separate power planes for core, I/O, and ground, all bypassed with high-quality low-ESL/ESR capacitors.

IEEE 1149.1 JTAG compatibility statement

For compatibility with IEEE 1149.1 JTAG programmers, the $\overline{\text{TRST}}$ pin may need to be externally pulled up via a 1-kΩ resistor. For these C64x devices, this pin is internally pulled down, holding the JTAG port in reset by default. This is typically only a problem in systems where the DSP shares a scan chain with some other device. Some JTAG programmers for these other devices do not actively drive $\overline{\text{TRST}}$ high, leaving the scan chain inoperable while the C64x JTAG port is held in reset. TI emulators *do* drive $\overline{\text{TRST}}$ high, so the external pullup resistor is not needed in systems where TI emulators are the only devices that control JTAG scan chains on which the DSP(s) reside. If the system has other devices in the same scan chain as the DSP, and the programmer for these devices does *not* drive $\overline{\text{TRST}}$ high, then an external 1-kΩ pullup resistor is required.

With this external 1-kΩ pullup resistor installed, care must be taken to keep the DSP in a usable state under all circumstances. When $\overline{\text{TRST}}$ is pulled up, the JTAG driver must maintain the TMS signal high for 5 TCLK cycles, forcing the DSP(s) into the test logic reset (TLR) state. From the TLR state, the DSP's data scan path can be put in bypass (scan all 1s into the IR) to scan the other devices. The TLR state also allows normal operation of the DSP. If operation without anything driving the JTAG port is desired, the pullup resistor should be jumpered so that it may be engaged for programming the other devices and disconneted for running without a JTAG programmer or emulator.

EMIF device speed

The rated EMIF speed of these devices only applies to the SDRAM interface on EMIFA when in a system that meets the following requirements:

- 1 bank (maximum of 2 chips) of SDRAM connected to EMIFA
- up to 1 bank of buffers connected to EMIFA
- EMIFA trace lengths between 1 and 3 inches

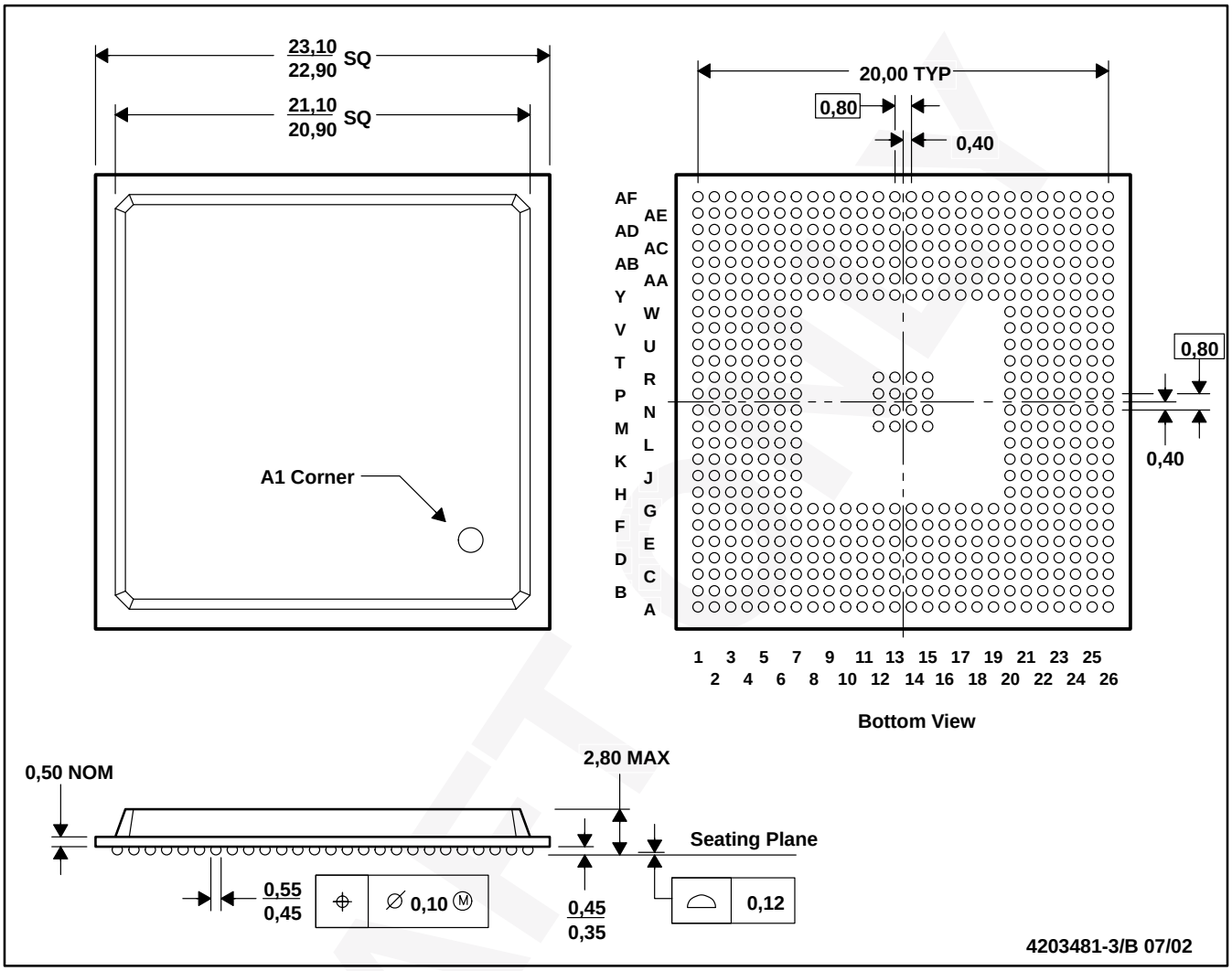
Other configurations may be possible, but timing analysis must be done to verify all AC timings are met. For more information on how to do a timing analysis and what can be done to fix marginal interfaces, see the *IBIS Analysis Methodology* application note (literature number **TBD**).

power saver module

TBD

MECHANICAL DATA

GDK (S–PBGA–N548) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Flip chip application only.

thermal resistance characteristics (S-PBGA package)

NO		°C/W	Air Flow (m/s†)
1	$R\Theta_{JC}$ Junction-to-case		N/A
2	$R\Theta_{JB}$ Junction-to-board		N/A
3	$R\Theta_{JA}$ Junction-to-free air		0.00
4	$R\Theta_{JA}$ Junction-to-free air		0.5
5	$R\Theta_{JA}$ Junction-to-free air		1.0
6	$R\Theta_{JA}$ Junction-to-free air		2.00
7	Psi_{JT} Junction-to-package top		N/A
8	Psi_{JB} Junction-to-board		N/A

† m/s = meters per second

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